

Metrology Challenges for 45nm Strained-Si Devices

V. Vartanian, M. Sadaka, S. Zollner, A. V-Y. Thean, T. White, B-Y. Nguyen, M. Zavala, L. McCormick, L. Prabhu, D. Eades, S. Parsons, K. Kim, J. Jiang, V. Dhandapani, J. Hildreth, R. Powers, G. Spencer, N. Ramani, J. Mogab
M. Kottke*, M. Canonico*, Q-H. Xie*, X-D. Wang*,
J. Vella*, L. Contreras*, D. Theodore*, R. Gregory*, B. Lu*, T. Kriske*, R. Liu†

**Advanced Products Research and Development Laboratory
Technology Solutions Organization**

Freescale Semiconductor, 3501 Ed Bluestein Blvd., MD:K-10, Austin, TX 78721

***Freescale Semiconductor, 2100 East Elliot Rd., MD:EL622, Tempe, AZ 85284**

†School of Microelectronics, Fudan University, Shanghai, China

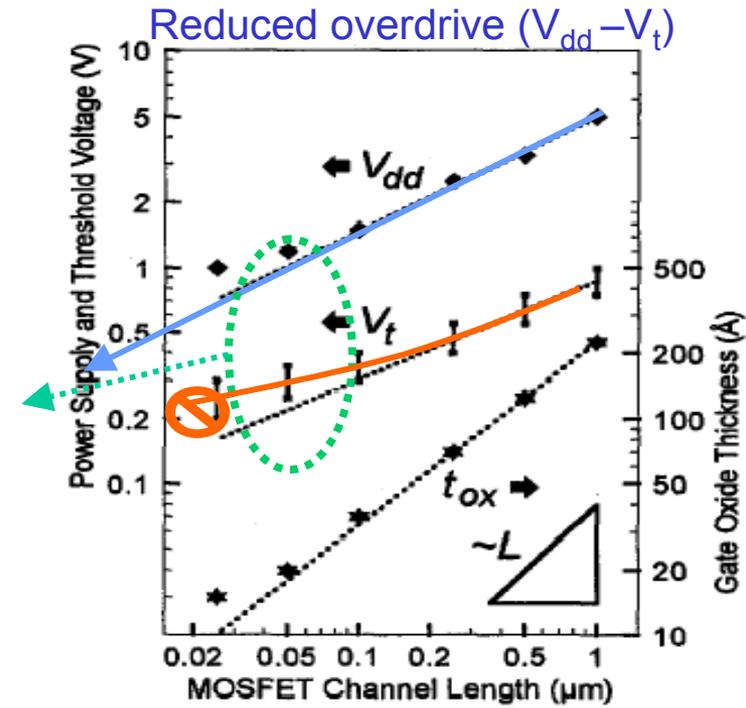
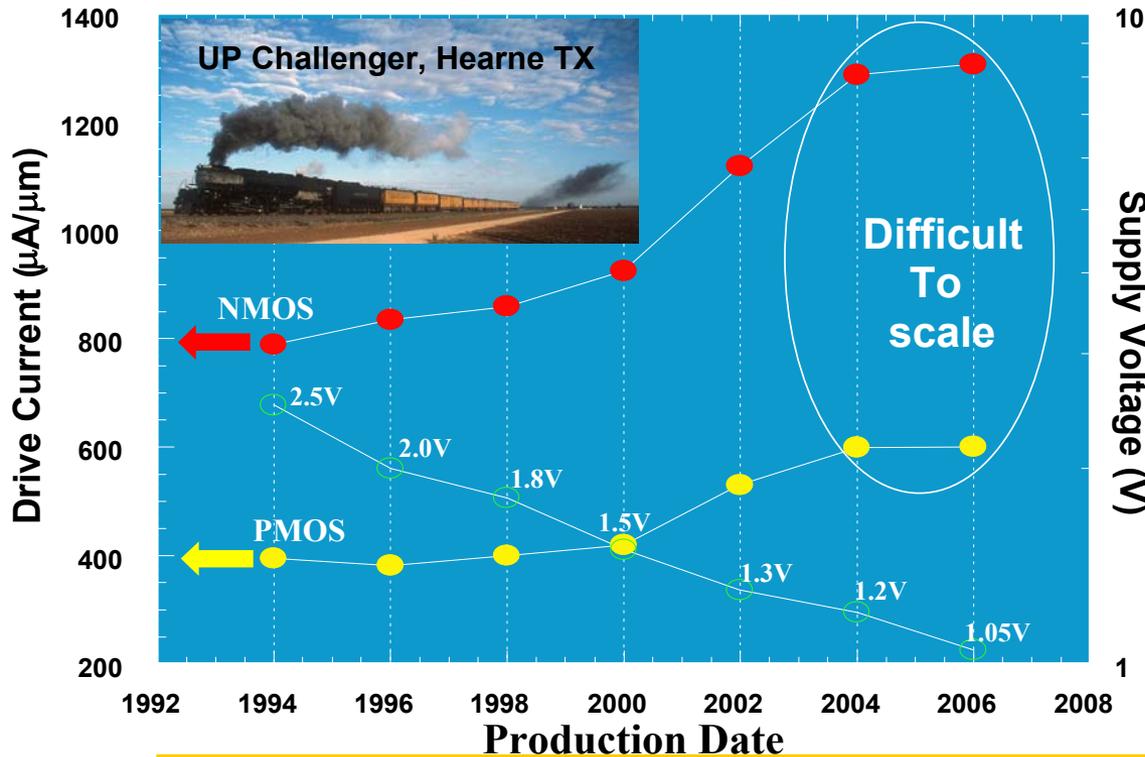
**2005 International Conference on Characterization and Metrology for ULSI Technology
March 15, 2005**

Agenda

- ✓ **Overview of Strained Si**
- ✓ **Metrology for Strained-Si**
- ✓ **Metrology for Defect Analysis**
- ✓ **Metrology for Substrate Characterization**
- ✓ **Metrology for Process Effects**
- ✓ **Emerging In-Line Metrology**
- ✓ **Summary**

- ✓ **Overview of Strained Si**
 - Metrology for Strained-Si
 - Metrology for Defect Analysis
 - Metrology for Substrate Characterization
 - Metrology for Process Effects
 - Emerging In-Line Metrology
 - Summary

Limits of Transistor Scaling



Challenge: maintain high drive current while simultaneously reducing power supply voltage

Traditional Scaling: leads to direct tunneling and high off-state current, and short-channel effects

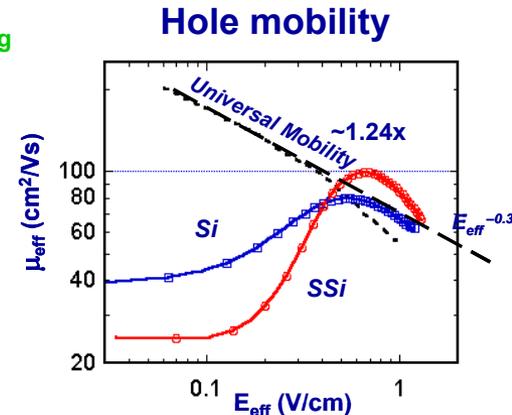
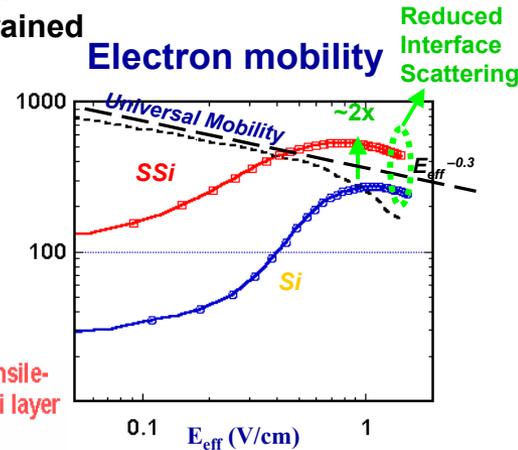
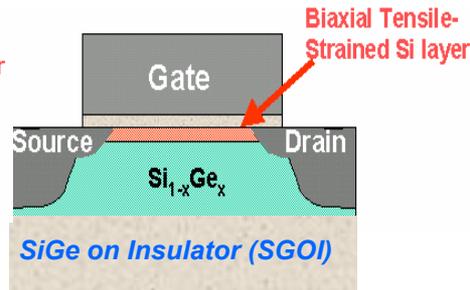
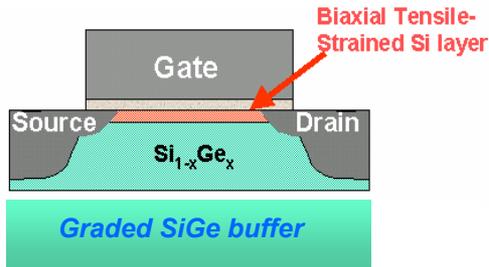
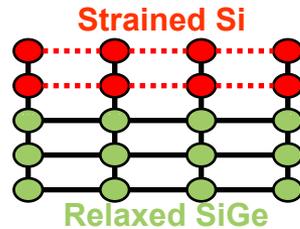
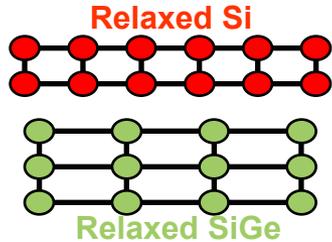
Solution: strained-Si

- higher electron and hole mobilities
- compatible with CMOS processing

Effects of Strained-Si Channels on Mobilities

Ge has a 4.2% larger lattice constant than Si

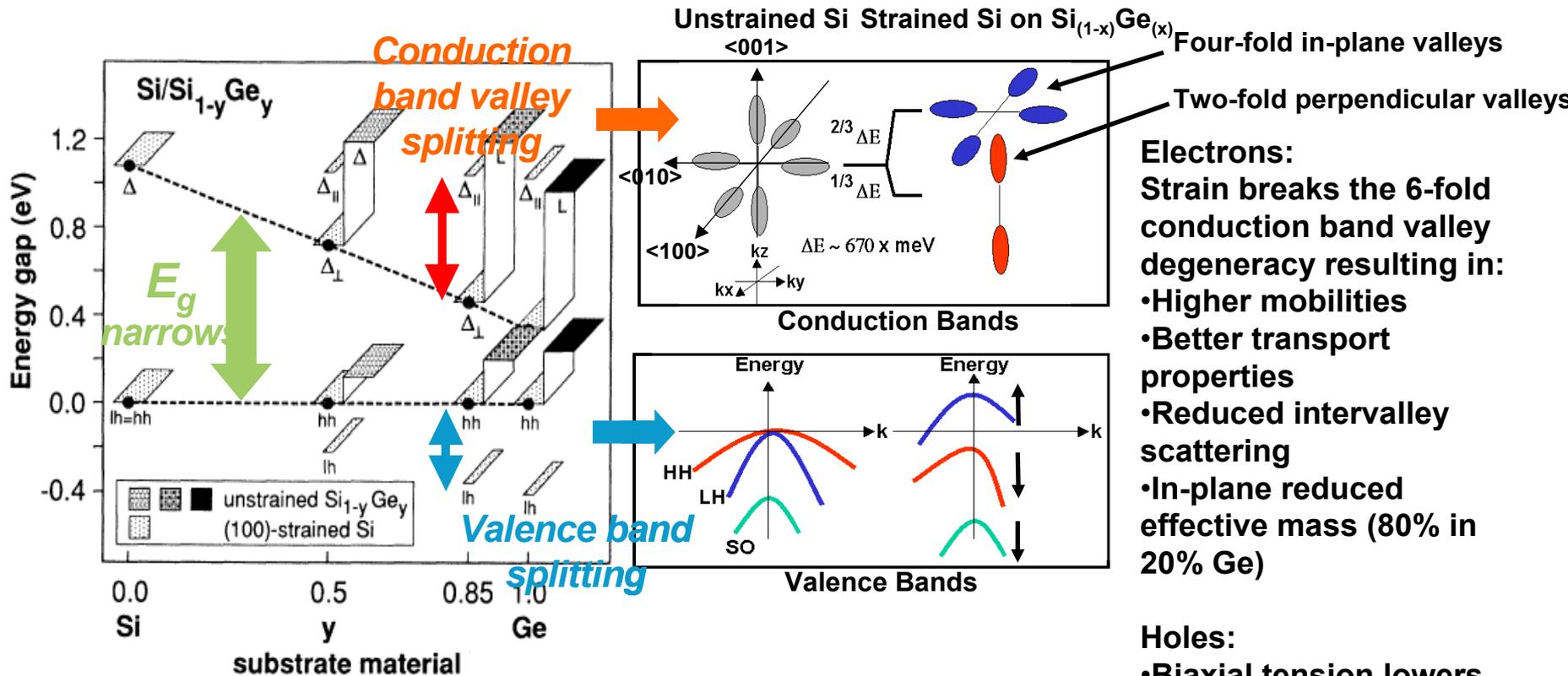
Pseudomorphic growth
No defects—smooth—fully strained



- Biaxial tensile strain increases electron and hole mobility above the universal mobility curve at high effective fields
- Higher mobility linearly increases drive current—
improved circuit speed without requiring new device structures
- ❖ *Strained-Si is closely compatible with traditional CMOS processing*

Where's the Enhancement Coming From?

Martin M. Rieger and P. Vogl, Phys. Rev. B 48, 14276-14287 (1993)



Electrons:
Strain breaks the 6-fold conduction band valley degeneracy resulting in:

- Higher mobilities
- Better transport properties
- Reduced intervalley scattering
- In-plane reduced effective mass (80% in 20% Ge)

Holes:

- Biaxial tension lowers HH and SO bands
- Reduced intervalley scattering
- In-plane and out-of-plane reduced effective mass (60% in 30% Ge)
- Splits bands/valleys

Greater levels of strain in the Si are required to effect the same hole mobility enhancement compared to electrons.

March 15, 2005

6

2005 International Conference on Characterization and Metrology for ULSI Technology, University of Texas at Dallas

Freescale™ and the Freescale logo are trademarks of Freescale Semiconductor, Inc.

All other product or service names are the property of their respective owners. © Freescale Semiconductor, Inc. 2004

Overview of Strained Si

✓ **Metrology for Strained-Si**

Metrology for Defect Analysis

Metrology for Substrate Characterization

Metrology for Process Effects

Emerging In-Line Metrology

Summary

- **Film morphology**



- Thickness of SOI layers
- Thickness of ultra-thin and stacked films
- Thickness of SiGe and Ge profile (graded or uniform)
- Magnitude and local variation of stress in Si channel (global vs local)

- **Film quality**

- Dislocation densities (TD's, MD's, pile-ups, twins) at buffer/channel interface)
- Roughness of Si/SiGe interface and Si surface
- Ge out-diffusion into Si channel and dopant diffusion in SiGe (as compared to Si)

- **Preferred tool requirements**

- Non-destructive (product wafers)
- Small spot size (need high spatial resolution)—patterned wafers
- Sensitivity to process drift; thermal stability of layers
- Need metrology to distinguish interfaces from bulk

- **Need development of new and emerging measurement technologies**

Thin-Film Analysis Techniques for Strained-Si CMOS

•Film Thickness Measurement

- Transmission Electron Microscopy (TEM)
- Spectroscopic Ellipsometry (SE)
- X-ray Reflectivity (XRR)
- X-ray Diffraction (XRD)
- Secondary Ion Mass Spectrometry (SIMS)
- Auger Electron Spectrometry
- Rutherford Backscattering Spectrometry (RBS)

•Elemental Composition

- X-ray Fluorescence (XRF)
- X-ray Diffraction (XRD)
- Auger Electron Spectrometry
- Spectroscopic Ellipsometry (SE)
- Secondary Ion Mass Spectrometry (SIMS)
- Rutherford Backscattering Spectrometry (RBS)
- Energy Dispersive Spectroscopy (EDS/TEM)

•Lattice Strain Characterization

- X-Ray Diffraction (XRD)
- UV Raman Spectroscopy
- High Resolution Lattice Image (HRTEM)

•Surface/Interface Roughness

- X-Ray Reflectivity (XRR)
- Atomic Force Microscopy (AFM)
- Transmission Electron Microscopy (TEM)

•Defect Density Inspection

- UV Raman Spectroscopy (Crystallinity)
- Transmission Electron Microscopy (TEM)
- Infrared Photoluminescence (PL)
- Schimmel Etch (for Etch Pit Density)

Transmission Electron Microscopy (TEM)

Capabilities

- Multi-layer thickness capability
- Excellent defect detection
- Elemental composition (with EDS)

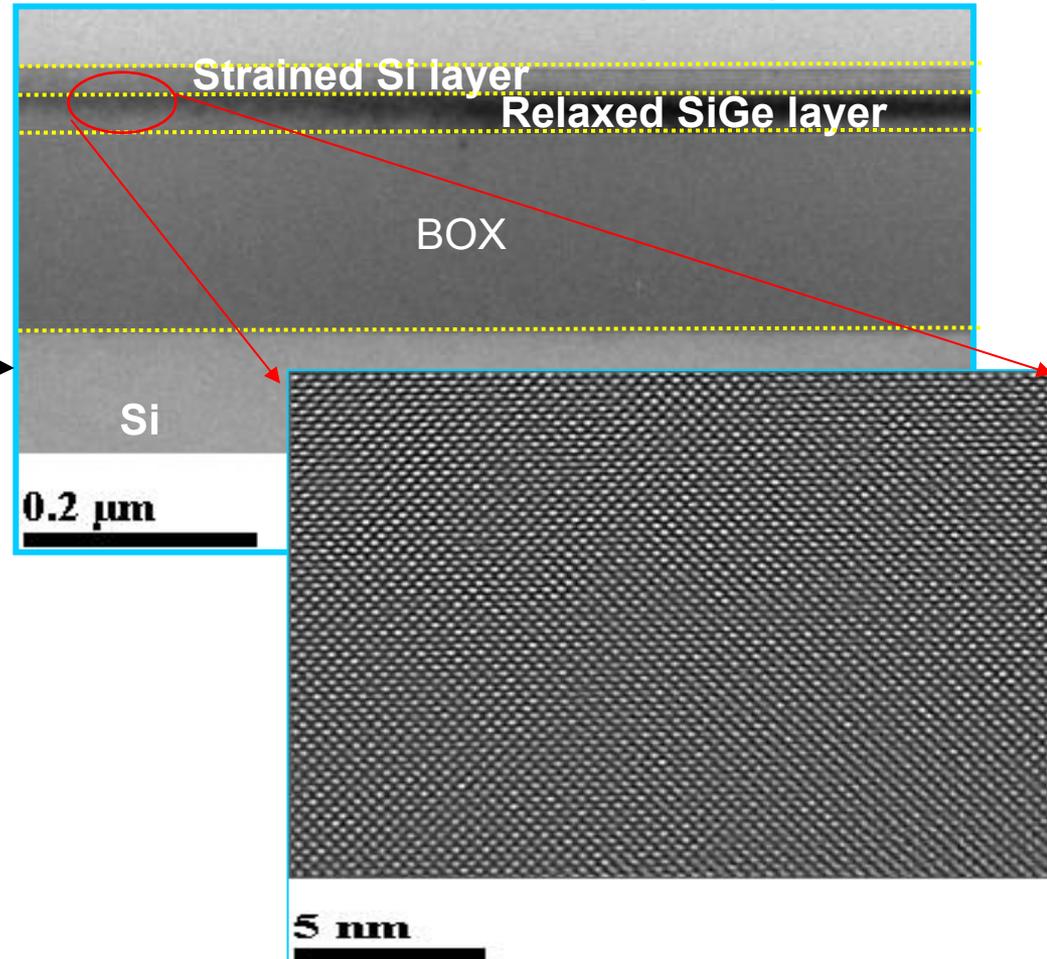
Advantages

- Provides accurate film thickness
- Excellent contrast between films
- Provides film interface information
- Provides information on crystallinity
- High resolution (higher than SEM)

Disadvantages

- Destructive; samples need thinning, down to $<50 \mu\text{m}$
- Specimen preparation is time and labor intensive (2-3 hrs typical)
- Image artifacts require expert interpretation of micrographs
- Samples may be sensitive to electron-beam damage
- Sample may not be representative

SiGe on Insulator (SGOI)



March 15, 2005

10

2005 International Conference on Characterization and Metrology for ULSI Technology, University of Texas at Dallas
Freescale™ and the Freescale logo are trademarks of Freescale Semiconductor, Inc.

All other product or service names are the property of their respective owners. © Freescale Semiconductor, Inc. 2004

Spectroscopic Ellipsometry (SE)

Capabilities

- Uses polarized light for stacked film optical thickness (refractive index)
- Elemental composition

Advantages

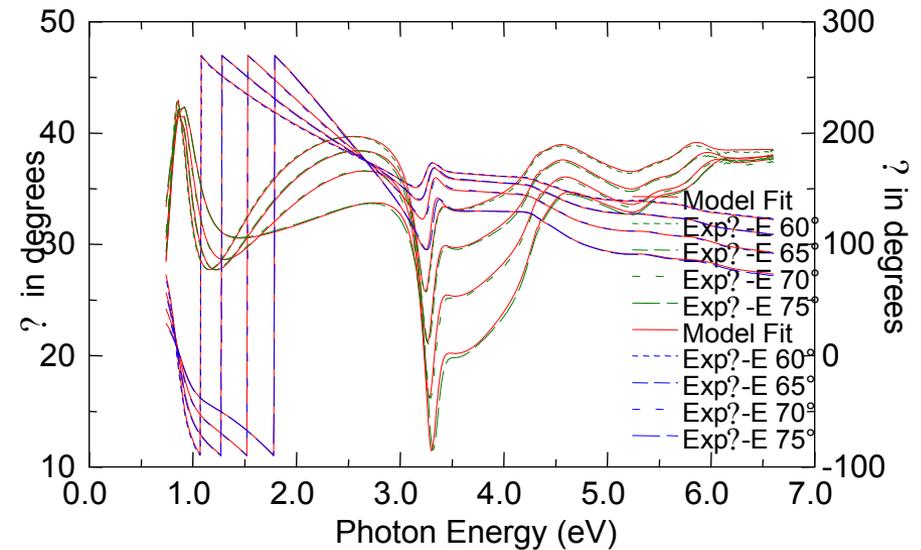
- Rapid
- Non-destructive
- Many in-line systems available
- Small spot size (25 μm) for features

Disadvantages

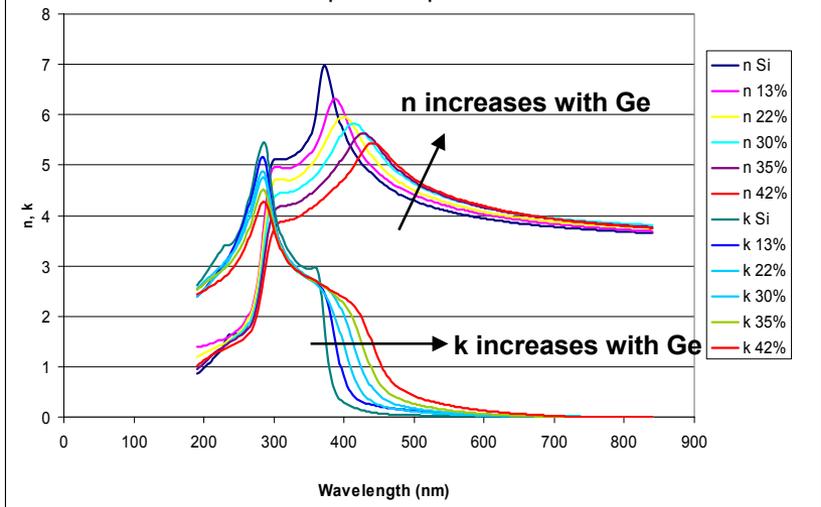
- Requires transparent films
- Does not measure quantities directly
- Quantifiable only with standards
- Difficult for thin conformal Si layer on rough relaxed SiGe
- Problems with fits when substrate stress is different from model stress

Need expanded SE models for high Ge concentration

SE of SSOI wafer



Lookup SiGe Component vs. nm



March 15, 2005

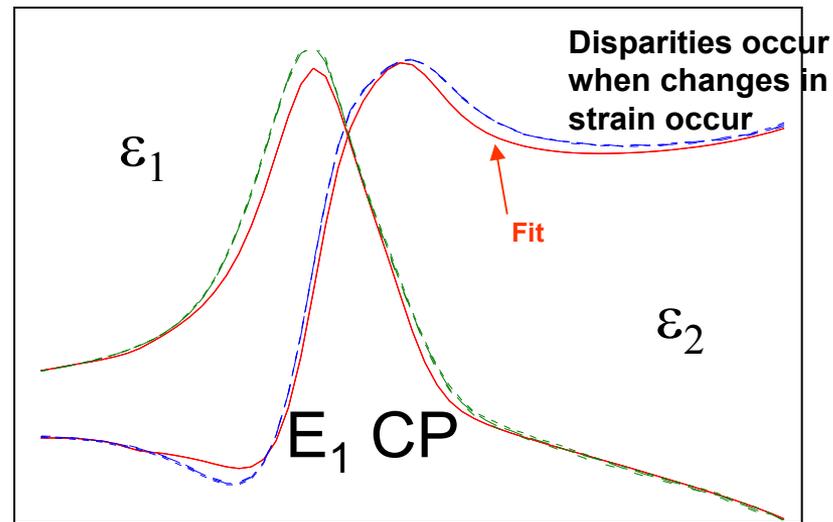
11

2005 International Conference on Characterization and Metrology for ULSI Technology, University of Texas at Dallas

Freescale™ and the Freescale logo are trademarks of Freescale Semiconductor, Inc.

All other product or service names are the property of their respective owners. © Freescale Semiconductor, Inc. 2004

Spectroscopic Ellipsometry (SE)



Sample was rough (typical for thick relaxed SiGe)

- Problems with fit (red)
- Fitting strained Si ellipsometry data with unstrained Si optical constants yields questionable results

- Limitations of SE--changes in optical properties from process-induced relaxation
- Requires more accurate models

Optical constants change as a function of strain.
Need a more robust technique if optical constants change.

Alternative to SE: X-Ray Reflectivity Spectrometry (XRR)

Capabilities

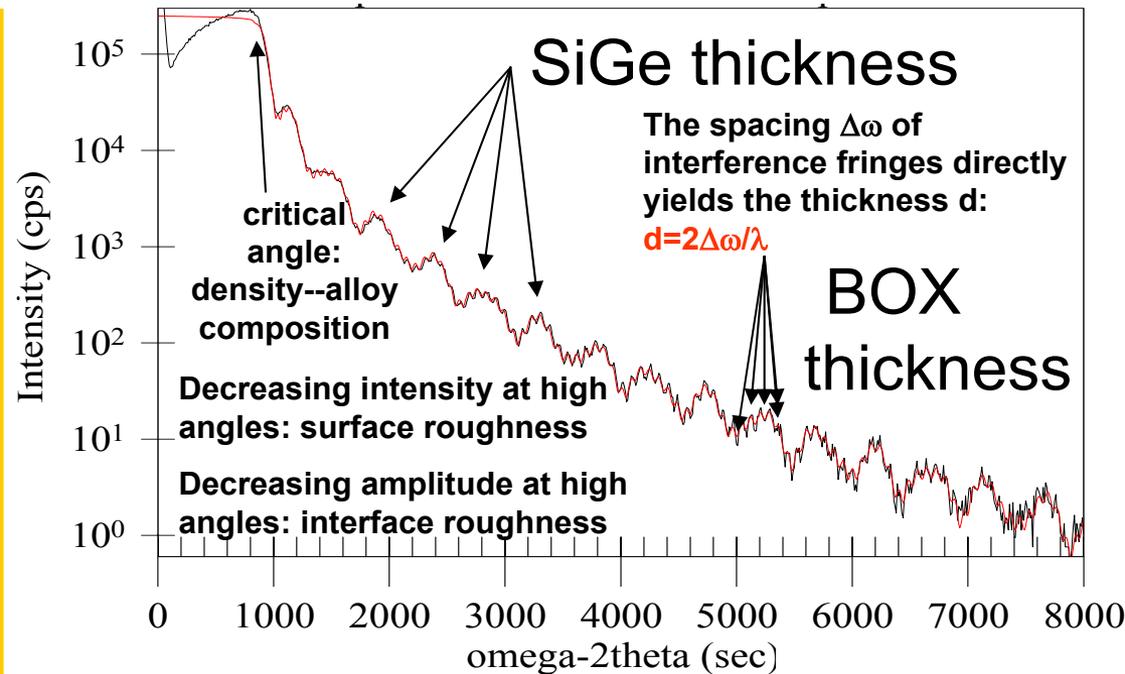
- Stacked film thickness, density, surface/interface roughness
- Most accurate in-line thin film metrology

Advantages

- Nondestructive
- Rapid
- X-rays penetrate optically opaque films

Disadvantages

- Works best on smooth samples; diffuse scattering on rough samples lowers beam intensity reaching deep layers
- Sensitive to wafer smoothness and curvature
- Spot size, $80\mu\text{m} \times \sim 3\text{mm}$
- Ge diffusion reduces density contrast



March 15, 2005

13

2005 International Conference on Characterization and Metrology for ULSI Technology, University of Texas at Dallas

Freescale™ and the Freescale logo are trademarks of Freescale Semiconductor, Inc.

All other product or service names are the property of their respective owners. © Freescale Semiconductor, Inc. 2004

X-ray Diffraction (XRD)

Capabilities

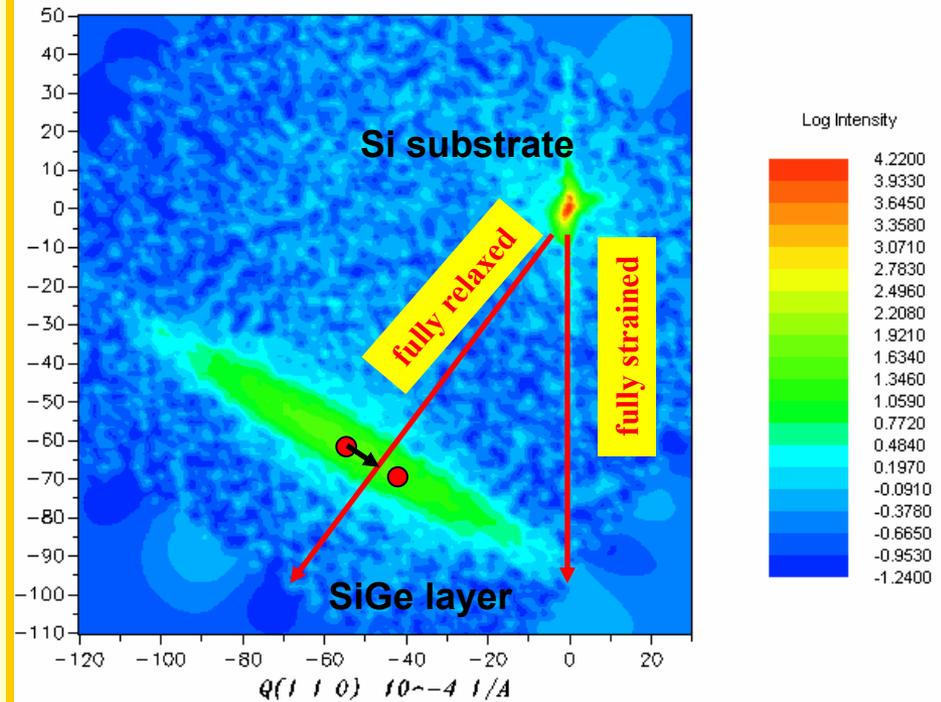
- Strain/stress
- Film thickness
- Composition

Advantages

- In-line monitoring tools available
- Non-destructive
- Rapid
- High-accuracy

Disadvantages

- Strain measurement straight-forward only on bulk Si wafers
- Strain measurement on SOI wafers is time-consuming
- Requires triple-axis reciprocal space maps



Capable of determining substrate off-cut and layer tilt

March 15, 2005

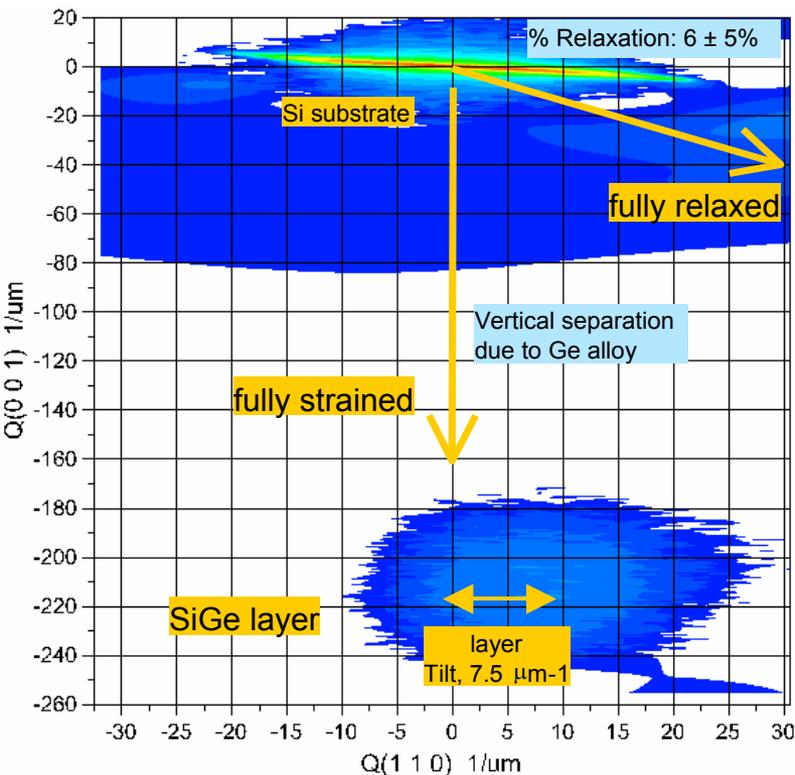
14

2005 International Conference on Characterization and Metrology for ULSI Technology, University of Texas at Dallas

Freescale™ and the Freescale logo are trademarks of Freescale Semiconductor, Inc.

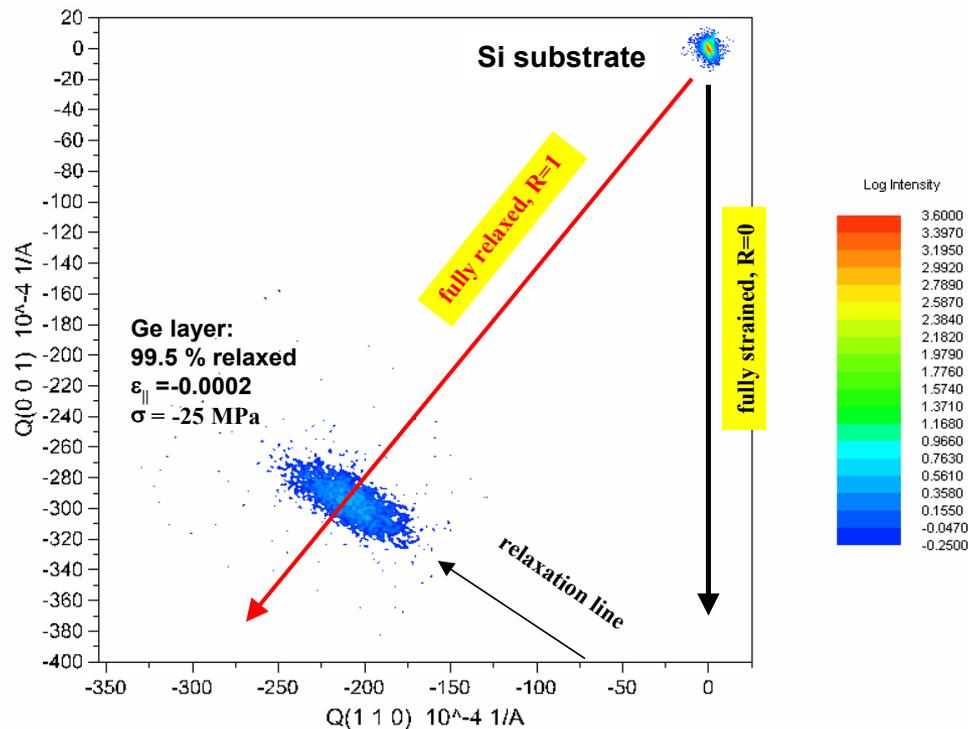
All other product or service names are the property of their respective owners. © Freescale Semiconductor, Inc. 2004

XRD Stress Measurement on SOI Using Reciprocal Space Maps



Fully Strained SiGe substrate

Fully strained layer (neglecting layer tilt) appears directly below the substrate. This confirms that the SiGe epilayer is nearly fully strained. A fully relaxed layer should appear along the arrow to the bottom right.



Fully Relaxed SiGe substrate

Fully strained layer (neglecting layer tilt) appears directly below the Si substrate. This confirms that the SiGe epilayer is nearly fully relaxed.

March 15, 2005

15

Secondary Ion Mass Spectrometry (SIMS)

Capabilities

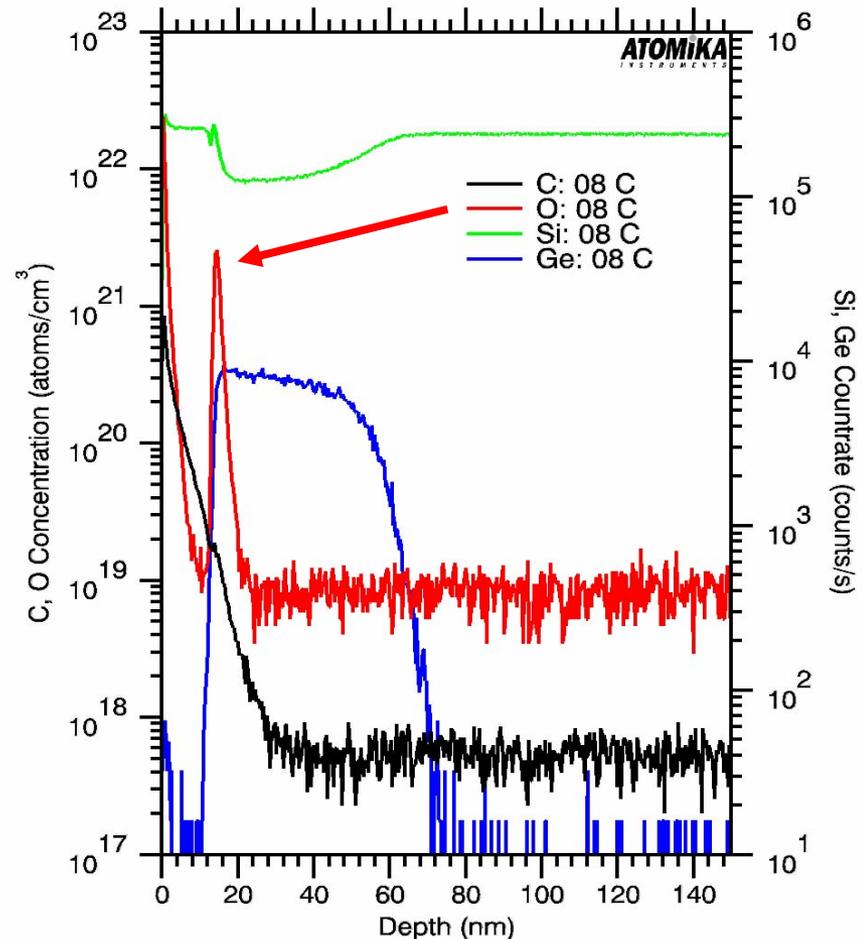
- Elemental composition and film thickness
- Determination of dopant profiles
- Identification of surface and bulk contaminants; Ge up-diffusion into Si channel (SGOI)

Advantages

- ppm/ppb detection sensitivity
- All elements detectable (H to U)
- Analysis possible on conductive or insulating samples
- Compositional maps are attainable

Disadvantages

- Destructive
- Quantifiable only with standards
- Isobaric mass interferences
- Time intensive data collection
- Nonlinear Ge yield with composition, charging
- Degradation of depth resolution for thin conformal Si layers on rough SiGe buffer



Oxide at Si and SiGe interface: effect of queue time between HF-last clean and epi.

March 15, 2005

16

2005 International Conference on Characterization and Metrology for ULSI Technology, University of Texas at Dallas

Freescale™ and the Freescale logo are trademarks of Freescale Semiconductor, Inc.

All other product or service names are the property of their respective owners. © Freescale Semiconductor, Inc. 2004

Auger Spectroscopy

Capabilities

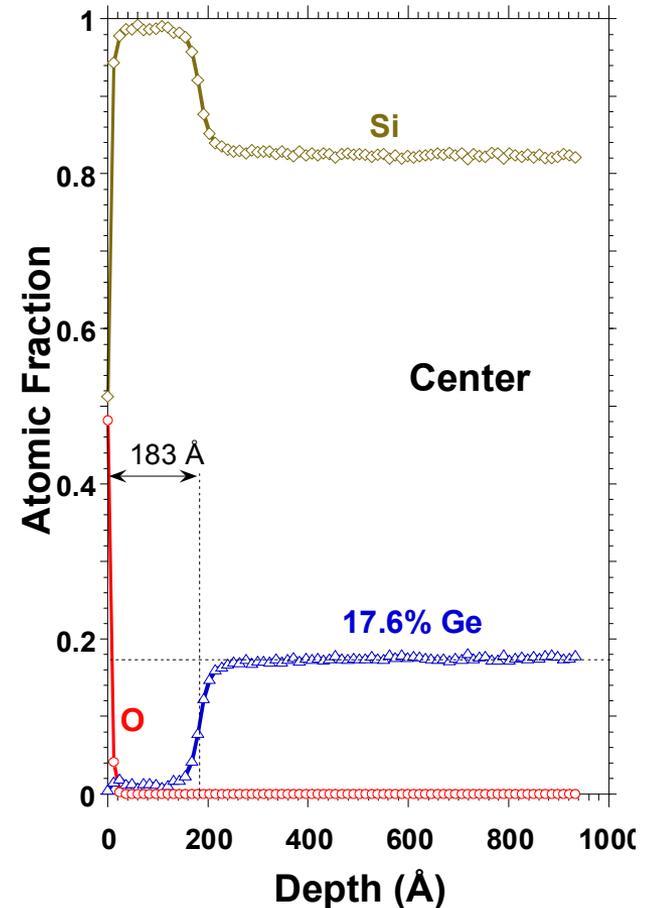
- Film thickness and elemental composition
- Sputter depth-profiling of multi-layered structures and films

Advantages

- Excellent spatial resolution—can analyze particles as small as 300 Å
- Excellent depth resolution—approximately 30Å
- Quantitative—good for quick stoichiometric checks
- Minimum detection sensitivity of a few atomic percent

Disadvantages

- Destructive
- Sample must be vacuum compatible
- Small sample—a few cm², same as SEM (full wafer tools available)
- Cannot detect H or He; 3 e⁻ process
- Charging may affect data collection on insulating samples
- Auger electron energy interferences exist (e.g., Ti & N)



Strained Si on thick SiGe buffer layer on bulk wafer

Rutherford Backscattering (RBS)

Capabilities

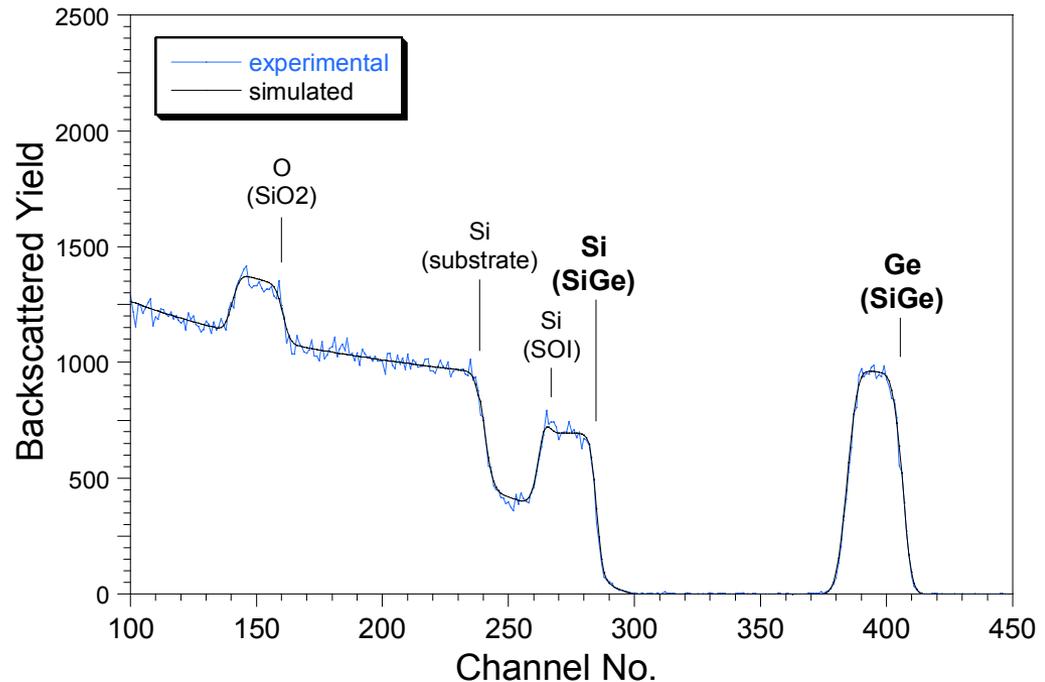
- Elemental composition and film thickness
- Multilayer capability
- Energy of a backscattered particle determines mass of the target atom

Advantages

- Rapid analysis; no standards required; simple spectra
- Sensitive to heavy elements in light matrix
- Analysis possible on conductive or insulating samples

Disadvantages

- Destructive
- Insensitive to light elements in a heavy matrix
- Requires smooth surface



Wafer (SiGe on SOI)	SE-Average SiGe Thickness (Å)	SE-Average Ge Composition (%)	Auger SiGe Thickness (Å ± 100Å)	Auger Ge Composition (%)	TEM SiGe Thickness (Å)	RBS SiGe Thickness (Å ± 100Å)	RBS Ge Composition (%)	SIMS Ge Composition (%)
Wafer 1 C	1260	23.63	1390	23.6	1290-1360	1300	23.5	19.5
Wafer 1 E					1250-1270	1300	21.7	21.2
Wafer 2 C	1658	27.00	1828	30.2	1770-1880	1700	29.6	27.2
Wafer 2 E					1620	1500	27.9	37.0
Wafer 3 C	xx	xx	1935	35.4	1700-2000	1800	35.0	36.6
Wafer 3 E					1120-1300	1700	34.8	29.5
Wafer 4 C	xx	xx	1795	41.1	1420-1980	1700	40.9	44.4
Wafer 4 E					1500-1960	1700	42.1	39.0

X-ray Fluorescence Spectrometry (XRF)

Capabilities

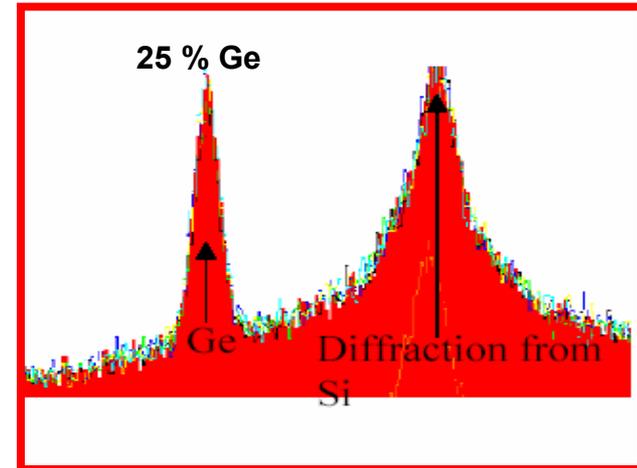
- Multi-element composition
- Good precision
- Fluorescence intensity is proportional to atomic density

Advantages

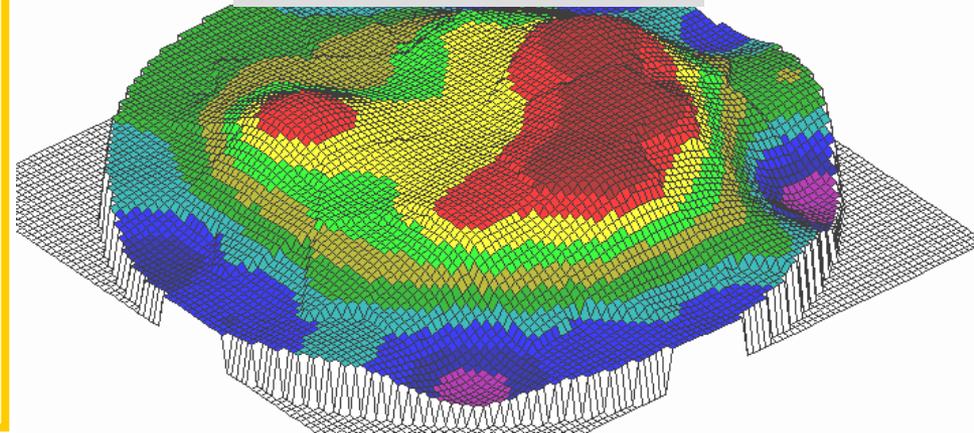
- Spot size (40 μ m)
- ppm capability in a few cases; more commonly, 0.01% detection limits
- Simple spectra
- Whole wafer analysis
- Non-destructive

Disadvantages

- Calibration standards required
- Some elements (e.g. Ge) have low fluorescence yield (long acquisition times)
- Matrix effects (fluorescence absorption and enhancement) must be compensated
- Only elements beyond O detectable



SiGe Ge Map by XRF



March 15, 2005

19

2005 International Conference on Characterization and Metrology for ULSI Technology, University of Texas at Dallas

Freescale™ and the Freescale logo are trademarks of Freescale Semiconductor, Inc.

All other product or service names are the property of their respective owners. © Freescale Semiconductor, Inc. 2004

Strain and Composition Measurement: UV Raman

Capabilities

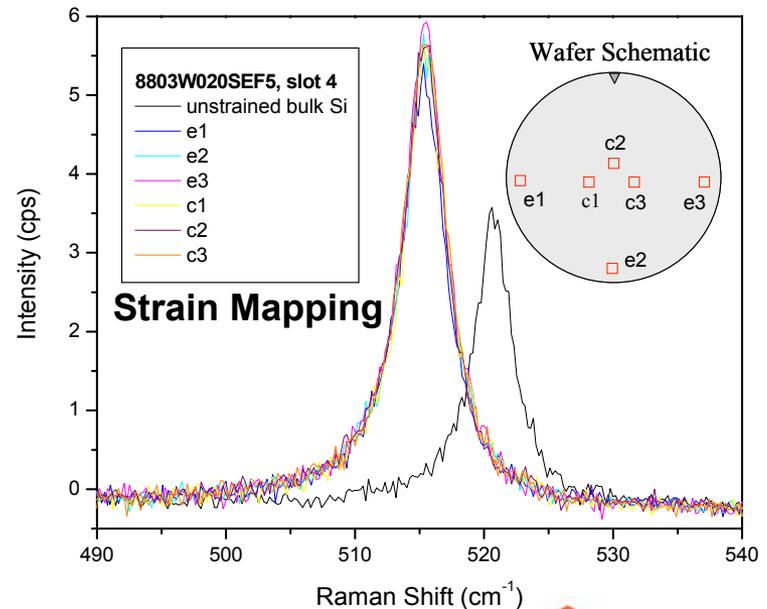
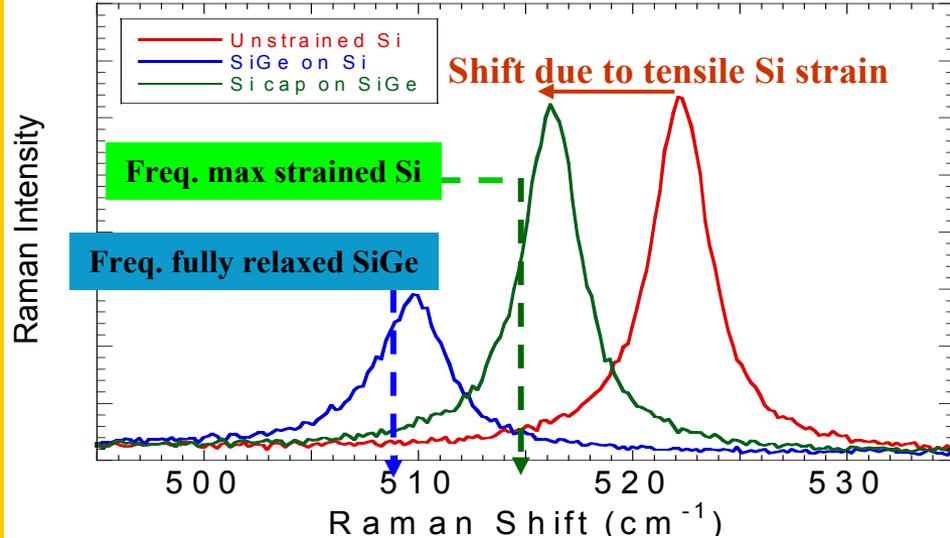
- Composition, crystallinity, strain/stress
- Phonon frequency shift in Si used to determine strain in Si channel
- Peak broadening related to defects: dislocations, disorder, Ge outdiffusion, strain nonuniformity

Advantages

- Non-destructive, no sample preparation
- Rapid (364 nm Ar-ion laser resonance Raman 10X faster than 325 nm He-Cd laser non-resonance Raman)
- Small spot size ($0.4 \mu\text{m}$)
- Not affected much by roughness
- Control of penetration depth ($325\text{nm} < 10 \text{ nm}$)

Disadvantages

- No in-line monitoring tools available for patterned wafers
- Requires complex data interpretation
- Ge composition variation (out-diffusion) affects accuracy of derived strain value.



March 15, 2005

20

Atomic Force Microscopy (AFM)

Capabilities

- Provides high-resolution surface roughness and atomic structure measurements

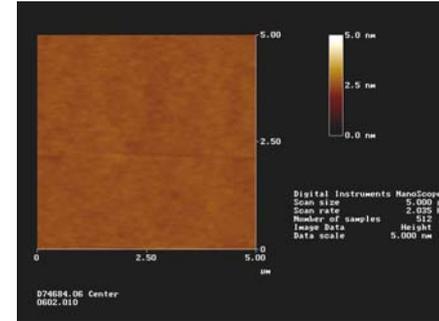
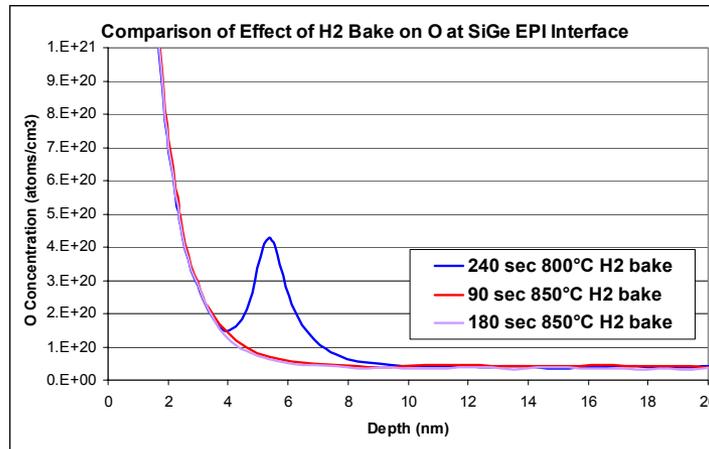
Advantages

- No sample preparation required

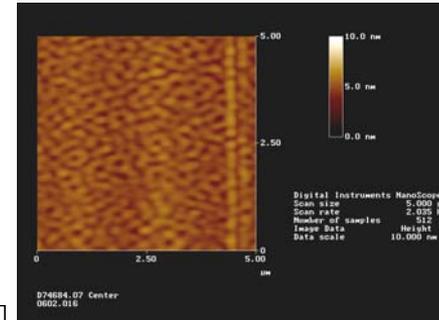
Disadvantages

- Small sampling area
- No chemical information provided
- Time-intensive
- Resolution affected by tip wear

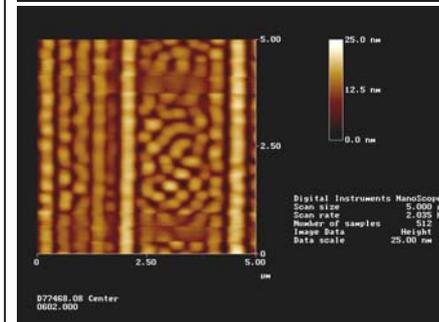
High temperature H₂ bakes eliminate O at SiGe/SiGe interface after SiGe regrowth, but SiGe relaxes—increasing surface roughness



240 sec 800°C H₂ bake



90 sec 850°C H₂ bake



180 sec 850°C H₂ bake

March 15, 2005

21

2005 International Conference on Characterization and Metrology for ULSI Technology, University of Texas at Dallas

Freescale™ and the Freescale logo are trademarks of Freescale Semiconductor, Inc.

All other product or service names are the property of their respective owners. © Freescale Semiconductor, Inc. 2004

Schimmel Etch

Capabilities

- Used when defect density is too low for TEM (sets upper limit of TDD = $1e7/cm^2$)
- Technique for assessing damage introduced into silicon wafer
- The count of pits provides a quantity for damage intensity
- Using preferential etching, the damage of the surface boundary zone in the Si wafer, esp. dislocations and microcracks, are detected

Advantages

- Rapid and sensitive
- Applicable to large areas
- Reliable way of determining defect density
- Simple interpretation

Disadvantages

- Destructive



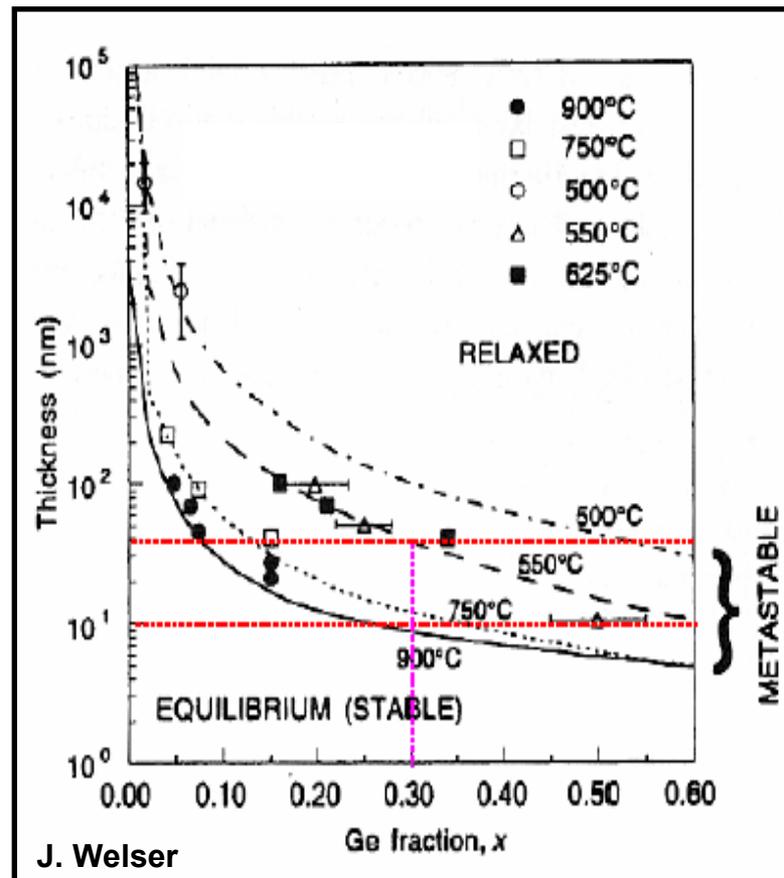
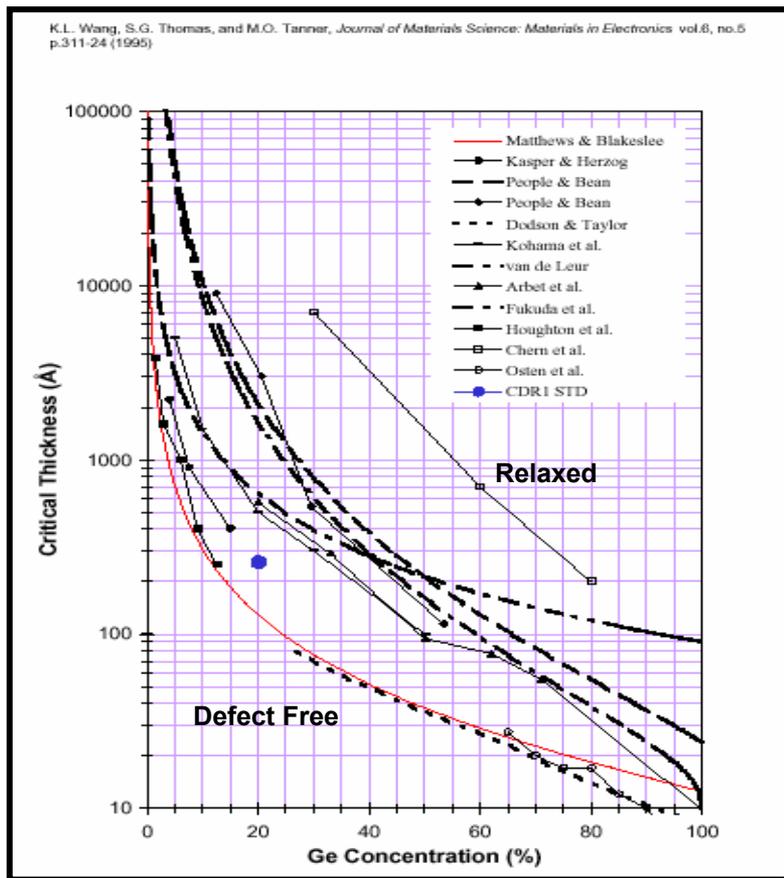
High density of misfit dislocations near the interface between SiGe and BOX.

Some misfit dislocations are observed with faint contrast.

Overview of Strained Si Metrology for Strained-Si

- ✓ **Metrology for Defect Analysis**
- Metrology for Substrate Characterization
- Metrology for Process Effects
- Emerging In-Line Metrology
- Summary

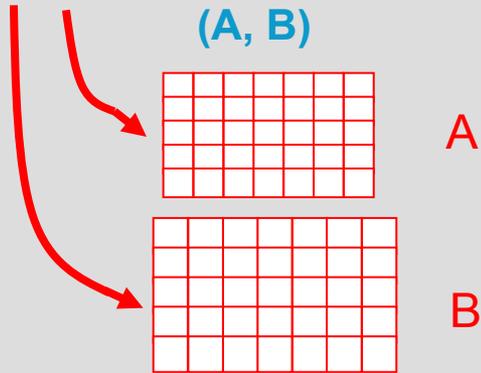
Material Challenges for Strained-Si—Critical Thickness



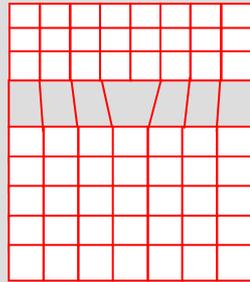
- MD's set an upper limit for strained-Si thickness for a given Ge concentration.
- Critical thickness decreases with increased Ge content and temperature.

Material Challenges for Strained-Si—Misfit (MD) and Threading Dislocations (TD)

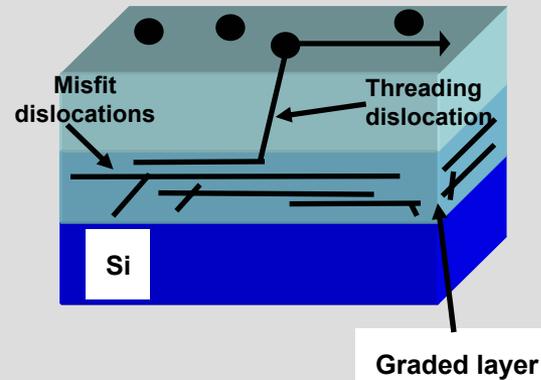
Lattice mismatched materials (A, B)



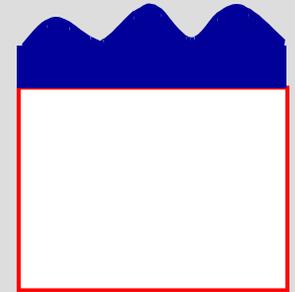
Misfit dislocation



Leakage sites



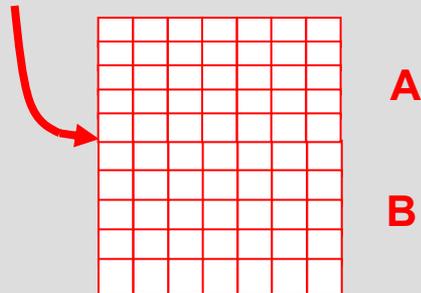
Surface roughness



mobility degradation

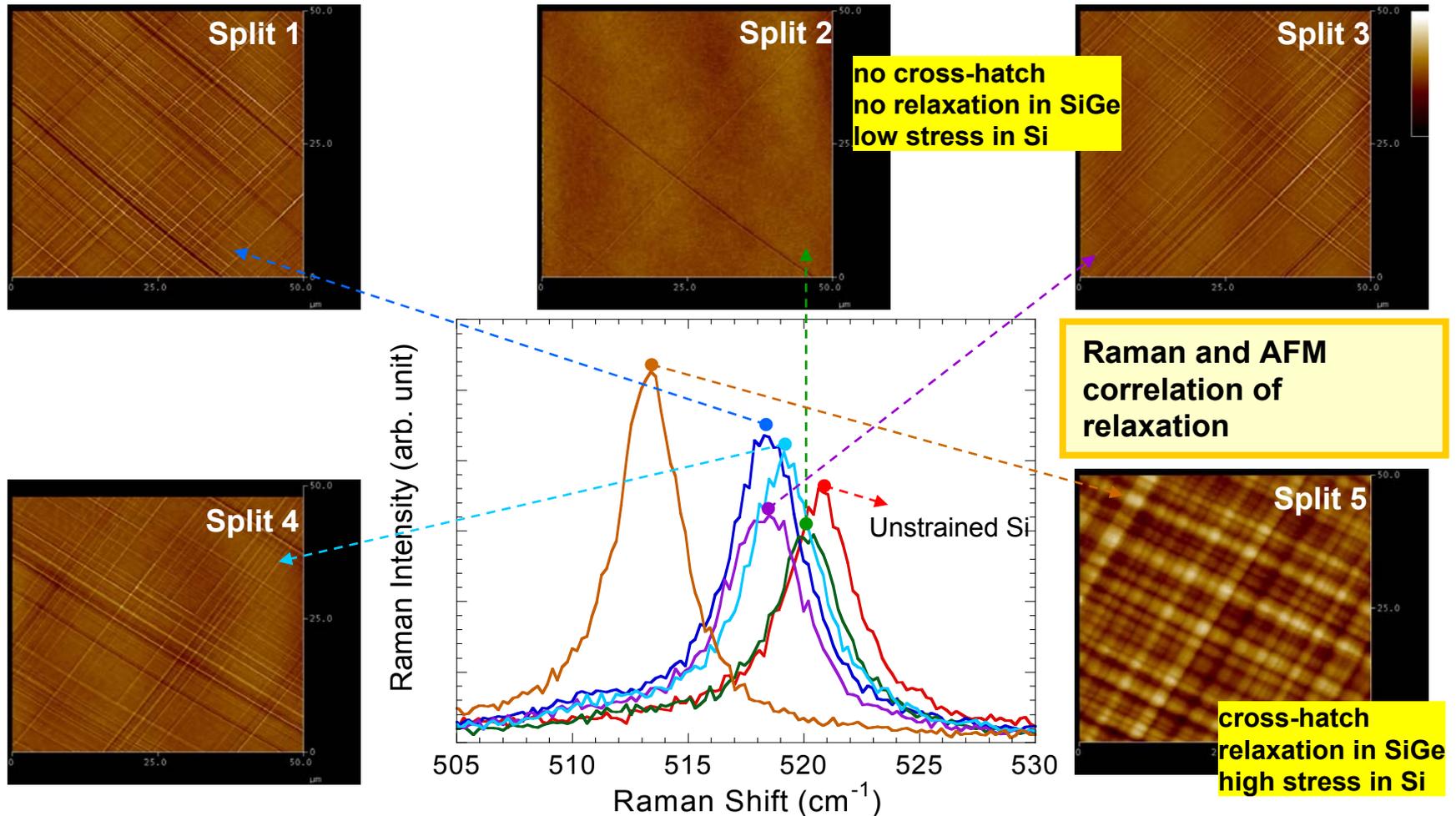
Pseudomorphic growth—smooth, no defects

A and B match at the interface



- Gliding mechanisms cause dislocations
- Device performance sets upper limit on dislocation density and roughness
- Non-uniform spatial strain distribution
- Spatial uniformity of strain
- **In-line metrology with high spatial resolution required with shallow penetration depth for surface layer analysis**

Ultrathin Si (~10 nm) on SiGe—Correlation of UV Raman and AFM: Effect of Relaxation on Surface Roughness

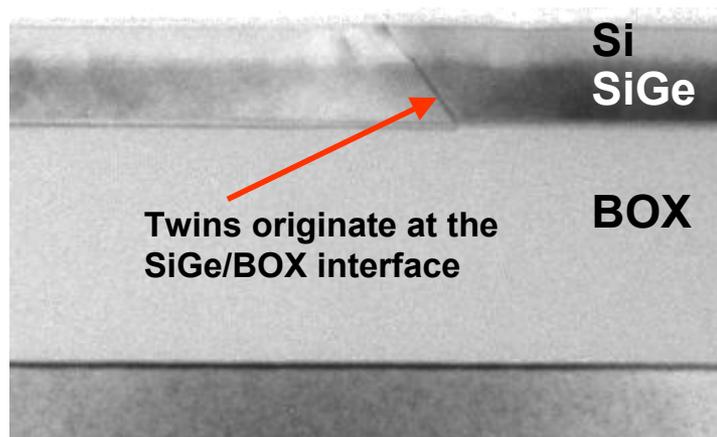
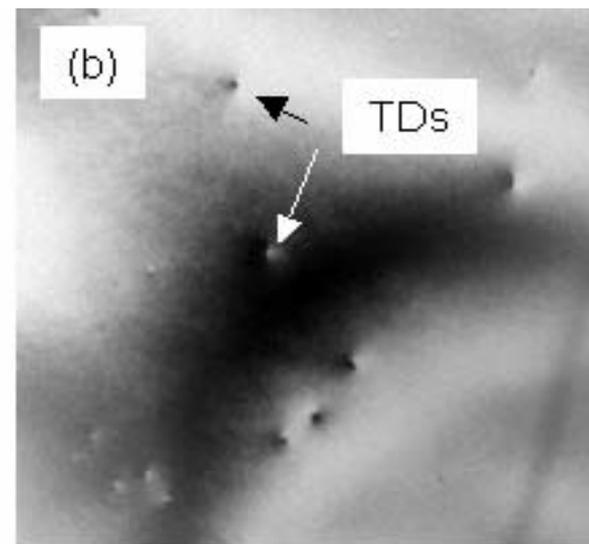
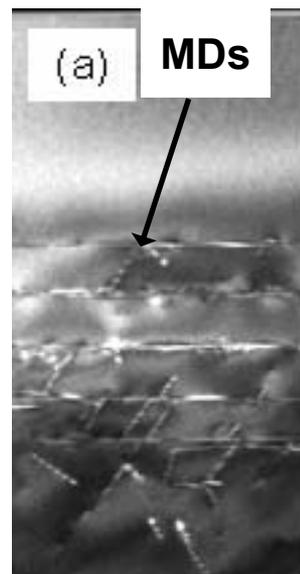


Higher SiGe relaxation => More biaxial Si tensile strain => more cross hatch pattern

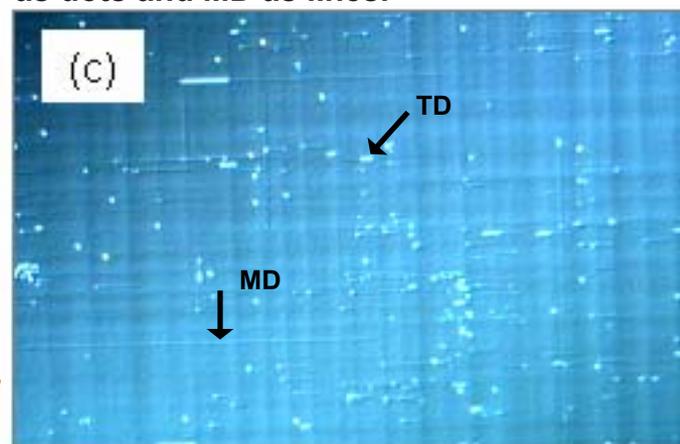
Material Challenges for Strained-Si—Misfit (MD) and Threading Dislocations (TD)

Dislocations confined in the gradient buffer layer region.

- MD's in the buffer develop into threading dislocation (TD) segments.
- TD's act as diode leakage sites and must be reduced preferably below 1.0×10^4 defects/cm².



TEM reveals how TDs intersect with the strained Si channel region.



100 nm

These techniques are all destructive!

March 15, 2005

27

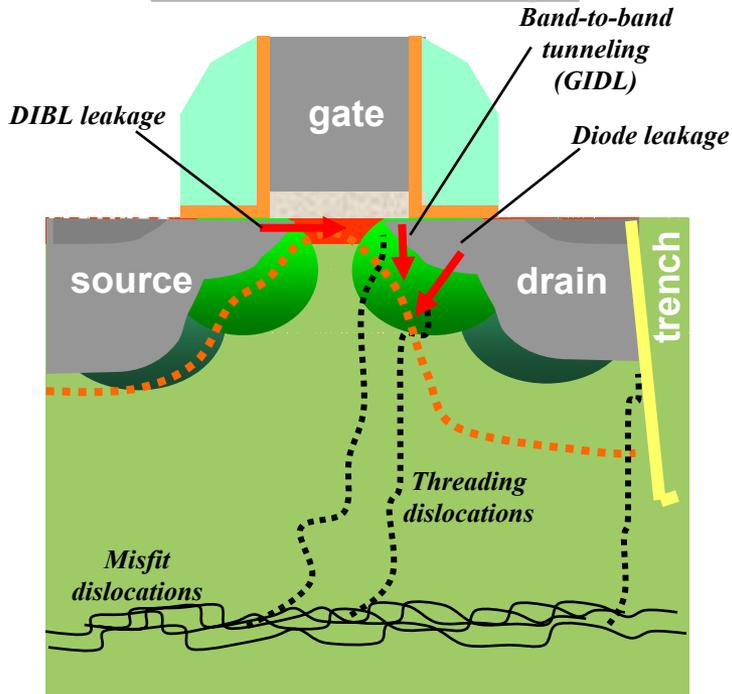
2005 International Conference on Characterization and Metrology for ULSI Technology, University of Texas at Dallas

Freescale™ and the Freescale logo are trademarks of Freescale Semiconductor, Inc.

All other product or service names are the property of their respective owners. © Freescale Semiconductor, Inc. 2004

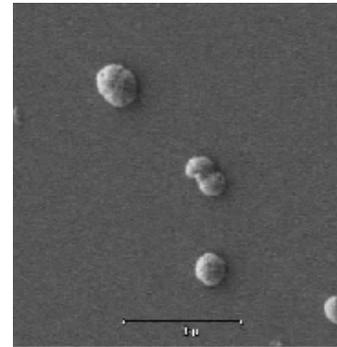
Importance of Reducing Defect Density

Subthreshold Leakages

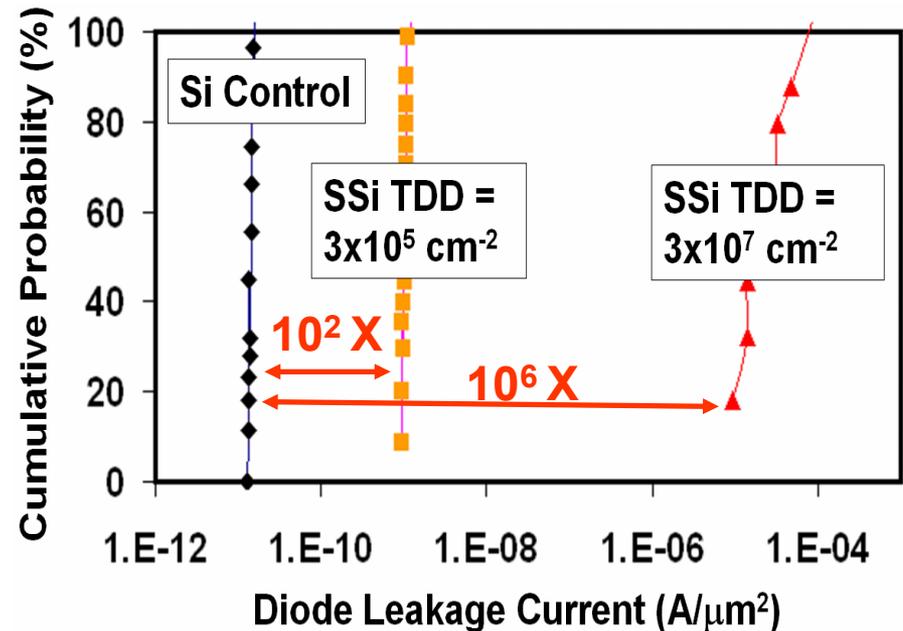
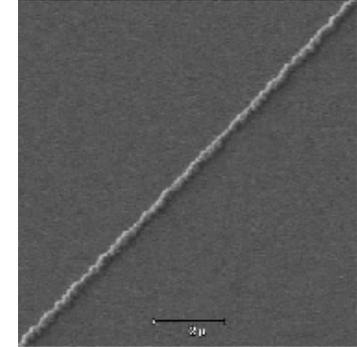


- Defect density control is critical to minimize leakage
- Application (High-Performance/Low-Power) determines choice of Ge content.

Threading Dislocations



Pile-ups



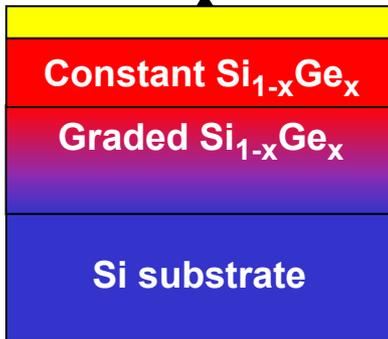
March 15, 2005

28

- Overview of Strained Si
- Metrology for Strained-Si
- Metrology for Defect Analysis
- ✓ **Metrology for Substrate Characterization**
- Metrology for Process Effects
- Emerging In-Line Metrology
- Summary

Strained-Si Substrate Options

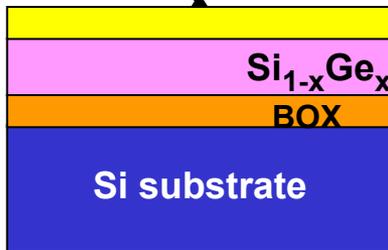
Strained Si channel



I. Strained-Si on bulk Si substrates

- Graded buffer layer approach

Strained Si channel



II. Strained-Si on insulator substrates

- Combines benefits of mobility enhancement of strained Si with benefits of SOI

Tensile-strained Si on relaxed SiGe-on-insulator approach (SGOI)

- Layer transfer
- Condensation (oxidation with HCl) to relax SiGe, enrich Ge

Strained-Si-on-insulator approach (SSOI)

- Layer transfer

March 15, 2005

2005 International Conference on Characterization and Metrology for ULSI Technology, University of Texas at Dallas

Freescale™ and the Freescale logo are trademarks of Freescale Semiconductor, Inc.
All other product or service names are the property of their respective owners. © Freescale Semiconductor, Inc. 2004

Launched by Motorola

 **freescale**
semiconductor

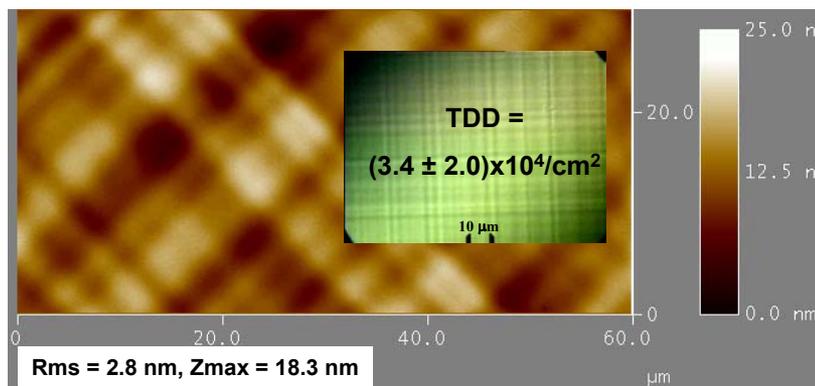
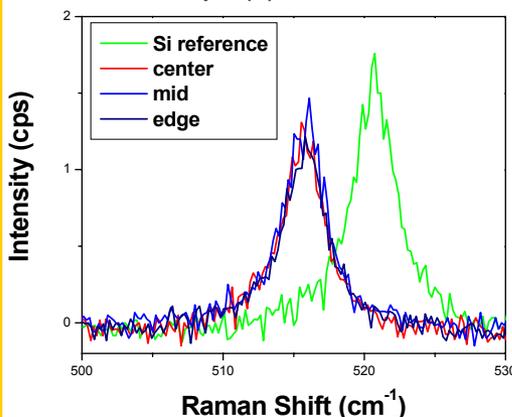
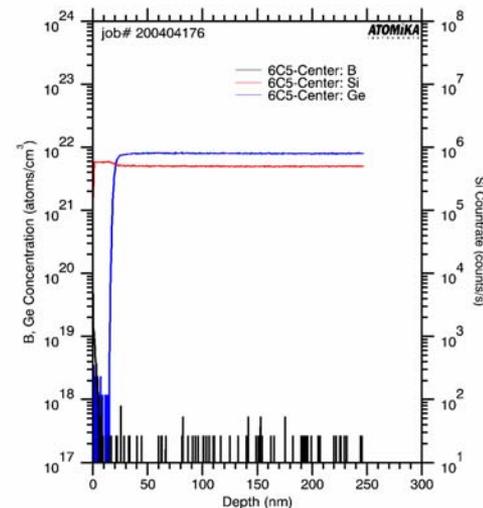
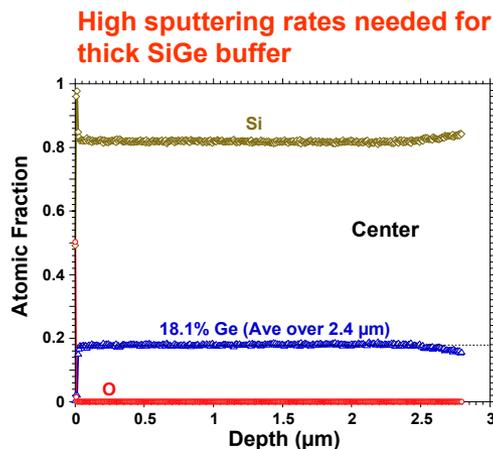
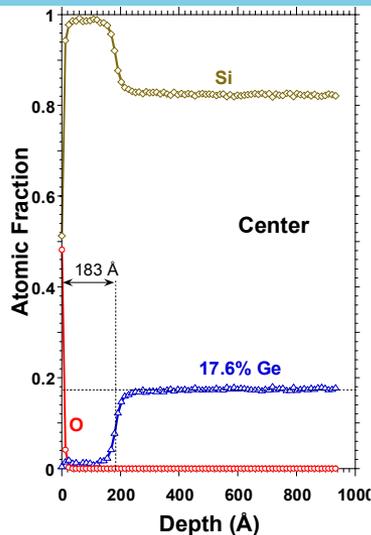
I. Strained-Si on Bulk Substrates

• Auger, and SIMS show the Ge profile in the graded SiGe, SiGe buffer and strained Si.

• AFM shows RMS ~3nm and a cross-hatch pattern.

• Si cap strain is 99% (SiGe 99% relaxation) based on ~17% Ge; excellent crystallinity compared to Si reference.

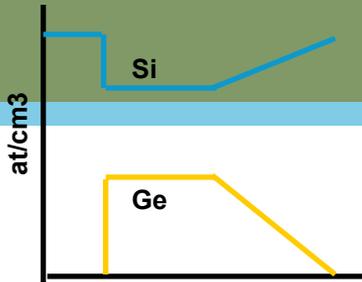
• Etch pit density ~ $5e4$ defects/cm².



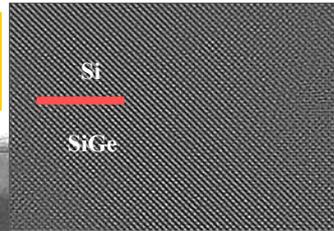
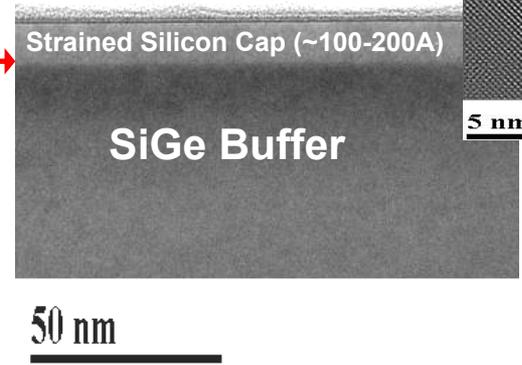
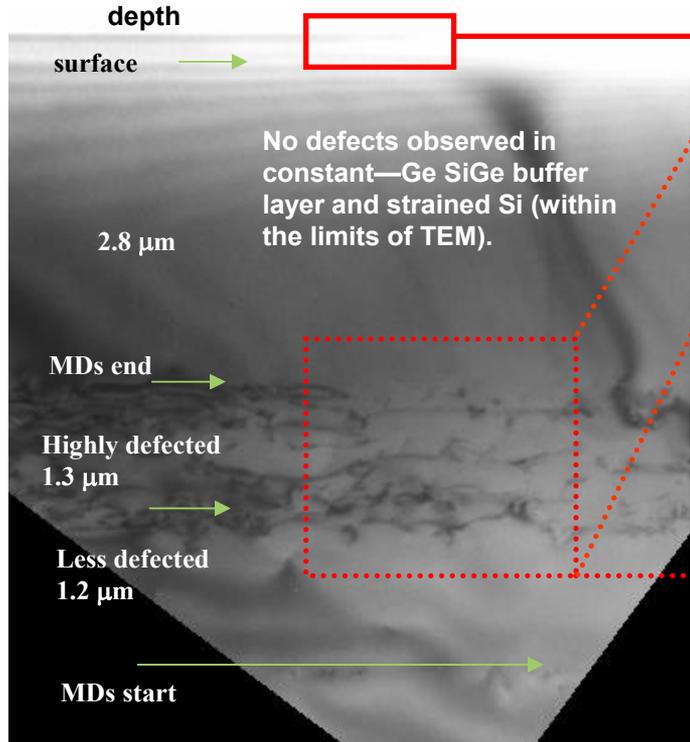
sample	Auger %Ge	Si-Si/Si phonon											
		measured freq	fully strained freq	shift from relaxed Si	remaining strain	relaxed strain	max strain	remaining stress	relaxed stress	max stress	% strained	measured FWHM	% deviation from relaxed Si FWHM
	(%)	(cm ⁻¹)	(cm ⁻¹)	(cm ⁻¹)				(GPa)	(GPa)	(GPa)	(%)	(cm ⁻¹)	(%)
Si reference		520.70		0.00	0.0000	0.0000	0.0000	0.00	0.00	0.00	0.0	3.64	0.0
center	17.6	515.67	515.62	-5.03	0.0065	0.0001	0.0066	1.17	0.01	1.19	99.1	3.53	-2.9
mid	17.3	515.79	515.71	-4.91	0.0064	0.0001	0.0065	1.15	0.02	1.16	98.4	3.50	-4.0
edge	17.2	515.80	515.74	-4.90	0.0064	0.0001	0.0064	1.14	0.01	1.16	98.8	3.65	0.2

March 15, 2005

I. Strained-Si on Bulk Substrates



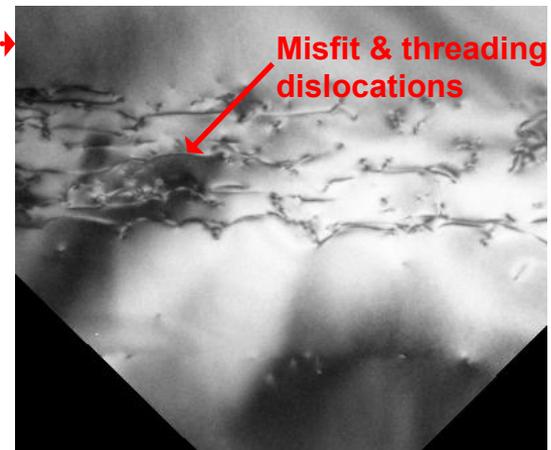
• Very good Si/SiGe interface.



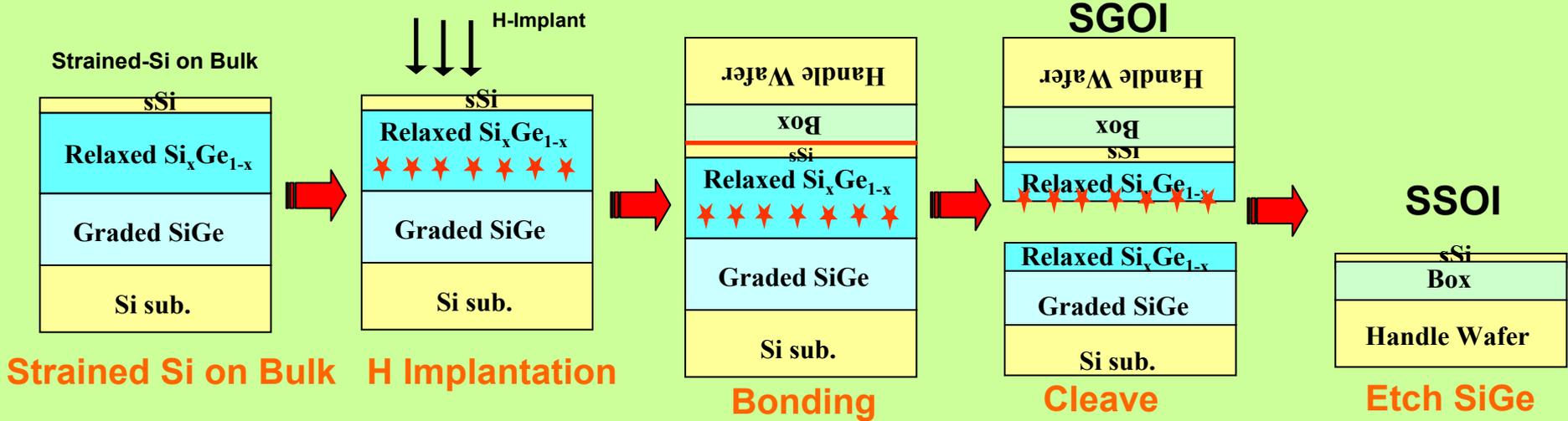
• TEM: Plan-view and cross-sectional;
 • Threading dislocation density ($1e4/cm^2$ upper limit)
 • Other defects (twins, misfits at buffer/channel interface)

$1 \mu m$ EPD = $1e5/cm^2$

• Trapping of misfits in the graded SiGe buffer.



Layer Transfer Approach—Strained-Si on SOI



SGOI:

- Bond relaxed SiGe on bulk substrates.
- Epitaxially grown strained-Si channel on relaxed SiGe.

SSOI:

- Bond Strained Si on relaxed SiGe on bulk substrates.
- Etch SiGe selectively and stop on strained Si.

Challenges

- Need two wafers, a donor and a handle wafer.
- Defectivity only as good as starting material.

Advantages

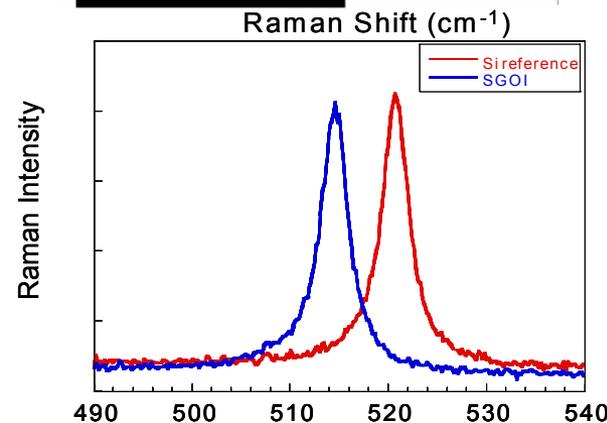
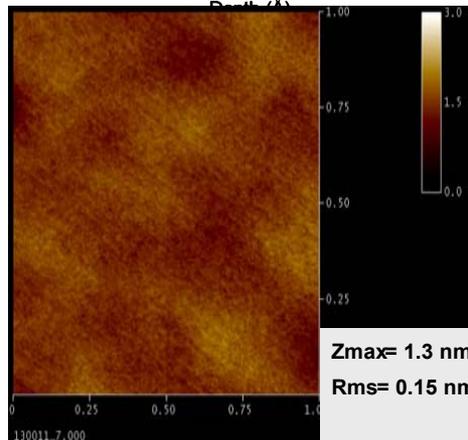
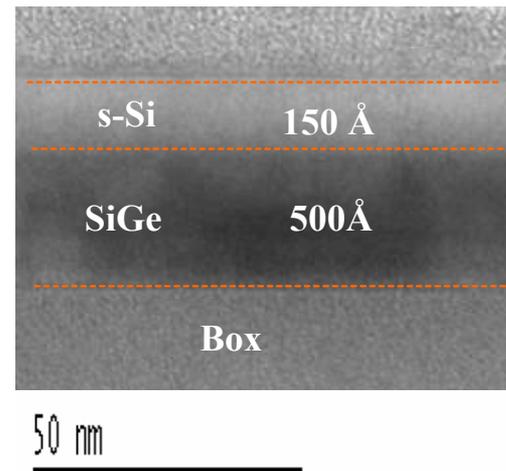
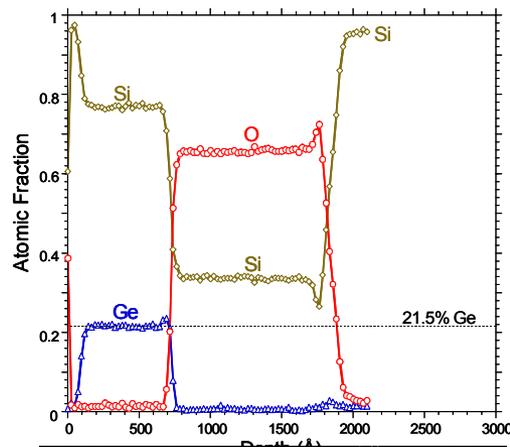
- Transfer thin layers directly on Box.
- Strained Si directly on insulator or relaxed SiGe directly on insulator.

March 15, 2005

33

II. Strained-Si on SiGe-On-Insulator (SGOI) Substrates—Layer Transfer

- TEM x-section shows $T_{Si}=15\text{nm}$ and $T_{SiGe}=50\text{nm}$.
- Very good Si/SiGe and SiGe/Box interfaces with no observed defects.
- Smooth surface (RMS~0.15nm).
- Etch pit density of $1\text{e}6$ defects/ cm^2 .
- 88% relaxation based on ~21% Ge.



Si-Si/Si freq						
measured	shift from relaxed Si	strain	stress (GPa)	XRD % Ge (%)	fully strained (cm⁻¹)	% strained (%)
(cm⁻¹)	(cm⁻¹)					
513.44	-7.26	0.0072	1.29	21.8	512.42	88

March 15, 2005

34

2005 International Conference on Characterization and Metrology for ULSI Technology, University of Texas at Dallas

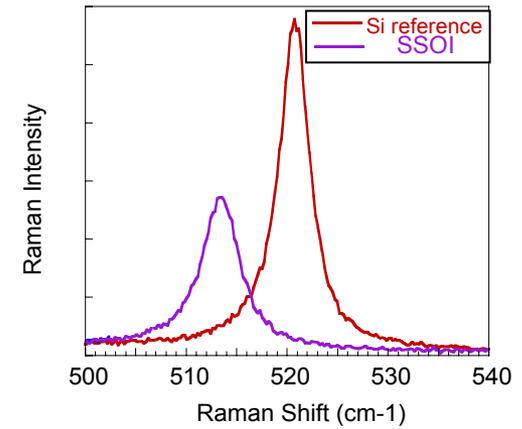
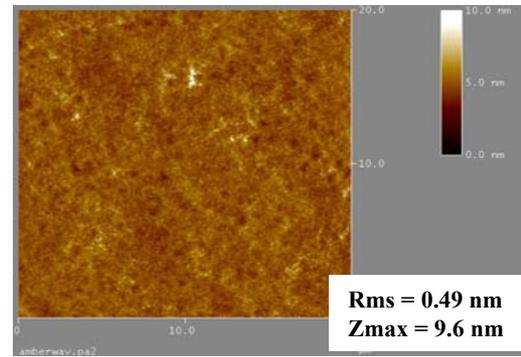
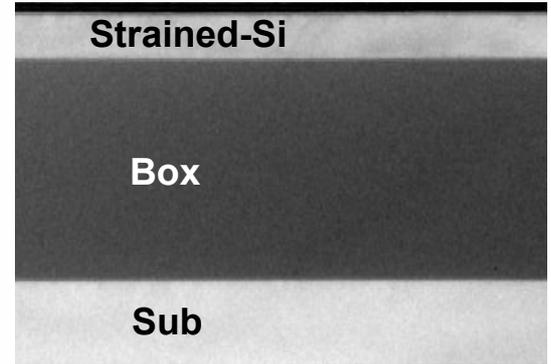
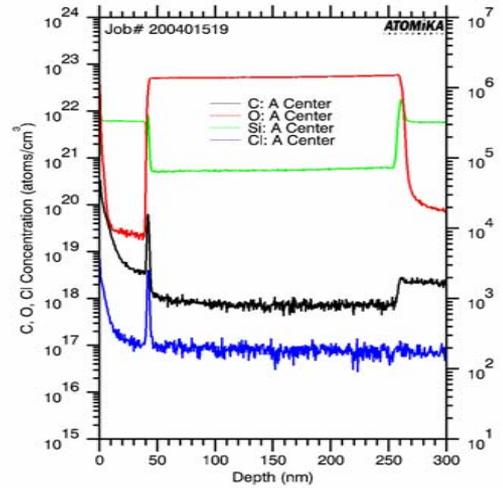
Freescale™ and the Freescale logo are trademarks of Freescale Semiconductor, Inc.

All other product or service names are the property of their respective owners. © Freescale Semiconductor, Inc. 2004



III. Strained-Si on Insulator (SSOI) Substrates—Layer Transfer

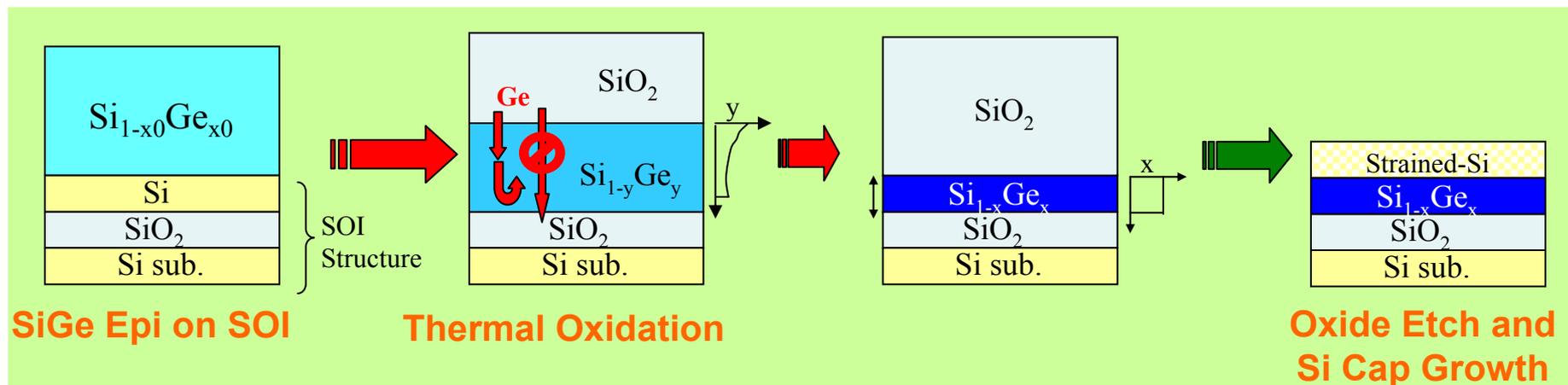
- Eliminates the need for SiGe below the strained-Si.
- Eliminates processing challenges associated with Ge.
- Si layer achieves 97% of maximum achievable strain.
- Smooth surface, RMS~0.49nm.
- Dislocation density is at least 1e6 defects/cm².



sample	Si-Si/Si freq							Si-Si/Si FWHM		Si-Si/SiGe
	measured	shift from relaxed Si	strain	stress	%Ge trans wfr	fully strained	% strained	measured	% deviation	fully relaxed
	(cm ⁻¹)	(cm ⁻¹)		(GPa)	(%)	(cm ⁻¹)	(%)	(cm ⁻¹)	(%)	(cm ⁻¹)
SSOI	513.36	-7.34	0.0073	1.31	20.0	513.10	96.6	4.50	21	

March 15, 2005

IV. Strained-Si on SiGe-On-Insulator (SGOI) Substrates—Condensation



- Condensation involves oxidation of epitaxial SiGe, where Ge gets rejected and SiO_2 is grown on top.
- Oxide is later etched off before a strained-Si cap is deposited on the enriched and relaxed SiGe.

Advantages

- Ultra-thin SiGe with high level of Ge enrichment.
- Allows balance between strain, thickness, Ge content

Challenges

- Achieving full relaxation while maintaining low defect density.

March 15, 2005

36

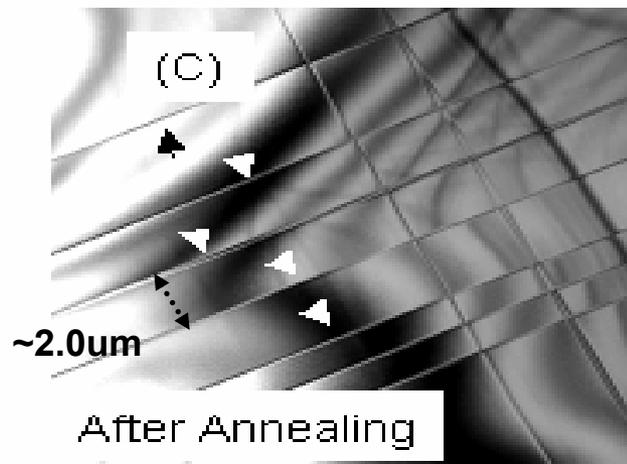
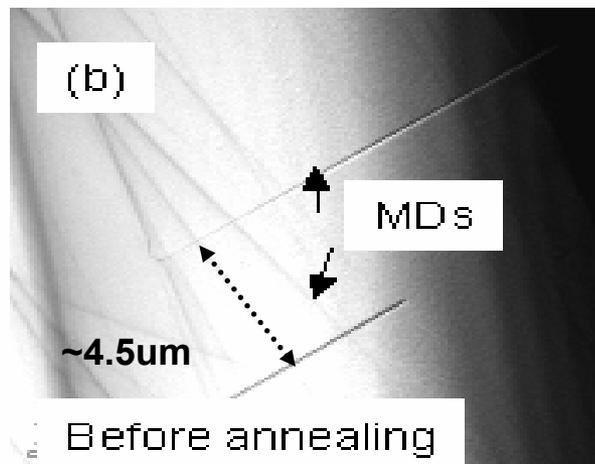
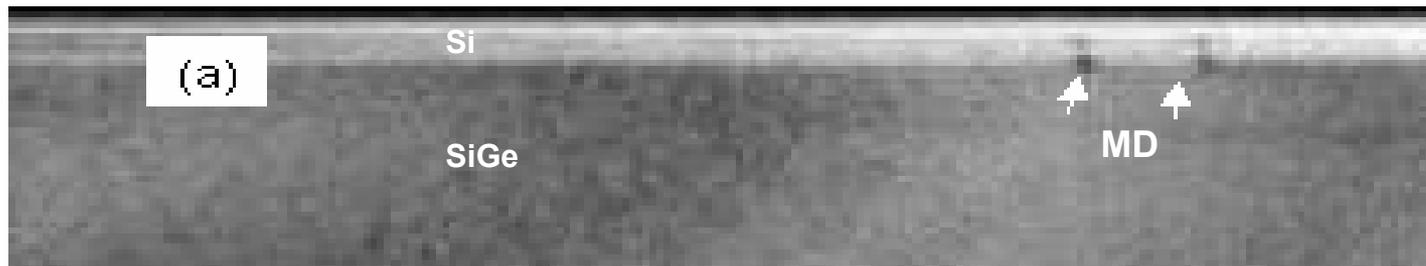
2005 International Conference on Characterization and Metrology for ULSI Technology, University of Texas at Dallas
Freescale™ and the Freescale logo are trademarks of Freescale Semiconductor, Inc.

All other product or service names are the property of their respective owners. © Freescale Semiconductor, Inc. 2004

Launched by Motorola
freescale
semiconductor

Overview of Strained Si
Metrology for Strained-Si
Metrology for Defect Analysis
Metrology for Substrate Characterization
✓ **Metrology for Process Effects**
Emerging In-Line Metrology
Summary

Process Challenges: Effect of High-Temperature Anneal on MD's



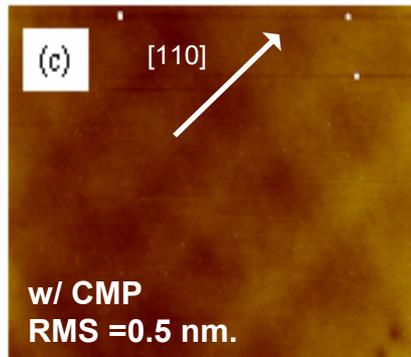
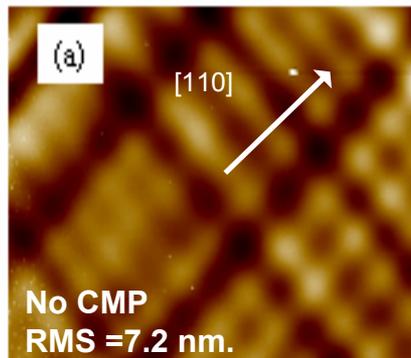
- MDs at the interface between the strained Si channel and SiGe layer.
- After annealing at 900°C for 60 sec density of MD increased ~2x.

Process Challenges: Effect of CMP on SiGe Surface Roughness

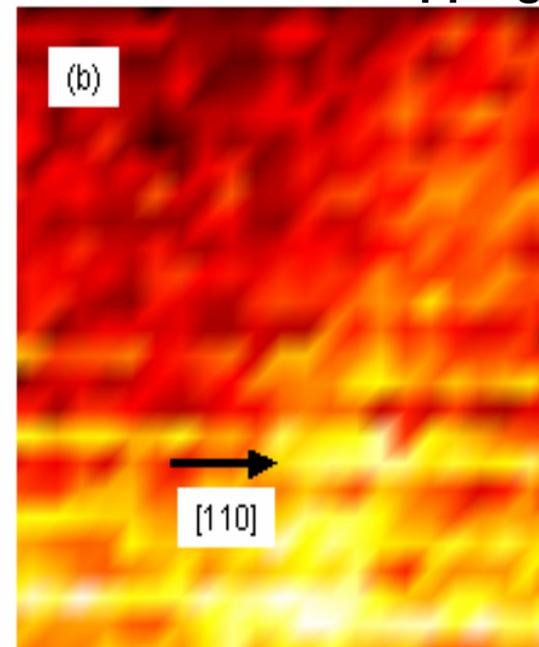
- Cross-hatch pattern causes spatial strain variation; correlates well with micro-Raman mapping.
- Characteristic of graded SiGe layer.

- Can create problems for lithography and surface inspection.
- Reduces the mobility of strained Si.
- Promotes dislocation formation at localized high stress regions.

AFM



Micro-Raman mapping

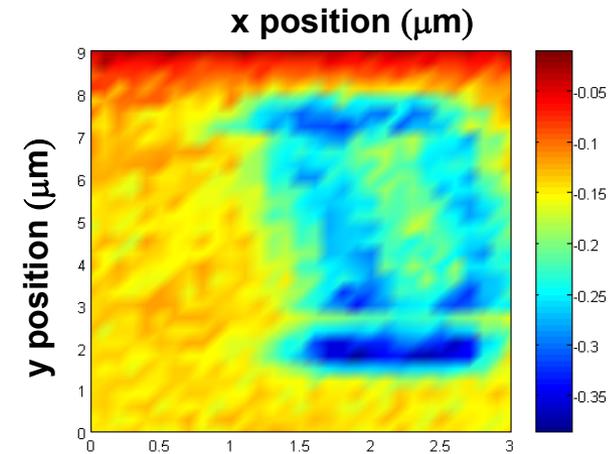
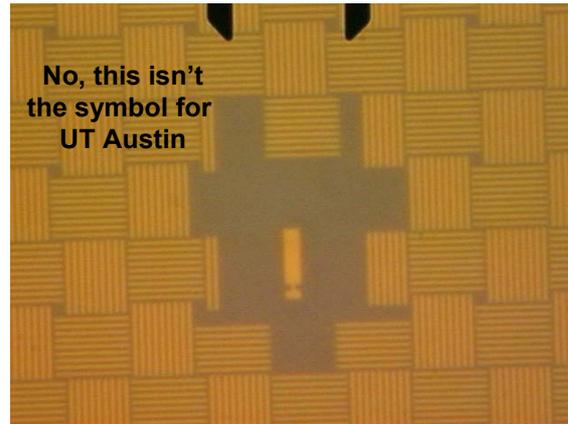
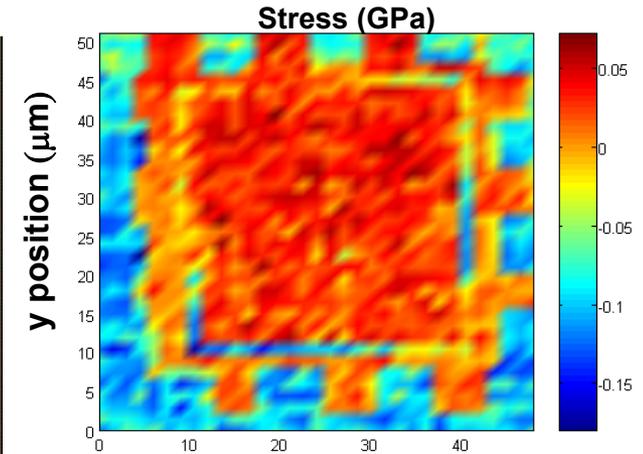
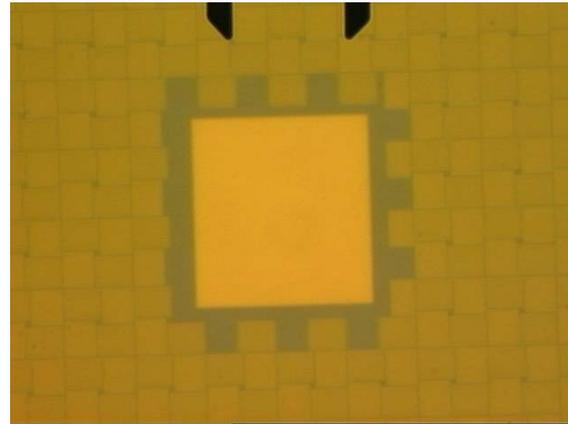


- ❖ Relaxation causes cross-hatching.
- ❖ Chemical mechanical polishing (CMP) reduces cross-hatching.

Overview of Strained Si
Metrology for Strained-Si
Metrology for Defect Analysis
Metrology for Substrate Characterization
Metrology for Process Effects
✓ **Emerging In-Line Metrology**
Summary

Emerging Technologies—Raman Stress Mapping

- Multi-site UV-Raman for strain and crystallinity assessments
- Needed for device-level assessments



Strain variations affect device performance

March 15, 2005

41

2005 International Conference on Characterization and Metrology for ULSI Technology, University of Texas at Dallas

Freescale™ and the Freescale logo are trademarks of Freescale Semiconductor, Inc.

All other product or service names are the property of their respective owners. © Freescale Semiconductor, Inc. 2004

Emerging Technologies—Infrared Photoluminescence (PL)

Capabilities

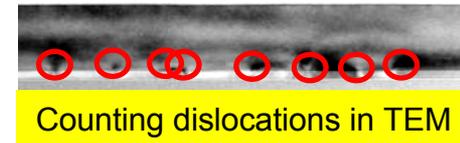
- Light is directed onto a sample (photo-excitation); excess energy is dissipated through luminescence
- Identifies defects (MD, TDD, pile-ups)
- Intensity and spectral content is a measure of material properties

Advantages

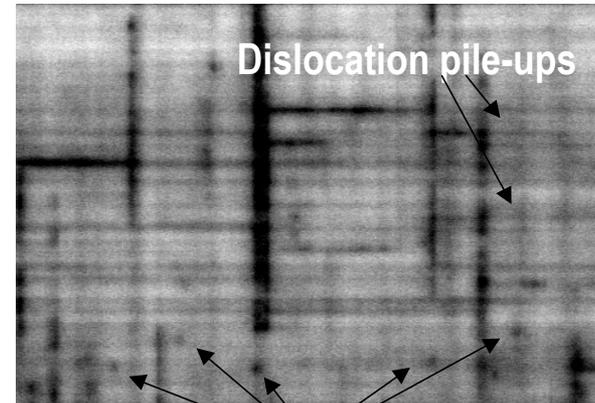
- Nondestructive, automated, rapid
- Whole-wafer maps allow rapid identification of inhomogeneities, misfit dislocations and stacking faults
- Can be added to Raman system
- High-resolution room-temperature PL mapping (SiPHER) has been demonstrated for both Si and SiGe wafers
- Correlates well with EPD

Disadvantages

- Can require cryogenic cooling of sample for best sensitivity

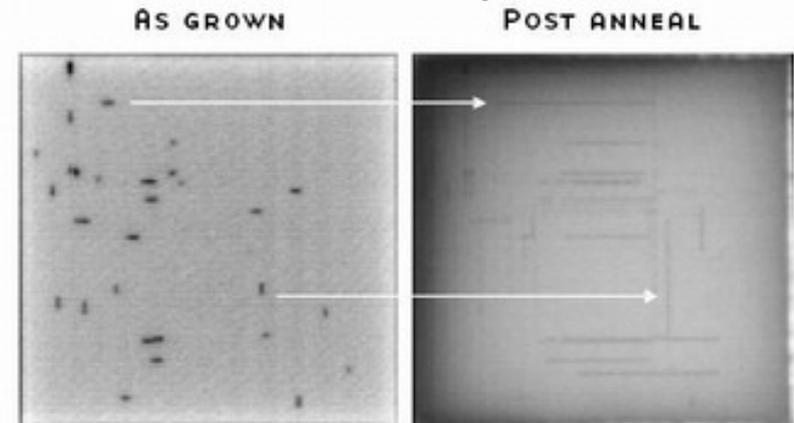


0.21 x 0.17 mm



Courtesy of SiPHER

Threading dislocations



MISFIT DISLOCATIONS PROPAGATE AT THE Si/SiGe INTERFACE

March 15, 2005

42

2005 International Conference on Characterization and Metrology for ULSI Technology, University of Texas at Dallas

Freescale™ and the Freescale logo are trademarks of Freescale Semiconductor, Inc. All other product or service names are the property of their respective owners. © Freescale Semiconductor, Inc. 2004

Motorola
freescale
semiconductor

Overview of Strained Si
Metrology for Strained-Si
Metrology for Defect Analysis
Metrology for Substrate Characterization
Metrology for Process Effects
Emerging In-Line Metrology
✓ **Summary**

Summary

- **Significant achievements in strained-Si on bulk and on insulator substrates.**
- **Device performance is sensitive to subtle changes in strain, film morphology, and defectivity.**
- **Metrology advances must be made to monitor substrates and detect process changes during manufacturing.**
- **Minimum detection size should keep step with technology node dimensions.**
- **Surface, embedded, and interface defects are increasingly important for device performance.**
- **Very rough surface (cross-hatch) due to misfit dislocations will be challenging for in-line optical inspection.**
- **Ultra-thin films are increasingly used, requiring shallow penetration depths.**
- **Determining composition and strain on the deep sub-micron device length scale is an unsolved problem.**
- **In-line metrology tools using these techniques are still under development.**



March 15, 2005

45

2005 International Conference on Characterization and Metrology for ULSI Technology, University of Texas at Dallas
Freescale™ and the Freescale logo are trademarks of Freescale Semiconductor, Inc.

All other product or service names are the property of their respective owners. © Freescale Semiconductor, Inc. 2004

