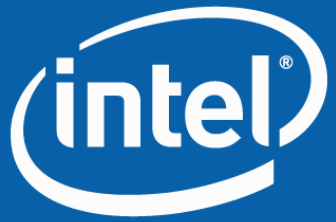


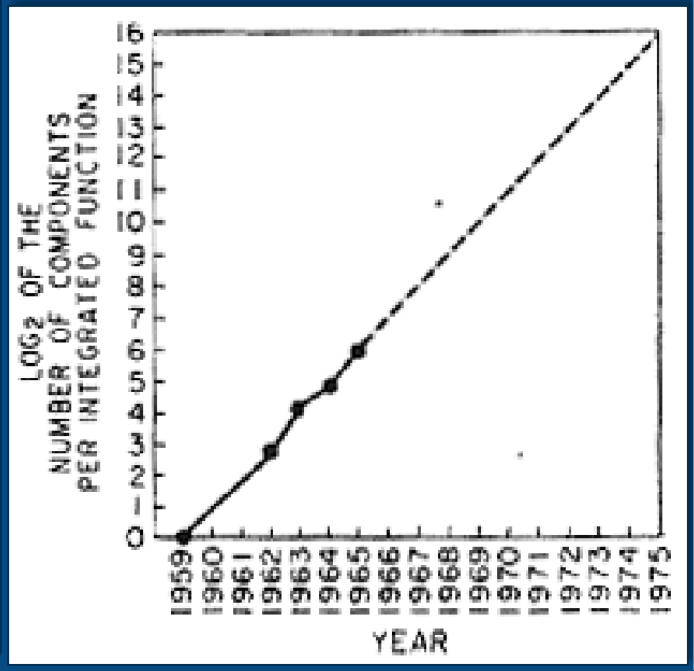
Defect Inspection for Advanced Technology Nodes

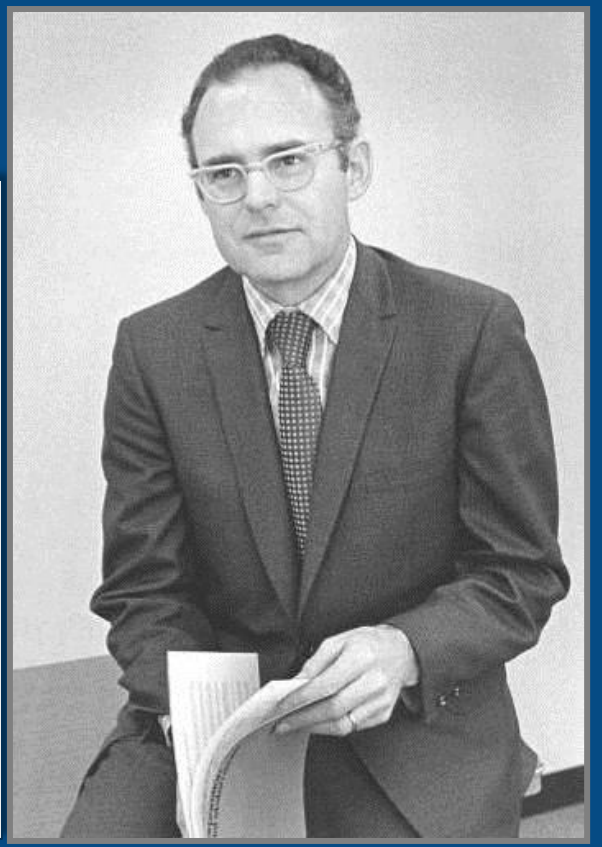
Tuyen K. Tran
Intel Corporation
April 15, 2015

Moore's Law - 1965

"**Reduced cost** is one of the big attractions of integrated electronics, and the cost advantage continues to increase as the technology evolves toward the production of larger and larger circuit functions on a single semiconductor substrate."

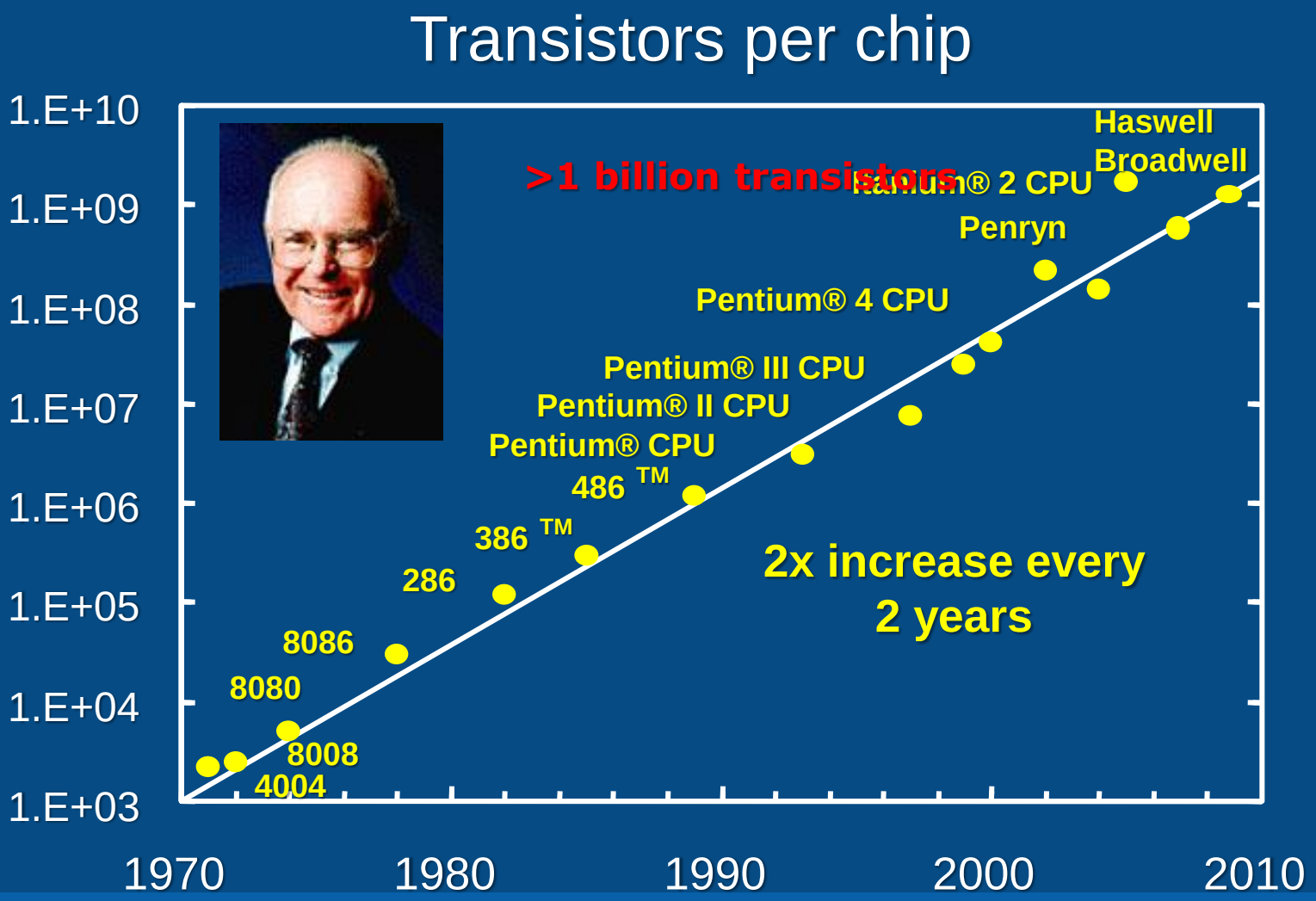
Electronics, Volume 38, Number 8, April 19, 1965



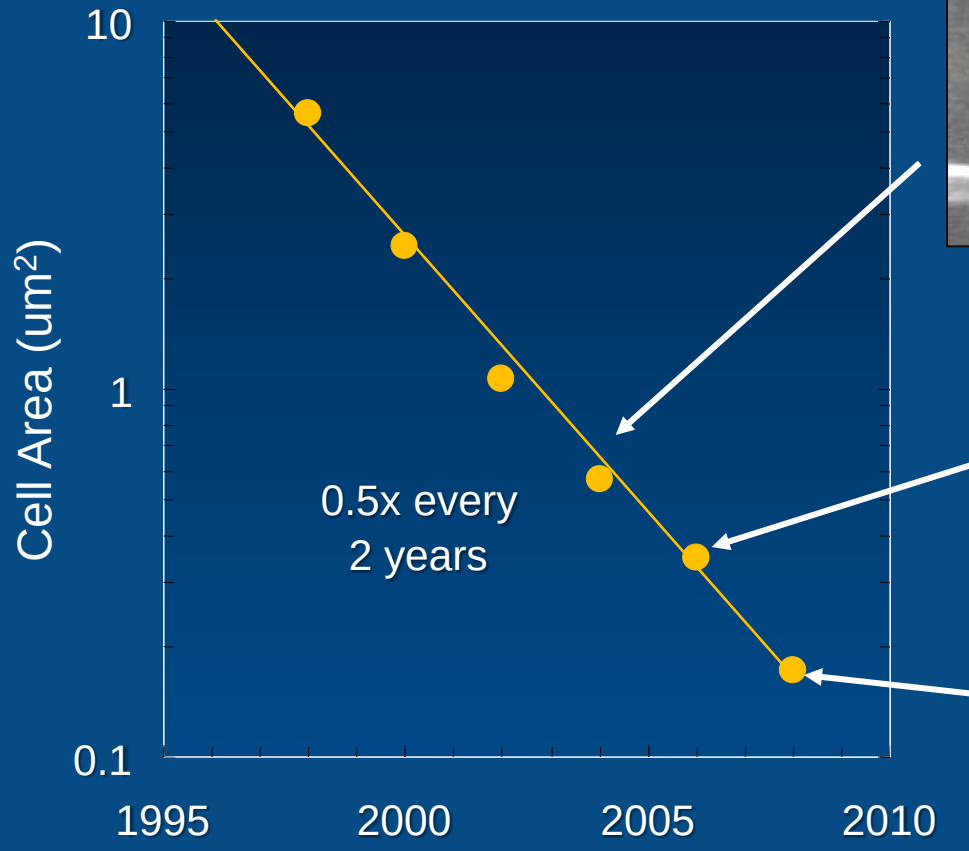


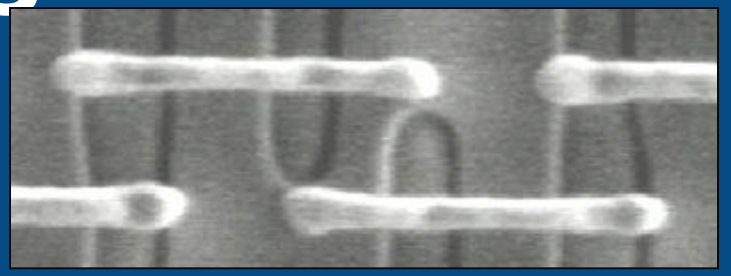
The number of transistors on a chip doubles approximately every two years

Moore's Law Continued Well Past 1965

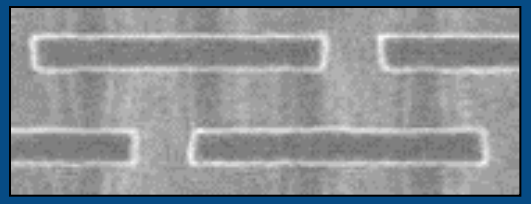


… Enable SRAM Cell Size Scaling

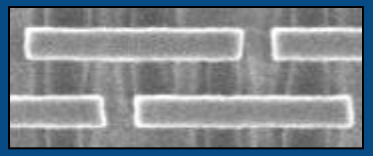




65 nm, 0.570 um²



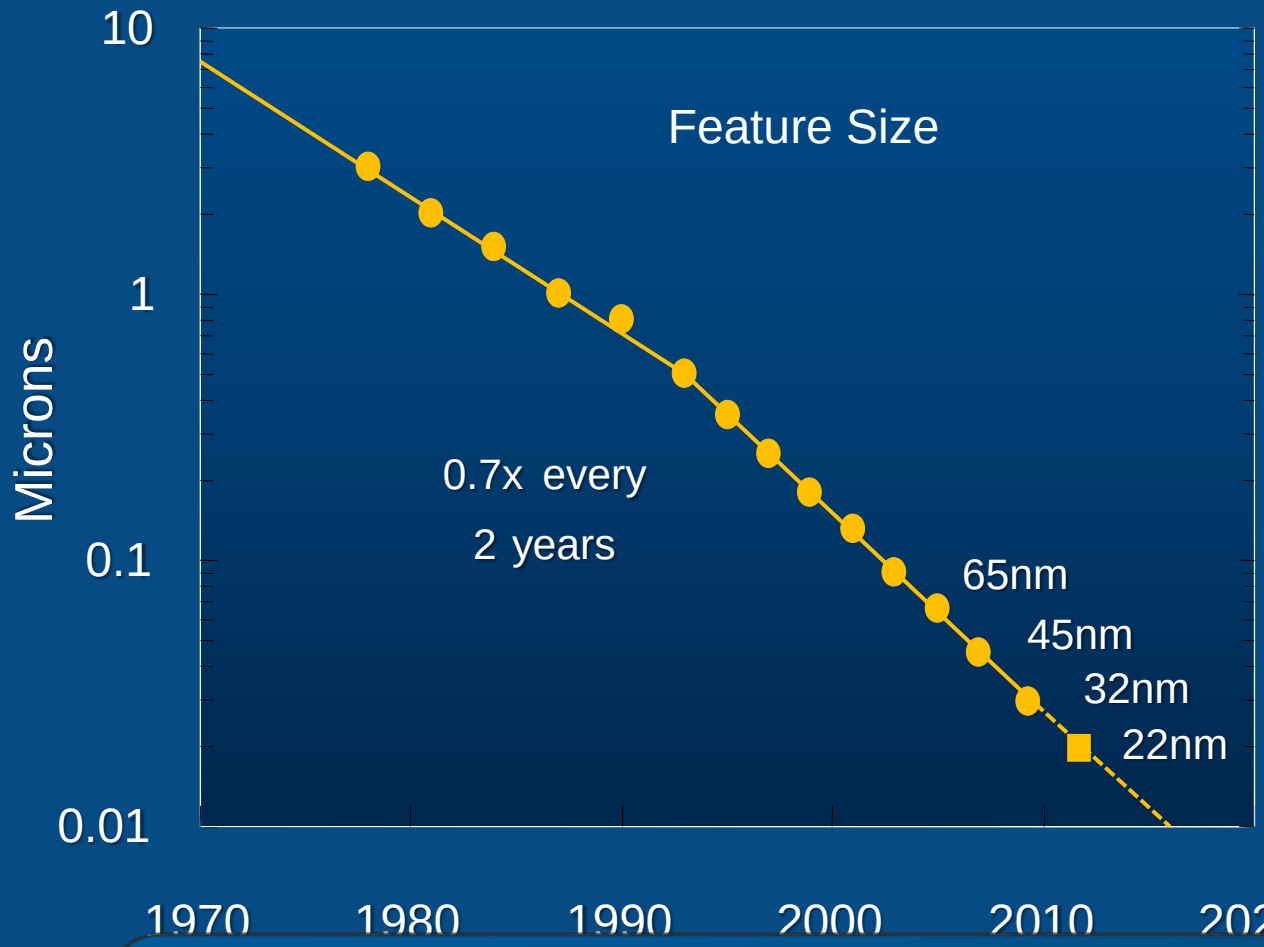
45 nm, 0.346 um²



32 nm, 0.171 um²

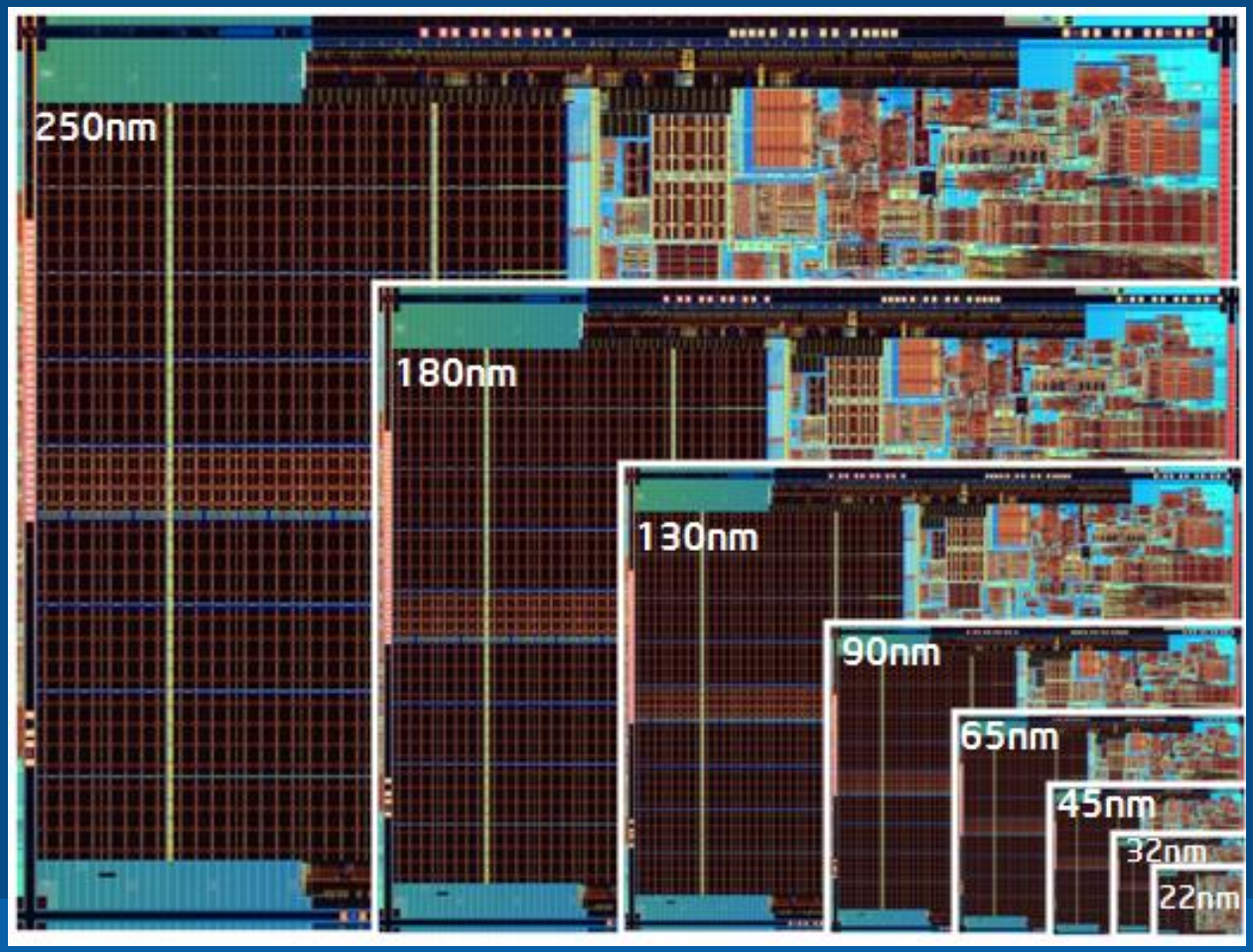
Transistor density continues to double every 2 years

Reductions in Feature Size …



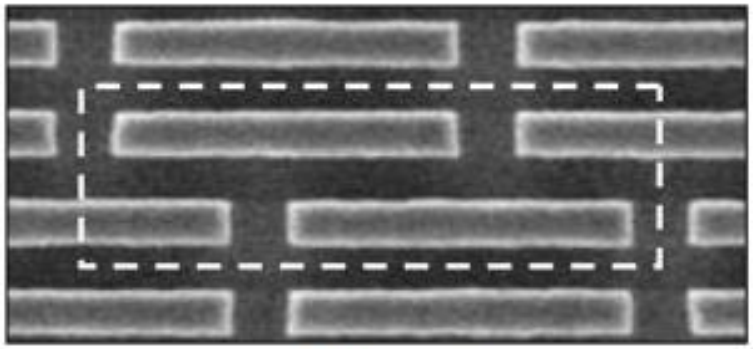
Transistor dimensions scale to improve performance, reduce power and reduce cost per transistor

Intel's pace of innovation



Intel 14 nm SRAM Cell

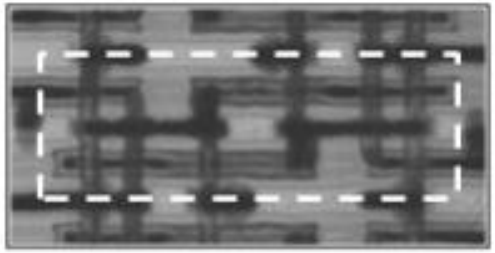
22 nm Process



.108 um²

(Used on CPU products)

14 nm Process



.0588 um²

(0.54x area scaling)

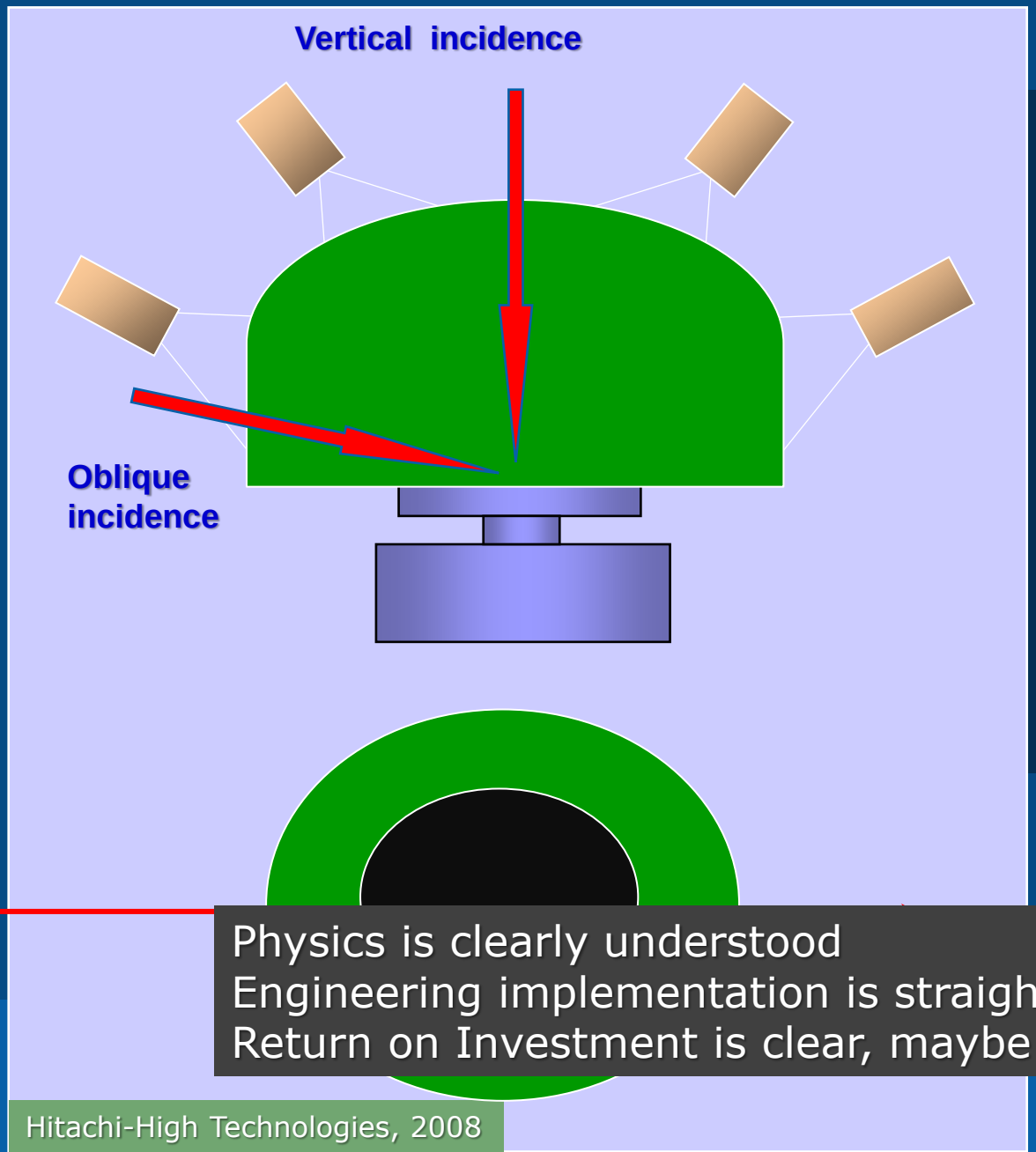
14 nm Design Rules + 2nd Generation Tri-gate Transistor Provides Industry-leading SRAM Density

Why Inspection/Yield?

- Better Yield = $$$
- Early results on new process → ~10^9 working transistor/chip
- But... some 10000000 transistors/interconnects did not work!

➢Reducing this number to 0 at the same time as performance & reliability goals are achieved is what process technology development is all about.

Unpattern Inspection Architecture



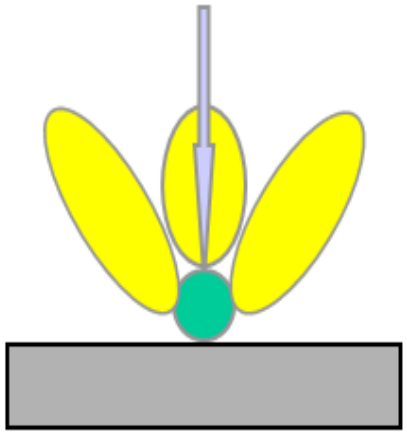
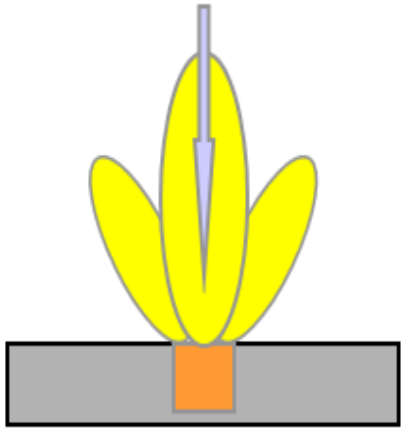
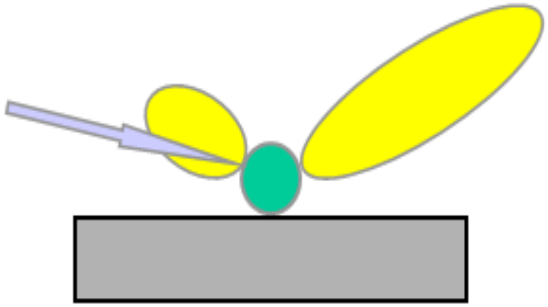
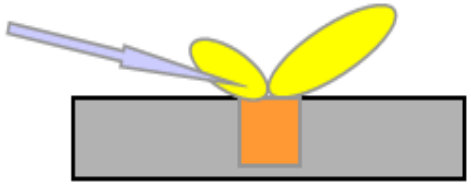
Key Attributes:

- Fully modelling-capable
- Collect as much photon as possible. (Net NA~1.0).
- Multiple collectors enable better distinguishing of Defect types: innie/outie.
- Normal/Oblique illumination enable better detection of certain epi-defects.

Physics is clearly understood
Engineering implementation is straight forward
Return on Investment is clear, maybe until recently…

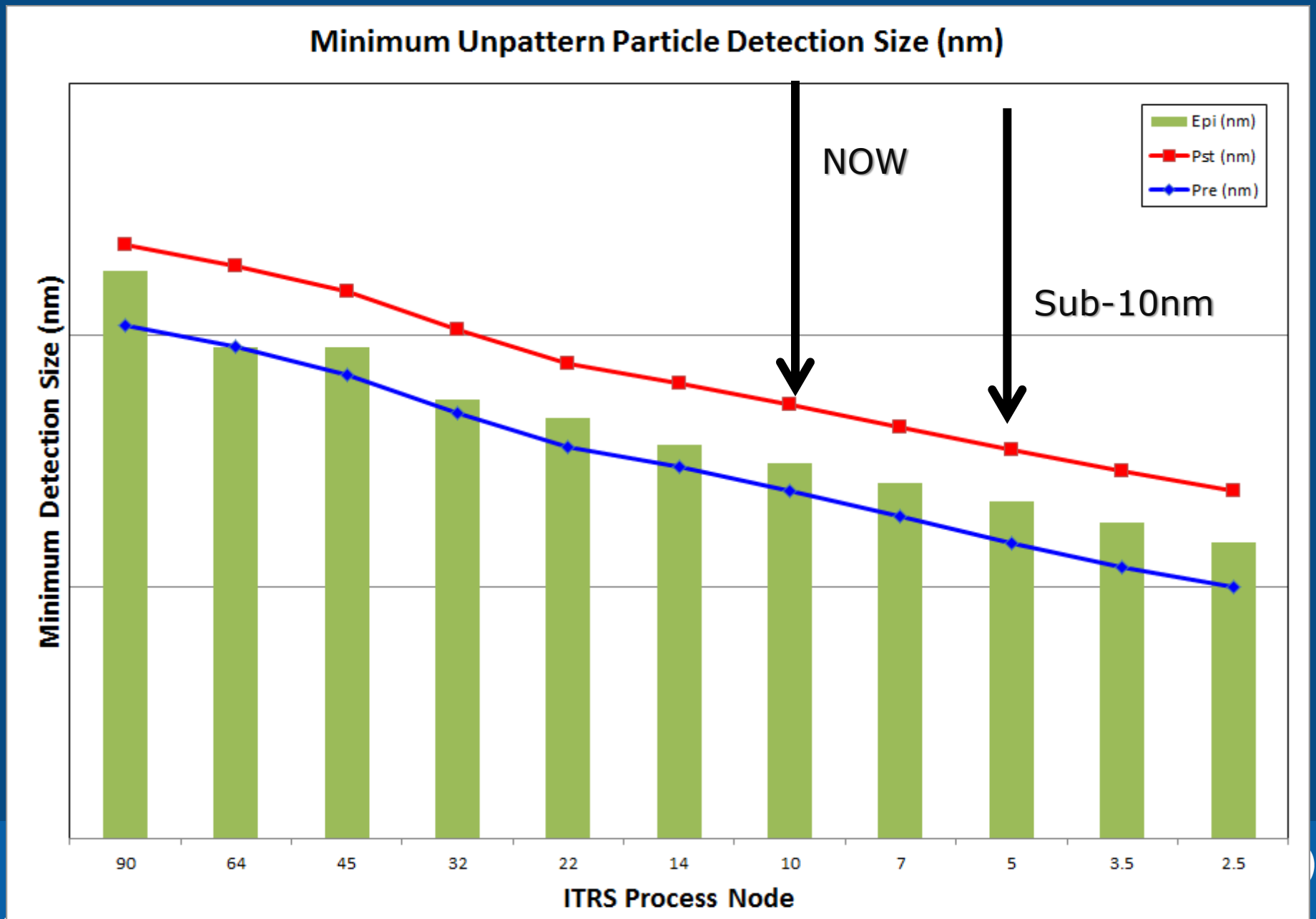
Hitachi-High Technologies, 2008

Unpattern Inspection Architecture

Beam	Particle	Scratch
Vertical incidence		
Oblique incidence		
Scattering intensity	Normal $\cong$ Tilted	Normal > Tilted

Hitachi-High Technologies, 2009

Unpattern Inspection Architecture



Unpattern Inspection Architecture

Laser λ	532 nm	488 nm	488 nm	457 nm	355 nm	325 nm	266 nm	213 nm	193 nm	157 nm
Power	1000 mW	200 mW	1000 mW	400 mW	300 mW	50 mW	200 mW	400 mW	200 mW	10 mW
Technology	DPSS	OPS	Ar-Ion	DPSS	DPSS	HeCd	DPSS	Other	Other	Other
Reliability/Lifetime	Good	Good	Good	Good	Good	Okay	Good	Okay	Poor	Poor
Bare Si Sensitivity	50 nm	53 nm	47 nm	49 nm	40 nm	48 nm	39 nm	≤20 nm	≤18 nm	≤10 nm
SOI	Poor	Poor	Poor	Poor	Good	Good	Good	Good	Good	Good
Damage	Thermal	No	Low	No	UV Low-k	UV Low-k	UV Films	UV Films	UV Films	Other

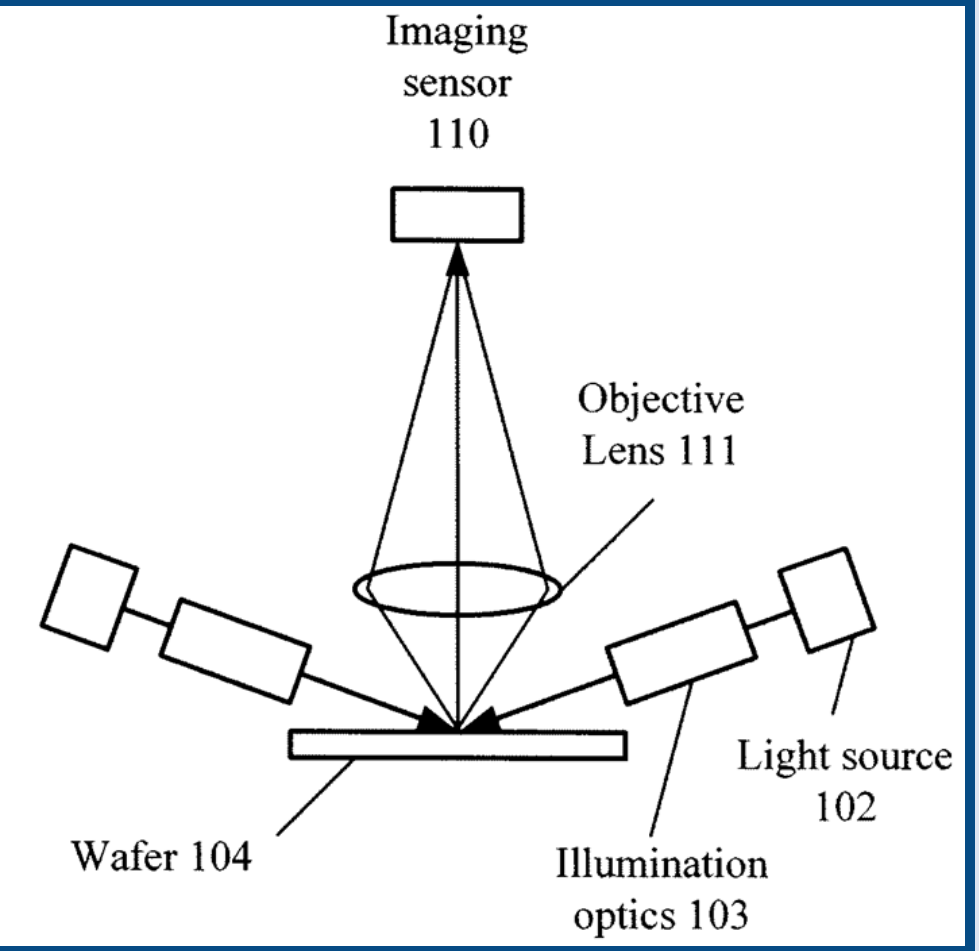
Unpattern Inspection: Inflection Point

- Achieving Si sensitivity below 10nm requires major fundamental changes: ≤193nm or slightly higher or employing Imaging architecture.
- Diminishing return in sensitivity on complex film stack, and may not reflect product performance.
- Does it even pay to inspect complex film stack on unpattern tools?
- Cross tool matching below sub-7nm sensitivity is difficulty. Every *half*-nm of sensitivity count!

Unpattern Potential Features

- The NEXT platform needs to be able to cover sensitivity through sub-5nm @ fast WPH, while providing additional necessary features:
  - World-class xy accuracy for 1μm SEM FOV with 5 points-deskew, and <5μm tool-to-tool overlay.
  - Topographic info in z-direction, begins with 75% accuracy, increase 10% more each further process.
  - Elemental composition of ALL defects detected in near real-time, with timelag of one-wafer scan equivalent.
  - Directional ADC capability, including back-to-front and forward/backward overlay.

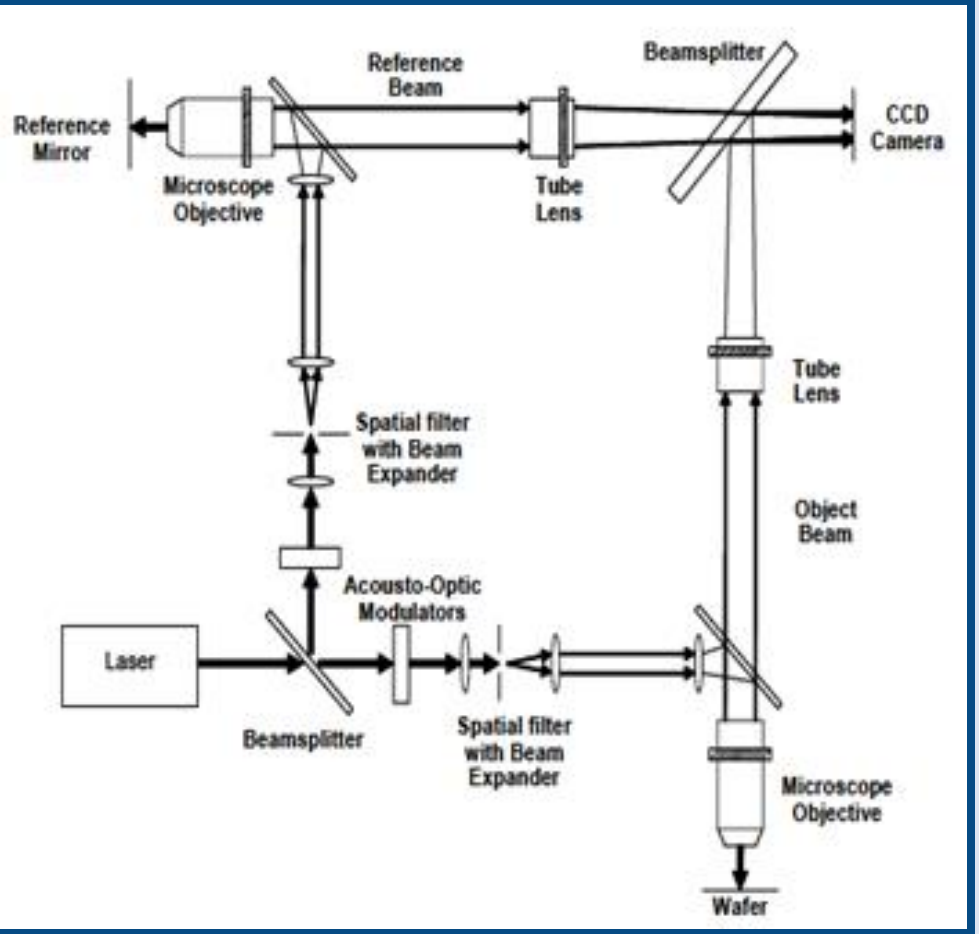
Optical Pattern Inspection: Darkfield



- State of the art sensitivity ~75nm in SRAM; much larger on logic area.
- Capable of mitigate noise due to process variation.
- Fast throughput
- Fully integrated with other infrastructures.
- Laser ablation concern

75nm sensitivity on 10nm process design rule is clearly not enough

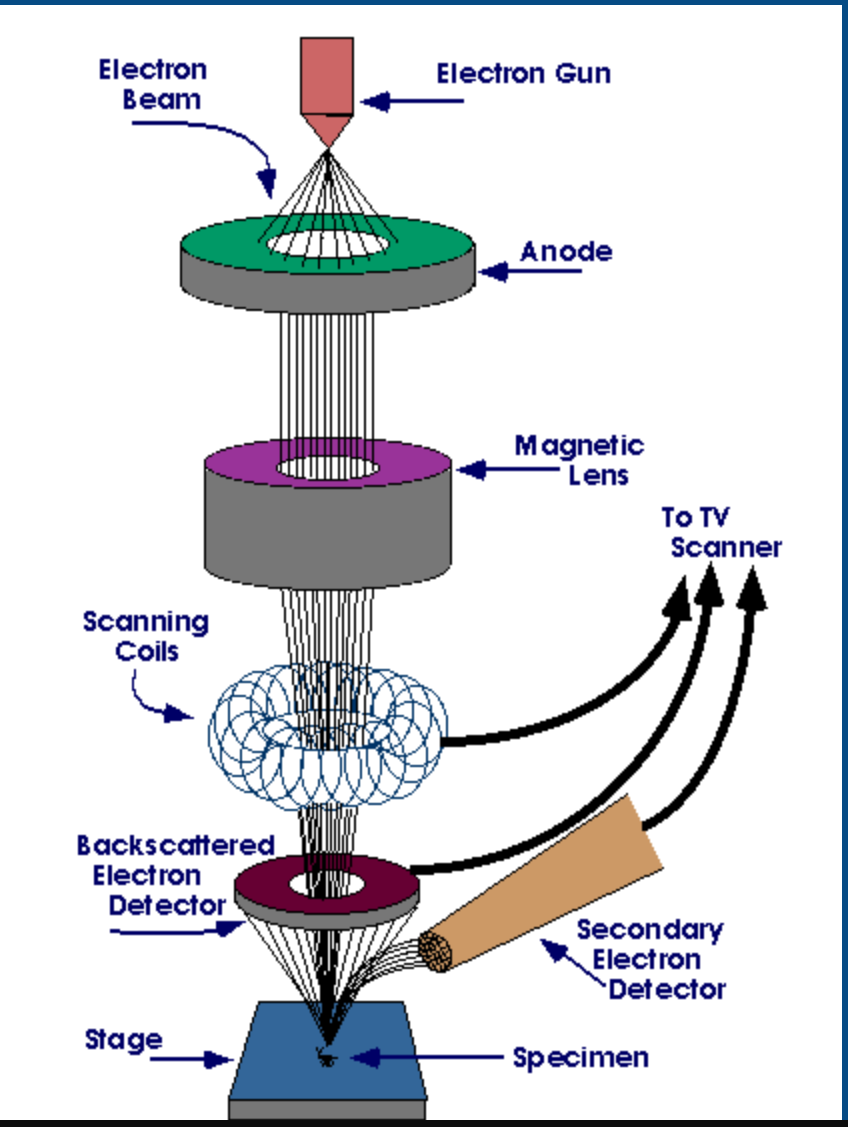
Optical Pattern Inspection: Brightfield



- State of the art sensitivity ~50nm in SRAM; larger on logic.
- Capable of mitigate noise due to process variation.
- Fully integrated with other infrastructures.
- Very slow throughput.
- Cost/Effectiveness is imbalanced.

50nm sensitivity on 10nm process design rule is clearly not enough

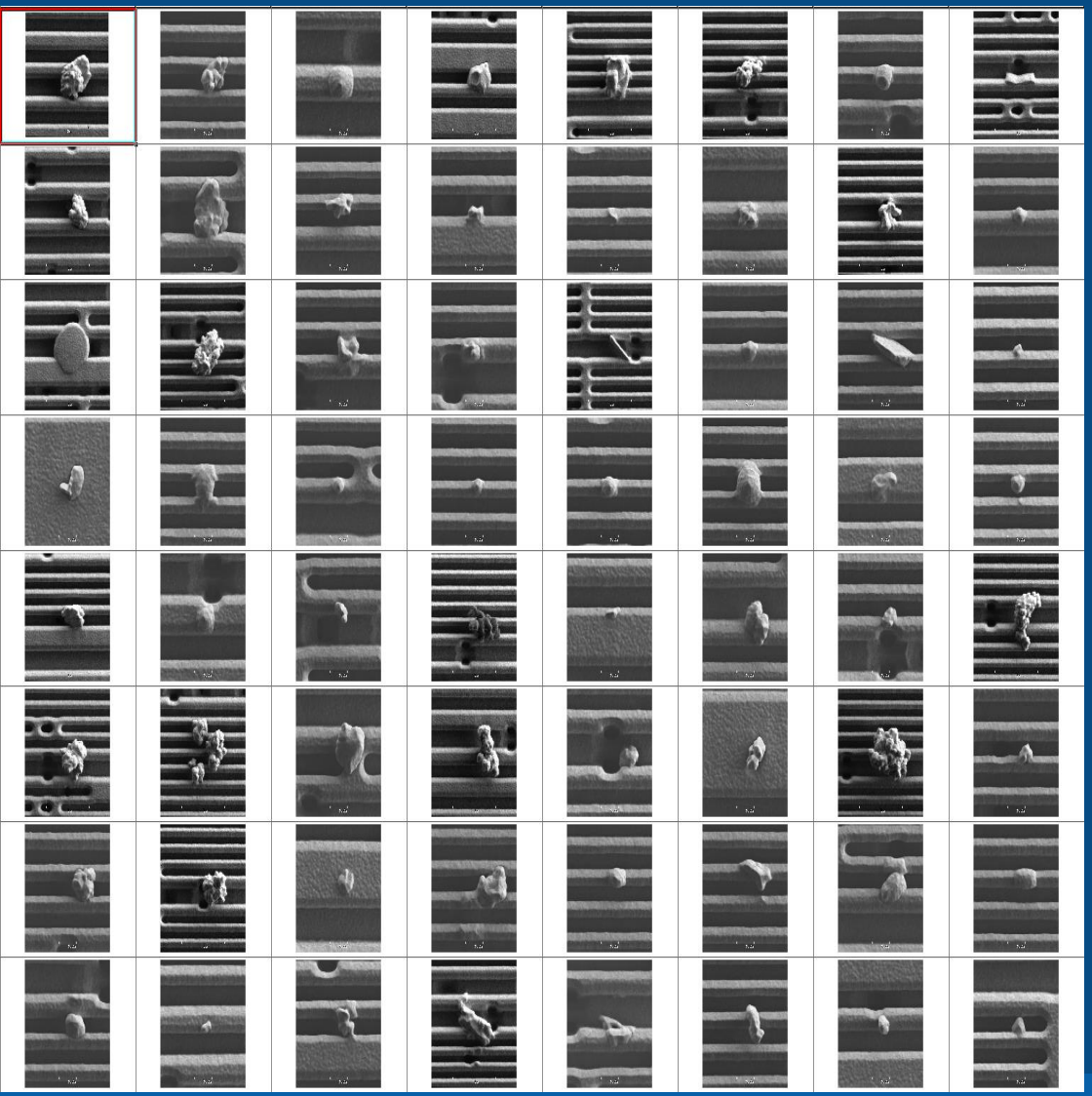
E-beam Inspection Tool: The next frontier



- State of the art resolution ~3nm with very large FOV
- Near capable of mitigate surface charge due to process variation.
- Very slow throughput: typical ~1die/week
- Serves as DOI finder for optical inspection tools.

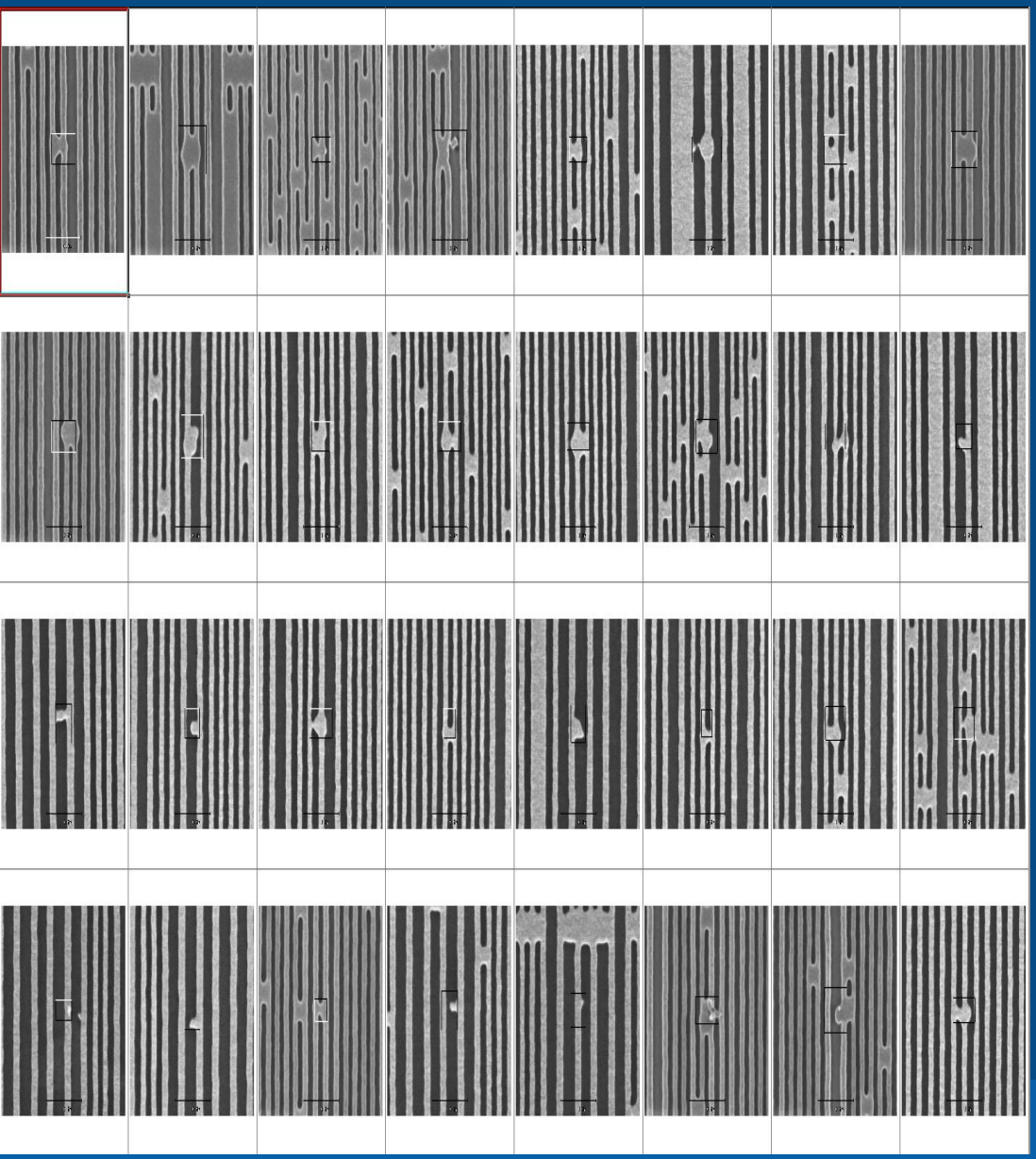
Major architectural change is required in order to become more effective in the semiconductor industry

Optically Detected Defect Gallery (1)



- Particle-like detected defect roughly follow pixel:defect size ratio of ~**3.25:1**
- Better sensitivity in SRAM than logic area due to non-FF'able.

Optically Detected Defect Gallery (2)



- Pattern-like detected defect roughly follow pixel:defect size ratio of ~**2.5:1**
- SRAM sensitivity is typically lower than that of logic area due to a lack of photons and/or aperturing.

The Darkfield Technical Roadmap

Item	Technology	Comment
Sensitivity	Shorter λ	**266nm, 213nm, 193nm, 157nm**
	Smaller spot size(s)	Bound by ablation & TPT
	Aperturing	Nearly free
	Sampling	Bound by TPT
	Laser Power	Ablation concerns
Speed	Multiple Spot sizes	Improving TPT @ optics complexity and cost
	Imaging Techniques	Potentially improving TPT @ cost

Green: Existing capability
Yellow: Technical roadmap not clear to achieve, or inconclusive
Red: No existing/viable demonstrated roadmap to get there

The Brightfield Technical Roadmap

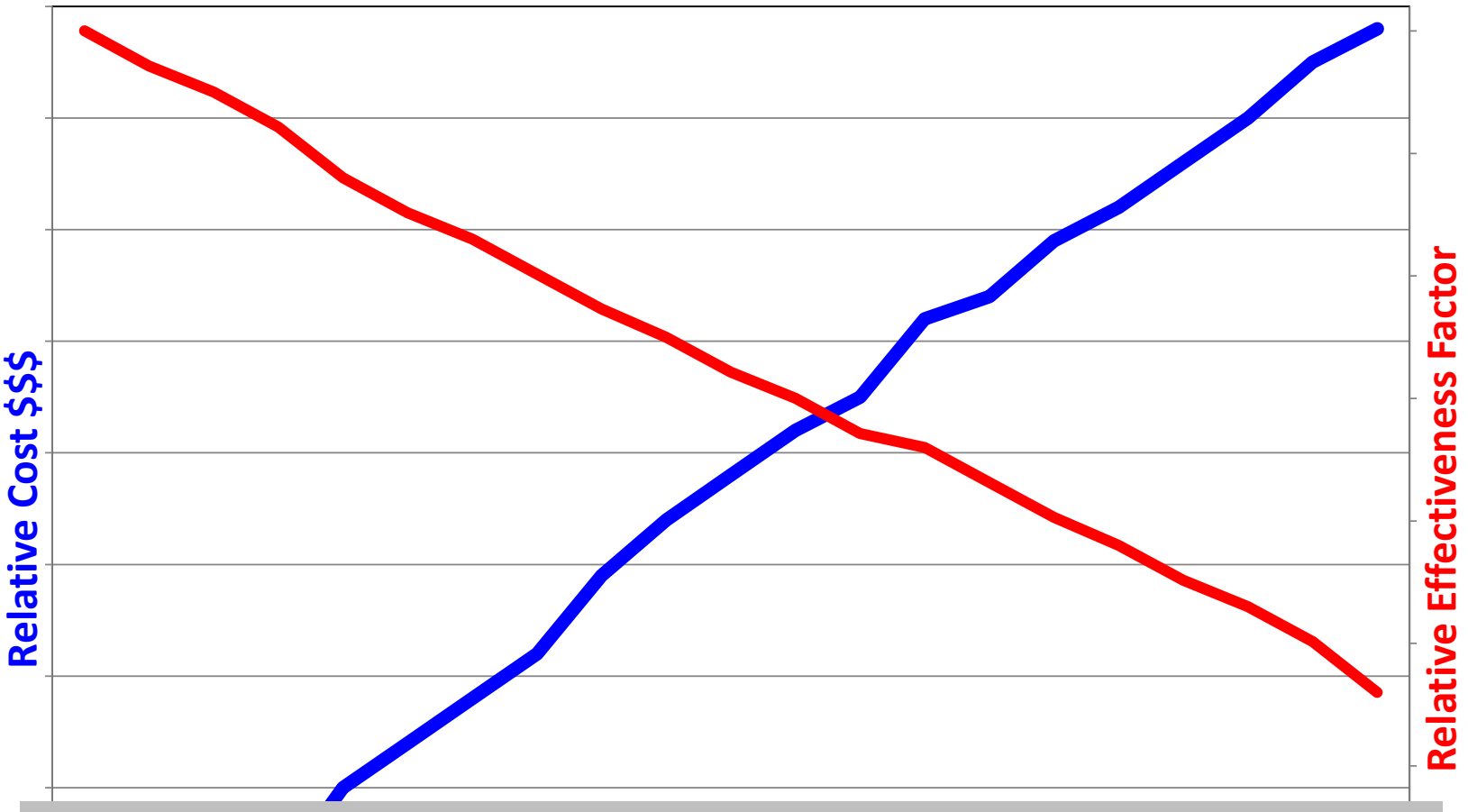
Item	Technology	Comment
Sensitivity	Shorter λ–bands	**266nm, 213nm, 193nm**
	Smaller pixel size(s)	Bound by ablation & TPT
	Aperturing for illumination & detection	Nearly free, bound by photon availability
	Sampling	Bound by TPT
	Effective d2db	Potentially improving sensitivity @ cost & complexity
	Brighter Light source	Difficult to find!
Speed	Multiple illuminations	Improving TPT @ optics complexity and cost

Green: Existing capability
Yellow: Technical roadmap not clear to achieve, or inconclusive
Red: No existing/viable demonstrated roadmap to get there

Challenges for equipment suppliers

Technology	Sensitivity (nm)	TPT (Wafer/hr)	How To get there
E-beam Inspection	Sub-1nm	1 die/hour	>1000 beams @ Sub-1nm resolution
BF Inspection	<5nm in SRAM	1 wafer/hour	<10nm pixel size @ ultra-bright short λ with full d2db
DF Inspection	<15nm in SRAM	1 wafer/hour	Oblique & Normal illumination with multiple λ's, with full aperture and limited d2db. Role-reversal with Unpattern
UnPattern Inspection	<5nm on epi wafer	26 wafer/hour	Near simultaneous Oblique & Normal illumination with multiple λ's, with full aperture. Role maybe severely limited.
Novel Inspection	Tight integration of e-beam technology + DFM and extensive process knowledge and computational lithography. (This is an area that Equipment Suppliers have much less Expertise to contribute compared to end users)		

Cost-Effectiveness Challenges…



Optical Inspection tool is one of the most Expensive tool in a Fab!
Yet, it does not do a good job @ improving Yield quickly

Cost-Effectiveness Factor…