CMOS TO BEYOND CMOS:
From Complex Structures to
Complex Material Systems

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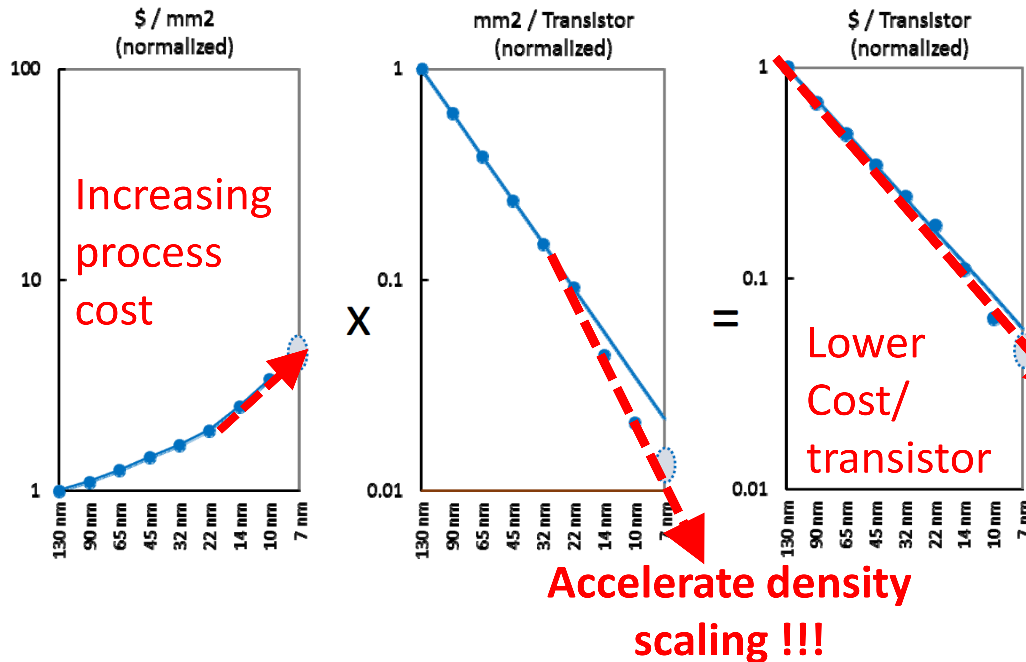
imec

NUS
National University of Singapore

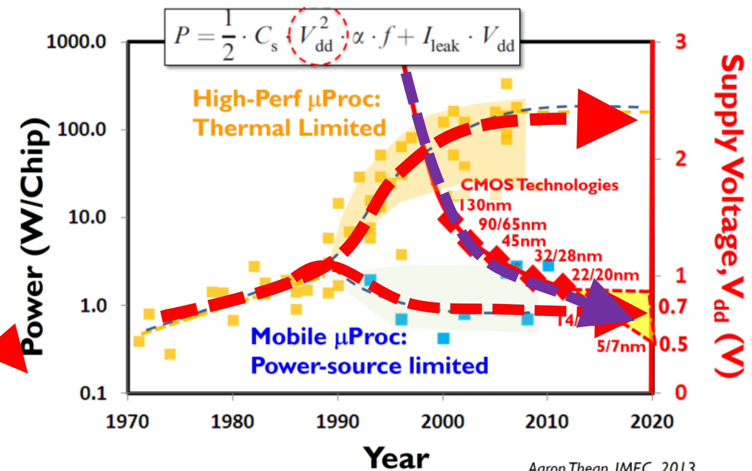
Technology Implications of **Moore's Law**

Offsetting Wafer Cost with Density



Bill Holt, Intel @ ISSCC 2016

Power Non-Scalability



Aaron Thean, IMEC 2013 (Adapted from various sources Includes T.Masuhara, IEEE-SSCM 2013)

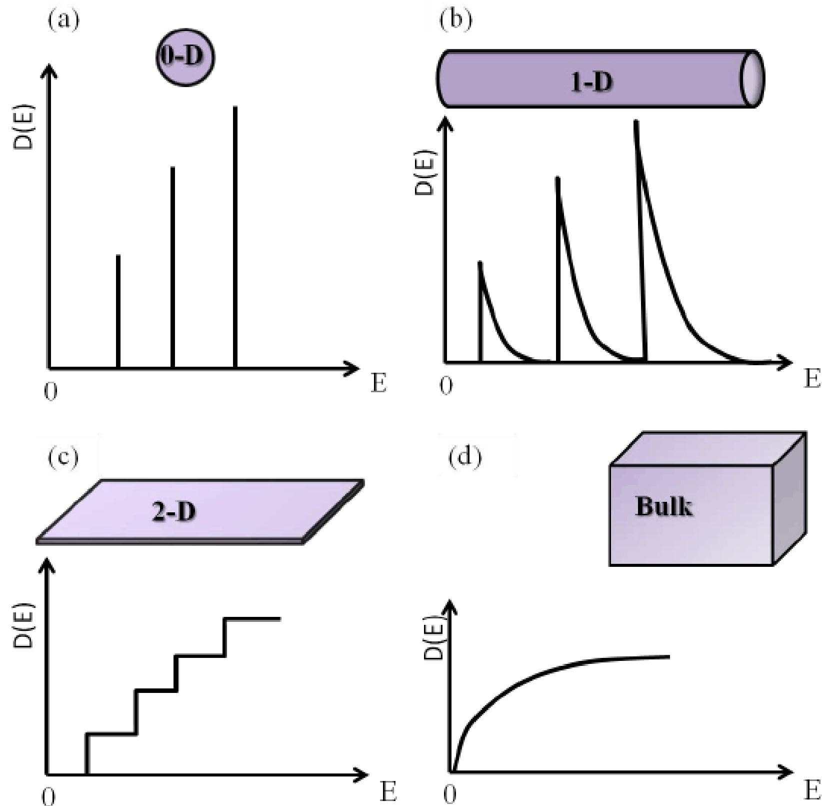
- **Accelerated Density Scaling Pressure** – Push for more Complex Device Structures
- **Power non-scalability** – Motivates search for Low-Energy Switch (Beyond CMOS?)

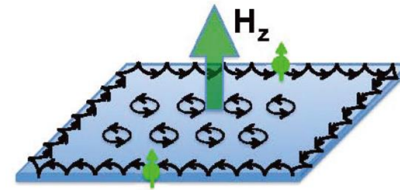
Outline

- Complex Structures
- Complex Material Systems: Beyond Silicon
- Emerging Material Systems: Beyond CMOS
- Messages

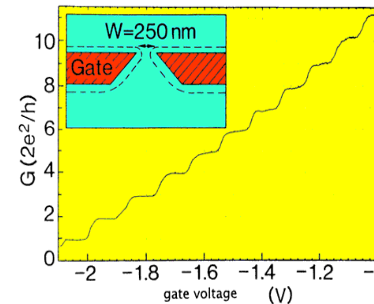
Complex Structures

Low-Dimensional Structures – **Interesting Solid-State Physics**

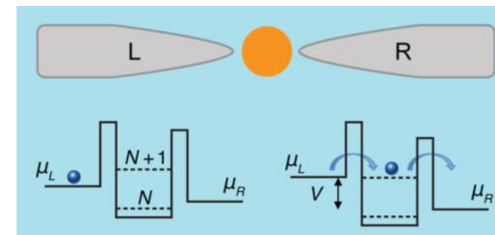




(b) Quantum Hall effect

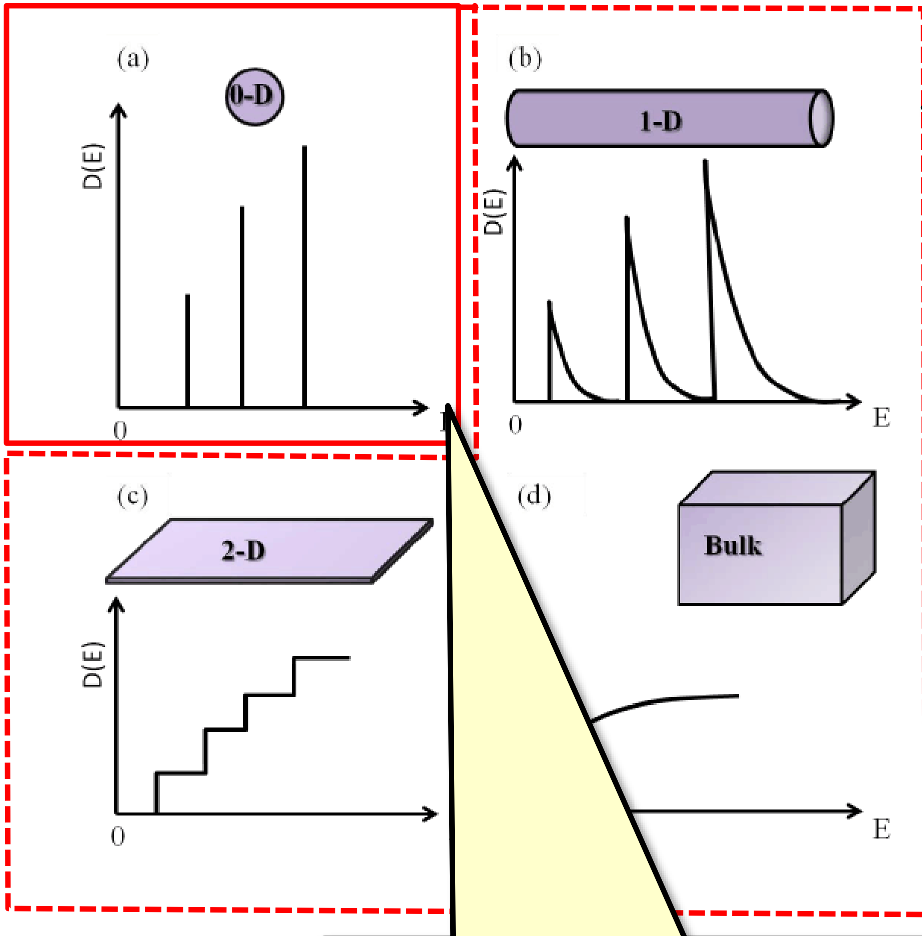


Quantum Point Contact

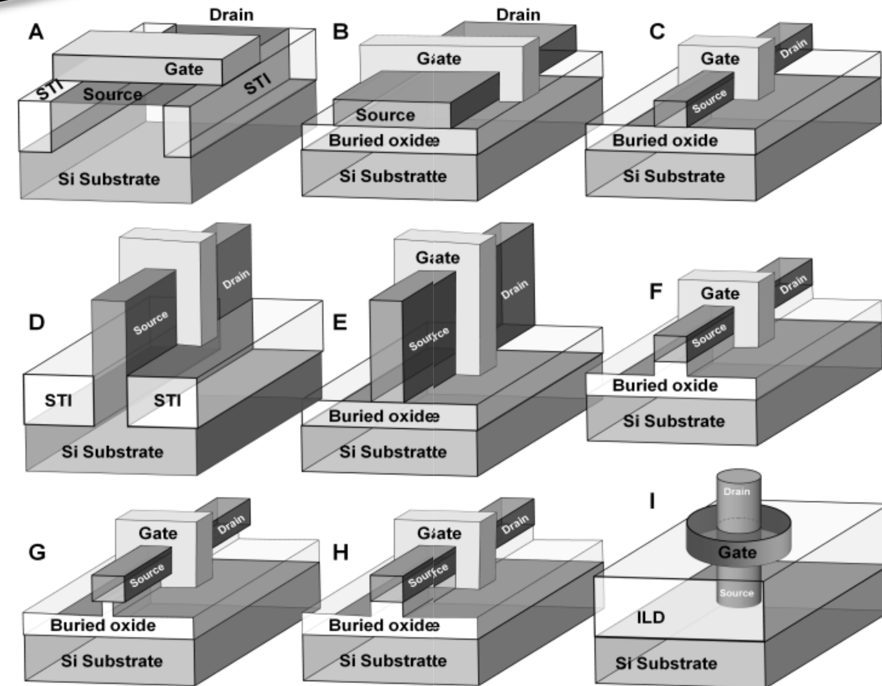


Coulomb Blockage in Quantum Dots

Low-Dimensional Structures – **Meet Transistor Technology**



Device structures toward 1D



0D systems: Present in todays' devices in the form of isolated atomic/bond defects

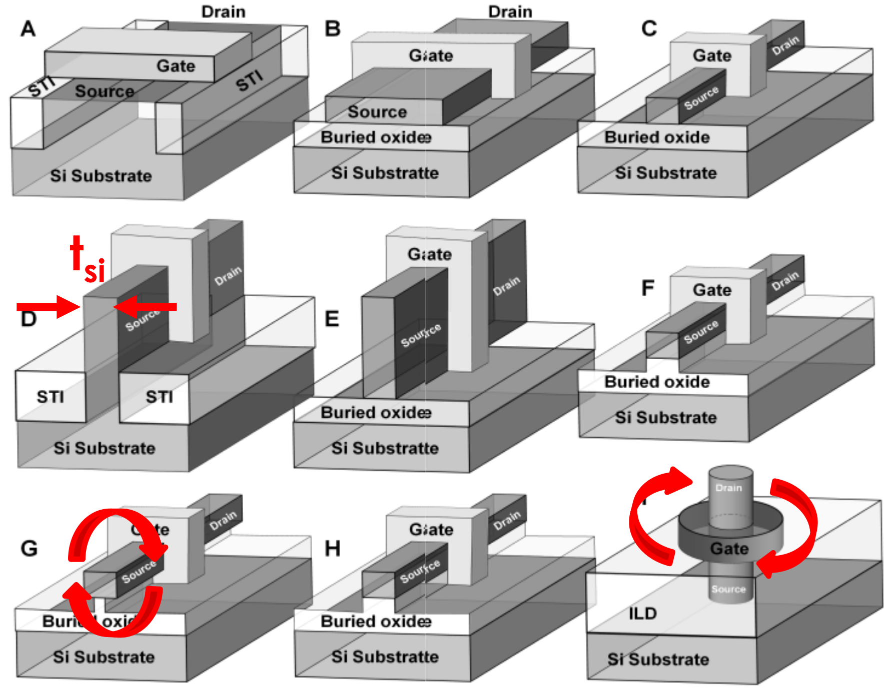
Low-Dimensional Structures –
Meet Transistor Technology

After: J.P. Colinge, “Multigate transistors: Pushing Moore's law to the limit “ SISPAD Page(s): 313 - 316

$$S=\frac{k_BT}{q}\ln(10)\frac{1}{1-2\exp\left(-\frac{L_G}{2\lambda}\right)}$$

“Steepness” of switch

Gate architecture	Natural length
Single gate	$\lambda_1=\sqrt{\frac{\varepsilon_{si}}{\varepsilon_{ox}}t_{si}t_{ox}}$
Double gate	$\lambda_2=\sqrt{\frac{\varepsilon_{si}}{2\varepsilon_{ox}}\left(1+\frac{\varepsilon_{ox}}{4\varepsilon_{si}}\frac{t_{si}}{t_{ox}}\right)t_{si}t_{ox}}$
Triple gate, square section	$\lambda_3=\sqrt{\frac{\varepsilon_{si}}{3\varepsilon_{ox}}\left(1+\frac{\varepsilon_{ox}}{4\varepsilon_{si}}\frac{t_{si}}{t_{ox}}\right)t_{si}t_{ox}}$
Quadruple gate, square section	$\lambda_4=\sqrt{\frac{\varepsilon_{si}}{4\varepsilon_{ox}}\left(1+\frac{\varepsilon_{ox}}{4\varepsilon_{si}}\frac{t_{si}}{t_{ox}}\right)t_{si}t_{ox}}$
Cylindrical GAA	$\lambda_{GAA}=\sqrt{\frac{2\varepsilon_{si}R^2\ln(1+\frac{t_{ox}}{R})+\varepsilon_{ox}R^2}{4\varepsilon_{ox}}}$

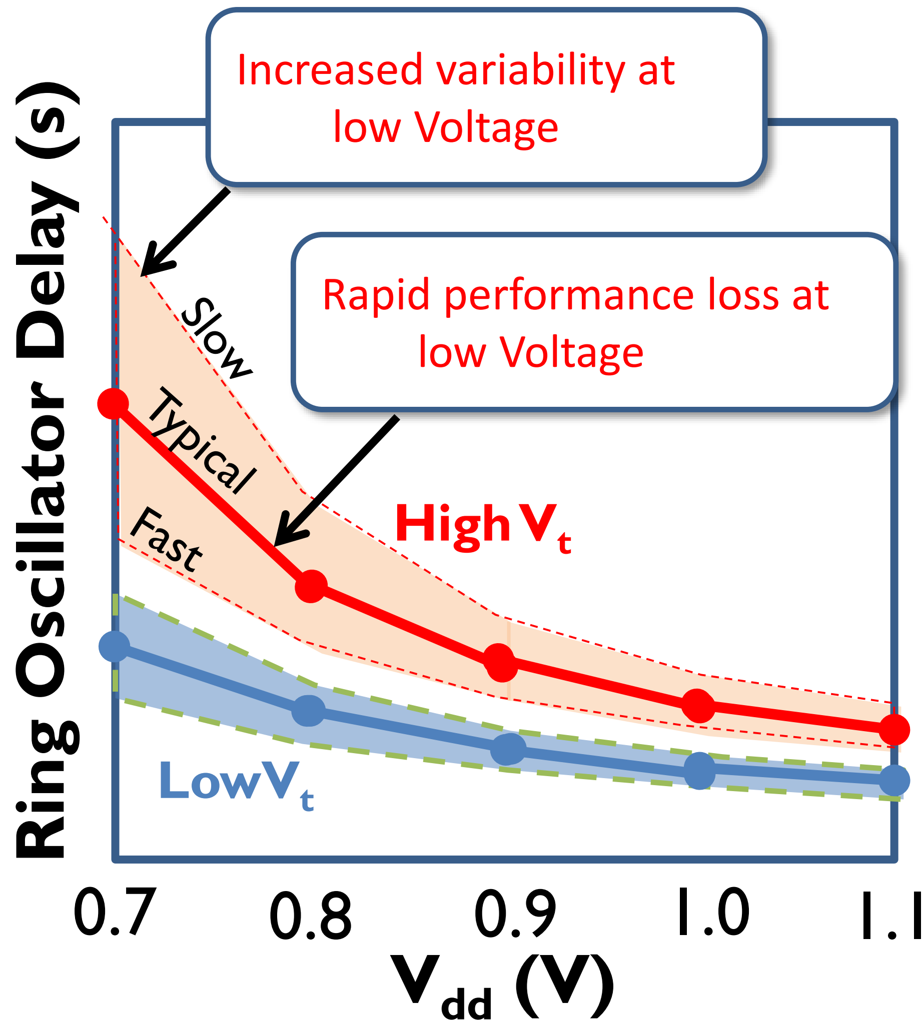


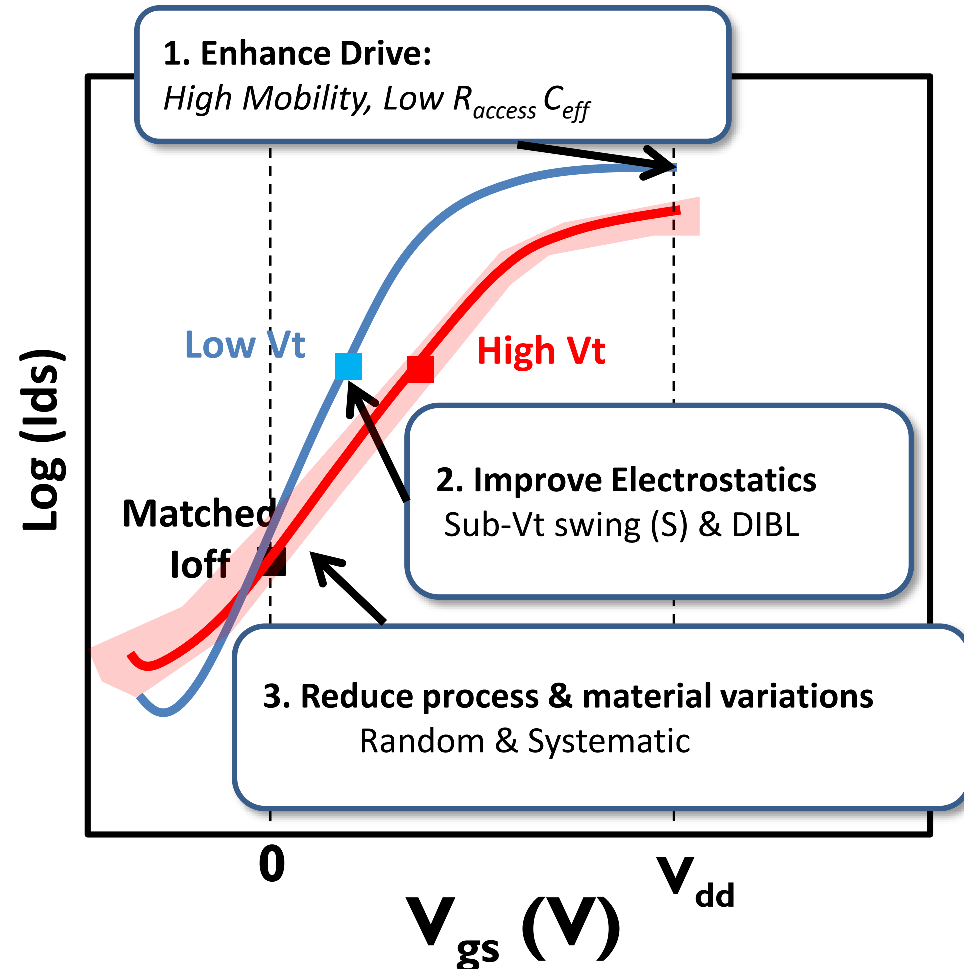
Nanowire R Vs.Fin t_{si}

Gate-All-Around (GAA)

- Electrostatic control of channel improves as L/λ ratio increases
- λ decreases with decreasing t_{si}
- λ decreases with increasing gate wrap
- λ decreases with reducing ε(channel) or increasing ε(gate ox)

The Role of the Low-Energy Transistor

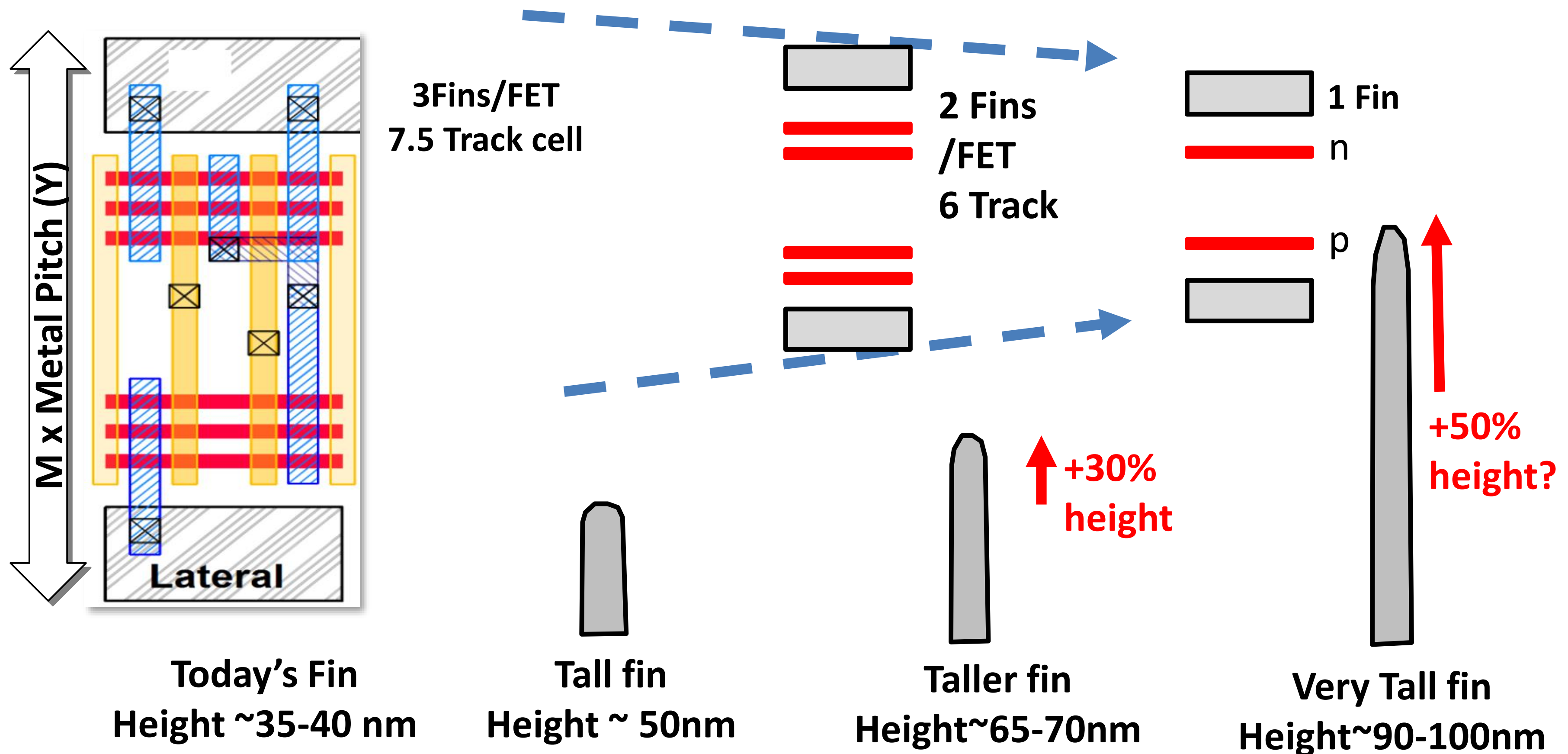




- Circuit performance loss & variability limits V_{dd} scaling
- Process & Transistor capability play critical roles

Enhancing Drive of the Circuits – Tall Fins

Y-Scaling: Cell Height Scaling – "Fin De-population with Taller Fins"

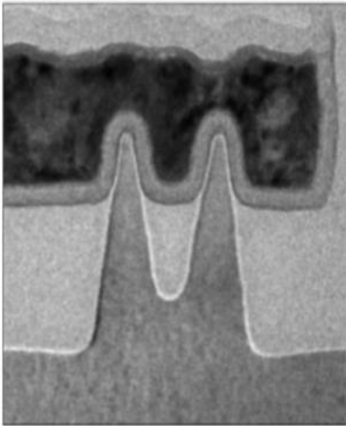


- Reduce the number of fins per transistor
- Need to make the drive (effective width) loss with taller devices
- Commensurate fin pitch scaling an offset the burden of Y scaling as well

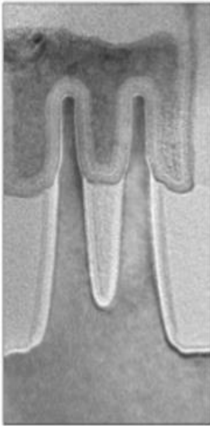
Fins Tomorrow (for 2020)

3nm Fins ~ 10-12 Si atoms

Fins Today

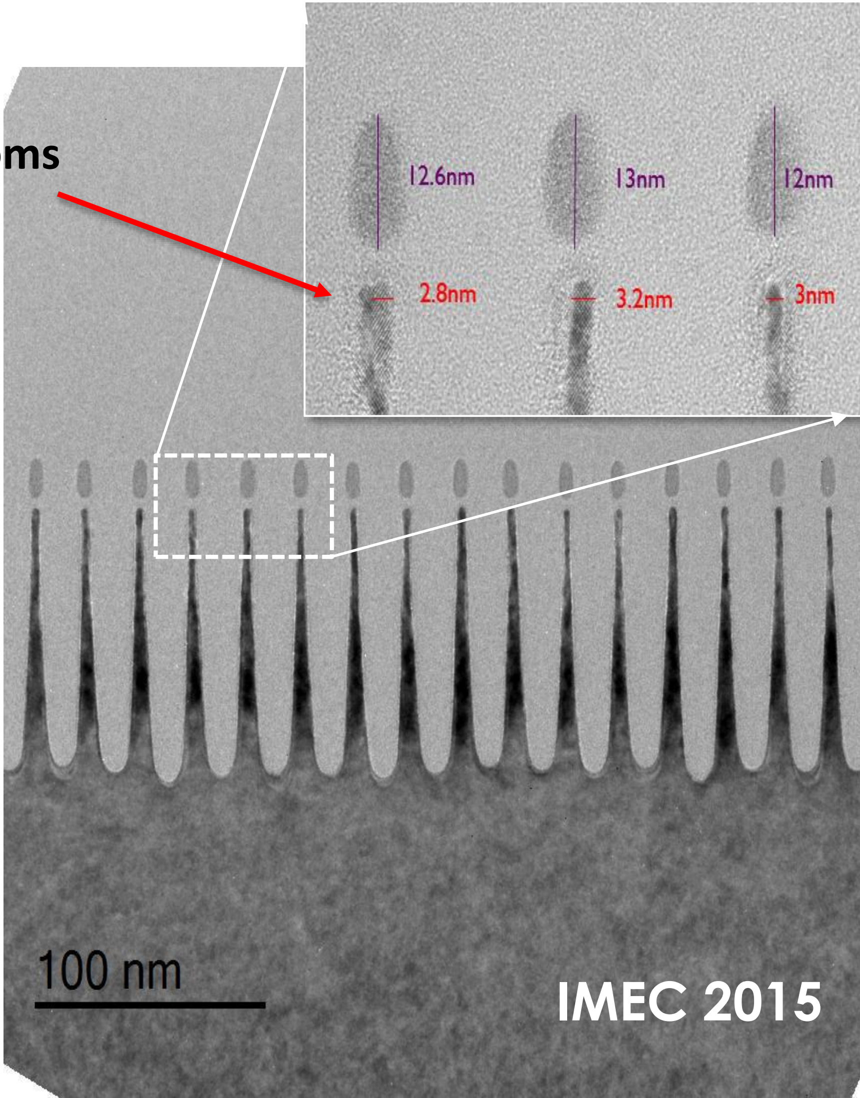


22 nm 1st Generation Tri-gate Transistor

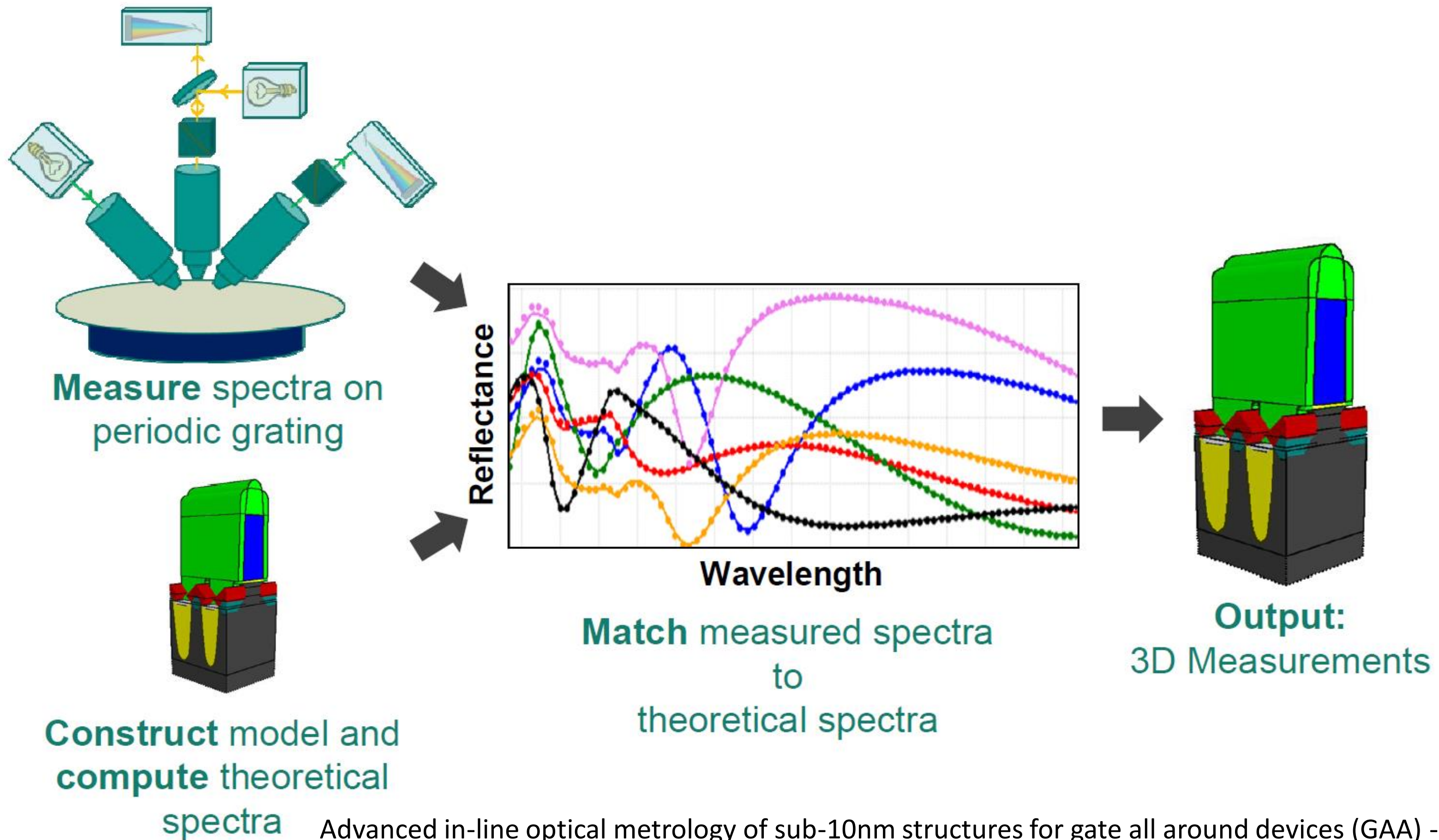


14 nm 2nd Generation Tri-gate Transistor

Intel Processes



Structural by Scatterometry - Optical Critical Dimension (OCD)

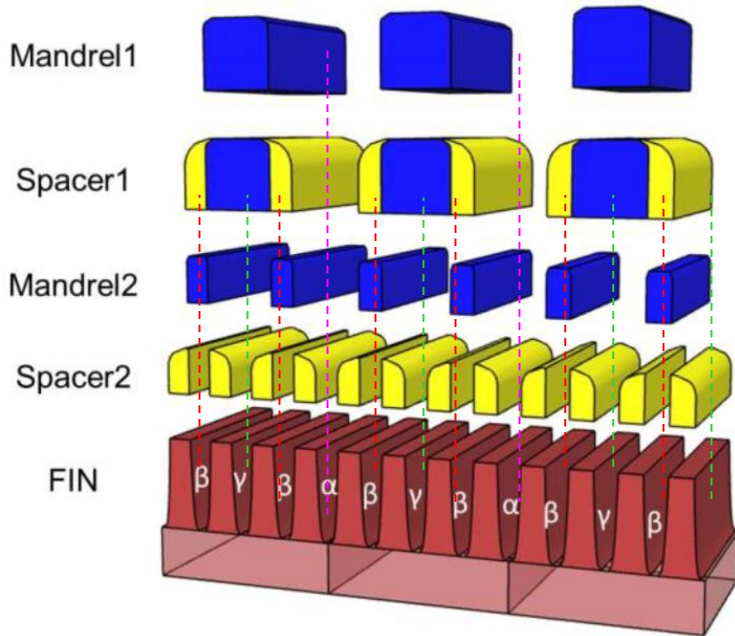


Advanced in-line optical metrology of sub-10nm structures for gate all around devices (GAA) - Muthinti, Raja; et. al. Proceedings of SPIE Volume: 9778 Article Number: 977810 Published: 2016

- Method to characterize large number of repetitive sub-optical dimension structures

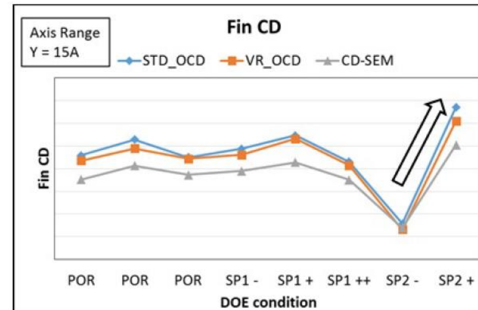
Self-Aligned Spacer Patterns Monitor by Scatterometry

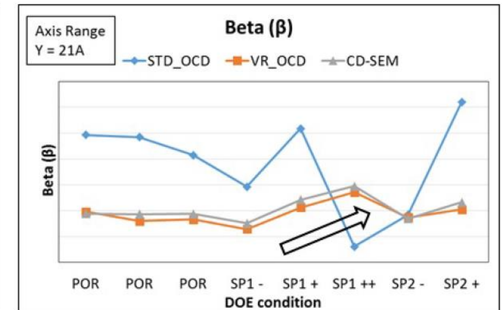
Self-Aligned Quadruple Patterning (SAQP)

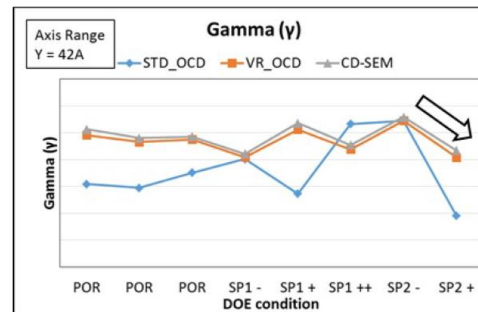


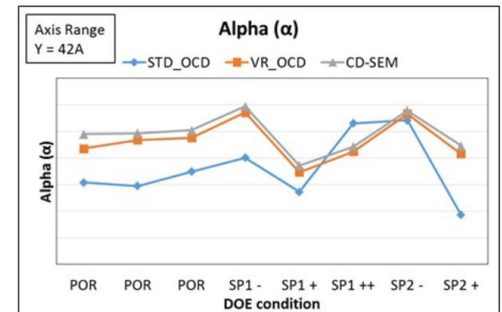
Fin Pitch walking Issue: $\alpha \neq \beta \neq \gamma$

Using Virtual-Reference OCD to correlate the pitch variation





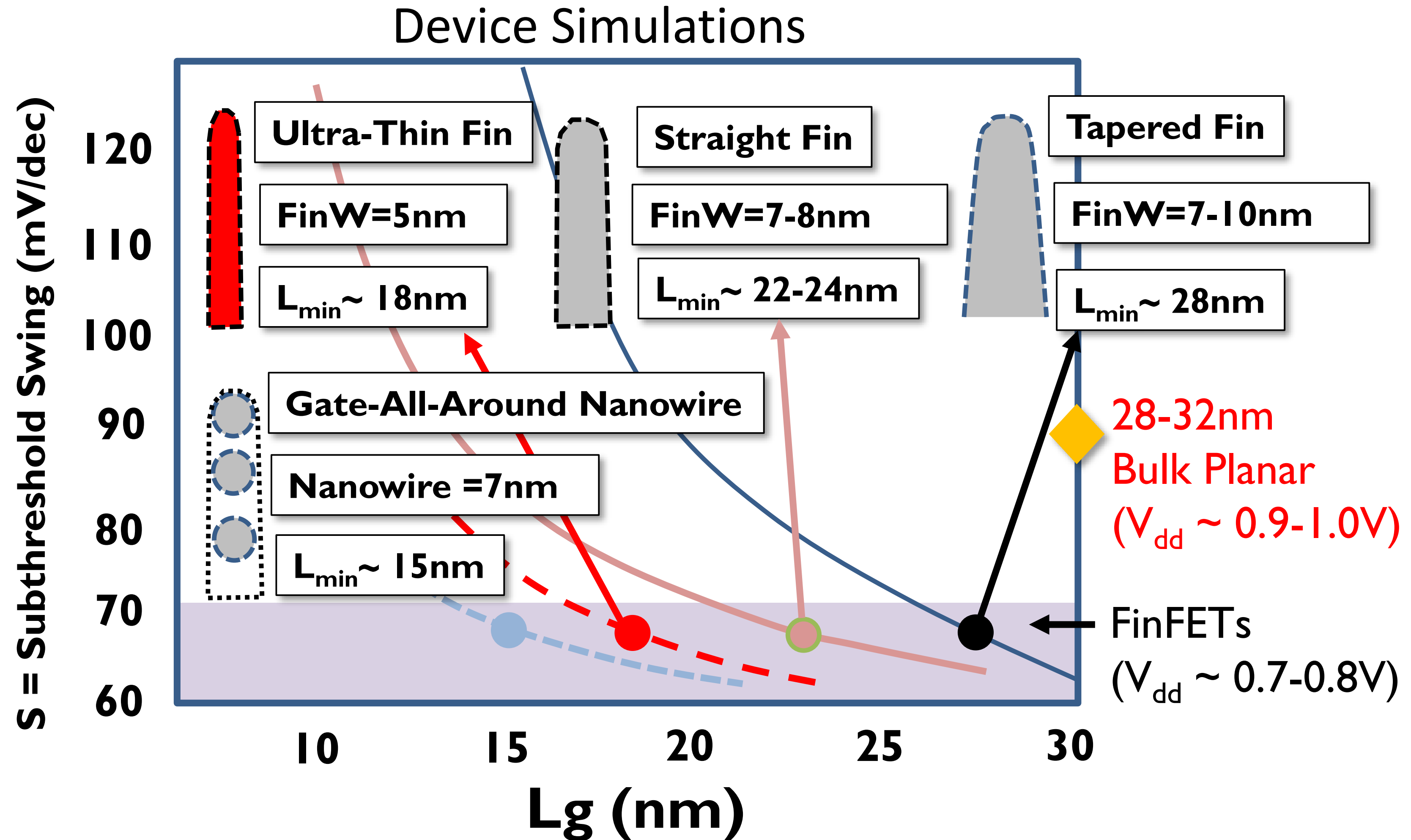




Reference information from actual CD-SEM measurements collected at the same process step as the OCD measurements

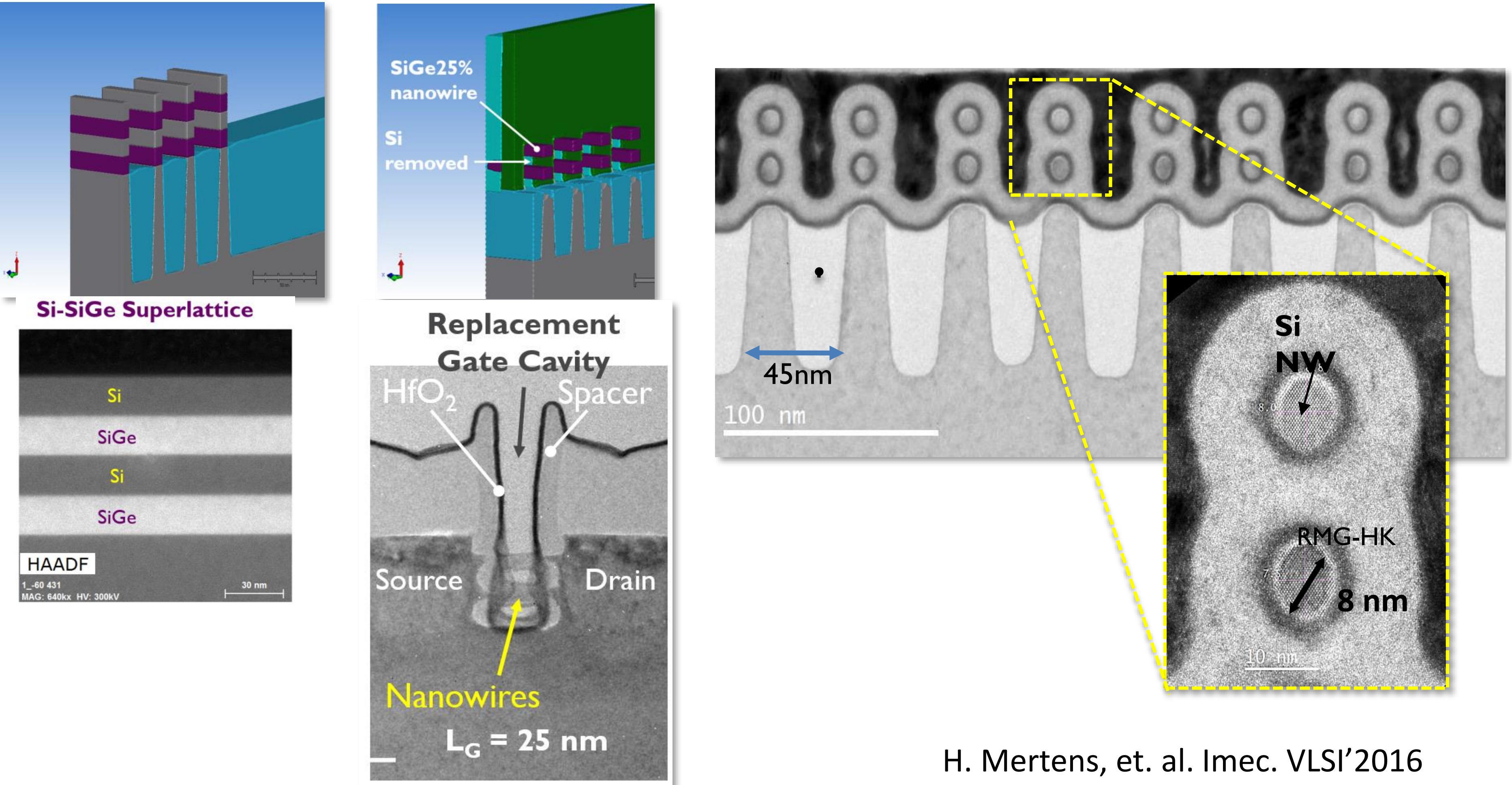
Scatterometry-based metrology for SAQP pitch walking using virtual reference
By: Kagalwala, Taher; et. al. (Nova & Globalfoundries, 30th Conference on Metrology, Inspection, and Process Control for Microlithography Location: San Jose, CA Date: FEB 22-25, 2016
Proceedings of SPIE Volume: 9778 Article Number: 97781W Published: 2016

End of FinFET Scaling – The Advent of Nanowires?



- FinFETs offered a Low-Voltage transistor option wrt bulk planar.
- To maintain electrostatics, simple FinFETs will hit limits

End of fin scaling: Nanowires (Target 2022-2024)

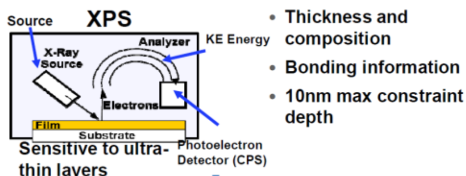


H. Mertens, et. al. Imec. VLSI'2016

•Increase complexity as we transition to the next device architecture

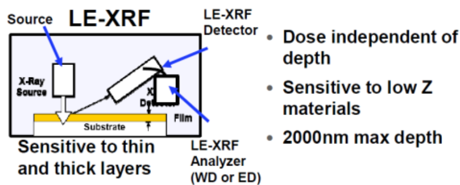
Structural & Material Analyses (Scatterometry+XPS+XRF)

X-Ray Photoelectron Spectroscopy (XPS) & Low Energy X-Ray Fluorescence (LE-XRF),



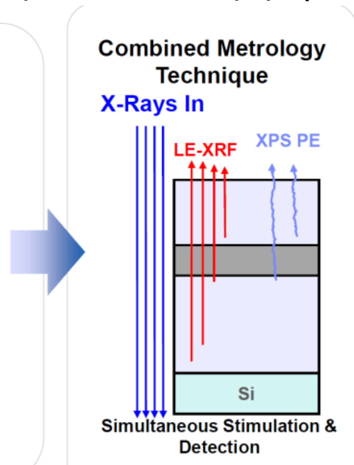
Sensitive to ultra-thin layers

- Thickness and composition
- Bonding information
- 10nm max constraint depth



Sensitive to thin and thick layers

- Dose independent of depth
- Sensitive to low Z materials
- 2000nm max depth



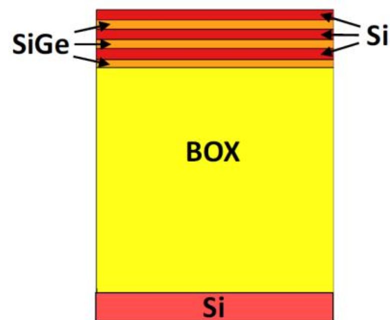


Figure 4: Film stack at the substrate formation step.

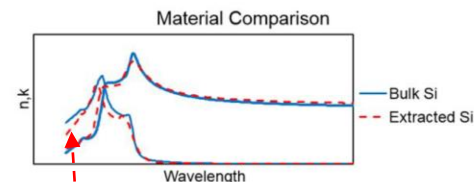


Figure 5: Modified (extracted) optical dispersions (n & k) of the silicon layers provided significantly better fit than the optical dispersions of bulk silicon. Possible explanations for this are described in the text.

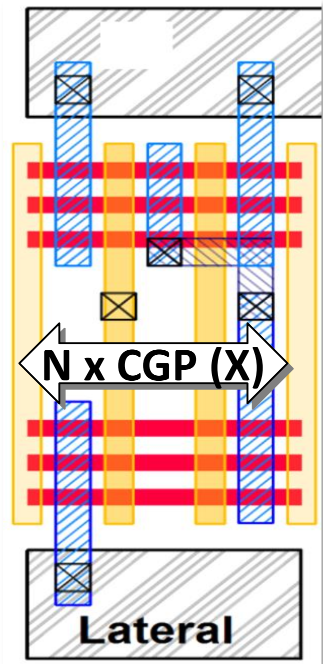
Based on n&k matching parameters:
Infer that Si in superlattic different from Bulk Si

- Scatterometry: Structure & Ge composition from volume data
- XPS: Accurate material anaysis
- XRF Benefit: “materials of the measured structure are transparent to the fluoresced (emitted) X-rays, so atoms can be easily “counted” with the technique”

Advanced in-line optical metrology of sub-10nm structures for gate all around devices (GAA)
By: Muthinti, Raja; et. al. Proceedings of SPIE Volume: 9778 Article Number: 977810 Published: 2016

Transistor-Influenced Approaches to scaling X-Y

X-Scaling: Cell Width Scaling – “Contacted Gate Pitch Scaling”



Gate Pitch

Contact – to – Gate (Spacer) Diminishing

Self-Aligned Contact

L_{gate}

GAA

FinFET

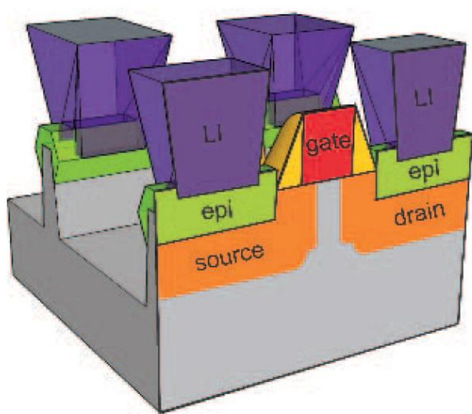
Physical Dimension (nm): 90, 60, 40, 10

3nm 5nm 7nm 10nm 14nm 20nm

CMOS Technology Nodes

- Need to scale Lg and Contact width to maintain CGP scaling
- Lg scaling limited by transistor electrostatics
- Contact width limited by transistor drive performance

High-Resolution 2-D Carrier Mapping in Scaled Devices



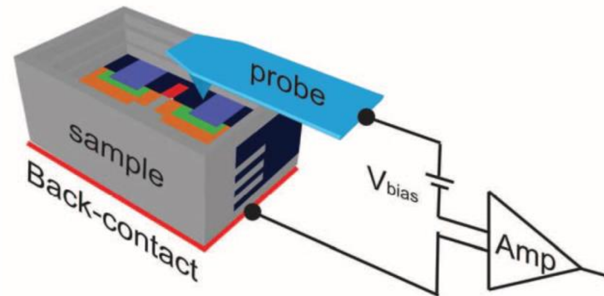
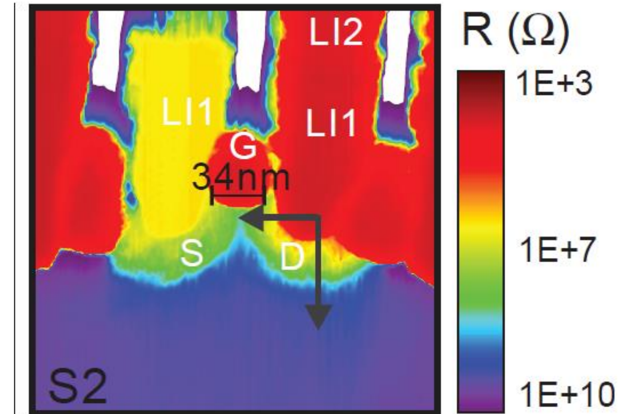


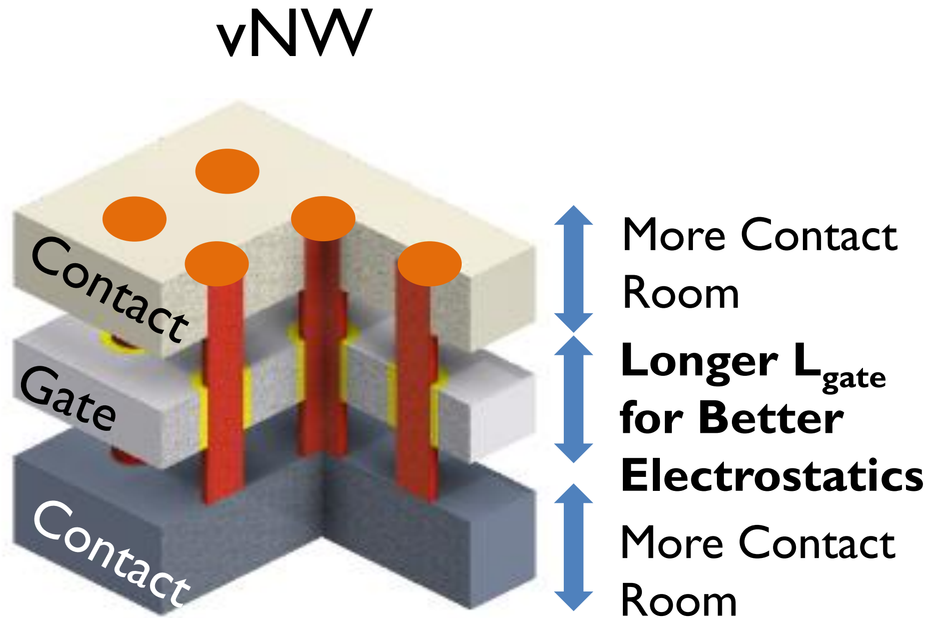
Fig. 1. 3D top-view of the scalpel-SSRM set-up. The diamond probe is utilized as a scalpel to remove material and reach the area of interest while scanning. Current (measured using a current amplifier) flowing between probe and back-contact at each position is a direct measure for the local resistivity and hence for the active dopant concentration.

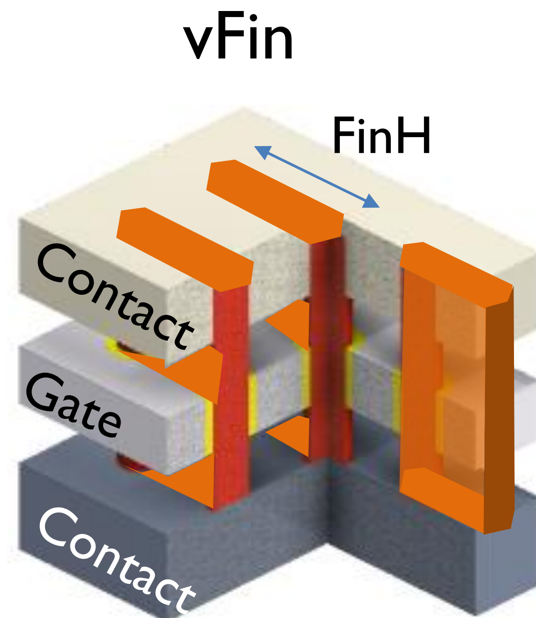


- Scalpel scanning spreading resistance (5 orders resolution) microscopy (s-SSRM) (sub-2nm resolution)
- To calibrate TCAD models, necessary for the design of highly scaled devices
- Possible as models for fault isolation in failure analysis as well

P. Eyben et. al. "Accurate prediction of device performance in sub-10nm WFIN FinFETs using scalpel SSRM-based calibration of process simulations,", 2016 International Conference on Simulation of Semiconductor Processes and Devices (SISPAD), pp. 287 – 290, 2016

Vertical GAA-FETs (Beyond 2025)





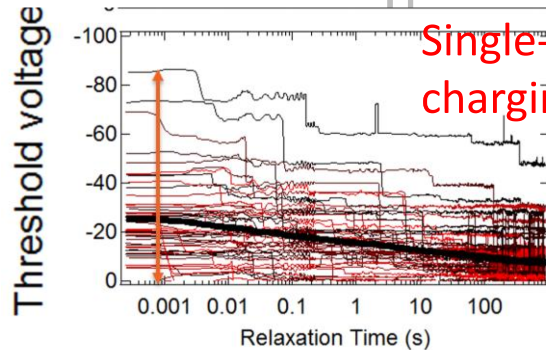
Best Electrostatics Capability but drive limited by NW density Per Foot Print

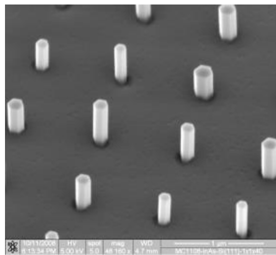
Lesser Electrostatics Capability **but can provide more current per foot print**

- Vertical GAA Fins may alleviate the drive constraints of vertical nanowires
- Need to trade off between Fin Height (FinH) and pitch Vs. Lgate
- Need to account for wire or Fin current direction & conduction orientation

Rising influence of Material Defects

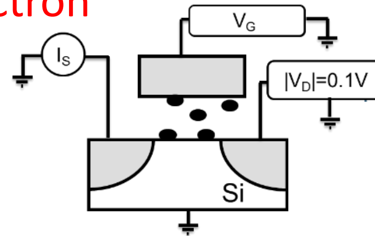
- **Mostly /All surface/Interface defect dominated**

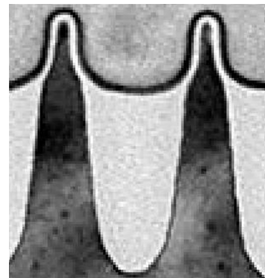




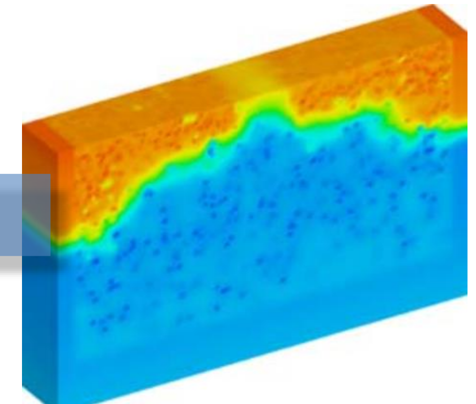
- **Decreasing body volume → Increase Surface traps/defects influence**
- **RTN-Vt instabilities**

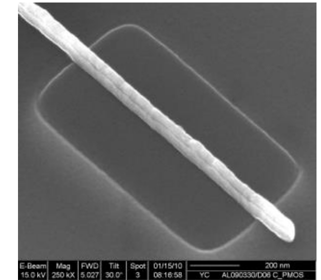
Single-electron charging





- **Planar FETs Random Dopants, Gate-stack**





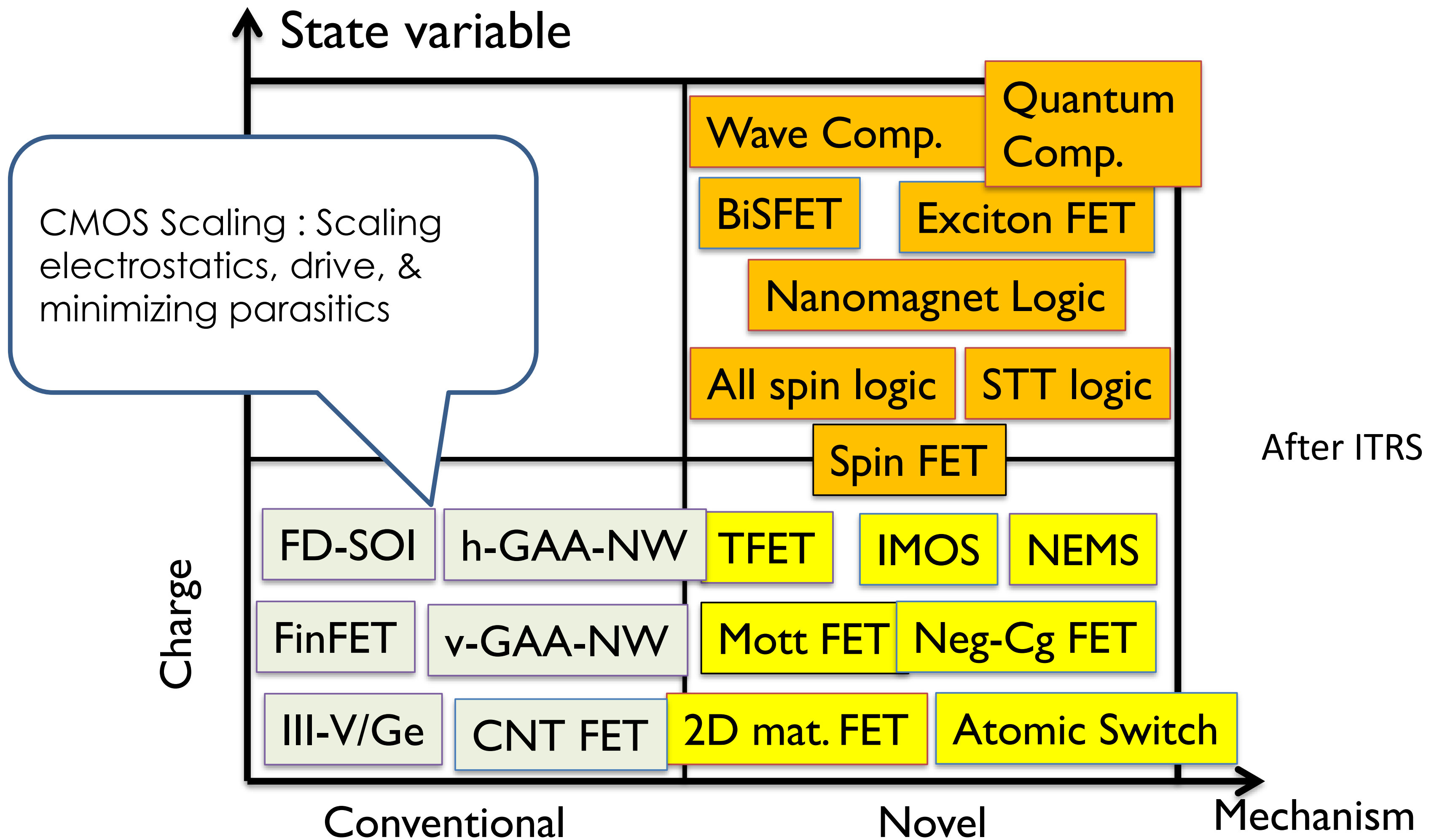
Random Telegraph Noise + BTI + 1/f **Random Dopants + BTI + 1/f**

- Increasing surface-to-volume ratio→ inc. influence of trap/defect-based variability

Complex Material Systems

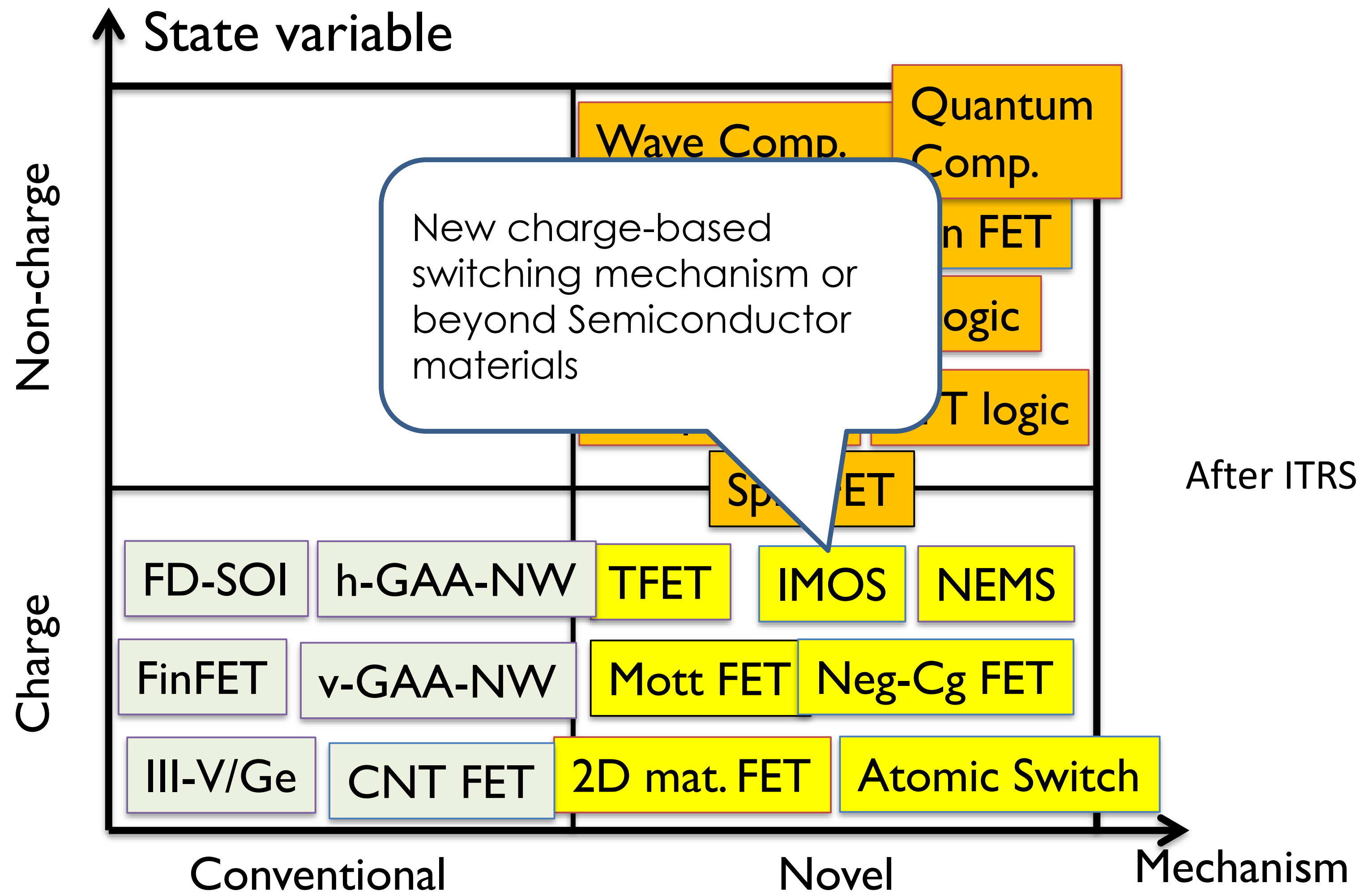
Beyond Silicon

Established Vs. Exploratory: Many Research Device Options



- Novel Device Architectures being explored: Charge Vs. Non-Charge based.

Established Vs. Exploratory: Many Research Device Options



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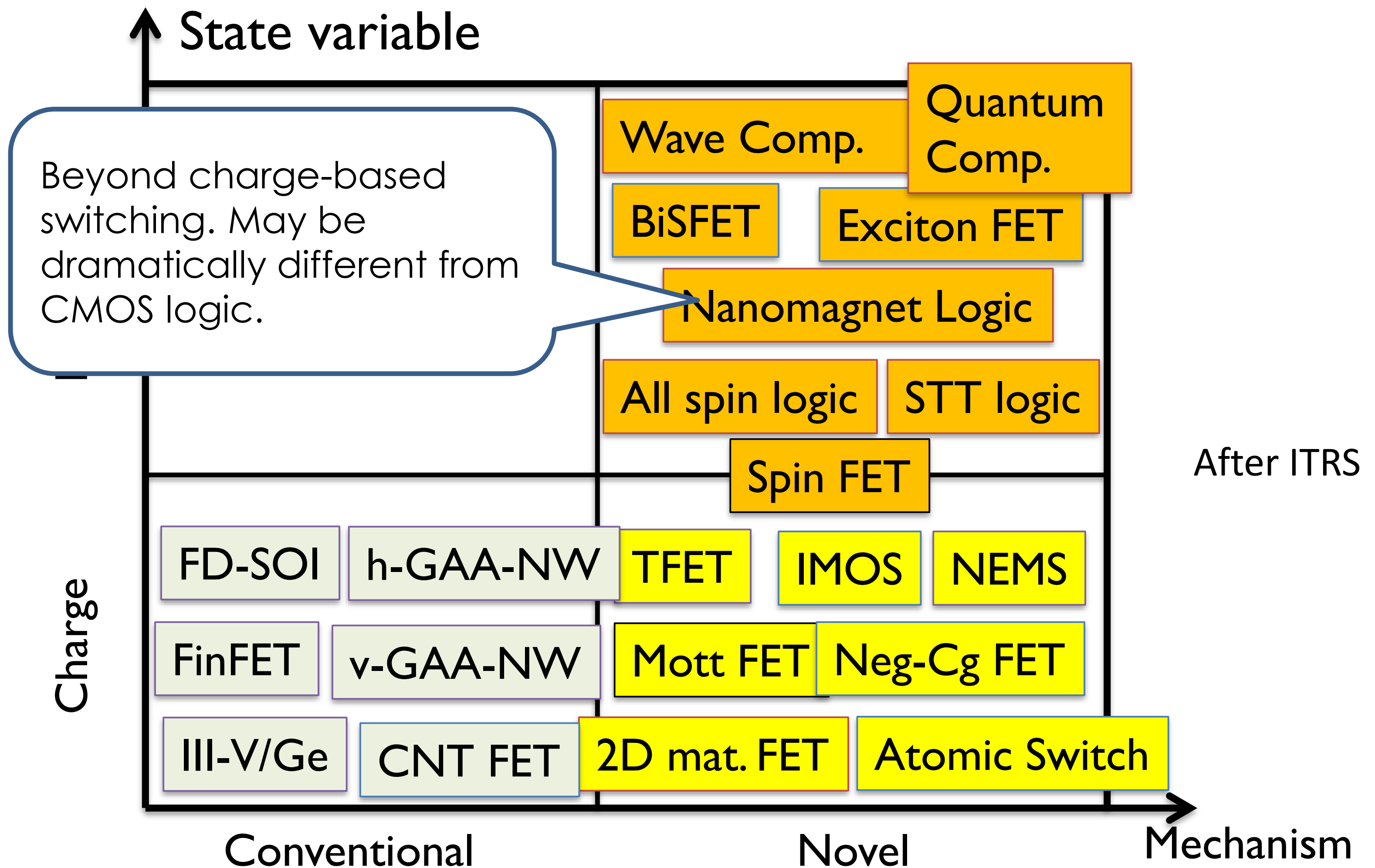

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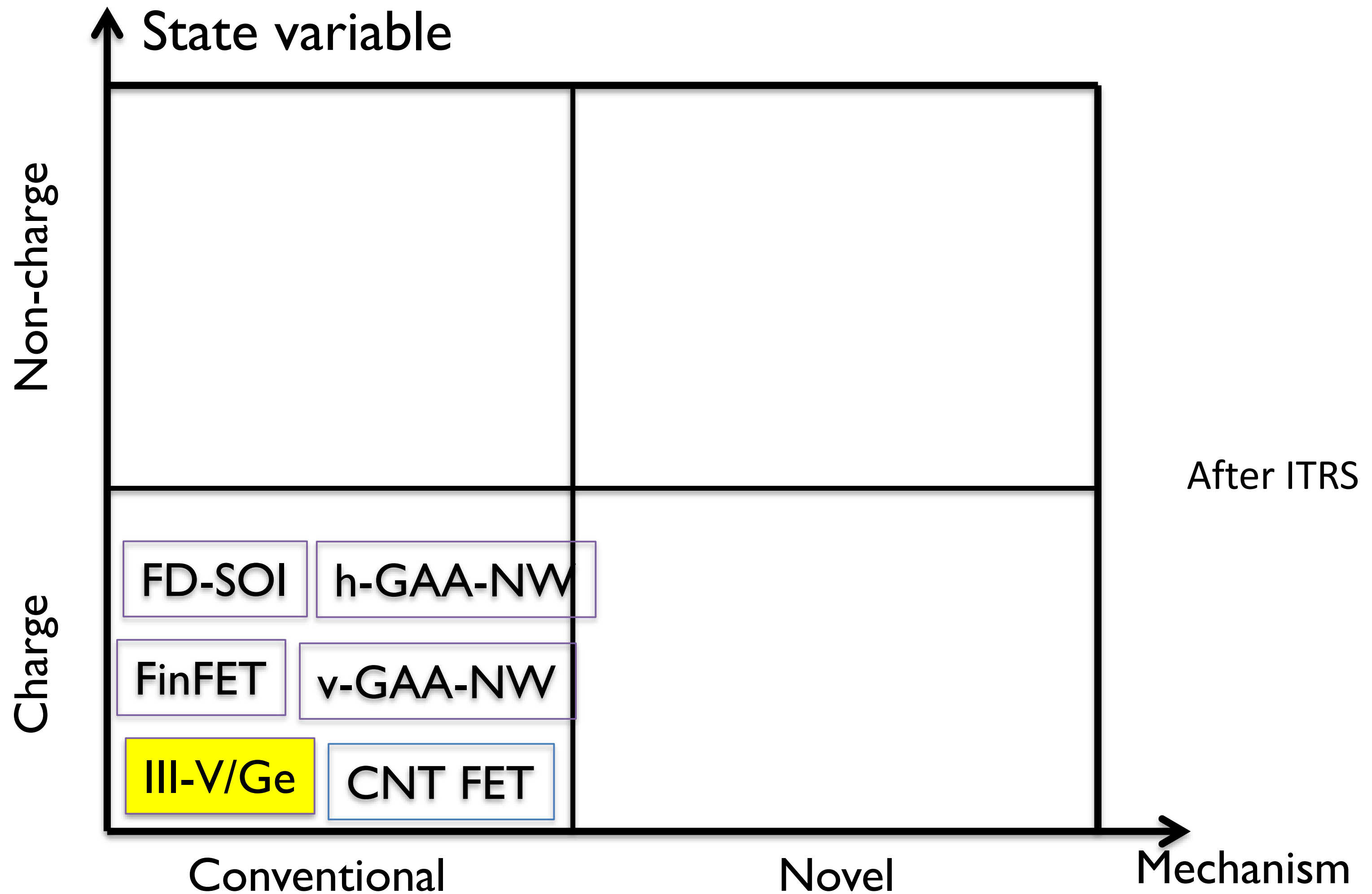
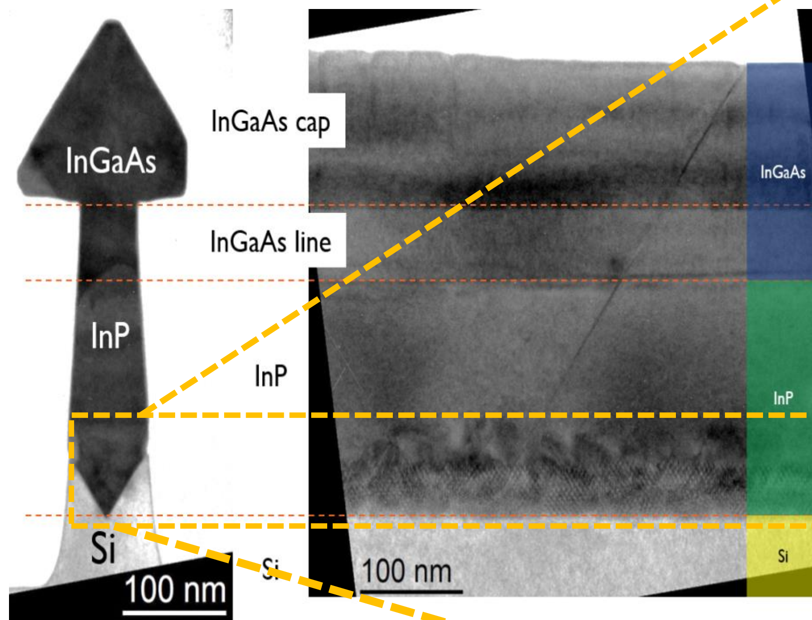
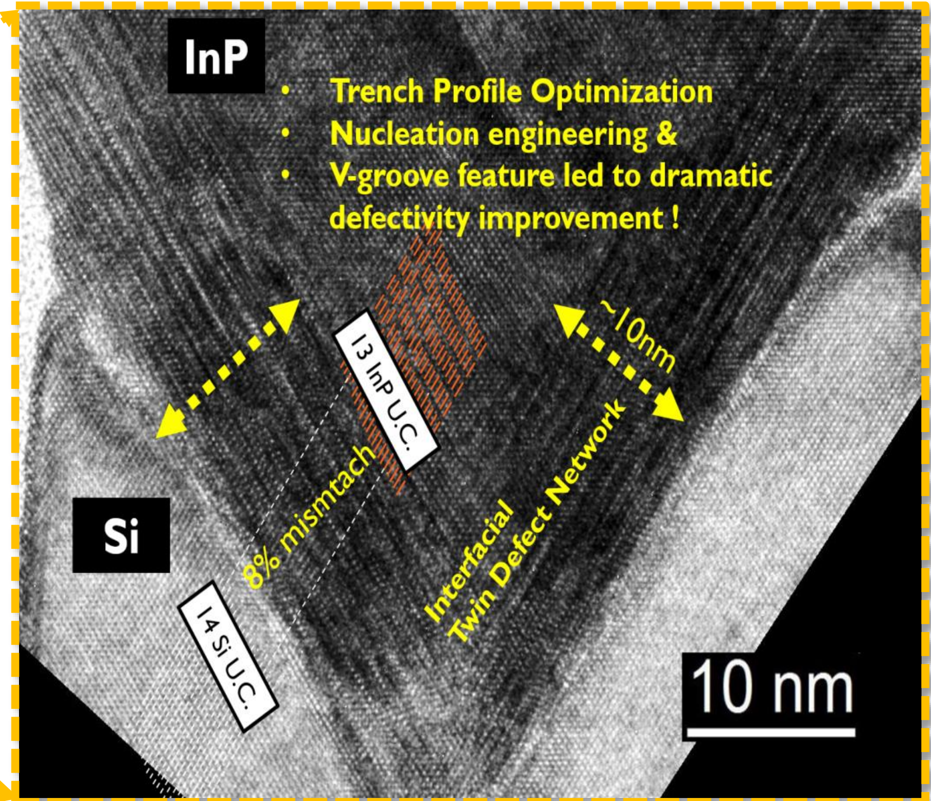


- Novel Device Architectures being explored: Charge Vs. Non-Charge based.

Defect Engineering



C. Merckling & IIIV Epi Team



- Unique defect trapping Innovation allows for InGaAs to be integrated in tight geometry in proximity to Si & other materials

Alloy Composition, Nanostructures, & Defects

Atom Probe Tomography

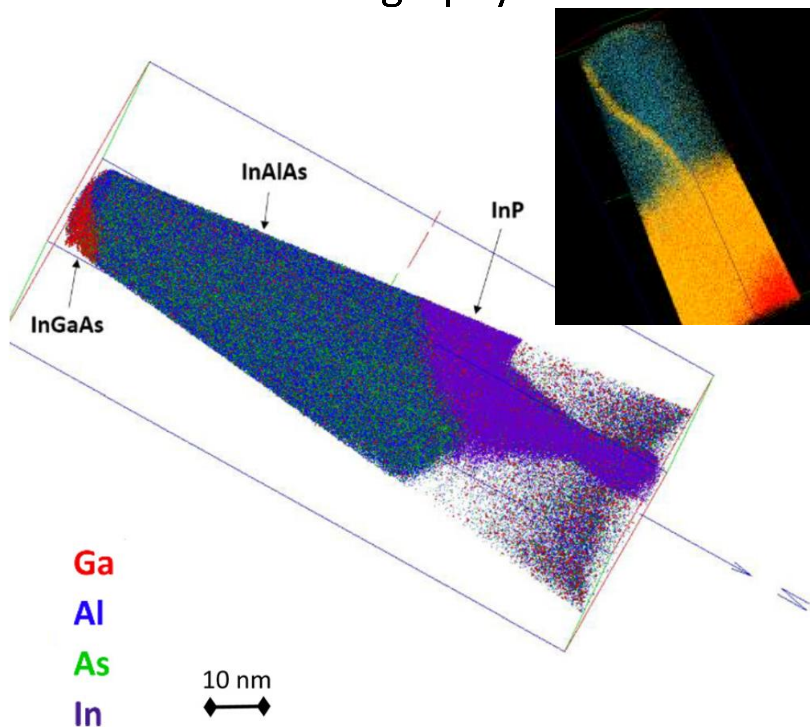
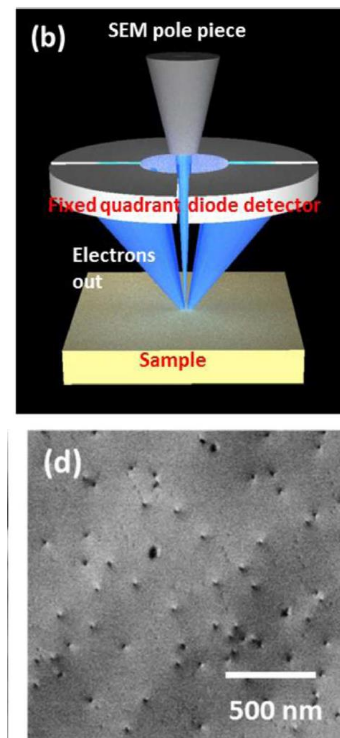


FIG. 10. (Color online) Three-dimensional APT reconstructed atom distribution within the 120 nm wide trench (InGaAs/InAlAs/InP stack).

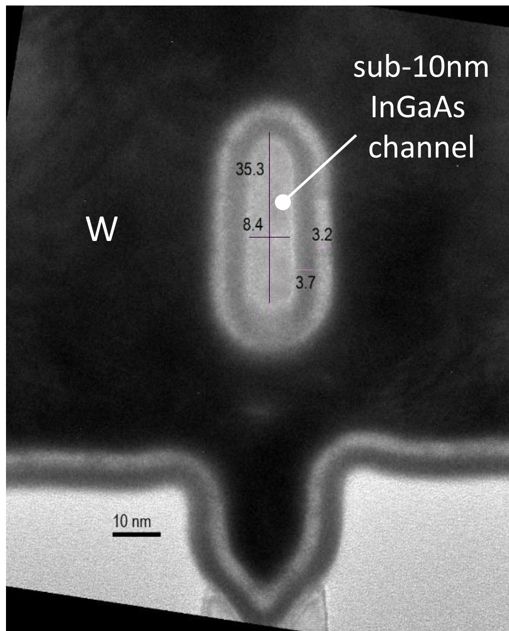
Composition analysis of III-V materials grown in nanostructures: The self-focusing-SIMS approach
By: Franquet, Alexis; Douhard, Bastien; Conard, Thierry; et al.
JOURNAL OF VACUUM SCIENCE & TECHNOLOGY B
Volume: 34 Issue: 3 Article Number: 03H127
Published: MAY-JUN 2016

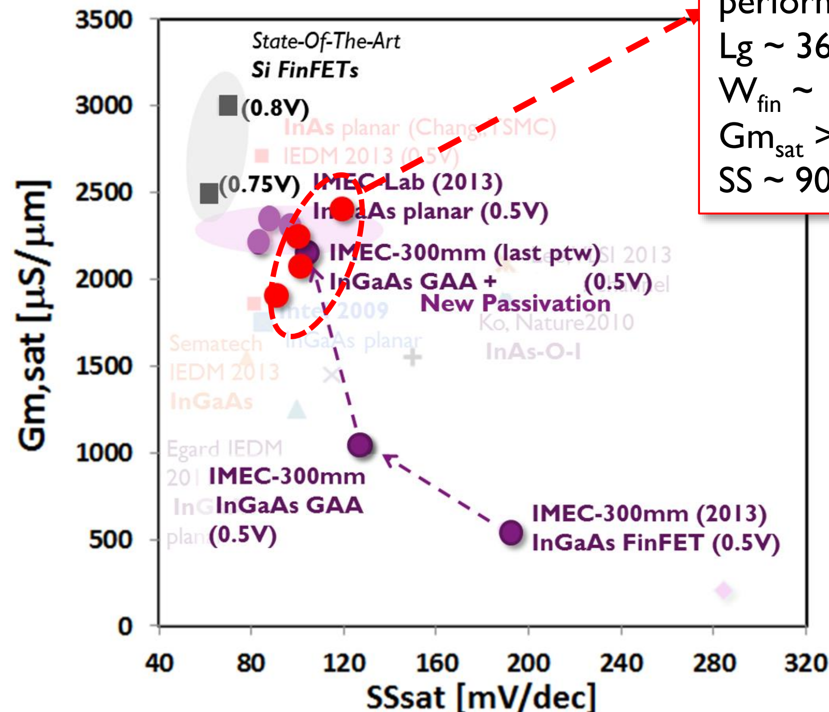
Electron channeling contrast imaging



Reprint of: Electron channelling contrast imaging for III-nitride thin film structures
By: Naresh-Kumar, G.; Thomson, D.; Nouf-Allehiani, M.; et al.
MATERIALS SCIENCE IN SEMICONDUCTOR PROCESSING
Volume: 55 Special Issue: SI Pages: 19-25 Published: NOV 15 2016

Scaled III-V Gate-Around devices

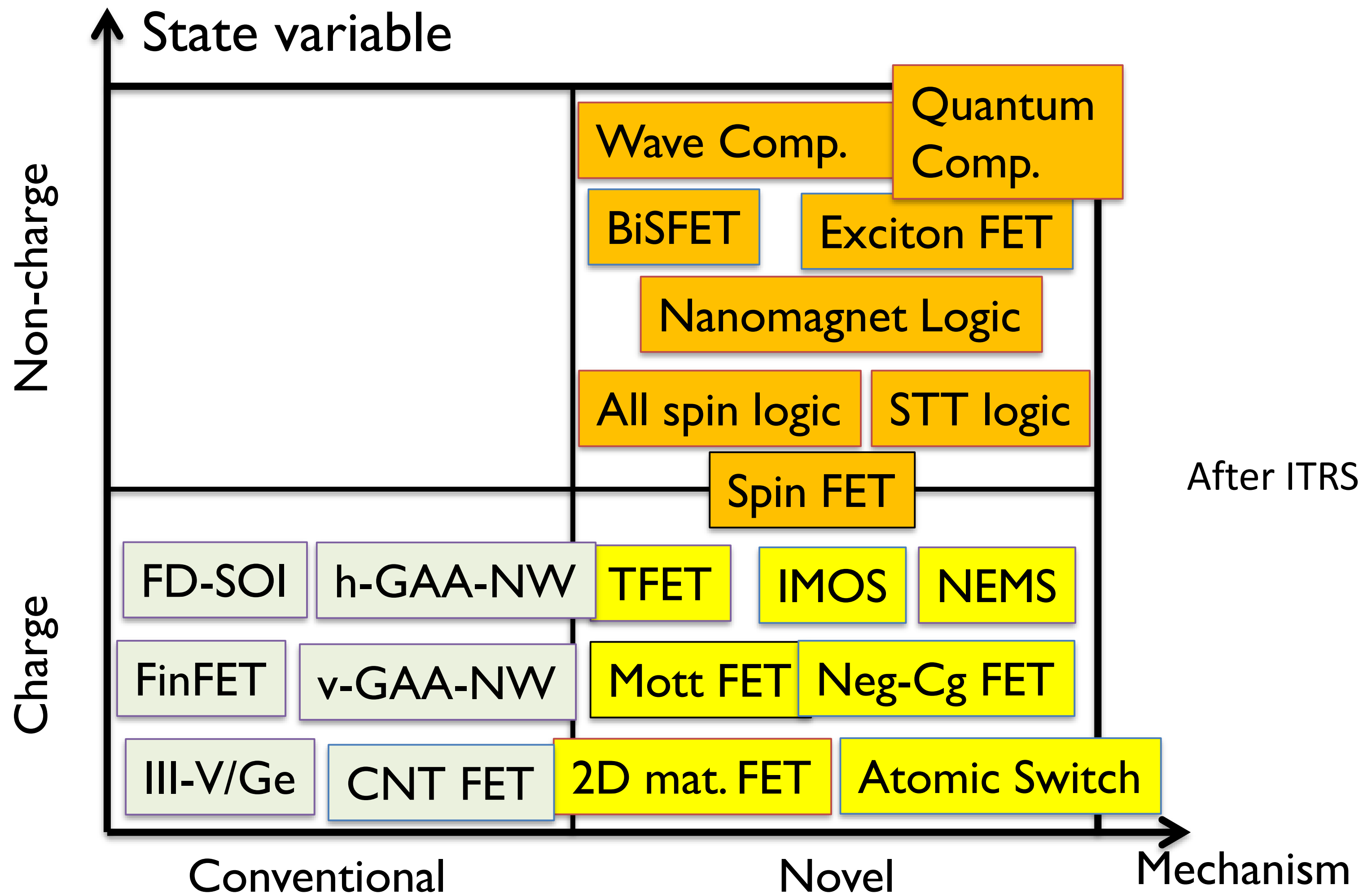




Record InGaAs channel performances for V_{dd}=0.5V
Lg ~ 36nm-46nm (NEW)
W_{fin} ~ 16nm (NEW)
Gm_{sat} > 2000 μS/μm
SS ~ 90-100mV/dec

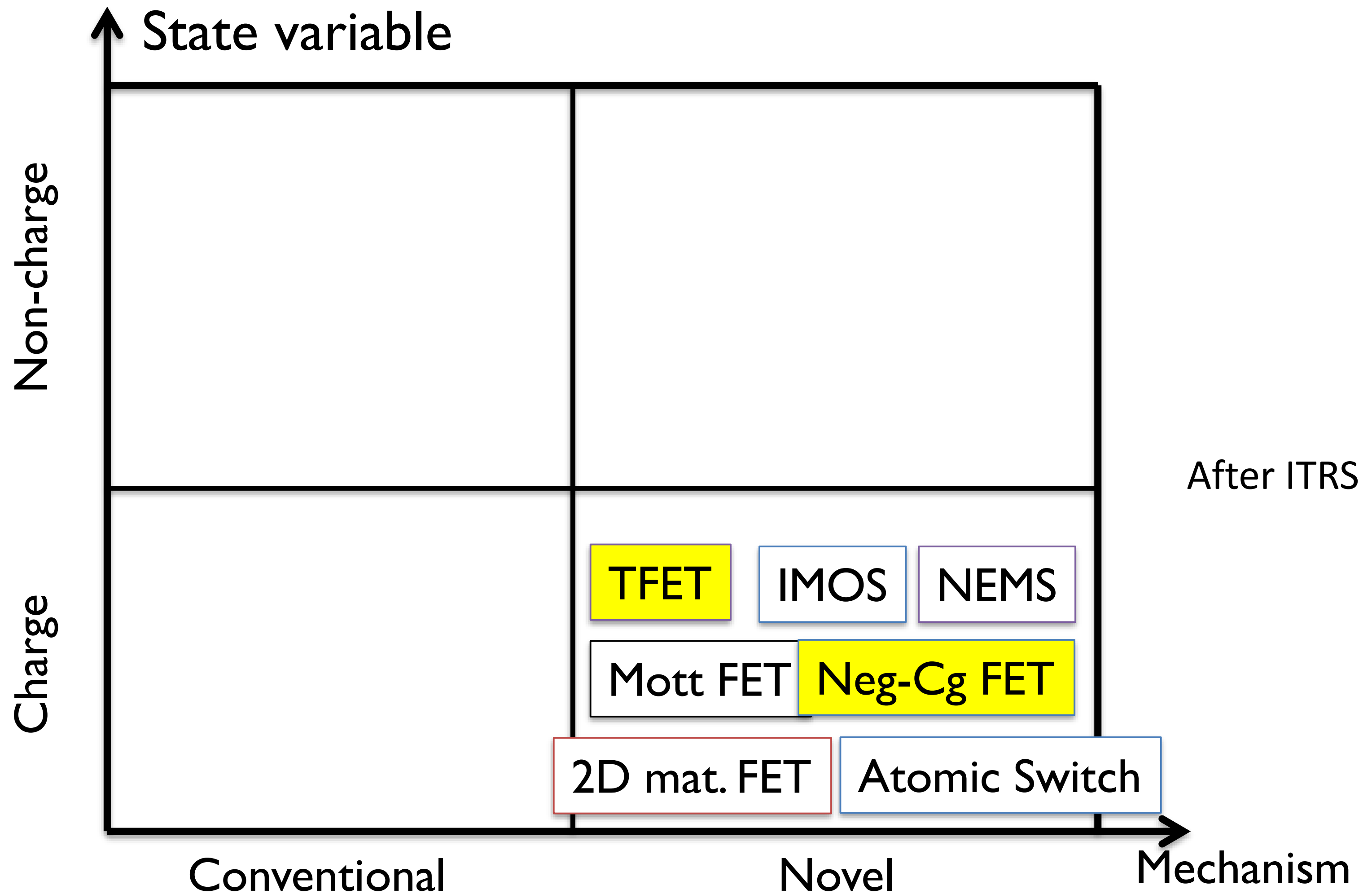
- Record performance for InGaAs GAA devices on 300mm substrates achieved at scaled dimensions
- **Reduction of bulk defects & atomic passivation of interface are key factors**

Established Vs. Exploratory: Many Research Device Options



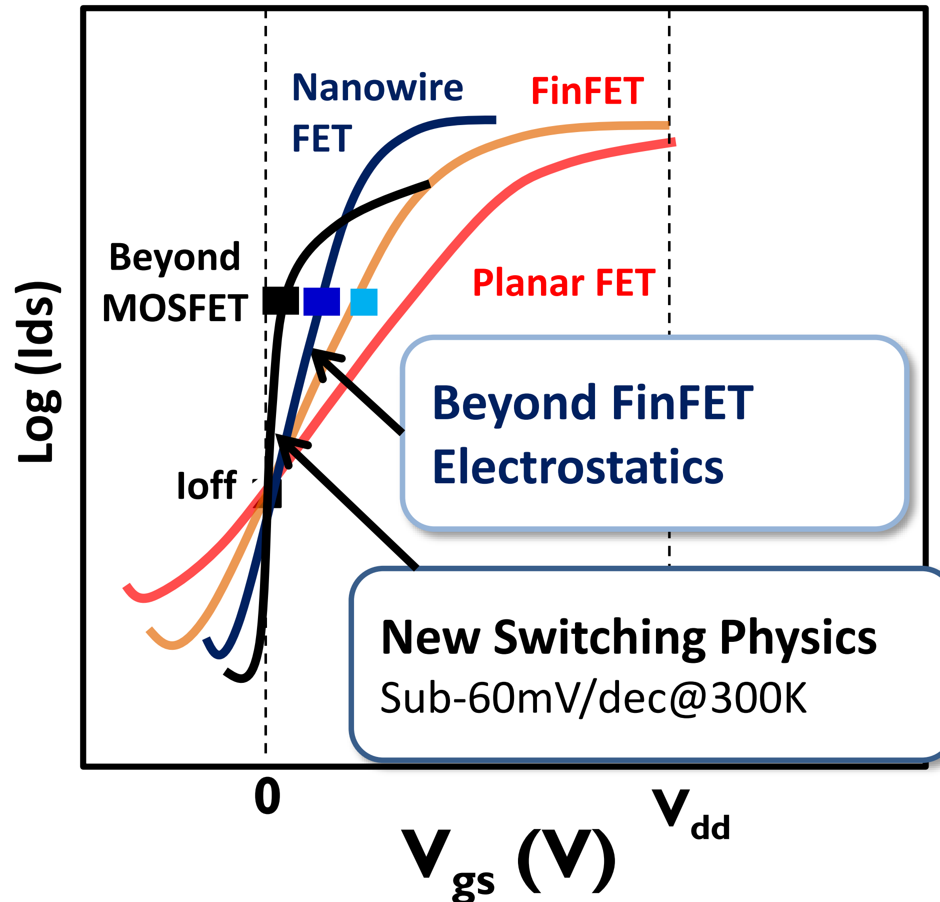
- Novel Device Architectures being explored: Charge Vs. Non-Charge based.

Established Vs. Exploratory: Many Research Device Options



- Novel Device Architectures being explored: Charge Vs. Non-Charge based.

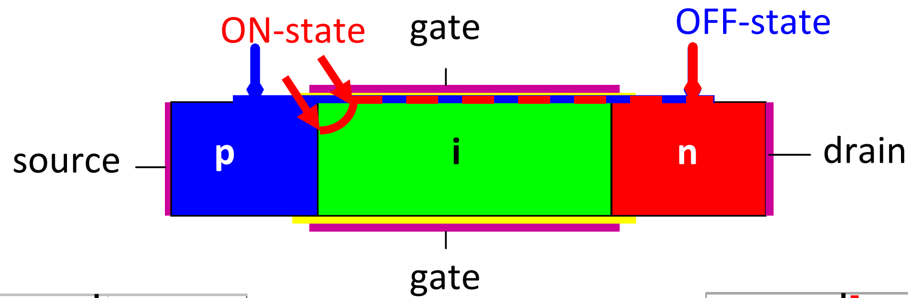
V_{DD} Scaling & Super-Steep Slope Devices

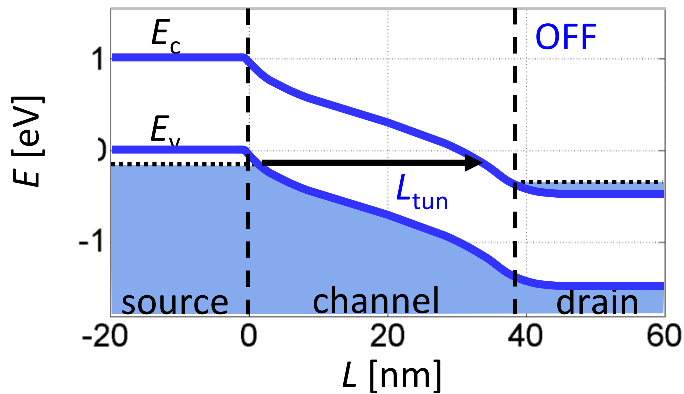


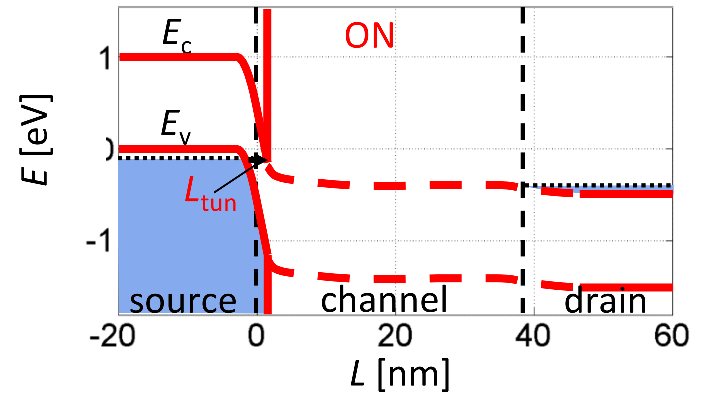
- Gate-All-Around Nanowire FET is the limit to MOSFET Subthreshold Swing Scaling
- Need new transistor options

Tunnel-FET (TFET)

TFET = reverse biased p-i-n diode with gate







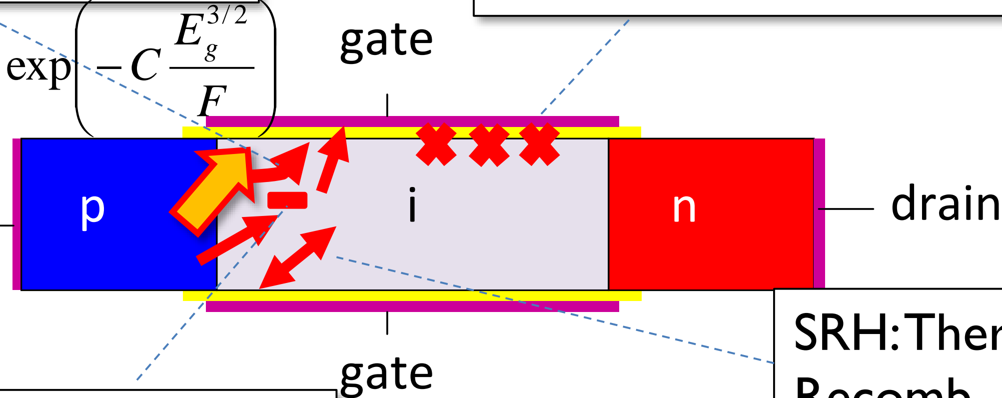
Promise of subthreshold swing < 60mV/dec

TFET Swing & leakage Detractors

Lateral (Point) Vs. Vertical (Line) Tunneling & resultant DOS

$$J_{BTBT} \propto \exp\left(-C\frac{E_g^{3/2}}{F}\right)$$

Dit: Interference & Fermi pinning due to interface defect states

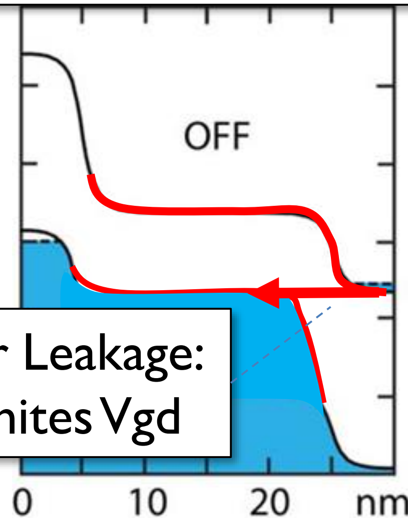


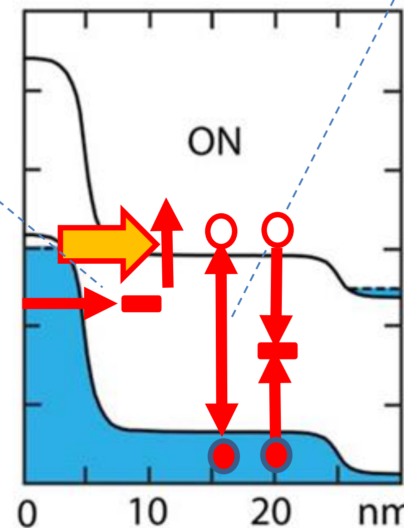
$$J_{trap} \propto C_2 \exp\left(\frac{-E_g/2 + \Delta E_T}{kT}\right)$$

SRH: Thermal Gen. & Recomb.

TAT: Trap-Assisted-Tunneling
Phonon-assisted Tunneling

$$J_{SRH} \propto C_1 \exp\left(-\frac{E_g/2}{kT}\right)$$



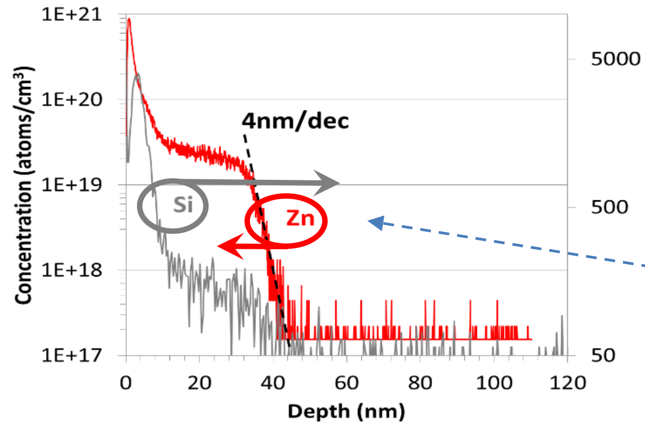


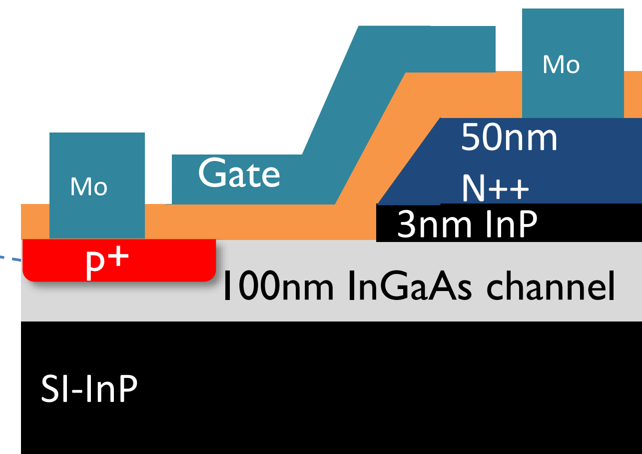
Ambipolar Leakage: Low Eg limites Vgd

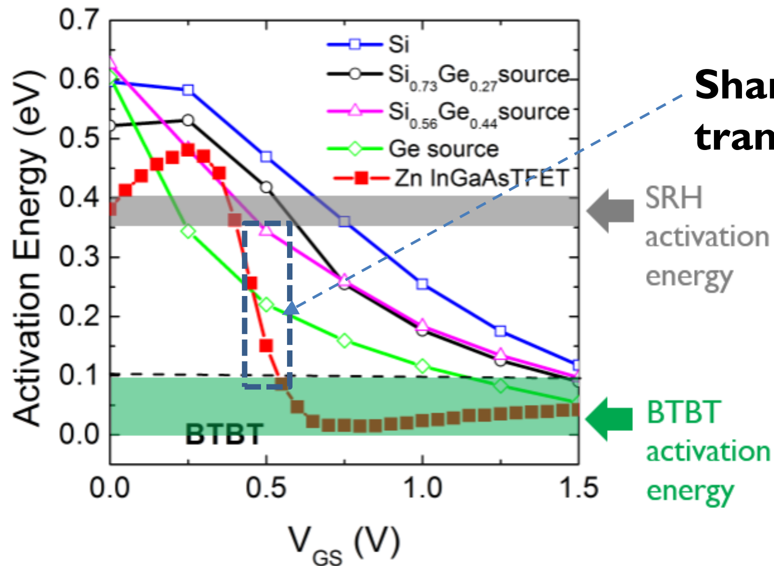
Low-TAT III-V Homojunction TFET

"Gentle" High p+ box-like Zn doped source by SOG diffusion

(Work follows approach of Noguchi (U. of Tokyo), IEDM 2013)







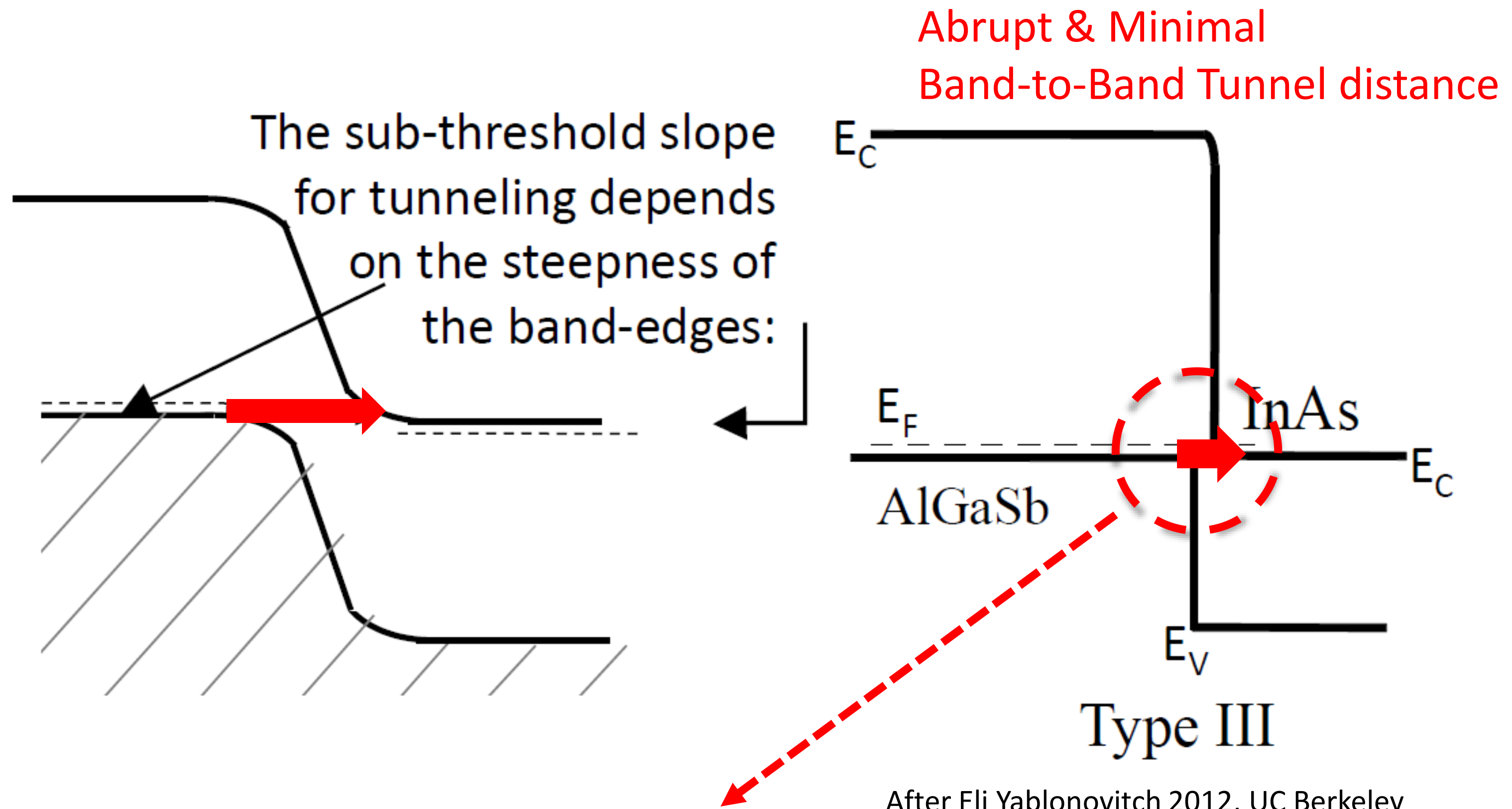
Sharp BTBT-SRH transition

SRH activation energy

BTBT activation energy

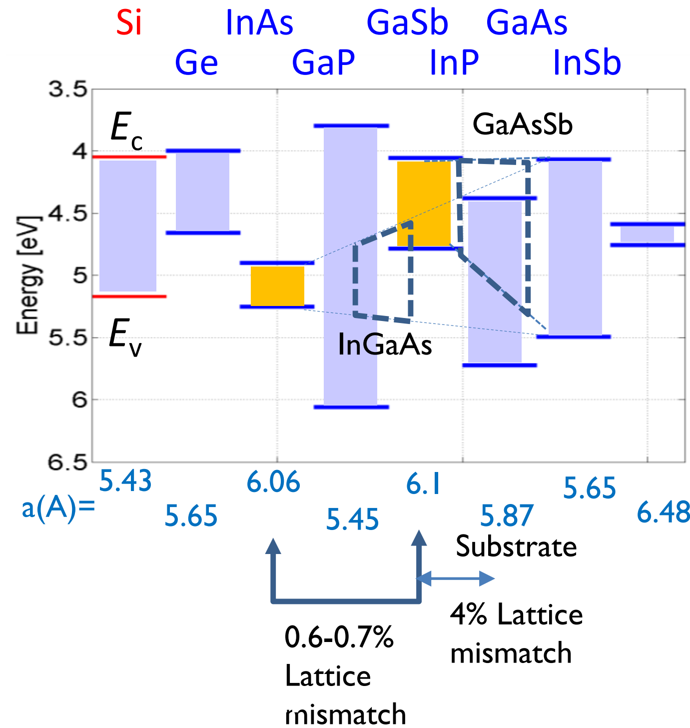
Benchmark shows significantly lower TAT

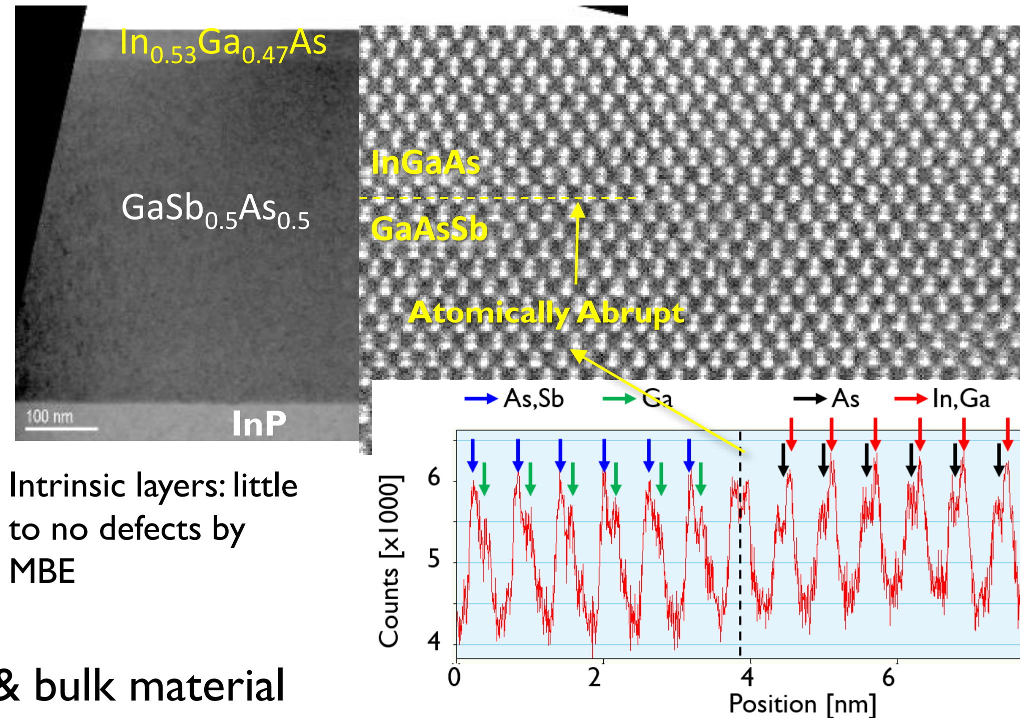
Heterostructure Tunnel Junctions



Lower tunnel resistance with shorter tunnel distance
Conduction modulated by alignment of band-to-band states

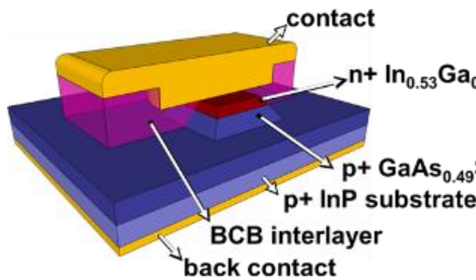
Hetero-structure Tunnel Junctions

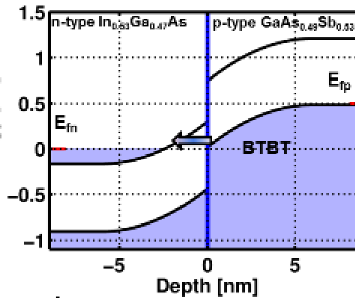


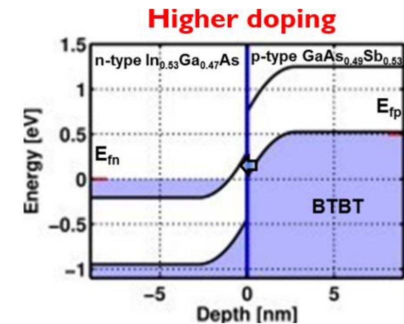


- Need abrupt low-defectivity junctions & bulk material
- Working on InAs/GaSb on GaAs and Si

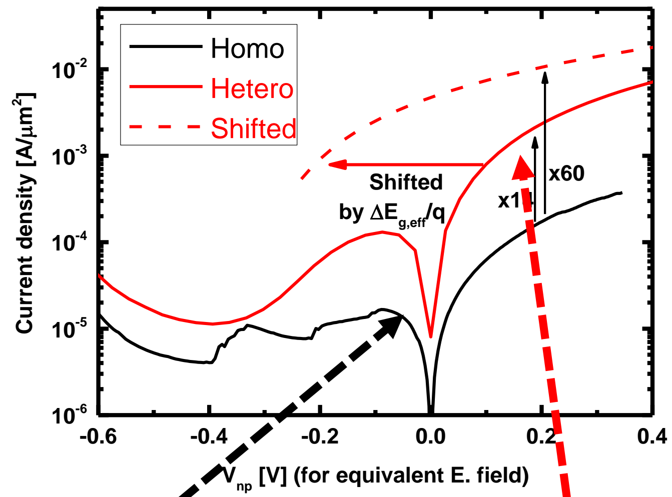
Hetero-structure Tunnel Junctions

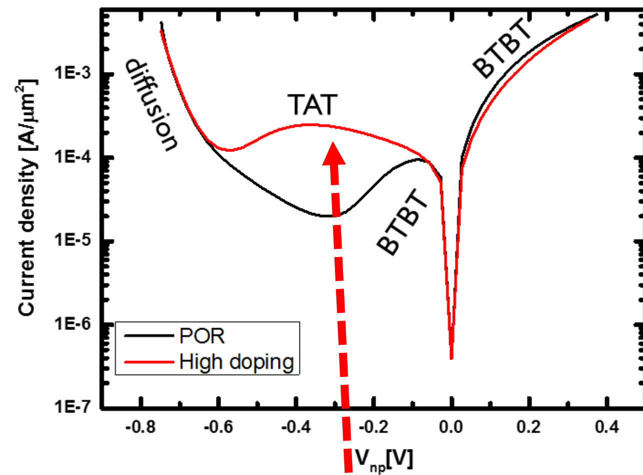






Increased BTBT confirmed





- Higher Doping increased TAT

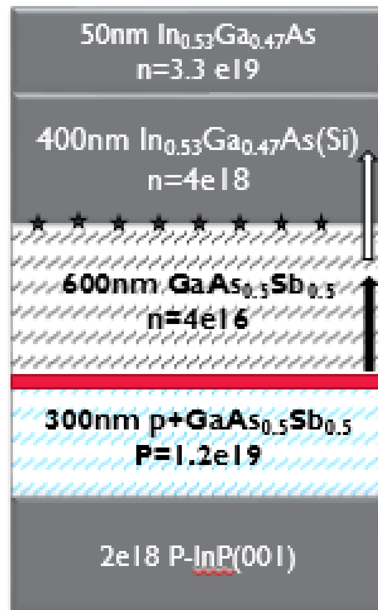
InGaAs-GaAsSb heterojunction
Higher band-to-band tunneling (BTBT)

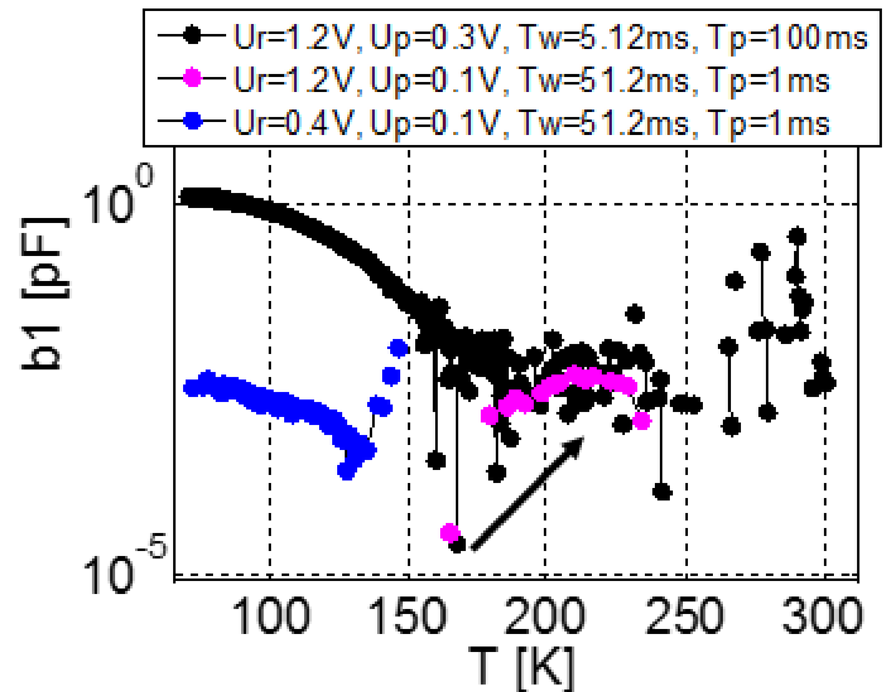
Trap-assisted tunneling (TAT) due to Increased doping destroys BTBT, under reversed bias.

InGaAs- homorojunction

Defect Energy Level Important: DLTS needed

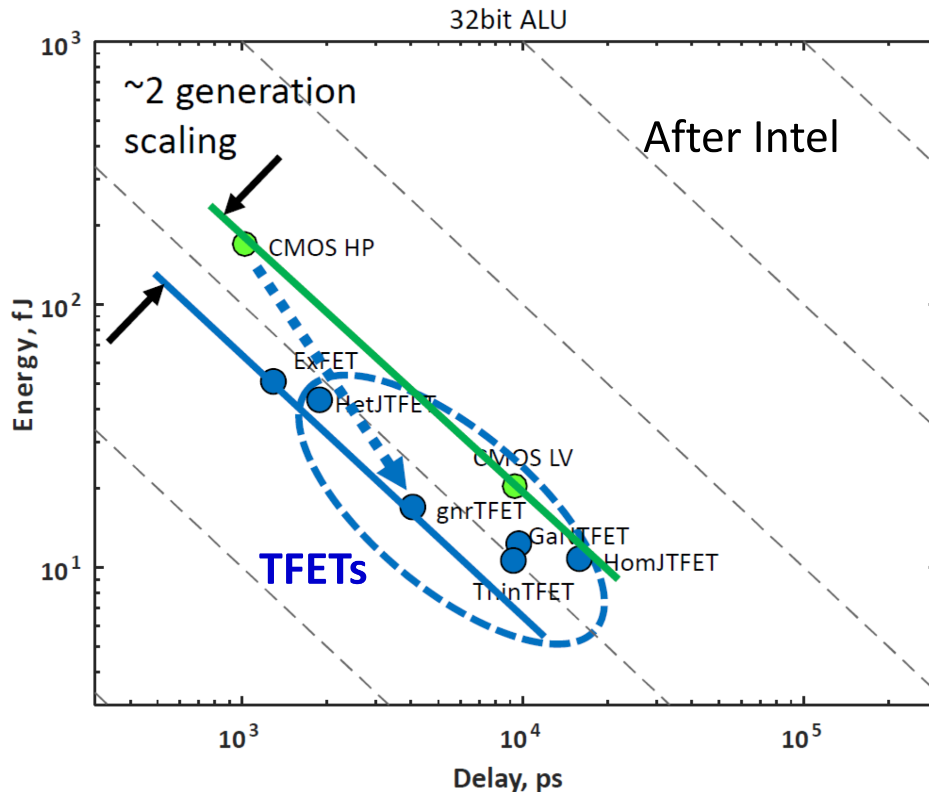
Defects in Heterogenous InGaAs/GaAsSb Diodes





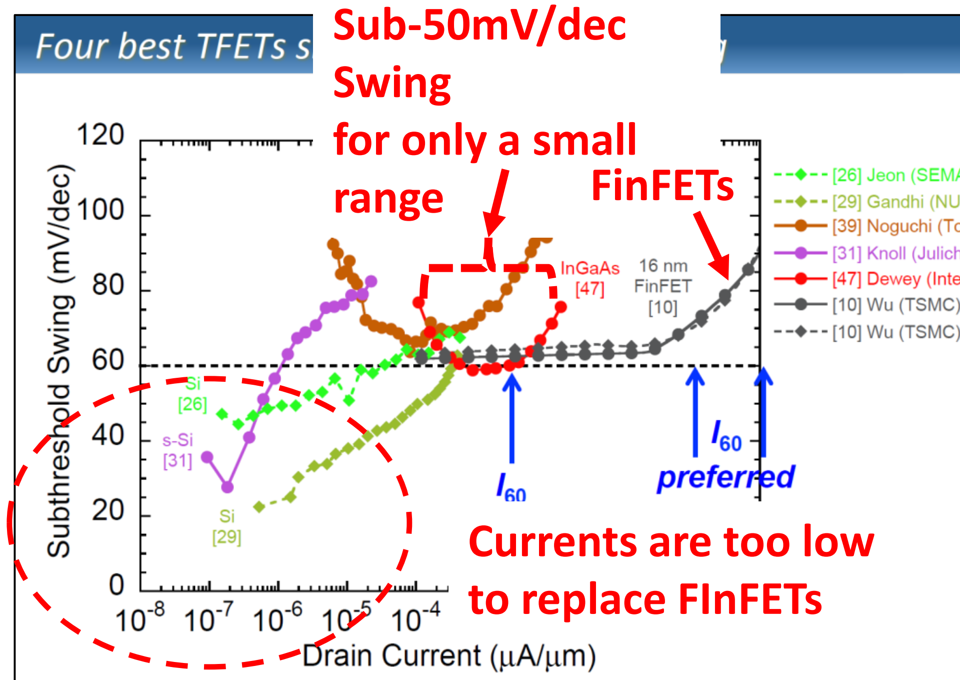
~200 K ; Temperature Independent Peak => Tunneling

The Promise & Challenges of TFETs



Bill Holt, Retired EVP Intel @ ISSCC 2016

Sources: ITRS 2011, Nikonov and Young, IEEE JxCDC, 1, 3-11 (2015); Manipatruni, Nikonov and Young, Arxiv cond-mat 1512.05428 (2015)



A. Seabaug, Tunnel FETs: The promise and the reality, 2014 ESSDERC/ESSCIRC Workshop

So far, TFETs key advantages for very low voltage – Difficult to drive any load – May need a system/circuit solution – TFET-MOSFET hybrid?

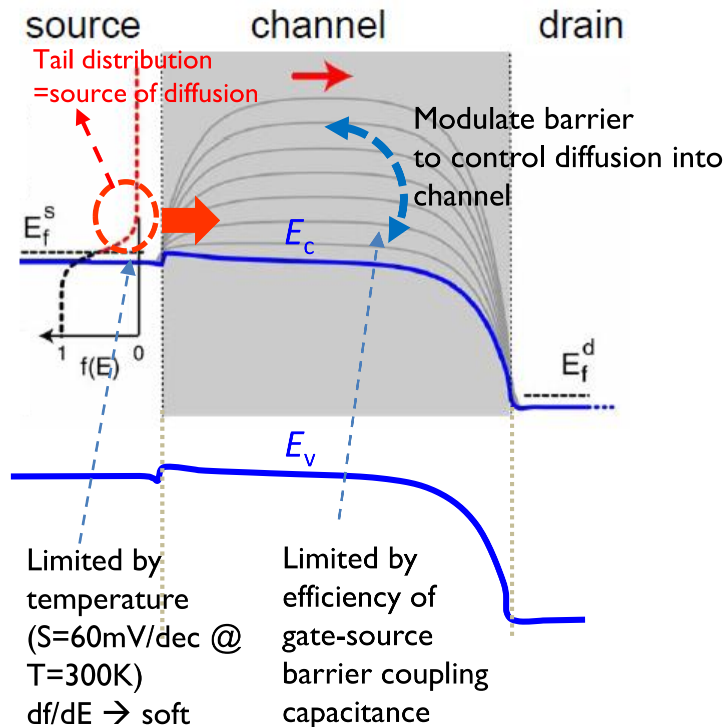
Negative-Capacitance Gate FET

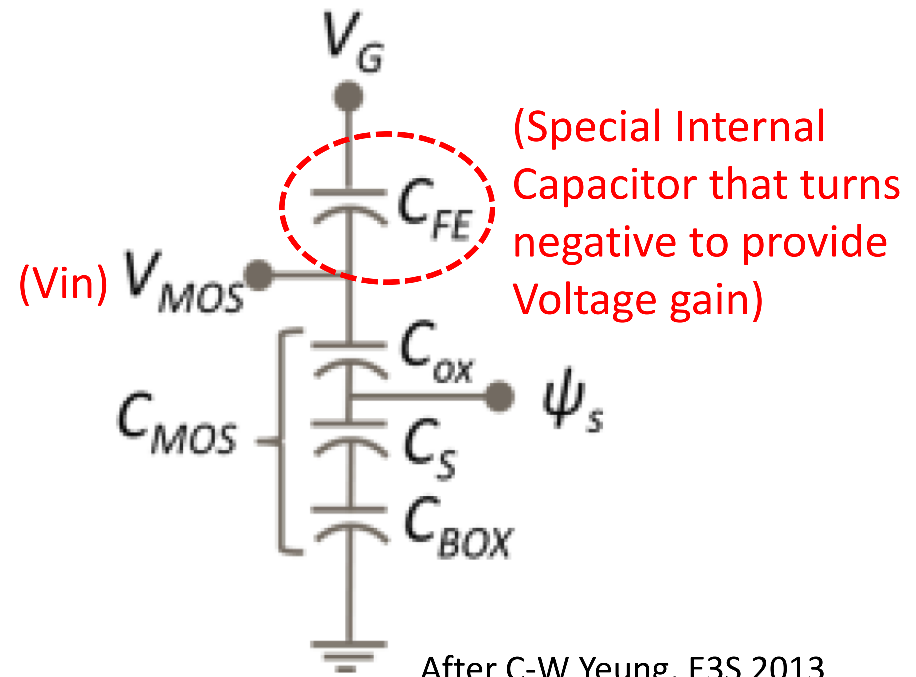
MOSFET or TFET gate-channel coupling

Subthreshold swing $S = \frac{\partial V_G}{\partial log_{10}(I_D)} = \left(\frac{\partial V_G}{\partial V_{in}}\right)\left(\frac{\partial V_{in}}{\partial log_{10}(I_D)}\right)$

Introduce positive gain

MOSFET

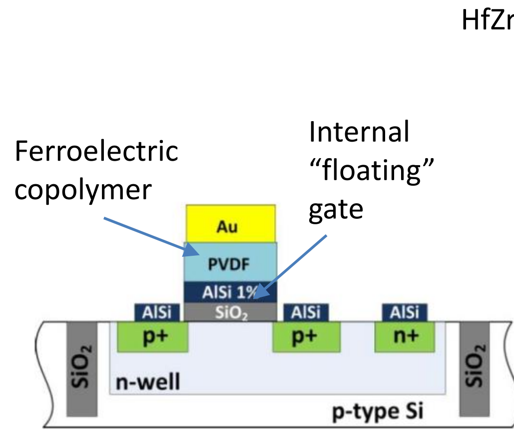


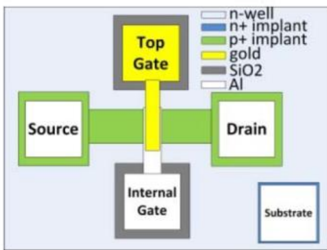


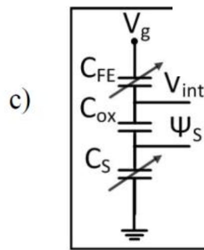
- Building in internal voltage gain (“voltage amplification”) in the gate capacitor

Some device structures

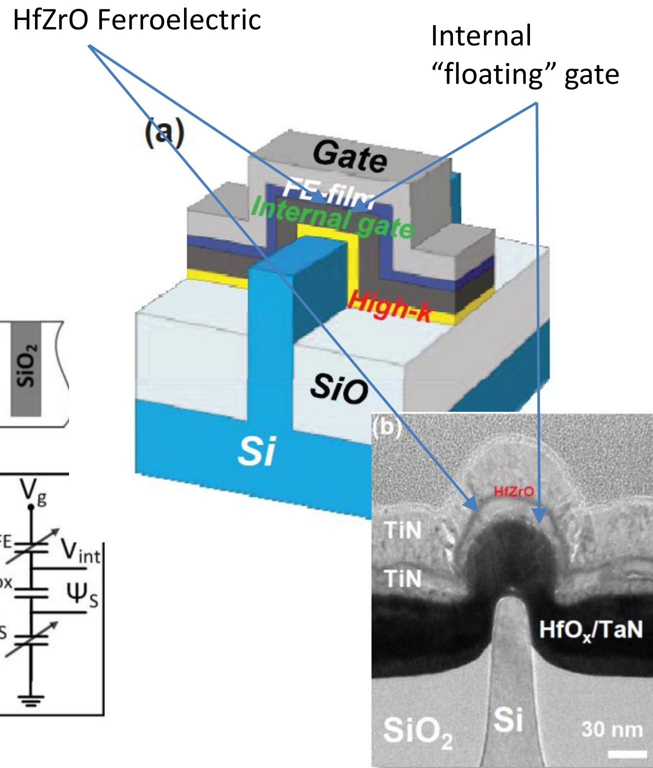
"Dielectric -on-Dielectric"
No internal gate



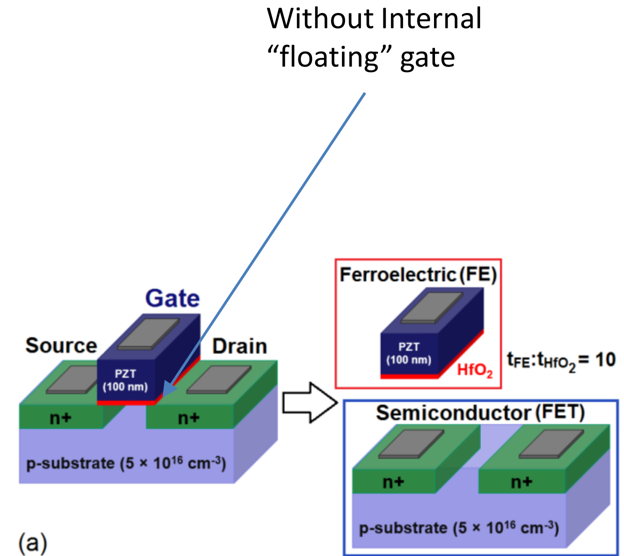




A. Rusu et al. *IEDM 2010* pp. 16.3.1–16.3.4. (Adrian Ionescu EPFL)



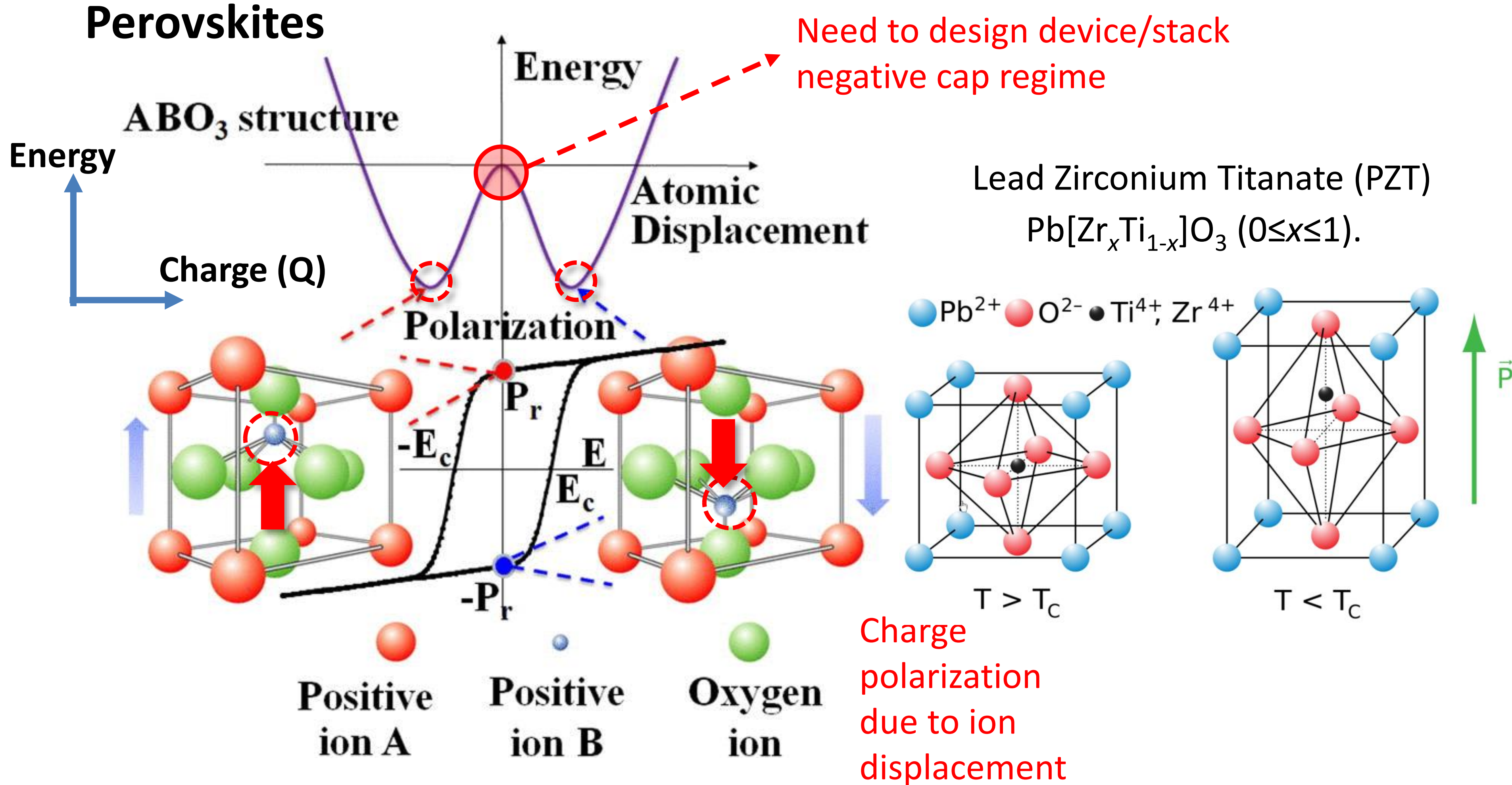
Li et al. *IEDM 2015* pp. 22.6.1–22.6.4. (C.Hu & S. Salahudin Berkeley)



S. Dasgupta et. al. EEE Journal on Exploratory Solid-State Computational Devices and Circuits
Year: 2015, Volume: 1
Pages: 43 – 48 (S. Datta Penn State)

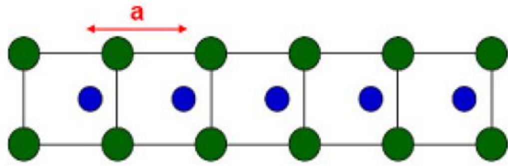
- Essentially a Ferroelectric Capacitor in series with metal-gate capacitor
- Internal gate introduced to (a) probe internal Fe-Cap (b) Equipotential interface to mitigate depolarization from transistor channel/SD regions, to achieve uniform field despite FE domain formation? Floating voltage node sensitive to leakage.
- No internal gate: Sensitive to FE-gate-Oxide trap density

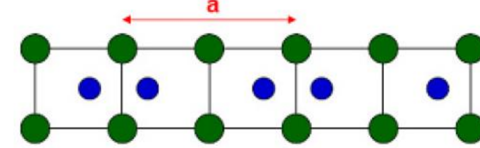
Negative Capacitance by Ferroelectrics



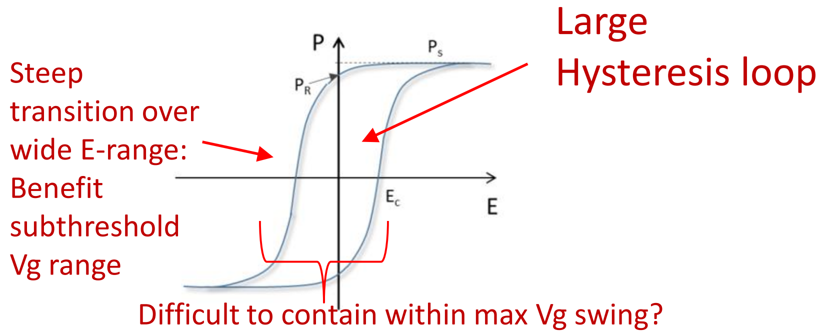
- Ferroelectric states determined by field-induced ion displacement
- Negative capacitance state is between stable ferroelectric states
- Needs special material & operation design to stabilize

Engineering the Hysteresis





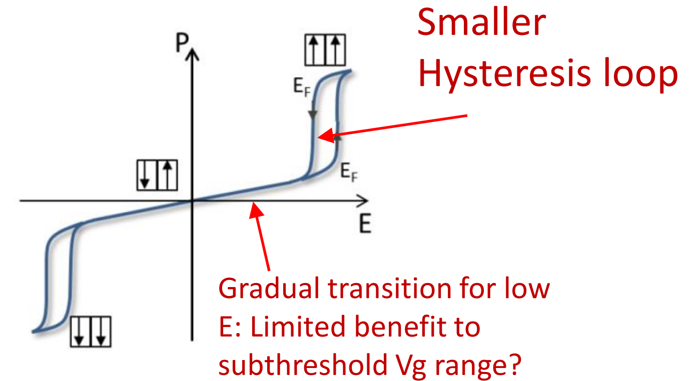
Ferro & Anti-Ferro
FE Thickness dependent



Steep transition over wide E-range: Benefit subthreshold Vg range

Large Hysteresis loop

Difficult to contain within max Vg swing?

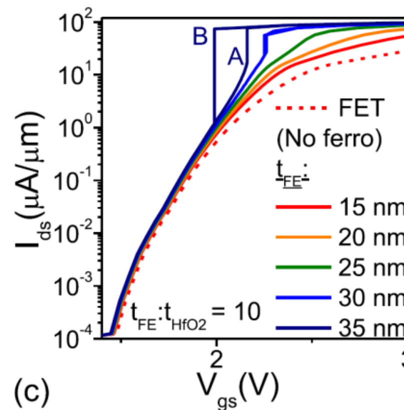


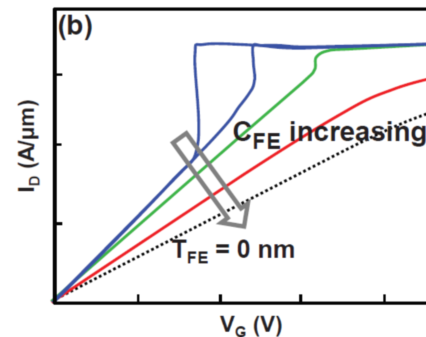
Smaller Hysteresis loop

Gradual transition for low E: Limited benefit to subthreshold Vg range?

Modeling:

Hence FE thickness dependence of hysteresis





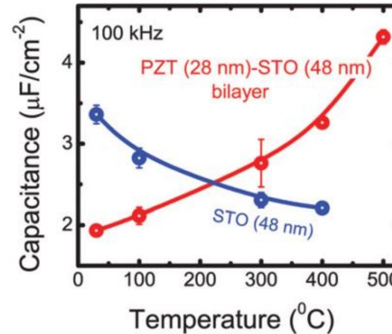
(Left) S. Dasgupta et. al. EEE Journal on Exploratory Solid-State Computational Devices and Circuits
Year: 2015, Volume: 1
Pages: 43 – 48 (S. Datta Penn State)
(Right) C. Hu et. al. in Device Research Conference (DRC), pp. 39-40, 2015.

- Unclear as to the practical trade-off available between minimizing hysteresis while improving SS significantly

Key factors for Logic Ferroelectric gate stack

1. **Quality of FE material & Deposition/Integration process?** – Crystalline Vs. Polycrystalline

2. **Temperature dependence**

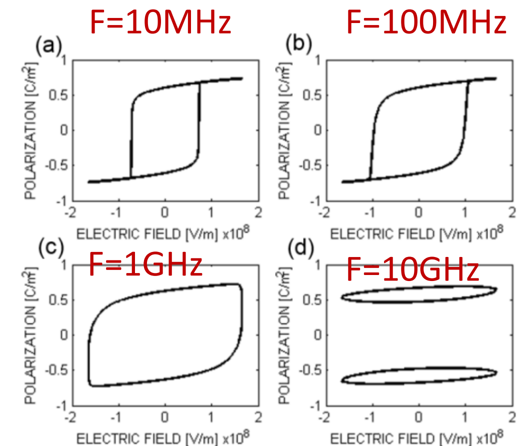


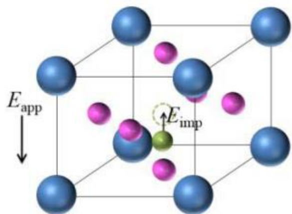
Asif Islam Khan, et. al.
Appl. Phys. Lett. 99, 113501 (2011);

3. **Switching speed limitation?**
   - Fmax ~ 10-20GHz?
   - limited by intermolecular forces of FE
   - Need new FE or Novel system solution

Simulations

Zhi Cheng Yuan; et. al. IEEE Transactions on Electron Devices Year: 2016, Volume: 63, Issue: 10 Pages: 4046 - 4052



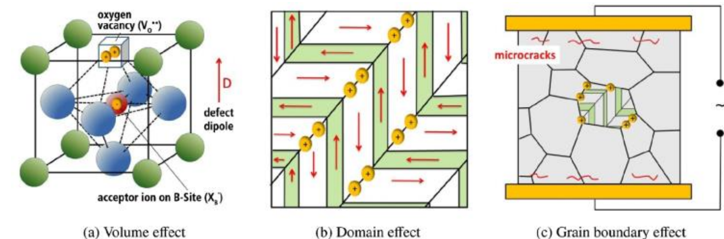


A
B
O

Damping force to impede polarization switching

Yang Li; et. al. IEEE TED
Year: 2016, Volume: 63, Issue: 9
Pages: 3636 – 3641 (NUS)

4. **Endurance of FE gate?**



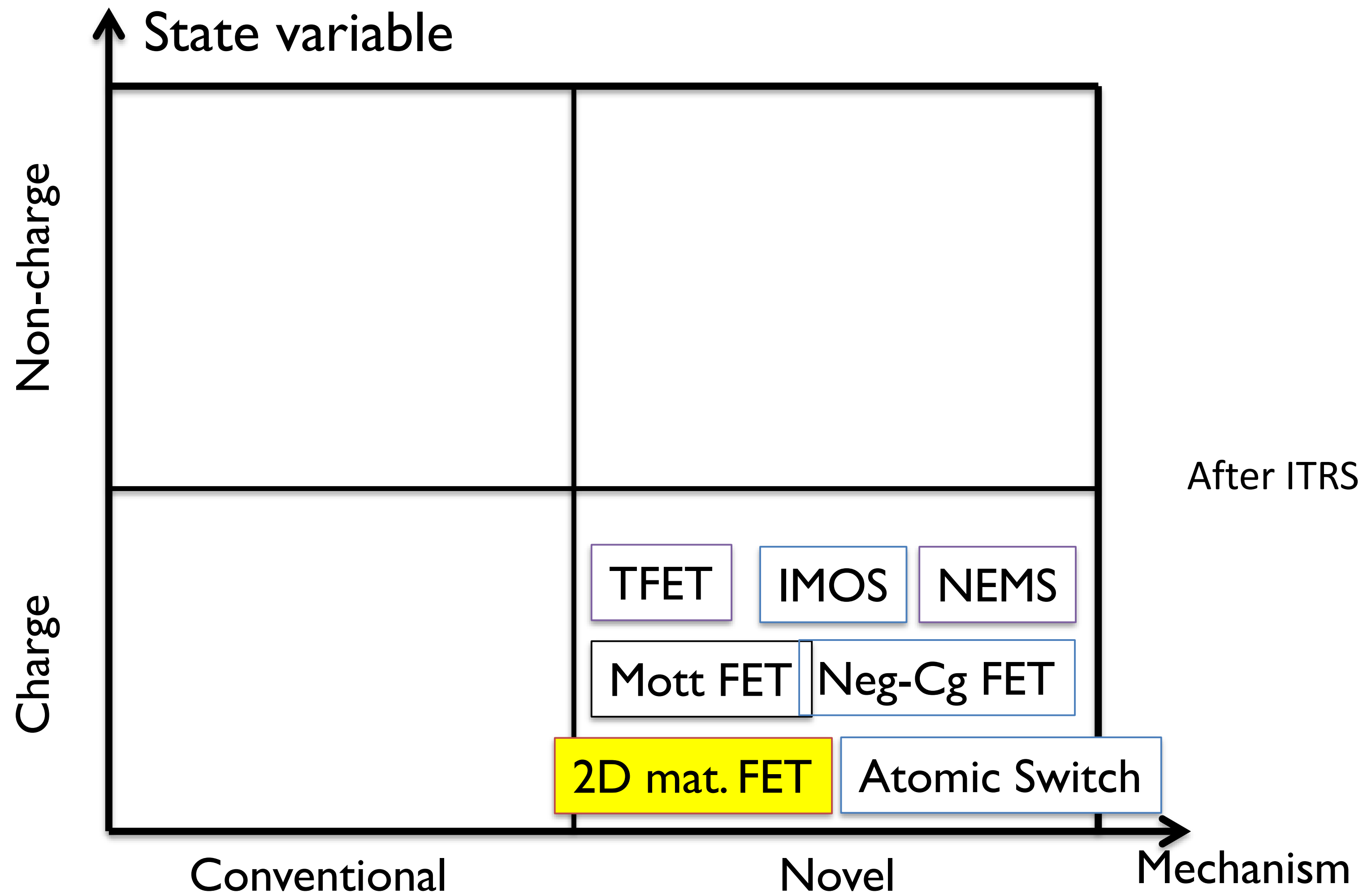
(a) Volume effect (b) Domain effect (c) Grain boundary effect

Volume effect: defect dipoles due to vacancies. Domain effect: Defect diffusion to domain walls due to energy minimization. Grain boundary effect: ions, vacancy diffusion to grain boundaries. Genenkoa, at. al. Material Sciences & Engineering: B vol 192, Feb 2015, pp 52-82.

Emerging Material Systems

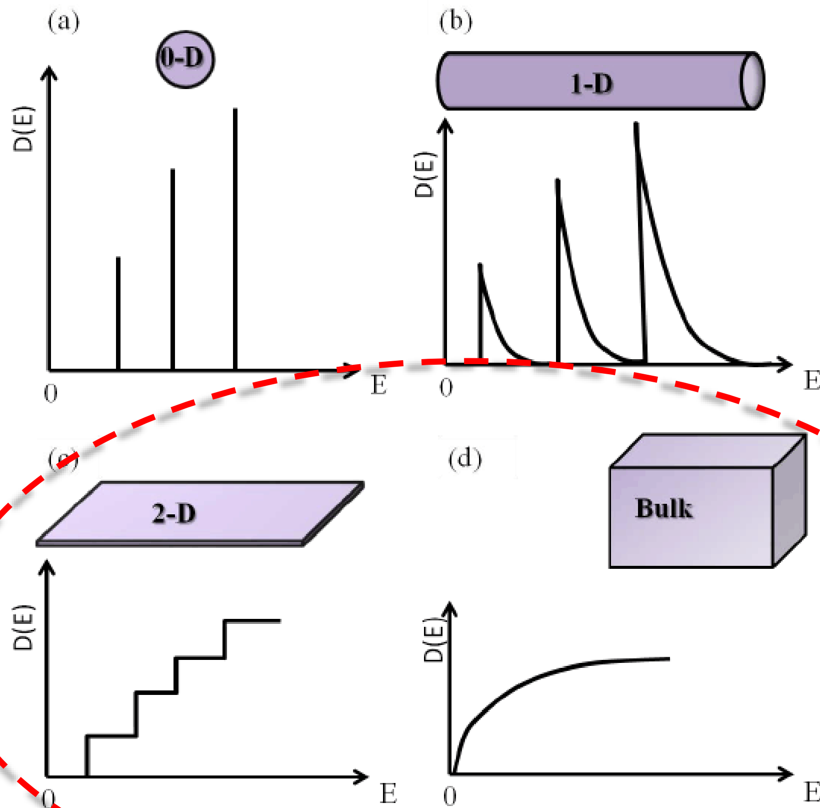
Beyond CMOS

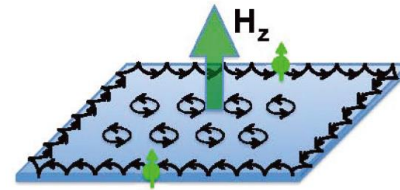
Established Vs. Exploratory: Many Research Device Options



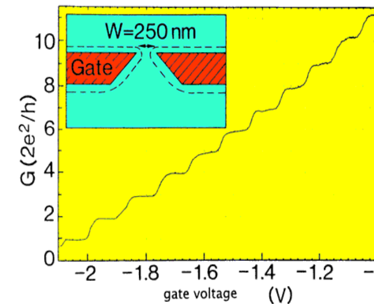
- Novel Device Architectures being explored: Charge Vs. Non-Charge based.

Low-Dimensional Structures – **Interesting Solid-State Physics**

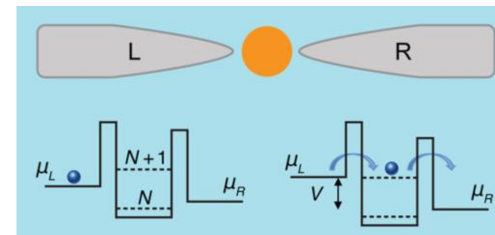




(b) Quantum Hall effect

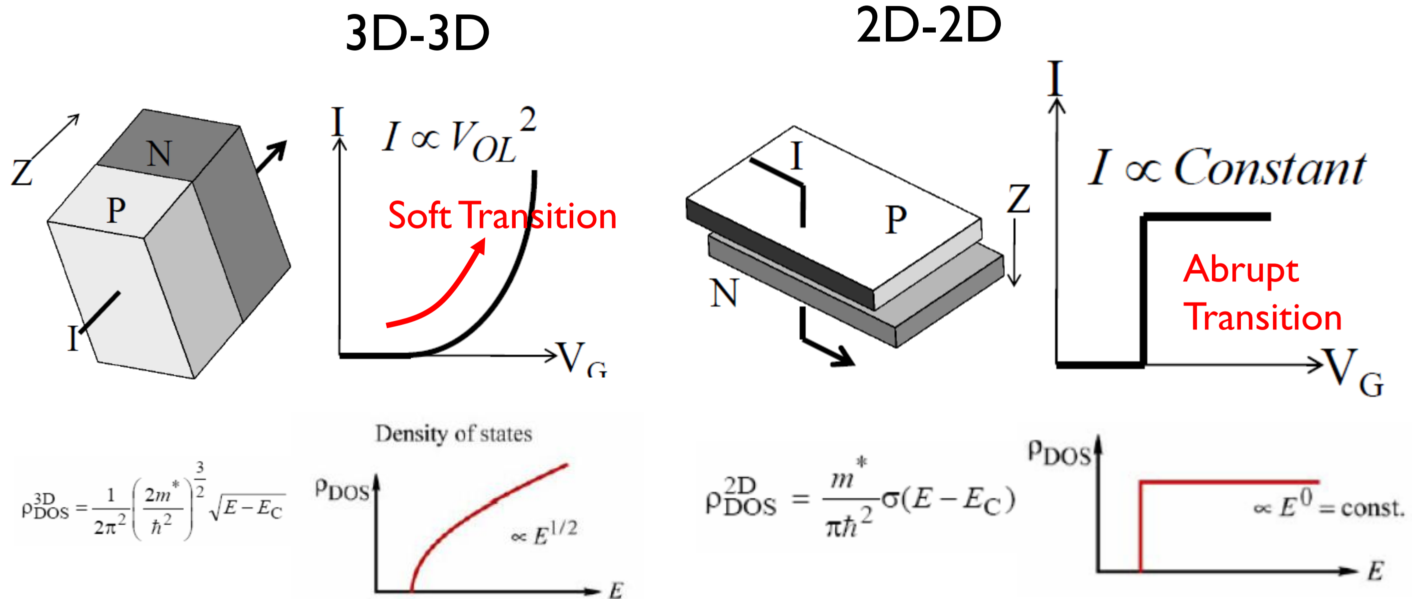


Quantum Point Contact



Coulomb Blockage in Quantum Dots

Beyond 3-D TFETs: Density of States Engineering

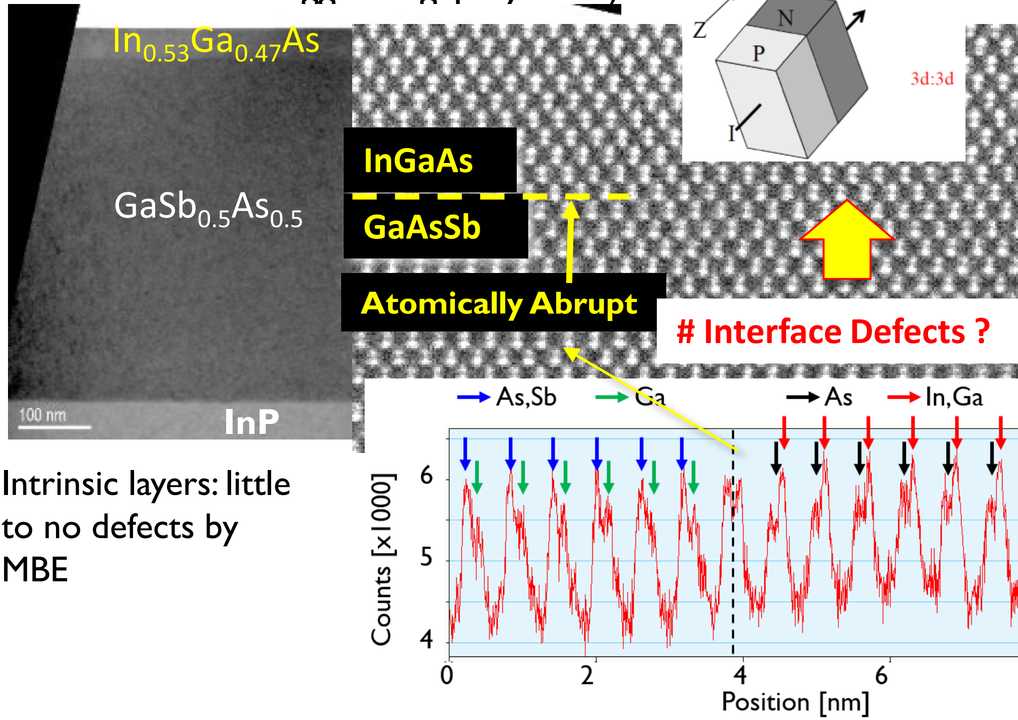


After Eli Yablonovitch 2012, UC Berkeley

- Steepness of swing over wide-Vg range limited by 3-D DOS
- Investigate 2-D TFET options

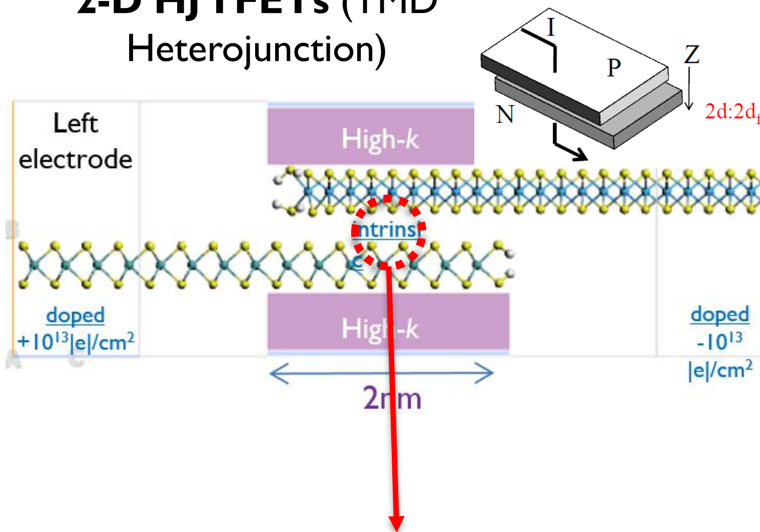
Heterojunction (HJ) TFETs with New Material Systems

3-D HJ TFETs (Lattice-Matched InGaAs-GaAsSb staggered gap by MBE)



Intrinsic layers: little to no defects by MBE

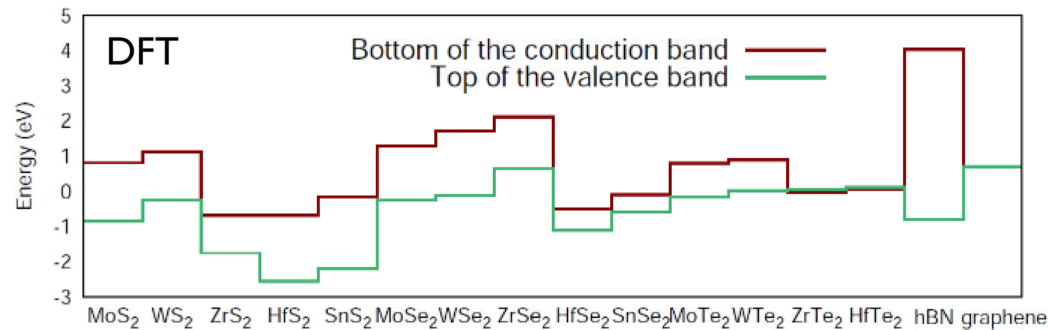
2-D HJ TFETs (TMD Heterojunction)



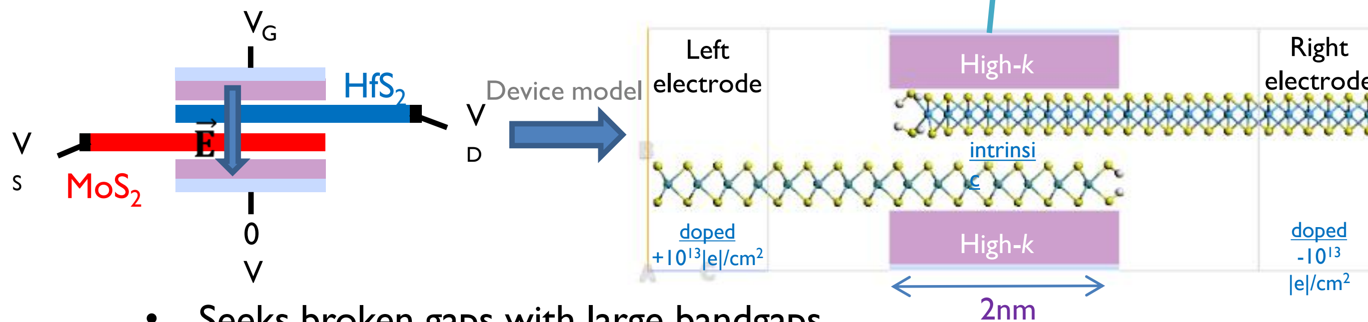
No physical bonds (Van der Waals) = Reduced defects ?

- Important to investigate heterojunction defect limiter to TFET operations
- 3-D heterojunction to 2-D VdW heterojunction transition may offer unique advantages

2-D TFETS with 2-D MX_2 (TMD) heterostructures ?



- **Evaluating** the impact of the gate on the drive current I_d in **MoS_2|HfS_2**
  - How will the charge transfer impact on the I-V curves?
  - Coupling NEGF and DFT (ballistic transport)



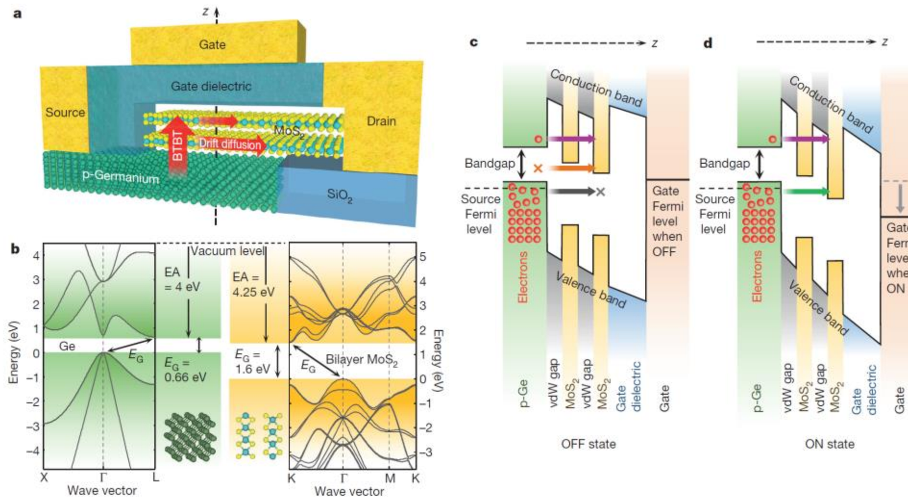
- Seeks broken gaps with large bandgaps
- Lattice mismatch is no longer an issue vDW stacking

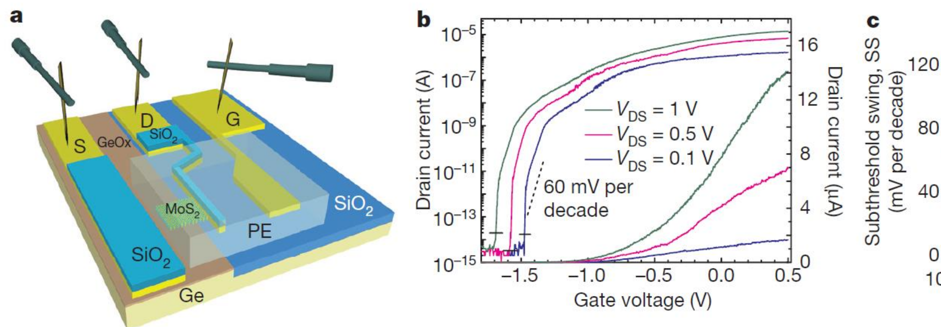
A subthermionic tunnel field-effect transistor with an atomically thin channel

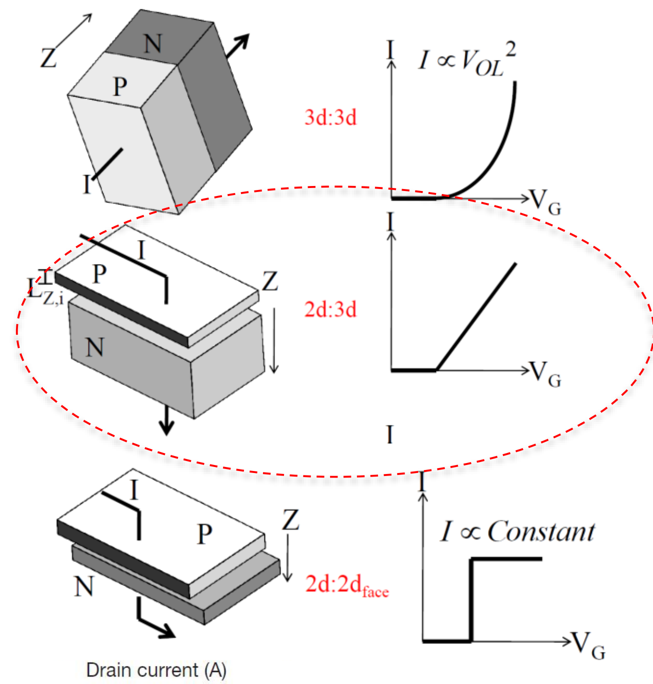
Deblina Sarkar[1], Xuejun Xie[1], Wei Liu[1], Wei Cao[1], Jiahao Kang[1], Yongji Gong[2], Stephan Kraemer[3], Pulickel M. Ajayan[2] & Kaustav Banerjee[1]

UCSB

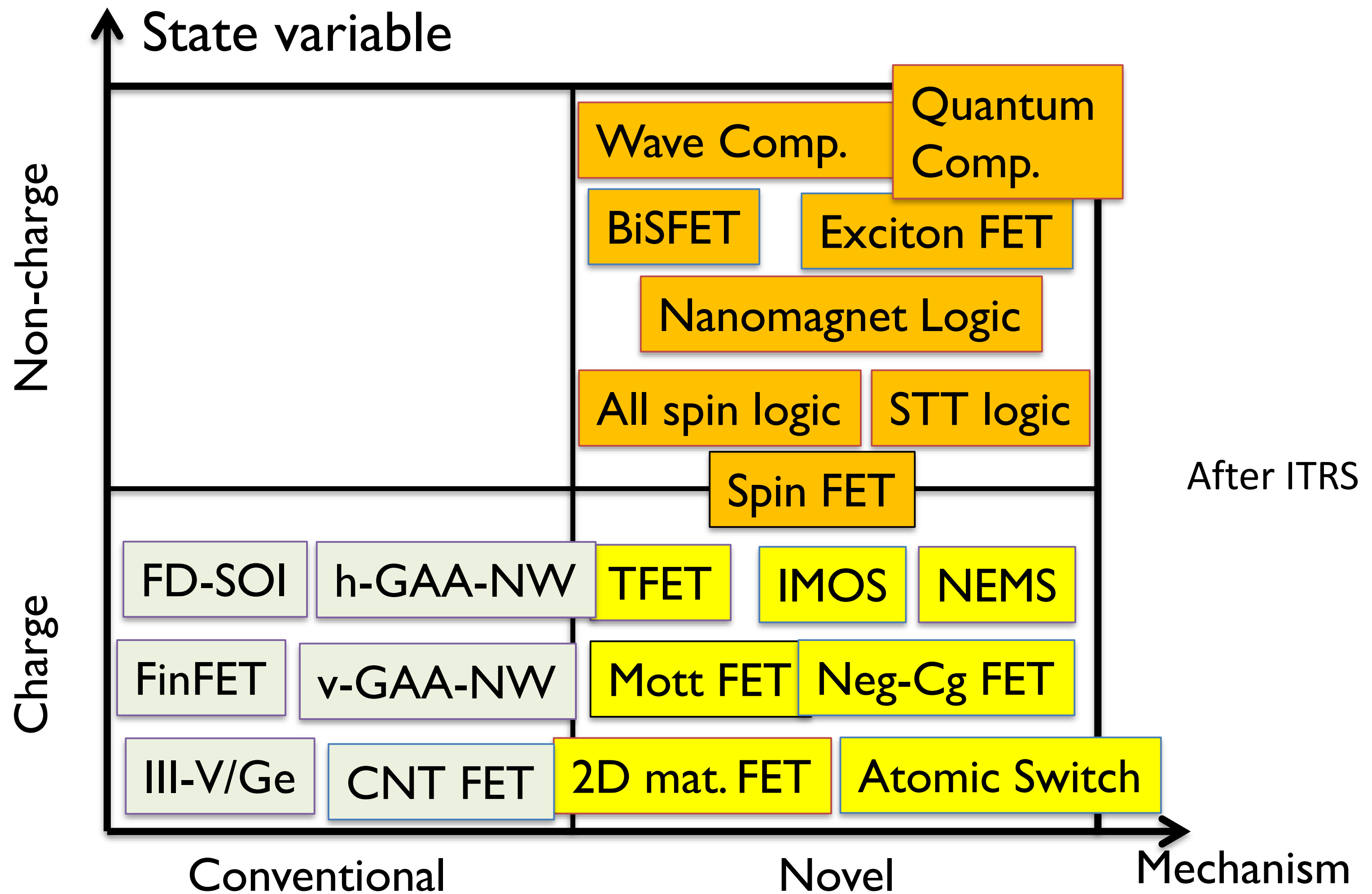
Nature 526, 91–95 (01 October 2015)





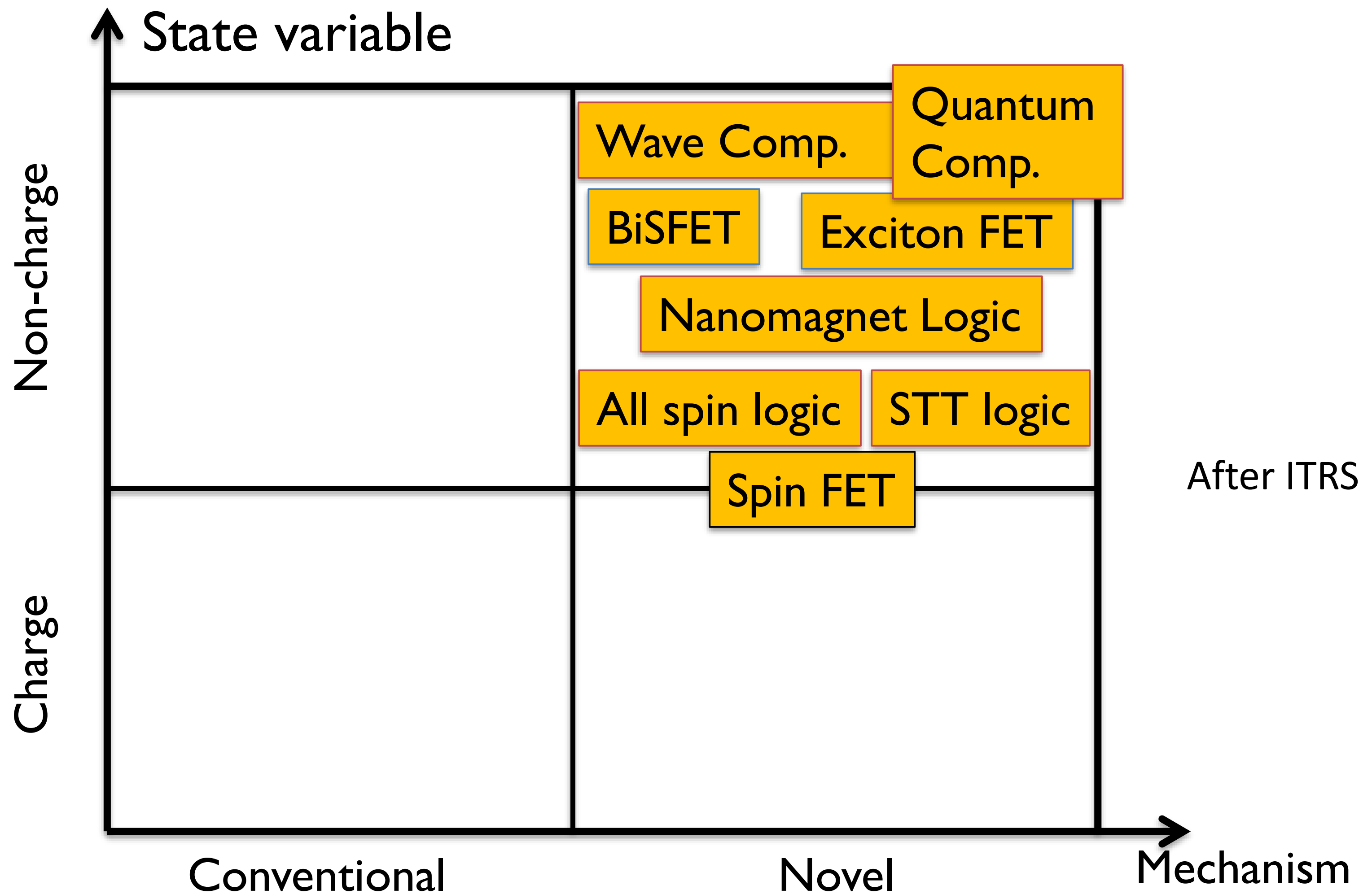


Established Vs. Exploratory: Many Research Device Options



- Novel Device Architectures being explored: Charge Vs. Non-Charge based.

Established Vs. Exploratory: Many Research Device Options



- Novel Device Architectures being explored: Charge Vs. Non-Charge based.

New devices that requires new computation system

32bit ALU

~2 generation scaling

After Intel

Energy, fJ: 10^1, 10^2, 10^3

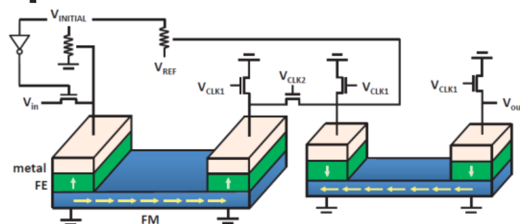
Delay, ps: 10^3, 10^4, 10^5

CMOS HP
ExFET
HetJTFET
CMOS LV
gnrTFET
GaNTFET
HomJTFET
ThinTFET
MESO
FEFET
NCFET
PiezoFET
SWD
SMG

Bill Holt, Intel @ ISSCC 2016

- CMOS ref
- Electronic
- Ferroelectric
- Straintronic
- Spintronic

Chang et. al. (Intel, Ian Young), "Clocked Domain Wall Logic using Magnetoelectric Effects," IEEE Journal on Exploratory Solid-State Computational Devices and Circuits
Year: 2016, Volume: PP, Issue: 99
Pages: 1 - 1

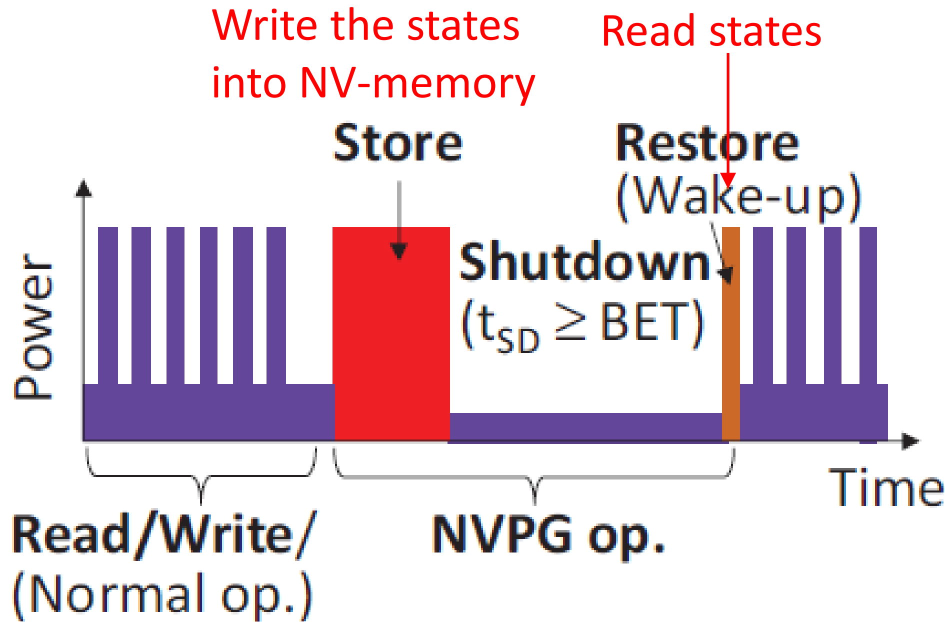


Magneto-Electric Spin-Orbital (MESO)

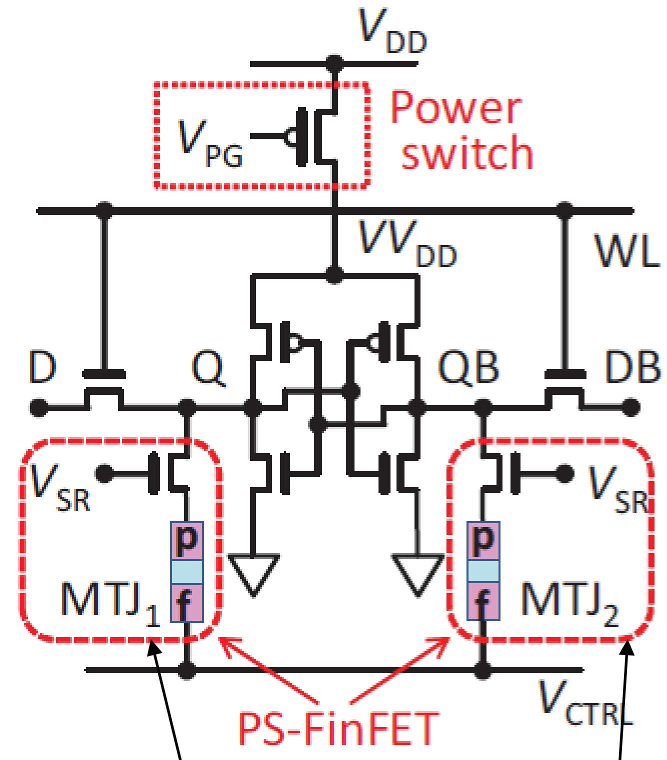
E.g. new material challenges
Like Magneto-electric effects
(Beyond scope of this presentation)

Reduce Memory Access Energy by Nonvolatile Logic

Comparative study of power-gating architectures for nonvolatile FinFET-SRAM using spintronics-based retention technology
Shuto, Yusuke ; Yamamoto, Shuu'ichirou ; Sugahara, Satoshi Design, Automation & Test in Europe Conference & Exhibition (DATE), 2015
Page(s): 866 - 871



Non-Volatile Power Gating (NVPG) -SRAM

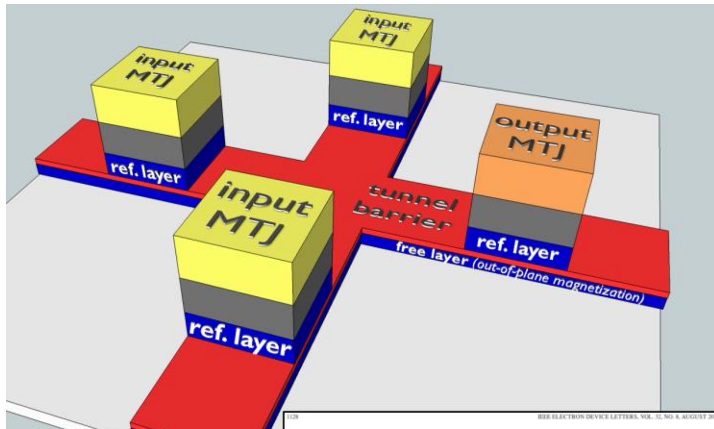


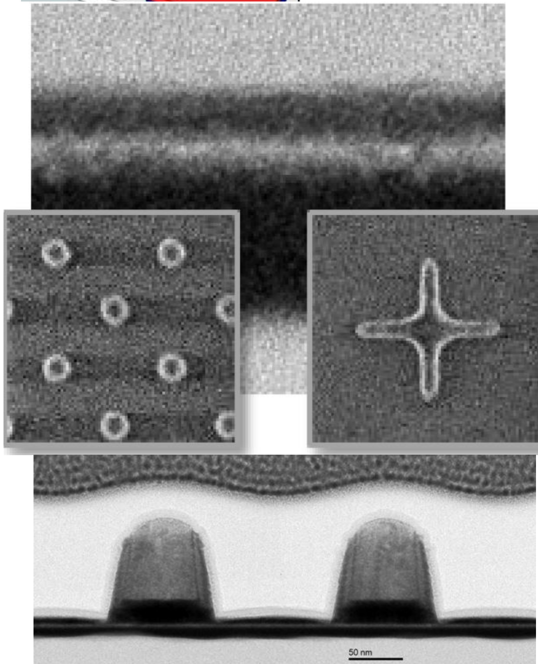
FinFETs with MTJs (NV elements)

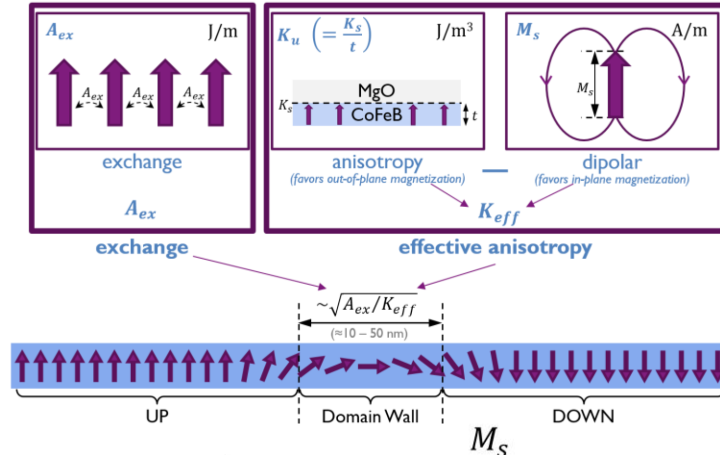
(1) copy the states Q & QB when V_{SR} is activated
(2) Restores Q & QB when SRAM wakes

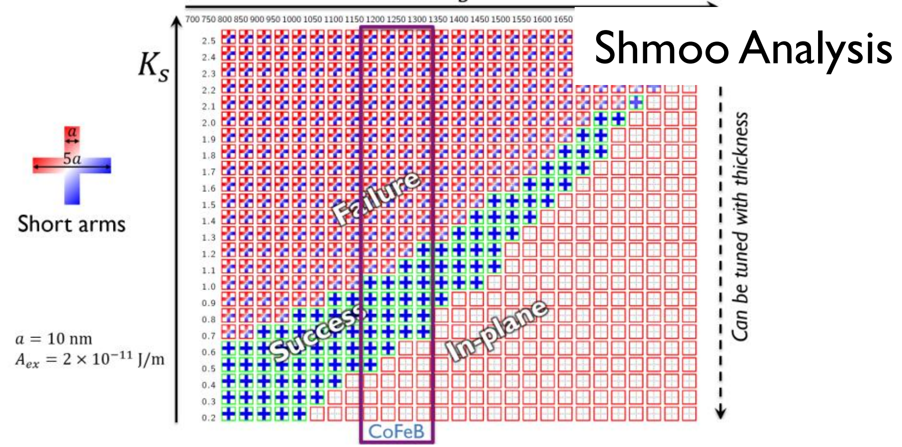
- Energy & time to retain the states by writing to NV memory is a large overhead that increase BET
- Making it only useful for Normally-Off Applications (i.e. long-sleep or long-idle systems)
- Unless we can build in NV elements very local to logic to reduce memory access energy

Spin-torque Majority Gate – More efficient NV Gate









Need dense structures to encourage exchange type DW interactions

Messages

- **Complex Structures** → Towards vertical and "atomically-thin" structures
  → **more surface/interface than volume**
  → Structural & Material Correlated analysis needed

- **Complex Material Systems** & The **rising impact of defects**
  → Their detection, characterization, & quantification become significant
  → Added complexity of nanostructure

- **New Materials Integration** → **Beyond Silicon & exotic Beyond CMOS Materials**
  E.g. Ferroelectrics, Magnetics may make their way into CMOS
  → Need multiple characterization methods integrated to support heterogeneous process integration

- **Metrology and Advanced Characterization critical**
  → **Can't steer if you can't see!**