IR-Drop Based Electromigration Assessment
Materials Data and Characterization Requirements

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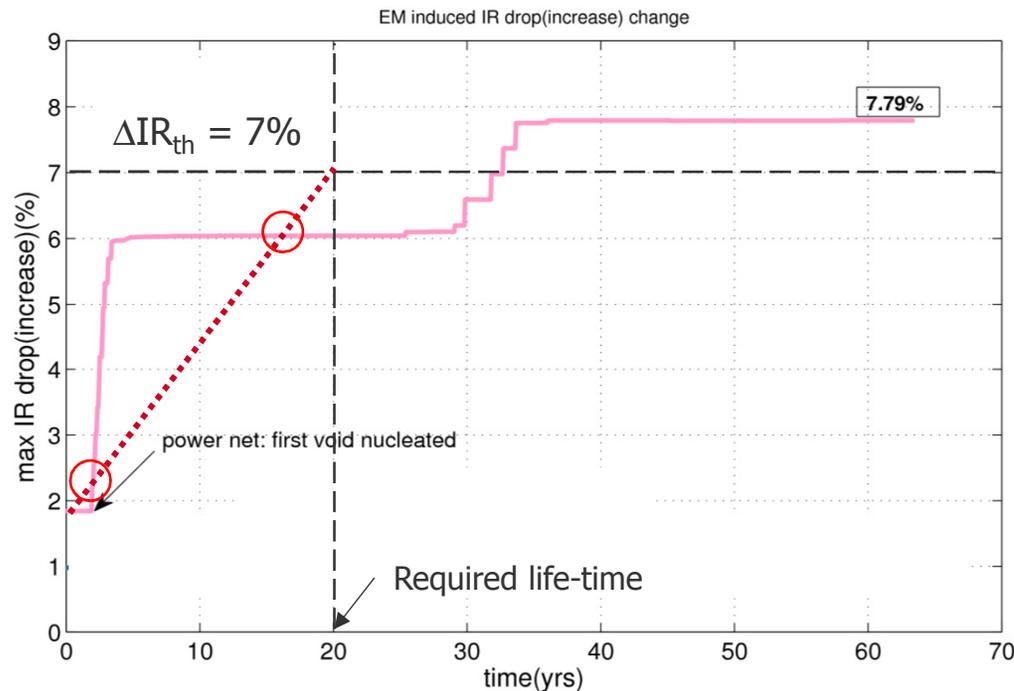
[2]Mentor Graphics, Armenia

[3]UCR, Riverside, CA, USA

Outline

- Introduction and motivations

- Chip design verification for sign-off EM assessment
  - On-chip interconnect elemental unit for EM reliability vs. standard test-structures
  - A role of interconnect redundancy in the resistance degradation
  - Power/ground grid vs. signal nets

- A role of residual stress and temperature in EM-induced degradation

- Methodology of across-interconnect residual stress assessment

- Methodology of across-interconnect temperature assessment

- Voiding-induced IR-drop degradation – parametric failure

- Multi-scale materials data as input for the simulation

- Characterization techniques for models/methodology validation

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Reliability vs. Performance

- Current assessment of chip reliability kills chip performance!

EM induced IR drop(increase) change

$\Delta IR_{th} = 7\%$

7.79%

max IR drop(increase)(%)

power net: first void nucleated

Required life-time

time(yrs)

Question:
How can one predict an IR-drop degradation for a particular chip design?

Answer:
- Accurate physics
- Solid models
- Fast and clever algorithm

- Reduction of the operation frequency or voltage at the instance in time when IR drop degradation (increase) exceeds a projected value is killing the chip performance while not affecting the chip EM reliability.

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Electromigration Basics

- Material depletion and accumulation occurring at the sites of atomic flux divergence results the localized tensile and compressive stresses

- Resulting stress gradient creates a backflow atomic flux

- If the electron-wind and back-stress forces balance each other before the critical stresses needed for void nucleation or metal extrusion are developed the interconnect segment will be immortal.
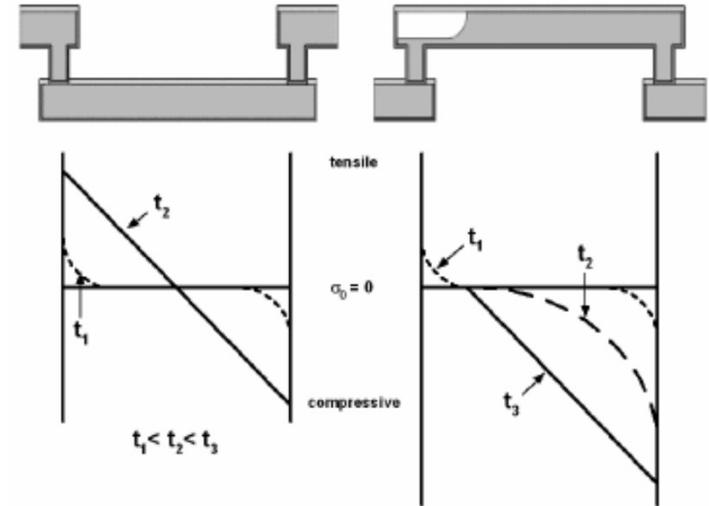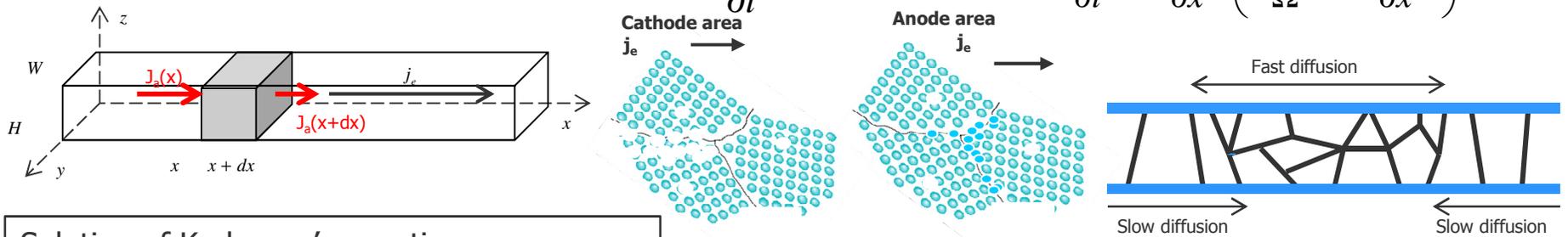

DC
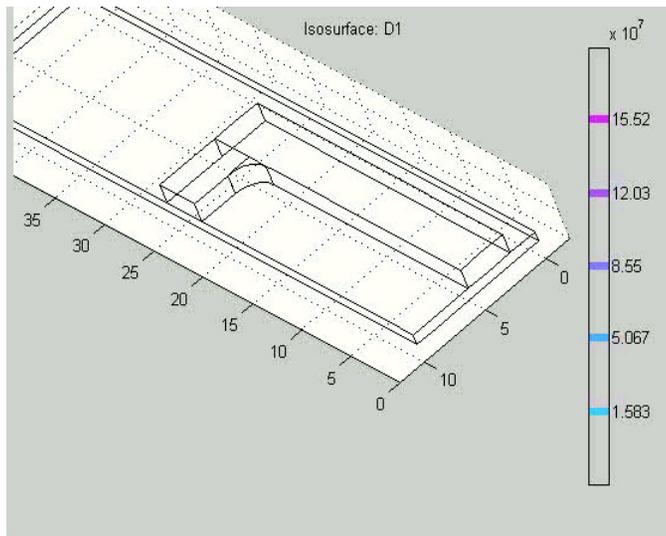
AC
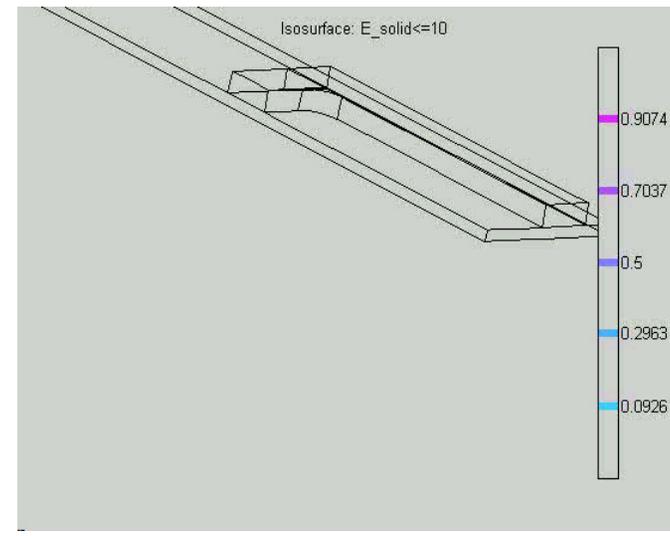
General Physical Model

If atom an flux divergences somewhere inside metal line then accumulation or depletion of atoms is happening there:

$$\frac{\partial N_A}{\partial t} + \vec{\nabla}\vec{J}_A = 0 \implies \frac{\partial \sigma_{Hyd}}{\partial t} = \frac{\partial}{\partial x}\kappa\left(\frac{eZ\rho j}{\Omega} + \frac{\partial \sigma_{Hyd}}{\partial x}\right)$$

Cathode area j_e **Anode area** j_e Fast diffusion

Slow diffusion   Slow diffusion

Solution of Korhonen's equation:
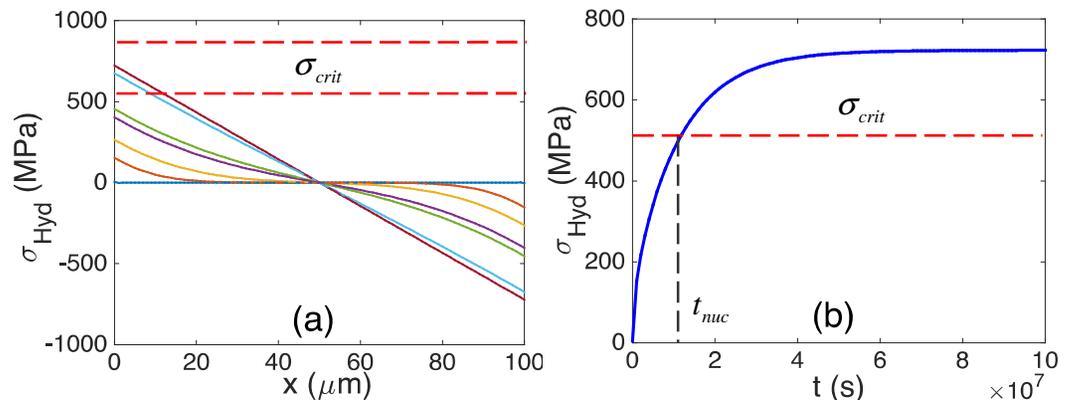
$$\sigma(x,t) = \sigma_{res} - \frac{eZ\rho j}{\Omega}\left(x + 4L\sum_{n=0}^{\infty}\frac{\cos(m_n(1/2 + x/L))}{m_n^2 \exp(m_n^2 \kappa t/L^2)}\right)$$

Condition for the stable void formation:

$$\sigma_{crit} = \sigma_{res} - \frac{eZ\rho j}{\Omega}\left(x + 4L\sum_{n=0}^{\infty}\frac{\cos(m_n(1/2 + x/L))}{m_n^2 \exp(m_n^2 \kappa \cdot t_{nuc}/L^2)}\right)$$

Nucleation time for stable, growing void:

$$t_{nuc} \approx \frac{L^2}{2D_0}\frac{k_B T}{\Omega B}e^{\frac{E_V + E_{VD} - \Omega^*\sigma_T - eZ\rho jL/2}{k_B T}}\ln\left\{\frac{\frac{eZ\rho jL}{2\Omega}}{\sigma_{res} + \frac{eZ\rho jL}{2\Omega} - \sigma_{crit}}\right\}$$
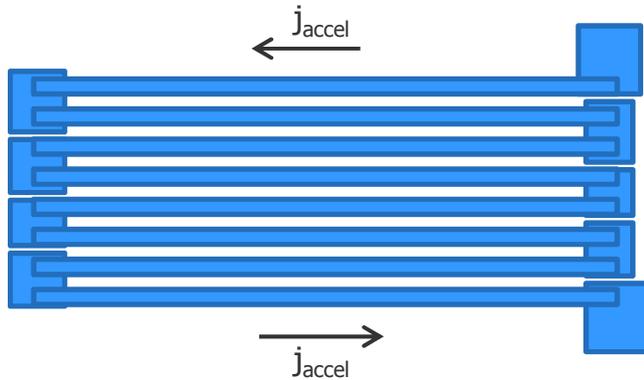
(a)

(b)

Evolution of the hydrostatic stress (a) along the metal line loaded with DC current, and at the cathode end of line, (b) j = 5x10⁹A/m², T = 400K.
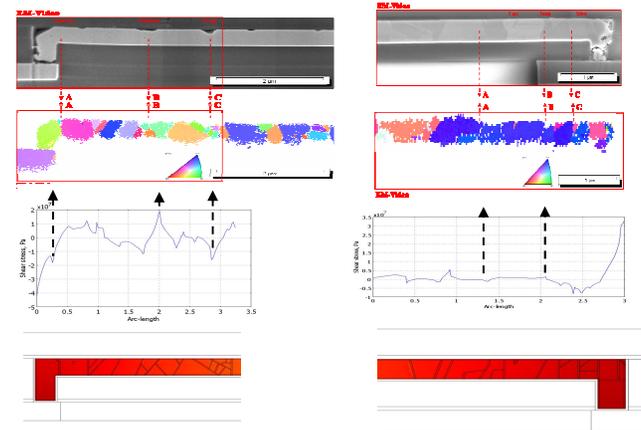
V. Sukharev, "Beyond black's equation: Full-chip Em/Sm assesment in 3D IC stack," *Microelectronic Engineering*, vol. 120, pp. 99–105, May 2014.

Black's equation based MTTF

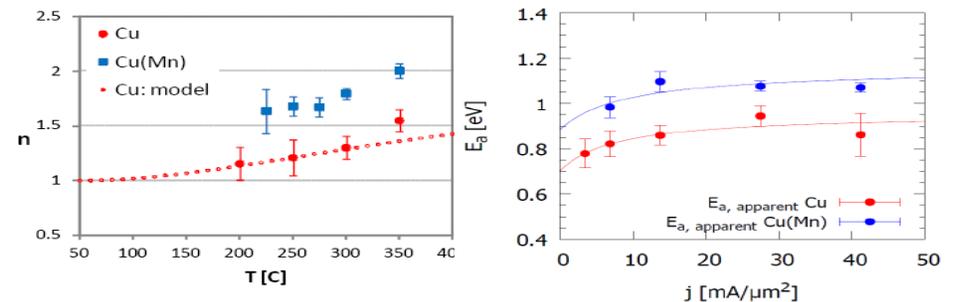EM accelerated test: T_{accel} and j_{accel}

- TTF averaged with the accepted distribution function provides mean time to failure (MTTF).

- A set of calculated MTTF obtained for different T_{accel} and j_{accel} is used for extraction of the current density exponent **n** and apparent activation energy **E** used in the Black's equation:

$$MTTF = \frac{A}{j^n} \exp\left\{\frac{E}{kT}\right\}$$

- Assuming an "universal" character of the extracted **n** and **E**, the MTTF at the used conditions is:

$$MTTF_{use} = MTTF_{accel}\left(j_{accel}/j_{use}\right)^n \exp\left\{\frac{E}{k}\left(\frac{1}{T_{use}} - \frac{1}{T_{accel}}\right)\right\}$$

Different lines characterizing by different microstructures reveal different times to failure (TTF)

Experiments demonstrates that **n** and **E** by themselves are the functions of **j** and **T**


M. Hauschildt, C. Hennesthal, G. Talut, et al. (GF & Fraunhofer), 2C.1.1, IRPS 2013

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EM Assessment – PROBLEM!

- Stress and temperature dependency of the current density exponent,
- Current density and temperature dependency of the activation energy
- Across-interconnect temperature and residual stress variation

ALL THESE FACTORS MAKE **QUESTIONABLE** USING BLACK EQUATION and BLECH LIMIT (CRITICAL PRODUCT) FOR ACCURATE EM ASSESSMENT!
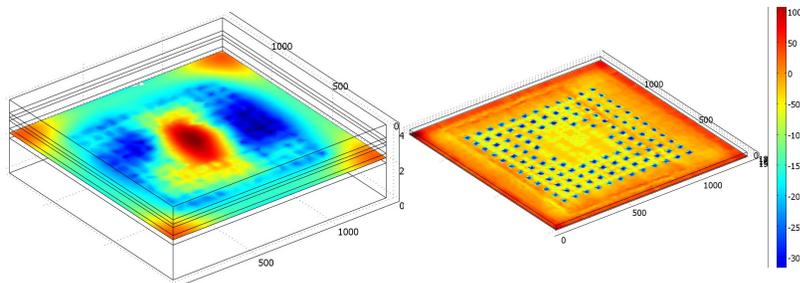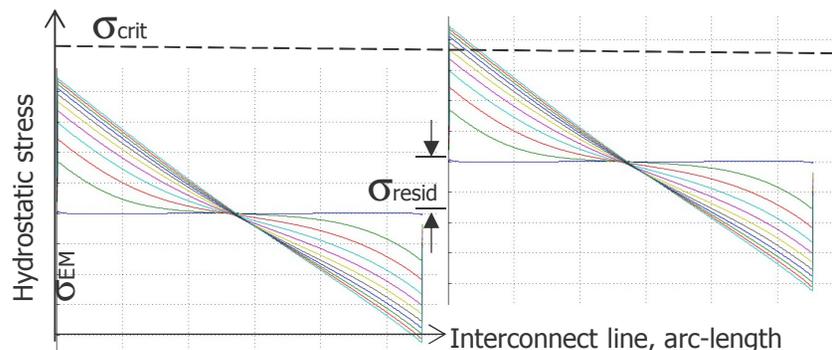
$$t_{nuc} = \frac{A(\vec{r},\sigma_{res})}{j^{n(T,\sigma_{res})}} \exp\left\{\frac{E(j,T)}{kT}\right\}$$

$$(j \times L)_{crit} = \frac{\Omega(\sigma_{EM} \pm \sigma_{res}(\vec{r},T))}{eZ\rho}$$

EM assessment requires:

- Current density assessment
- Temperature assessment
- Residual stress assessment

V. Sukharev and E. Zschech, "Multi-scale simulation flow and multi-scale materials characterization for stress management in 3D through-silicon-via integration technologies – Effect of stress on 3D IC interconnect reliability", AIP Conference Proceedings **1601**, 18 (2014); DOI: 10.1063/1.4881339

Chip-scale EM assessment
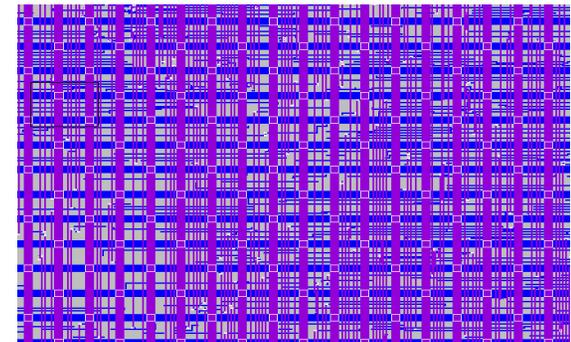
Interconnect functionality

- interconnectivity for signal propagation
  -*bidirectional pulsed currents*
- voltage delivery
  -*unidirectional current*
  - **_power grids, more susceptible to EM effect_**
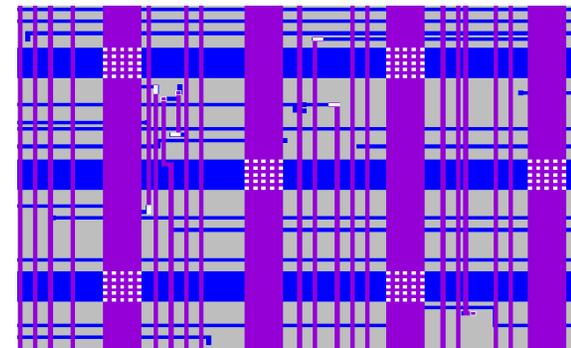
Interconnect tree
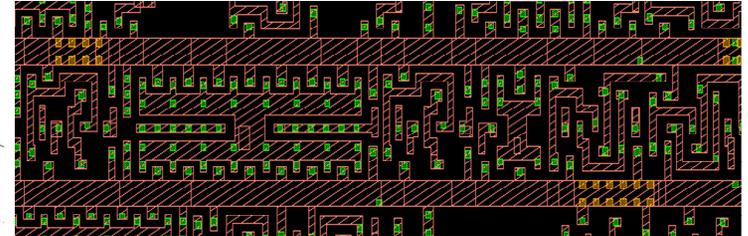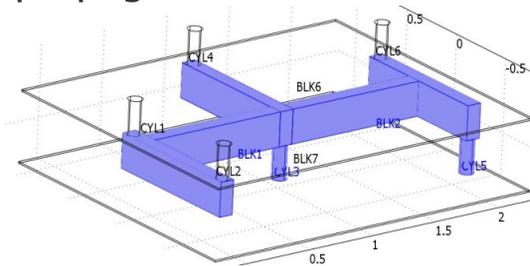
Traditional segment-based EM assessment

- single segment based stress analysis
  - *assume individual segment is confined by diffusion barriers*
  - **_however_**, *in power grids, atoms can diffuse in the interconnect tree, stress redistribution*
- EM induced failure rate of the individual segment

EM induced degradation in power grids

- high level of redundancy
- *Failure*: loss of performance, parametric failure
 - *cannot deliver needed voltage to any point of the circuitry*

New methodology for EM assessment:

- IR drop based assessment
- physics based models for void initiation and evolution

FCDPhysics2010

STRESS ASSESSMENT

IC Problem

- Consumer demand is driving the need for thinned substrates, introduction of new connectivity structures (e.g. 3D stacking, TSVs, C4- and u-bumps) that cause unexpected device performance

artist impression of thin die subject to stress
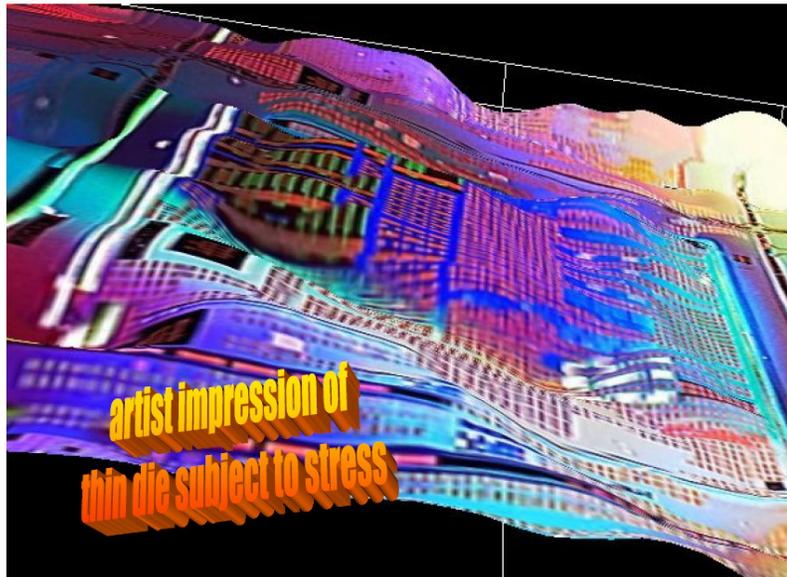
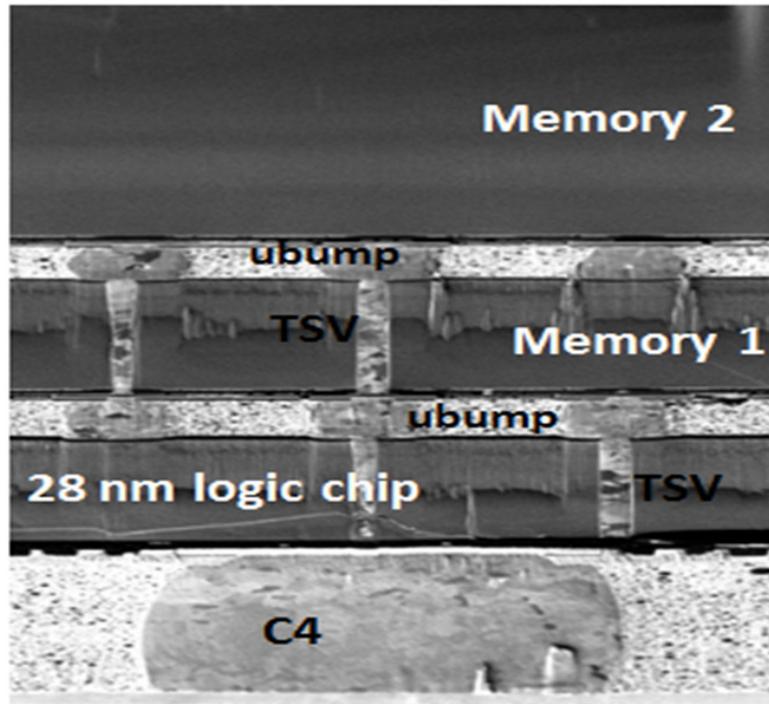You don't want this to happen when stacking a thin die on top of a thick bottom die

How to avoid ?!

How to design for this !

IMEC

- Mechanical stress caused by IC architecture and packaging impacting MOSFET characteristics/performance – **Chip-Package-Interaction (CPI)**
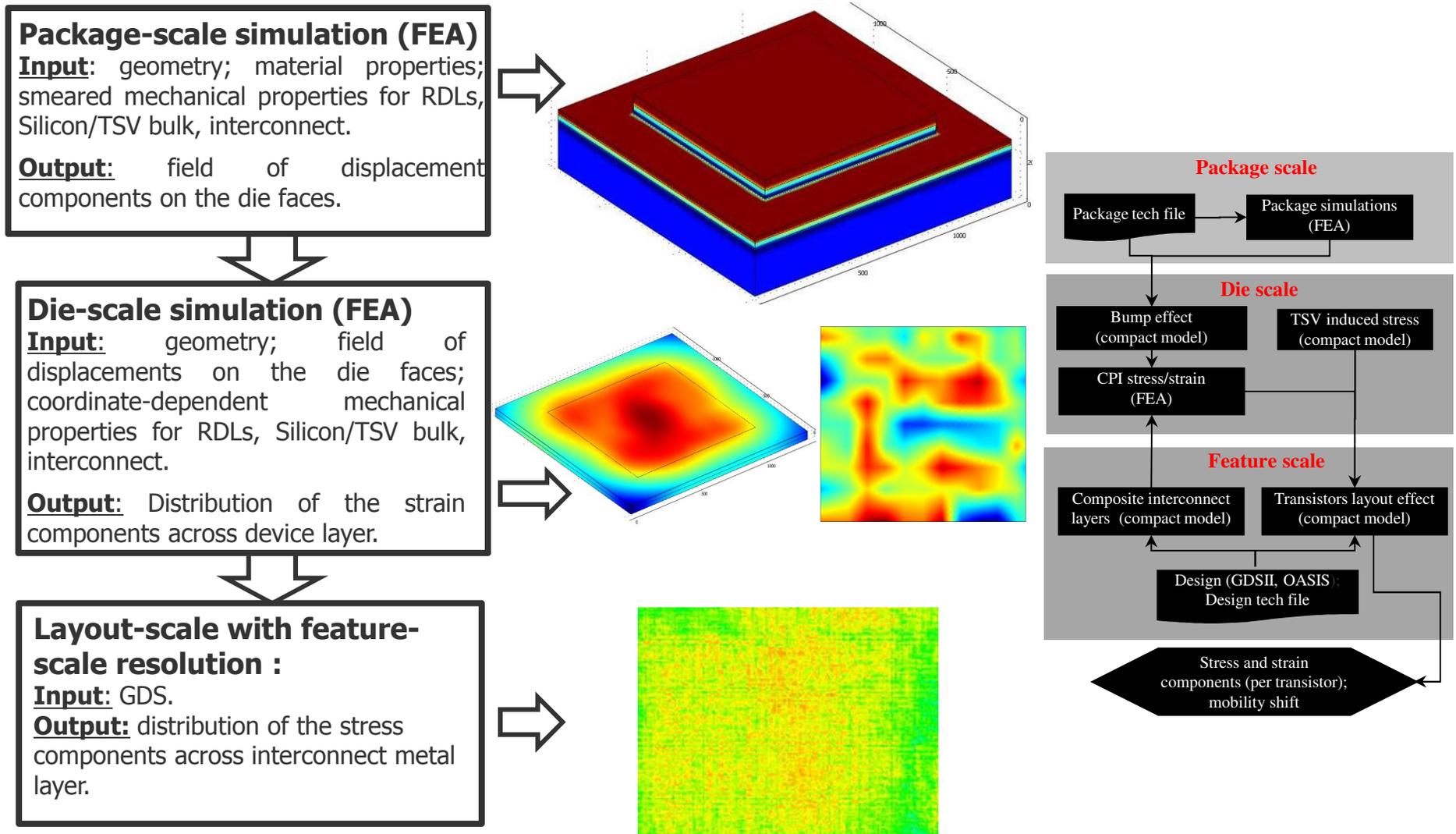
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What is 3D TSS (Through Si Stacking) Technology
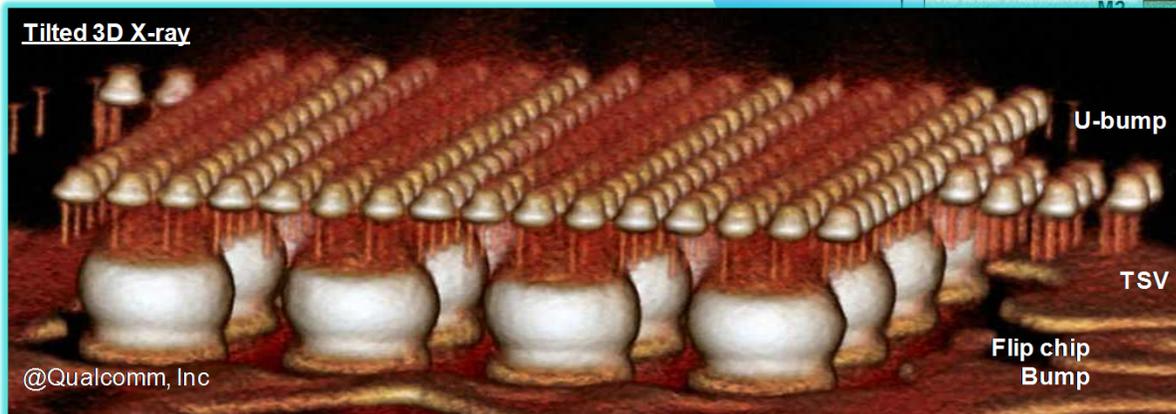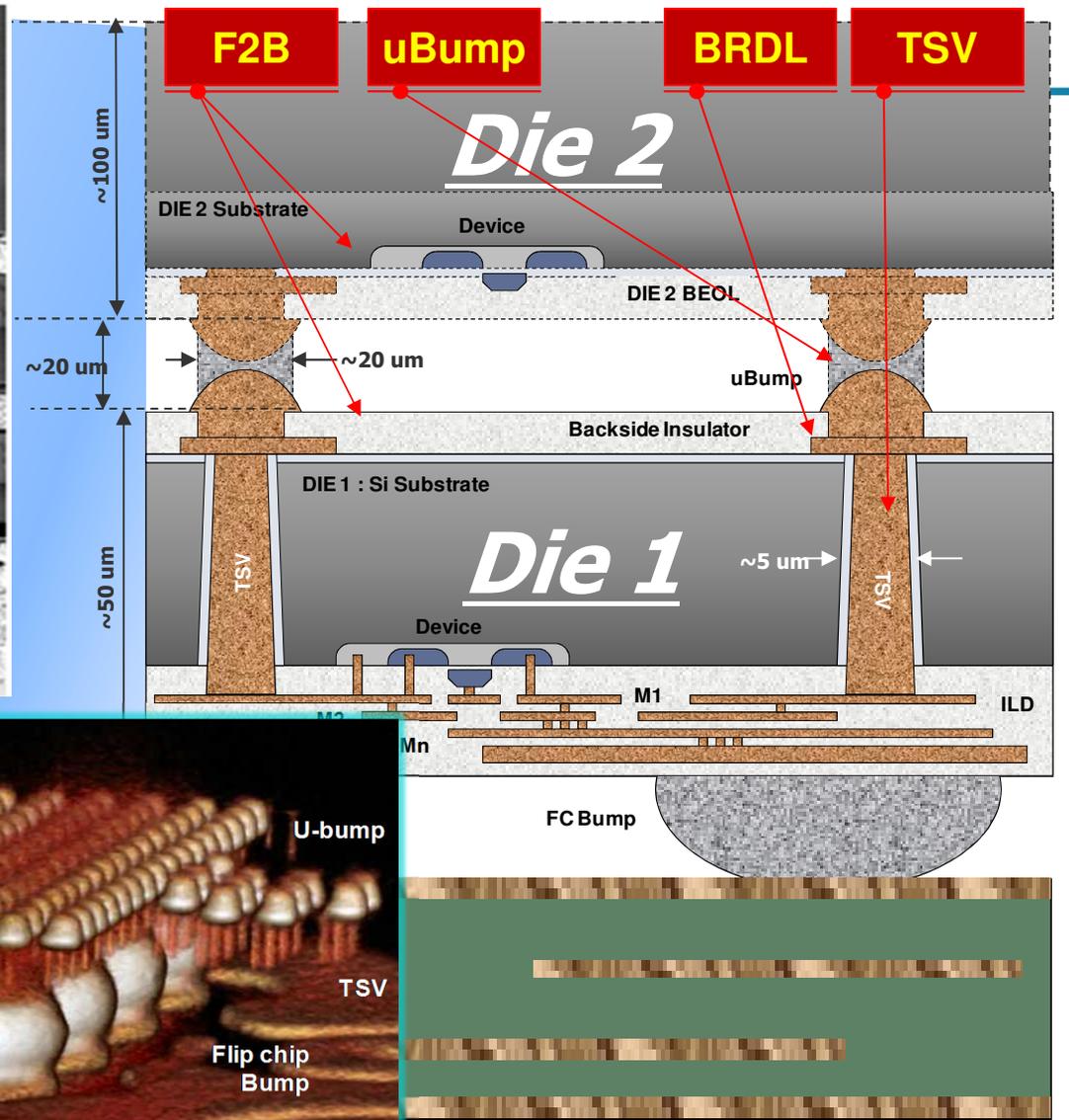
Memory 2

ubump

TSV

Memory 1

ubump

28 nm logic chip

TSV

C4

Tilted 3D X-ray

@Qualcomm, Inc

U-bump

TSV

Flip chip Bump

F2B **uBump** **BRDL** **TSV**

Die 2

~100 um

DIE 2 Substrate

Device

DIE 2 BEOL

~20 um

~20 um

uBump

Backside Insulator

DIE 1 : Si Substrate

~50 um

Die 1

~5 um

TSV

TSV

Device

M1

M2

Mn

ILD

FC Bump

R. Radojcic, E. Zschech, V. Sukharev, "Managing the Effects of Mechanical Stress on Performance of Modern SoCS", iMAPS 2013, Hand-out for Tutorial T7.

Multiscale methodology for calculation of device-to-device variation of stress: Stress Exchange Format

Package-scale simulation (FEA)
Input: geometry; material properties; smeared mechanical properties for RDLs, Silicon/TSV bulk, interconnect.

Output: field of displacement components on the die faces.

Die-scale simulation (FEA)
Input: geometry; field of displacements on the die faces; coordinate-dependent mechanical properties for RDLs, Silicon/TSV bulk, interconnect.

Output: Distribution of the strain components across device layer.

Layout-scale with feature-scale resolution :
Input: GDS.
Output: distribution of the stress components across interconnect metal layer.

Package scale

Package tech file → Package simulations (FEA)

Die scale

Bump effect (compact model)   TSV induced stress (compact model)

CPI stress/strain (FEA)

Feature scale

Composite interconnect layers (compact model)   Transistors layout effect (compact model)

Design (GDSII, OASIS); Design tech file

Stress and strain components (per transistor); mobility shift

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Effective mechanical properties of BEoL, BRDL interconnects and Si/TSV bulk layer

- Theory of the mechanical properties of anisotropic composites is employed.

- Required input: (a) Thermo-mechanical properties of each material – metal, dielectric: CTE, Young's moduli, Poisson factors; (b) fraction of dispersed phase; (c) routing direction of the metal layer.

- For each bin of each layer of interconnect, depending on routing direction: for example the Young's modulus:

$$E_\parallel^{i,j} = E_M \rho_M^{i,j} + E_D\left(1 - \rho_M^{i,j}\right)$$

$$E_\perp^{i,j} = \frac{E_M E_D}{E_D \rho_M^{i,j} + E_M\left(1 - \rho_M^{i,j}\right)}$$
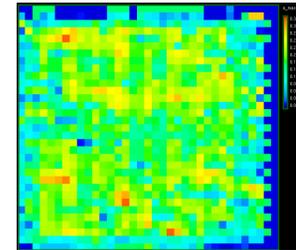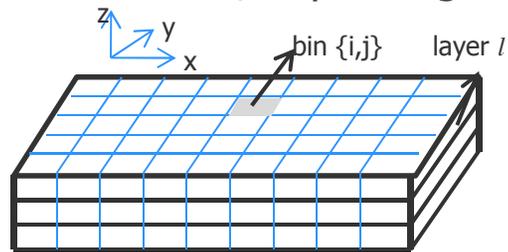
Young's modulus components for M1 layer
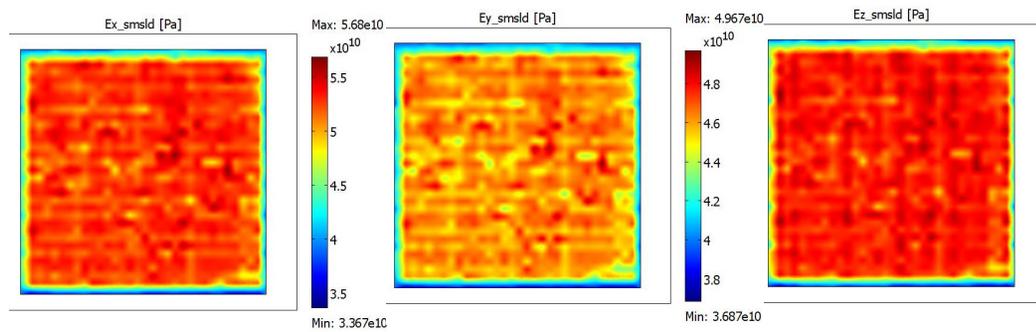
E_x for bulk Si/TSVs: bin size 20 (left) and 100nm (right), TSV 6nm, spacing 40nm.
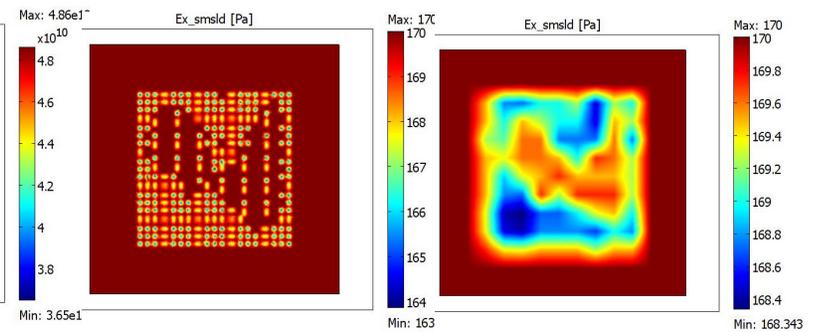
V. Sukharev et al., "Multi-scale simulation methodology for stress assessment in 3D IC: effect of die stacking on device performance," J. Electron. Test. 28(1), 63–72 (2012).

Supported Compact Models

1. **Package-scale: Warpage-Induced Stress**
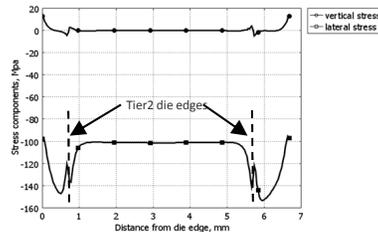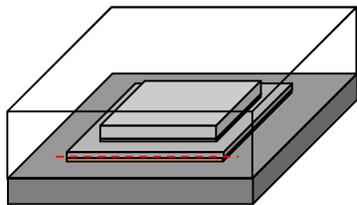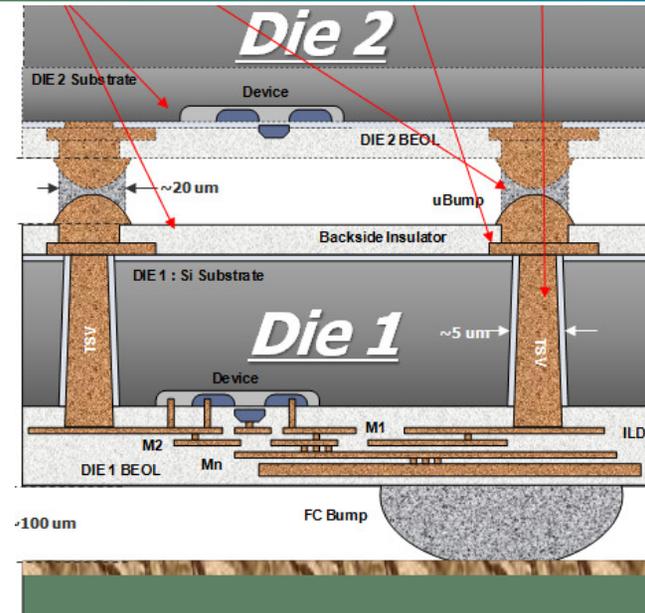

2. **Compact Model for Bump-Induced Displacements**
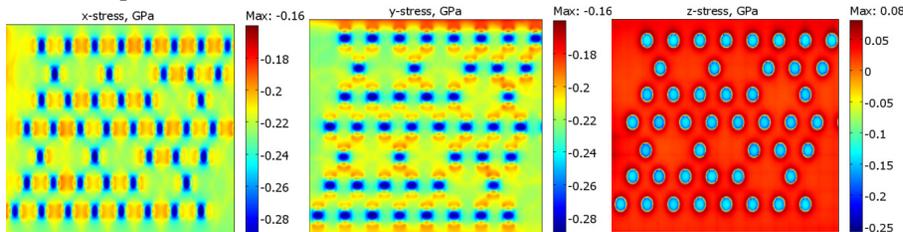
$$P_{x(y)} \sim (E_b - E_u)\frac{\Delta u_{x(y)}^W}{D} \qquad P_z \sim E_b\left(\frac{\Delta u_z^W}{H} + (\alpha_b - \alpha_u)\Delta T\right)$$

3. **Effect of Non-Uniform Interconnect**
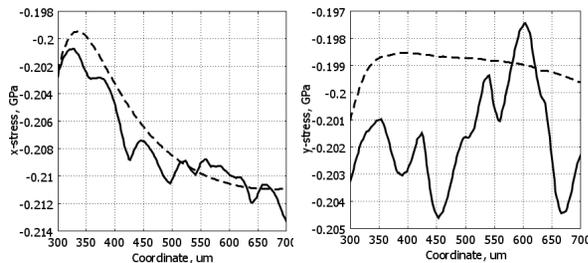
Stress component distributions obtained with: "smeared" (dashed line) and non-uniform (solid line) interconnects.

4. **Compact Model for TSV-Induced Stress:**

Based on: S. Ryu, K. Lu, X., et Al., , "Impact of Near-Surface Thermal Stresses on Interfacial Reliability of Through-Silicon Vias for 3-D Interconnects", IEEE TDMR, VOL. 11, NO. 1, (2011) pp. 35-43

A. Kteyan, et al. "Stress assessment for device performance in three-dimensional IC: linked package-scale/die-scale/feature-scale simulation flow", J. Micro/Nanolith. MEMS MOEMS 13(1), 011203 (Jan–Mar 2014)
FCMN2015, Dresden
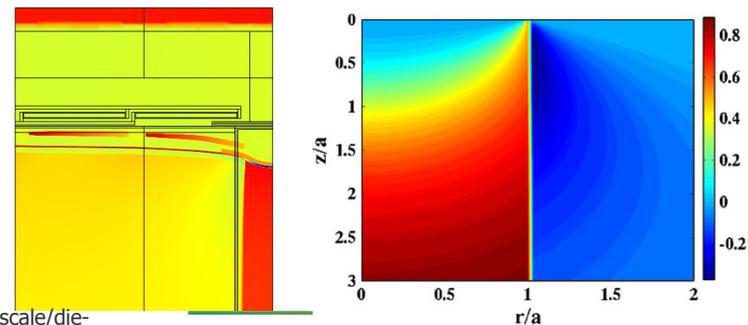
Residual stress in on-chip interconnect

Interconnect face warpage
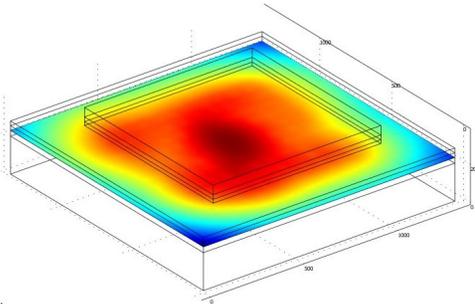
Hydrostatic stress in M1 layer
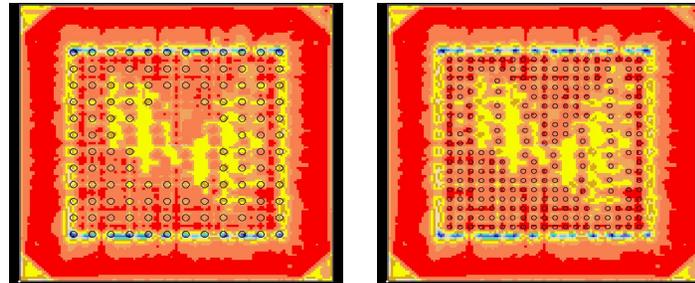
Residual (hydrostatic) stress distribution across M1 layer with the overlaid C4 bumps, (left) and u-bumps (right).

Interconnect tree is a elemental EM reliability unit representing a continuously connected, highly conductive metal (Cu) lines within one layer of metallization, terminated by diffusion barriers.

TREE 37
TREE 41

TREE 41 VDD zoomed

TREE 1296

M1 tree=37 VDD

M1 tree=41 VDD

M3 tree=1296 VDD
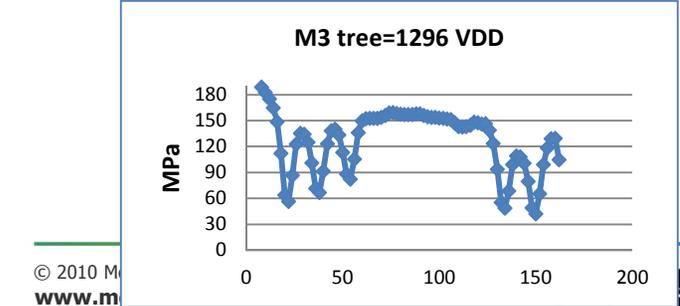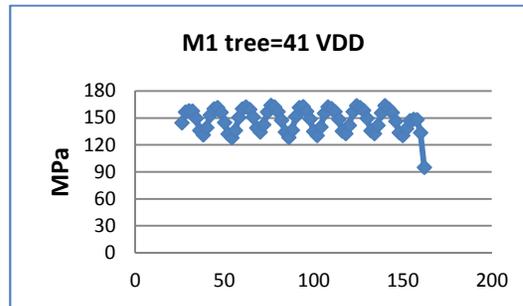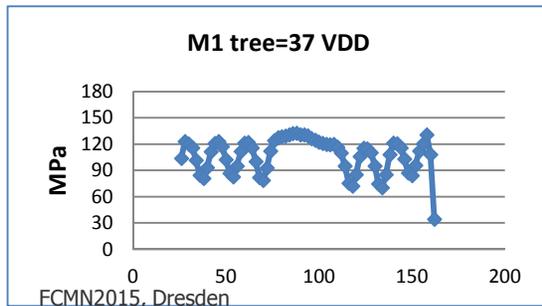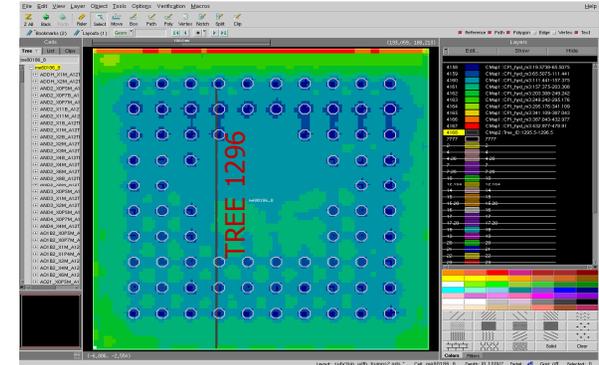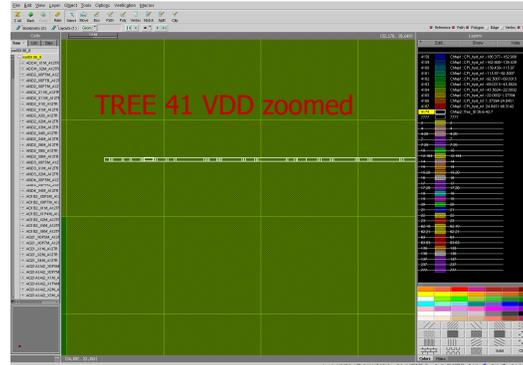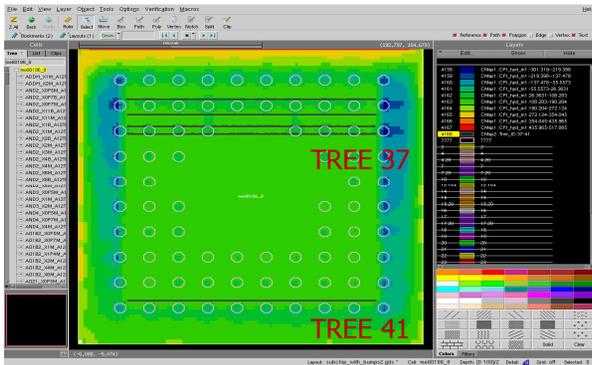
TEMPERATURE ASSESSMENT

Major components

- **MGC's effective thermal properties extractor.**

  - Each interconnect layer is considered as a composite: a mixture of metal fibers included in a dielectric matrix.
  - Calculates the effective thermal conductivity (k_i, i=x,y,z), specific heat of each interconnect layer as a function of local metal density (ρ_M).

  - Lateral components $K_{x,y}$ inside each metal layer are determined by a routing direction:

  - Parallel to the routing direction:
    $$k_{II} = \rho_M k_M + (1 - \rho_M) k_{ILD}$$

  - Normal to the routing direction:
    $$k_{\perp} = k_{ILD}\left[1 + \frac{\rho_M}{k_{ILD}/(k_M - k_{ILD}) + (1 - \rho_M)/2} \right]$$

  - A vertical component:
 $$k_Z = \rho_M k_M + (1 - \rho_M) k_{ILD}$$

- **Thermal Netlist Builder.**

  - A die is represented by a 3D array of cuboidal thermal cells. Each cell contains a thermal node, and is characterized by local effective thermal properties(R_{th}, C_{th}).
  - The array transforms into a thermal netlist.

- **SPICE simulator.**

  - Calculates transistor power consumption.
  - Solves for temperature for each thermal node.

Effective thermal properties of a die

ρ_M

k_x

k_y

k_z

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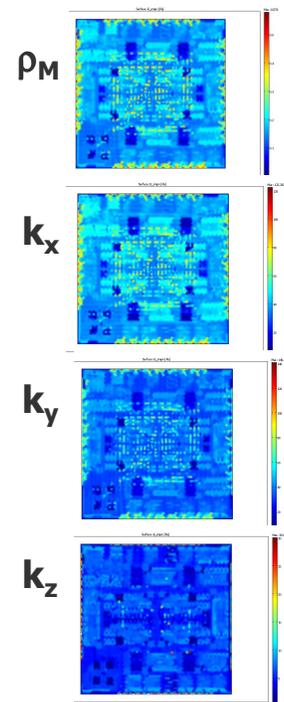
From effective thermal props to thermal netlist

- Construct an array of cuboidal cells of dimension, LxLxt :
  "L" is user-supplied binSize.

- For each cell, MGC's engine uses Calibre to extract local metal density, and calculates effective thermal properties.

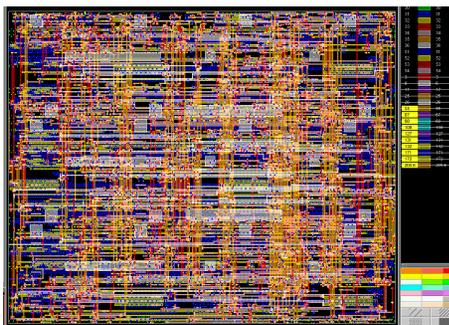- Thermal netlist builder transforms effective thermal properties into R_{th} and C_{th}.

$$R_{top/bottom.i} = \frac{1}{k_{z,i}} \frac{t_{M6}/2}{L^2} \; ; \; R_{north/south,i} = \frac{1}{k_{y,i}} \frac{L/2}{t_{M6}L} \; ; \; R_{east/west,i} = \frac{1}{k_{x,i}} \frac{L/2}{t_{M6}L}$$

$$C_{cell,i} = S_i \cdot (L \cdot L \cdot t_{M6})$$

- The array transforms into a thermal netlist.

- Consideration on boundaries
  - Fixed T with V source & R=0; Insulation with large R.
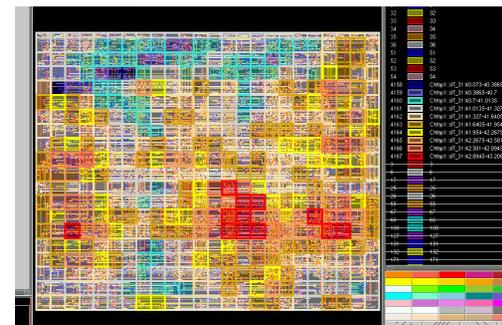
Cell i: $(\rho_{Mi}, k_{xi}, k_{yi}, k_{zi}, S_i)$

L
L
t_{M6}
t_{V5}
t_{M5}

z // top
y // north
x // east
C_{th}
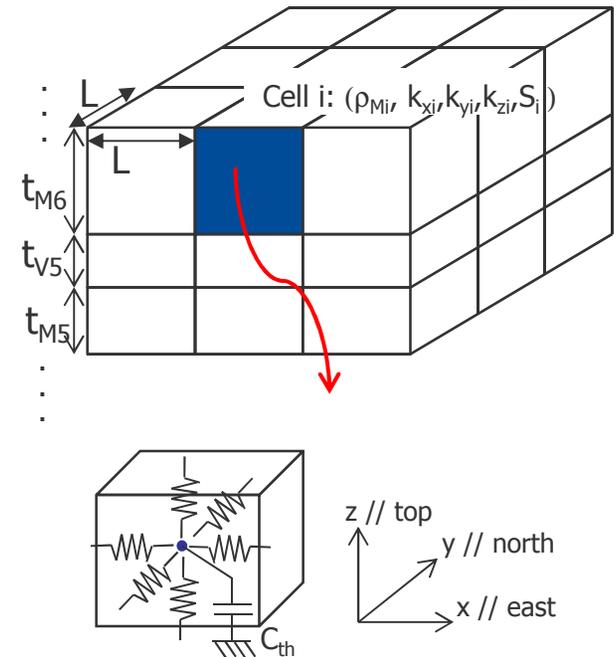
Design

Power map
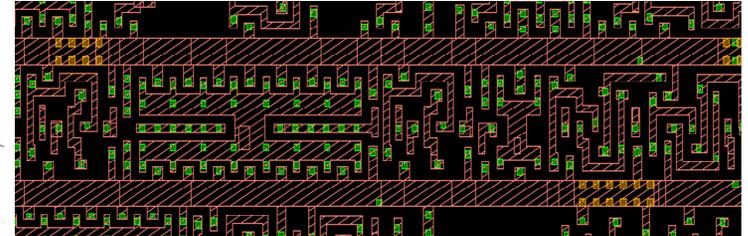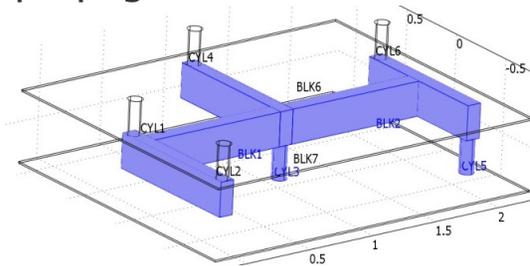
Temperature across M1

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INTERCONNECT SCALE EM MODELING

Chip-scale EM assessment
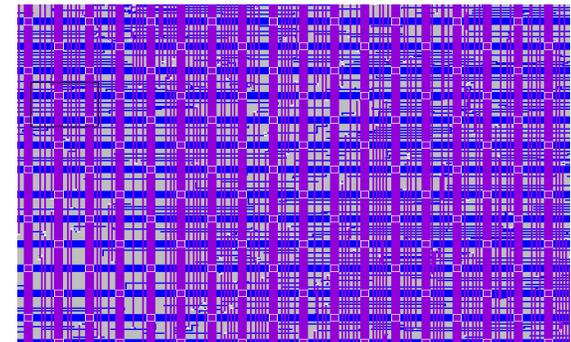
Interconnect functionality

Interconnect tree

- interconnectivity for signal propagation
  - *bidirectional pulsed currents*
- voltage delivery
  - *unidirectional current*
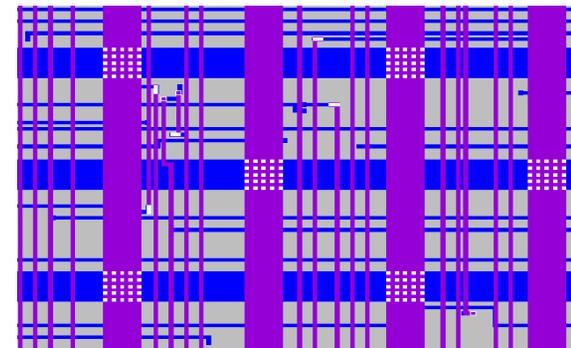 - **power grids, more susceptible to EM effect**

Traditional segment-based EM assessment

- single segment based stress analysis
  - *assume individual segment is confined by diffusion barriers*
  - ***however**, in power grids, atoms can diffuse in the interconnect tree, stress redistribution*
- EM induced failure rate of the individual segment
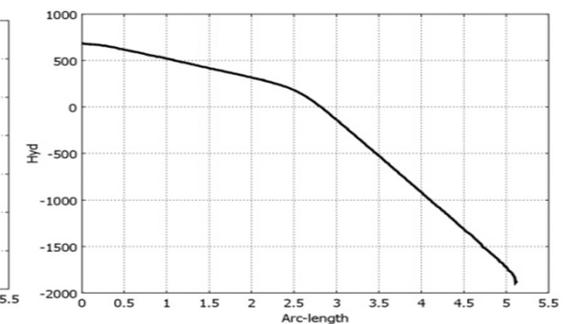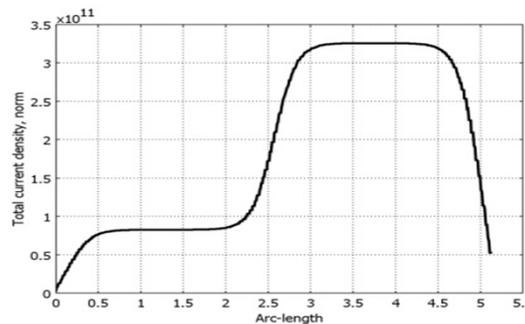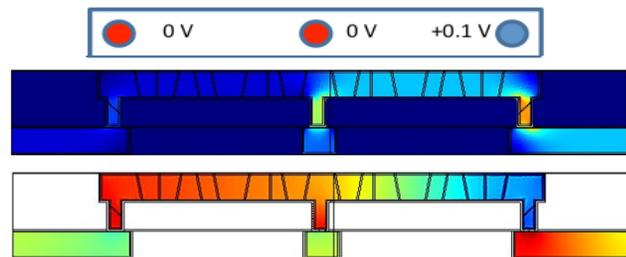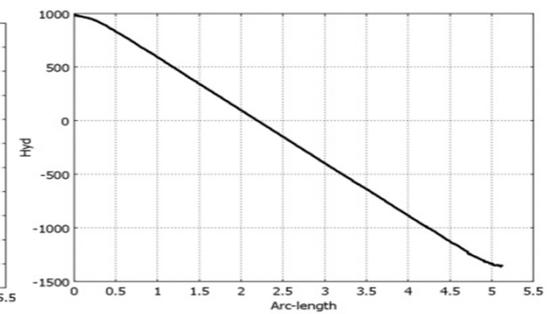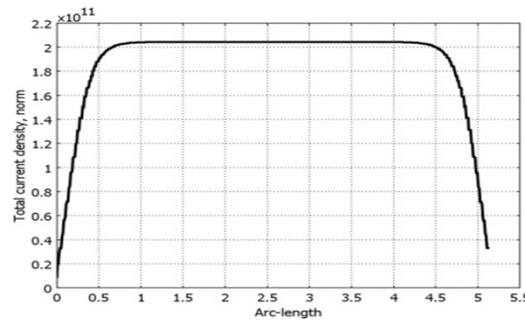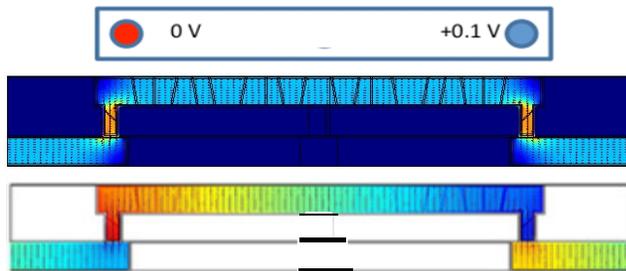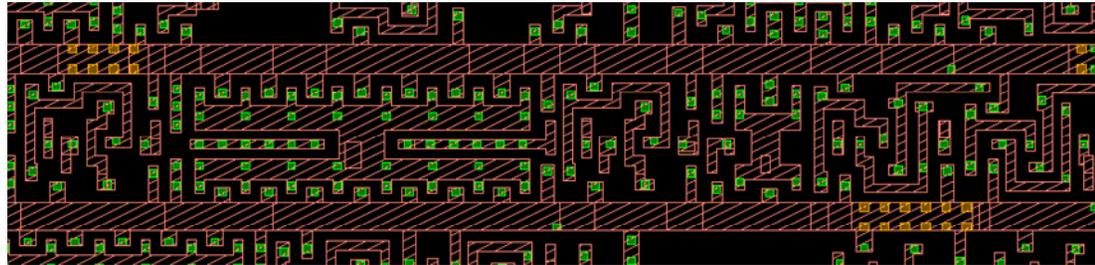
EM induced degradation in power grids

- high level of redundancy
- *Failure*: loss of performance, parametric failure
  - *cannot deliver needed voltage to any point of the circuitry*

New methodology for EM assessment:

- IR drop based assessment
- physics-based models for void initiation and evolution

Interconnect segment vs. wire


Current density

Hydrostatic stress

P. Gibson, M. Hogan, and V. Sukharev, "Electromigration analysis of full-chip integrated circuits with hydrostatic stress," in *2014 IEEE International Reliability Physics Symposium*, 2, pp. 2.1–2.7, 2014.

Mentor Graphics®

Closed-form analytical solution for stress evolution in the multi-branched interconnect tree
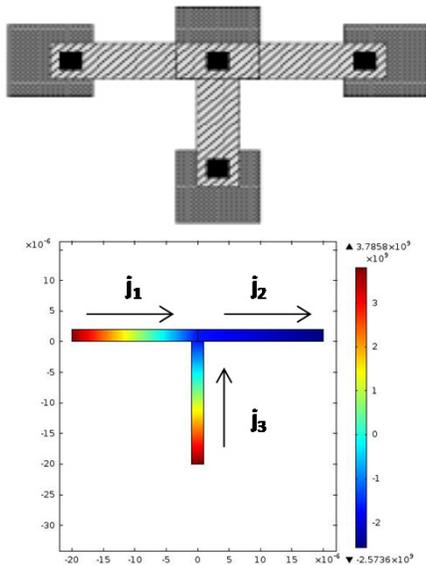
T-shaped interconnect tree with shown directions of the electron flows.
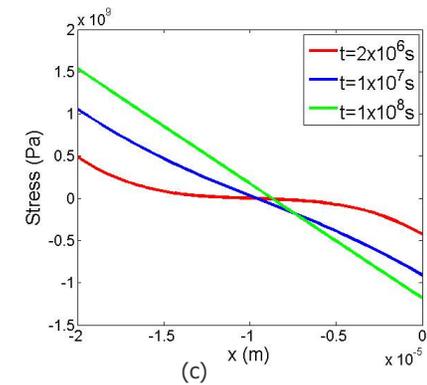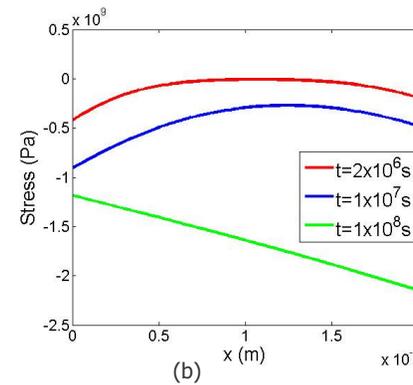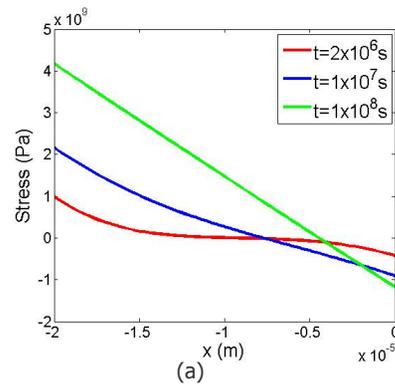
Evolution of the stress distribution along the segment of the shown T-shaped tree; (a) line 1, (b) line 2, and (c) line 3.

If we disassemble these brunches a standard stress evolution will take place in each of them:

V. Sukharev, X. Huang, H.-B. Chen, and S. X.-D. Tan, "IR-Drop Based Electromigration Assessment: Parametric Failure Chip-Scale Analysis" in *Computer-Aided Design (ICCAD), 2014 IEEE/ACM International Conference on*, pp. 428–434, 2014.
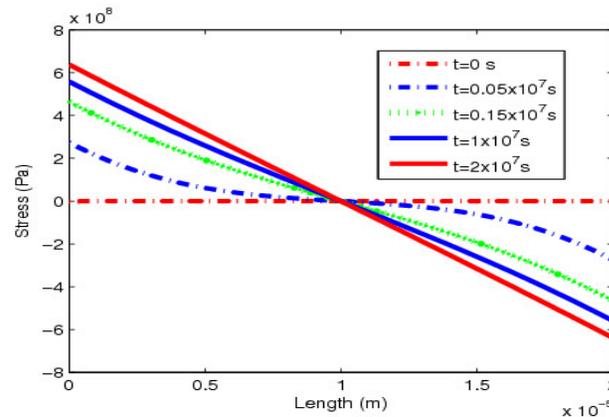
Steady state distribution of the hydrostatic stress inside interconnect tree in void-less regime
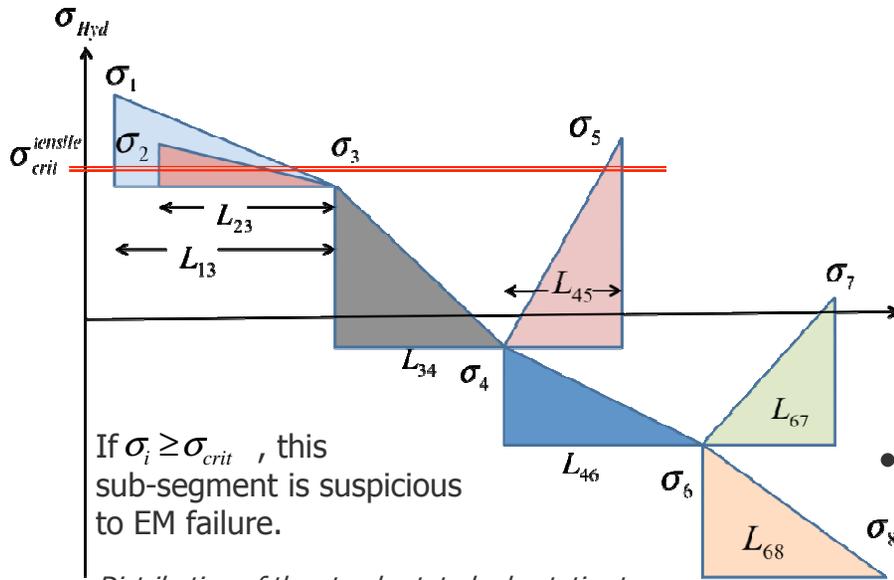
- Assume (just for a moment) that the void less steady state was achieved in the tree.

  For the steady state: $\quad \sigma_i^{cathod} - \sigma_j^{anode} = \Delta\sigma_{ij} = \dfrac{eZ\rho\left(j_{ij}L_{ij}\right)}{\Omega}$
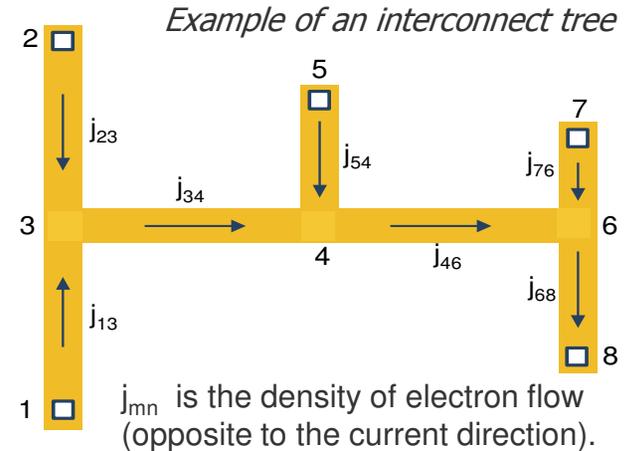
- Consider the redistribution of the atoms between sub-segments due to unblocked sub-segment ends:

$$\sum_{i=1}^{7}\left(\sigma_i - \left[\sigma_T + \frac{B}{3}\left(\frac{R_i}{\delta}\right)e^{-\frac{E_V}{kT_{Zs}}} + \frac{eZ\rho\left(j_{ij}L_{ij}\right)}{2\Omega}\right]\right)L_{ij} = 0$$

Example of an interconnect tree

j_{mn} is the density of electron flow (opposite to the current direction).

- Previously, we use uniform temperature distribution:
  The shortest void nucleation time is characterized by the biggest steady state stress $\sigma_{\mathrm{m}}\left(j_1, j_{2,...}, j_n\right)$,

$$t_{nuc}^{\mathrm{m}} \approx \frac{L_{max/min}^2}{2D_0} e^{\frac{E_V + E_D}{kT}} \frac{kT}{\Omega B}\exp\left\{-\frac{f\Omega\sigma_{\mathrm{m}}\left(j_1, j_{2,...}, j_n\right)}{kT}\right\}$$

$$\cdot \ln\left\{\frac{\sigma_{\mathrm{m}}\left(j_1, j_{2,...}, j_n\right) - \sigma_{\mathrm{Re}s}}{\sigma_{\mathrm{m}}\left(j_1, j_{2,...}, j_n\right) - \sigma_{crit}}\right\}$$

- With temperature variation: Void nucleation time is affected by both T and hydrostatic stress. Consider both factors to find the first nucleated void ($\min\{t_{nuc}^i\}$)

If $\sigma_i \geq \sigma_{crit}$, this sub-segment is suspicious to EM failure.

Distribution of the steady state hydrostatic stress along the considered tree

FCMN2015, Dresden

X. Huang, T. Yu, V. Sukharev, and S. X.-D. Tan, "Physics-based electromigration assessment for power grid networks," in Design Automation Conference (DAC), 2014, 51th ACM/EDAC/IEEE, 2014.

Voiding

When void is nucleated the stress at the void surface is zero. The solution of the stress kinetics equation with the zero-flux co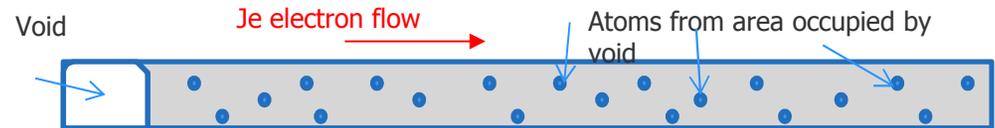ndition at the downstream (anode) end of the line is [**J. He and Z. Suo, AIP Conf. Proceedings, vol. 741, 2004**]: $\left(t \geq t_{nuc}\right)$

$$\sigma(x,t) = -\frac{eZ\rho j L}{\Omega}\left(\frac{x}{L} + \frac{8}{\pi^2}\sum_{n=0}^{\infty}\frac{(-1)^n}{(2n-1)^2}\sin\left[\frac{(2n-1)\pi x}{2L}\right]\exp\left\{-\left(\frac{2n-1}{2}\pi\right)^2\frac{t}{\tau}\right\}\right)$$

Here,

$$\tau = \frac{L^2}{\kappa} = \frac{L^2 k_B T}{DB\Omega}$$

Once the stress field is solved, the void volume is calculated from the volume of atoms drifted into the line:

Void   Je electron flow   Atoms from area occupied by void

$$V = -A\int_0^L \Omega N_{PL}\,dx = -A\int_0^L \Omega\left(\frac{\sigma}{B}N_A\right)dx = -A\int_0^L\left(\frac{\sigma}{B}\right)dx = \frac{eZ\rho j L^2 A}{2\Omega B}\left(1 + \frac{32}{\pi^3}\sum_{n=0}^{\infty}\frac{(-1)^n}{(2n-1)^2}\exp\left\{-\left(\frac{2n-1}{2}\pi\right)^2\frac{t}{\tau}\right\}\right)$$
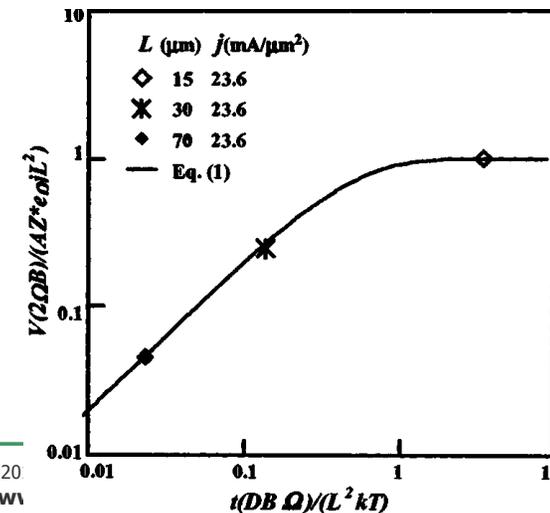
There are two limiting cases for volume void:
1. Short time; stress in the line is small, so

$$\Gamma(\vec{r}) = \frac{D}{\Omega k_B T}eZ\rho j \quad \text{and} \quad V = \Omega\Gamma At = \frac{eZ\rho j DAt}{k_B T}$$

2. Steady state was reached; the atomic flux vanishes, void volume is saturated:

$$\sigma(x) = -\frac{eZ\rho j x}{\Omega} \quad \text{and} \quad V_{sat} = -A\int_0^L\left(\frac{\sigma}{B}\right)dx = \frac{eZ\rho j L^2 A}{2\Omega B}$$

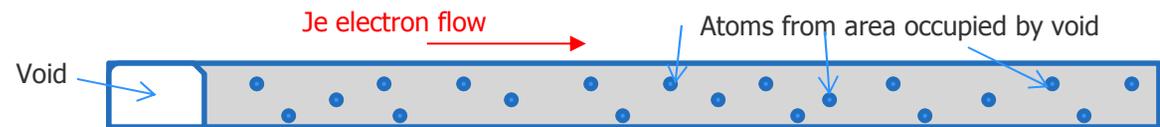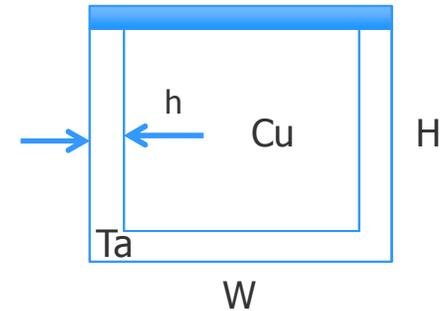| L (µm)	j(mA/µm²)
◇ 15	23.6
✳ 30	23.6
◆ 70	23.6
— Eq. (1)	

Void growth-induced line resistance change

Once V(t) is known the kinetics of line resistance can be easily calculated.

For a void volume at an instance in time t we have:

$$V_{void}(t) = \vartheta * (t - t_{nuc})HW \qquad \vartheta = \frac{DeZ\rho j}{kT}$$

Or, when current density depends on time:

$$V_{void}(t) = HW \frac{DeZ\rho}{kT} \int_{t_{nuc}}^{t} j(t)dt$$

For the corresponding change in the line resistance we can write:

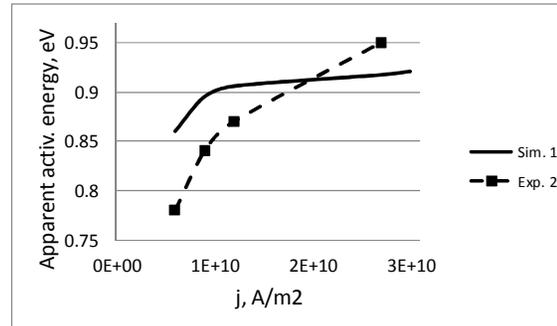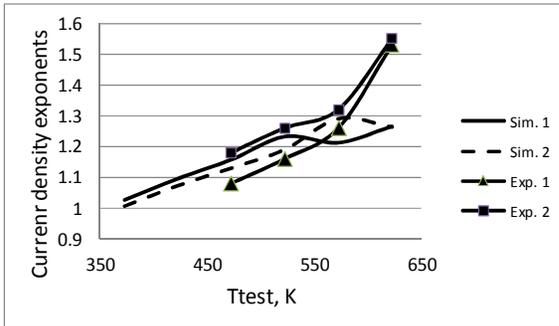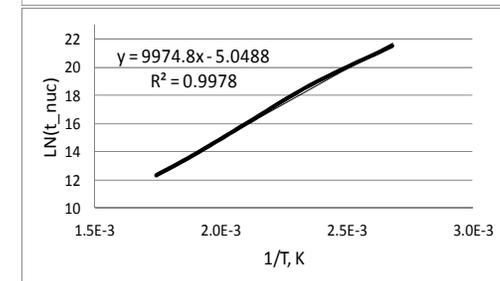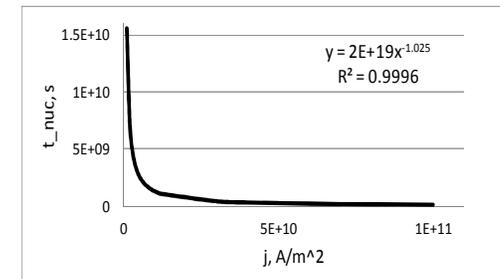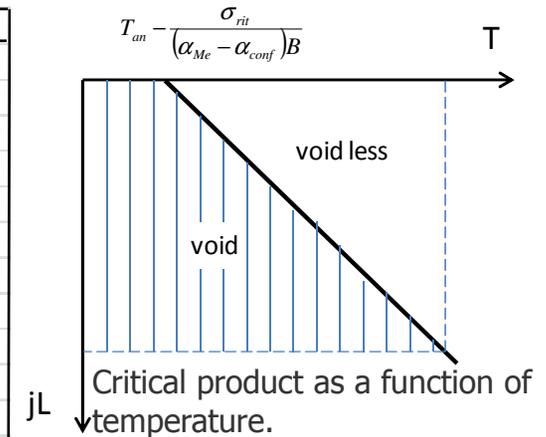$$\Delta R = R_{Ta}^{Void} - R_{Cu}^{Void}$$

$$\frac{1}{R_{Ta}^{Void}} = \frac{1}{R_{Ta}^{void\_wall}} + \frac{1}{R_{Ta}^{void\_wall}} + \frac{1}{R_{Ta}^{void\_bottom}}$$

$$R_{Ta}^{void\_wall} = \rho_{Ta}\frac{\vartheta * (t - t_{nuc})}{hH}; \ R_{Ta}^{void\_bottom} = \rho_{Ta}\frac{\vartheta * (t - t_{nuc})}{hW}; \ R_{Cu}^{Void} = \rho_{Ta}\frac{\vartheta * (t - t_{nuc})}{HW}$$

$$\Delta R(t) = \vartheta * (t - t_{nuc})\left[\frac{\rho_{Ta}}{h(H + 2W)} - \frac{\rho_{Cu}}{HW}\right] \approx \vartheta * (t - t_{nuc})\frac{\rho_{Ta}}{h(H + 2W)} = \frac{V_{void}(t)\rho_{Ta}}{h(H + 2W)HW}$$

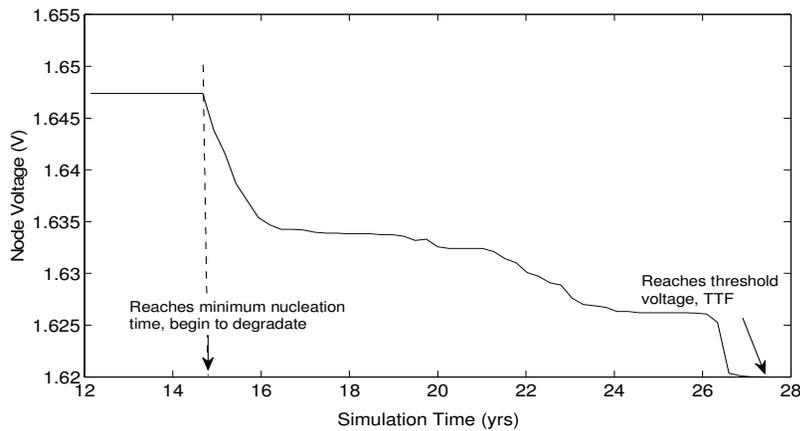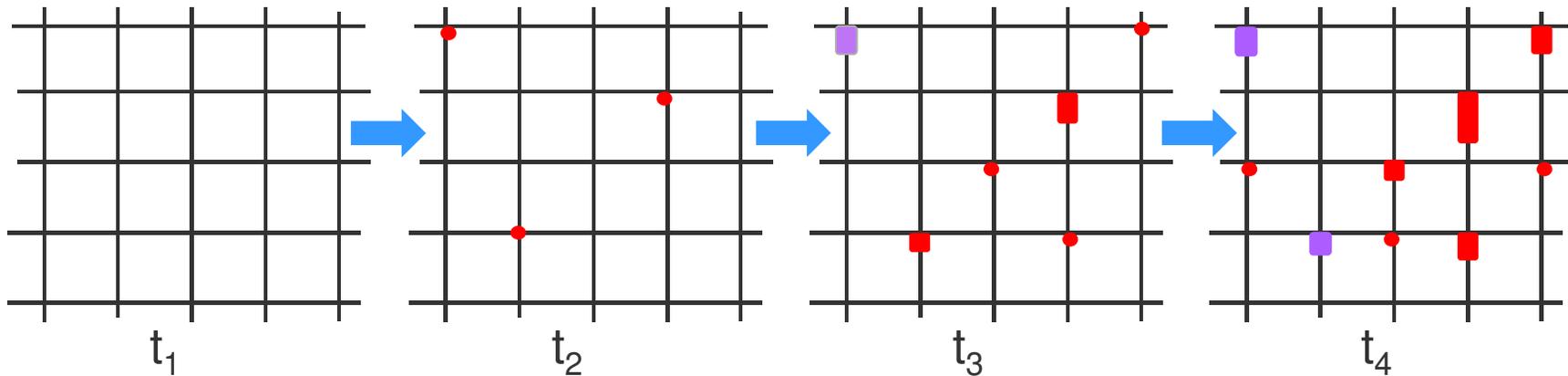# Void nucleation time and void growth time as the functions of the current density and test temperature

	Void nucleation							Void growth					
J/Ttest	323	373	423	473	523	573	623	373	423	473	523	573	623
1.00E+09	T-void	1.55E+10	IMMORT	IMMORT	IMMORT	IMMORT	IMMORT	R<Rcrit	IMMORT	IMMORT	IMMORT	IMMORT	IMMORT
2.00E+09	T-void	6.98E+09	7.09E+08	IMMORT	IMMORT	IMMORT	IMMORT	R<Rcrit	R<Rcrit	IMMORT	IMMORT	IMMORT	IMMORT
3.00E+09	T-void	4.51E+09	3.52E+08	3.85E+07	IMMORT	IMMORT	IMMORT	R<Rcrit	R<Rcrit	R<Rcrit	IMMORT	IMMORT	IMMORT
4.00E+09	T-void	3.33E+09	2.38E+08	1.87E+07	4.16E+06	IMMORT	IMMORT	R<Rcrit	R<Rcrit	R<Rcrit	R<Rcrit	IMMORT	IMMORT
5.00E+09	T-void	2.64E+09	1.80E+08	1.29E+07	1.63E+06	IMMORT	IMMORT	R<Rcrit	R<Rcrit	R<Rcrit	R<Rcrit	IMMORT	IMMORT
6.00E+09	T-void	2.19E+09	1.45E+08	9.93E+06	1.13E+06	2.19E+05	IMMORT	R<Rcrit	R<Rcrit	R<Rcrit	R<Rcrit	R<Rcrit	IMMORT
7.00E+09	T-void	1.87E+09	1.22E+08	8.09E+06	8.76E+05	1.49E+05	3.98E+04	R<Rcrit	R<Rcrit	R<Rcrit	R<Rcrit	R<Rcrit	R<Rcrit
8.00E+09	T-void	1.63E+09	1.05E+08	6.84E+06	7.18E+05	1.16E+05	2.65E+04	R<Rcrit	R<Rcrit	R<Rcrit	R<Rcrit	R<Rcrit	R<Rcrit
9.00E+09	T-void	1.45E+09	9.21E+07	5.92E+06	6.10E+05	9.52E+04	2.06E+04	R<Rcrit	R<Rcrit	R<Rcrit	R<Rcrit	R<Rcrit	R<Rcrit
1.00E+10	T-void	1.30E+09	8.21E+07	5.22E+06	5.31E+05	8.11E+04	1.69E+04	R<Rcrit	R<Rcrit	R<Rcrit	R<Rcrit	R<Rcrit	R<Rcrit
1.10E+10	T-void	1.18E+09	7.40E+07	4.68E+06	4.70E+05	7.08E+04	1.45E+04	R<Rcrit	R<Rcrit	R<Rcrit	R<Rcrit	R<Rcrit	R<Rcrit
1.20E+10	T-void	1.08E+09	6.74E+07	4.23E+06	4.22E+05	6.29E+04	1.27E+04	R<Rcrit	R<Rcrit	R<Rcrit	R<Rcrit	R<Rcrit	R<Rcrit
3.00E+10	T-void	4.28E+08	2.59E+07	1.57E+06	1.49E+05	2.11E+04	4.00E+03	9.09E+09	1.19E+08	3.93E+06	2.53E+05	2.66E+04	4.01E+03
5.00E+10	T-void	2.56E+08	1.54E+07	9.21E+05	8.71E+04	1.22E+04	2.29E+03	4.81E+09	6.27E+07	2.08E+06	1.34E+05	1.41E+04	2.12E+03
7.00E+10	T-void	1.83E+08	1.09E+07	6.53E+05	6.15E+04	8.57E+03	1.60E+03	3.28E+09	4.27E+07	1.42E+06	9.14E+04	9.60E+03	1.44E+03
9.00E+10	T-void	1.42E+08	8.48E+06	5.05E+05	4.75E+04	6.61E+03	1.23E+03	2.49E+09	3.24E+07	1.08E+06	6.93E+04	7.29E+03	1.10E+03

$$T_{an} - \frac{\sigma_{rit}}{(\alpha_{Me} - \alpha_{conf})B}$$

void less

void

Critical product as a function of temperature.

$y = 2E+19x^{-1.025}$
$R^2 = 0.9996$

t_nuc, s

j, A/m^2

$y = 9974.8x - 5.0488$
$R^2 = 0.9978$

LN(t_nuc)

1/T, K

Extracted dependencies of n on T_{test} (a), and E_a on j (b) for Sim. 1 (T_{ZS}=653 K, s$_{crit}$=500MPa) and Sim. 2 (T_{ZS}=723 K, s$_{crit}$=600MPa) vs. experimental data.

Extraction of the current density exponent, (a), and the apparent activation energy, (b), based on the calculated t_{nuc}.

Currenr density exponents — Ttest, K — Sim. 1 / Sim. 2 / Exp. 1 / Exp. 2

Apparent activ. energy, eV — j, A/m2 — Sim. 1 / Exp. 2

EM-induced supply voltage degradation

t_1 t_2 t_3 t_4

- Nucleated void   - Growing void

- Saturated void

EM induced voltage degradation in IBMPG power net

X. Huang, T. Yu, V. Sukharev, and S. X.-D. Tan, "Physics-based electromigration assessment for power grid networks," in Design Automation Conference (DAC), 2014, 51th ACM/EDAC/IEEE, 2014.
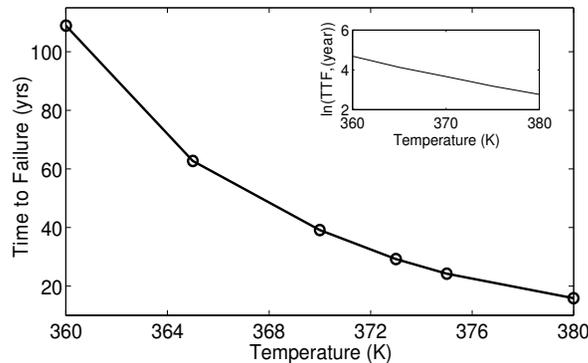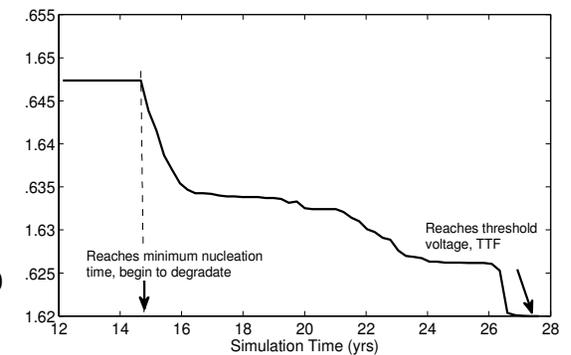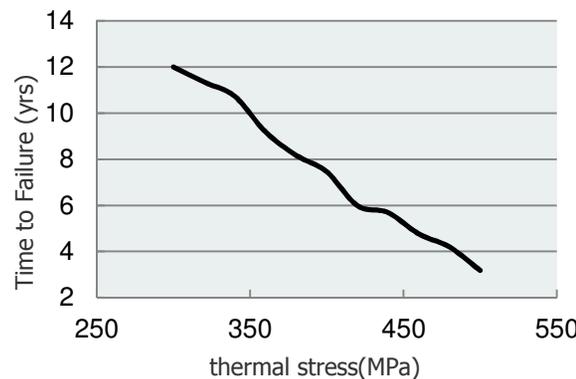
Mentor Graphics

EM Assessment Results in IBM Benchmarks

✧ Current source values are modified to ensure initial IR drop of any node is smaller than the threshold value

TABLE: COMPARISON OF POWER GRID MTTF
USING BLACK'S EQUATION AND PROPOSED MODEL

Power Grid		Time to Failure (yrs)		Proposed model	CPU time of Our Method
Name	Nodes	Black's Equation			
		Series	Mesh		
IBMPG2	61797	7.82	10.67	15.66	54.66min.
IBMPG3	407279	15.77	19.95	27.61	19.61hr.
IBMPG4	474836	12.58	23.68	29.20	19.93hr.
IBMPG5	497658	6.34	11.1	23.05	54.87min.
IBMPG6	807825	9.53	13.97	17.80	32.52hr.
IBMPGNEW1	715022	13.64	17.50	22.48	6.89hr.
IBMPGNEW2	715022	12.44	18.77	20.12	5.99hr.

✧ Both Black's equation based series and Mesh models lead to pessimistic predictions

(a) Voltage drop (V) distribution and (b) Initial steady state hydrostatic stress (Pa)distribution predicted by initial current density in IBMPG2.
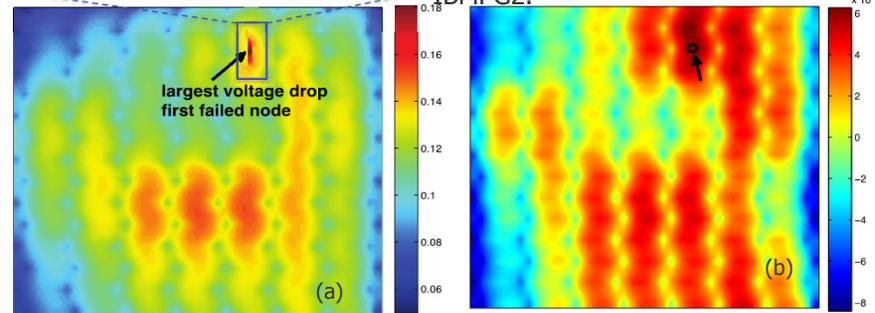
✧ In this work, the first failure is most likely to happen at the nodes where the initial hydrostatic stress is large

✧ EM effect is sensitive to temperature

  - *TTF exponentially relates to temperature (the same as Black's equation)*

✧ Reducing chip temperature/ temperature gradient could extend TTF

Voltage at the first failed node over time

X. Huang, T. Yu, V. Sukharev, and S. X.-D. Tan, "Physics-based electromigration assessment for power grid networks," in Design Automation Conference (DAC), 2014, 51th ACM/EDAC/IEEE, 2014.

EXAMPLE OF IR-DROP EM ASSESSMENT

CHIP-SCALE EM ASSESSMENT CONSIDERING THE IMPACT OF TEMPERATURE AND CPI STRESS VARIATIONS

Layout
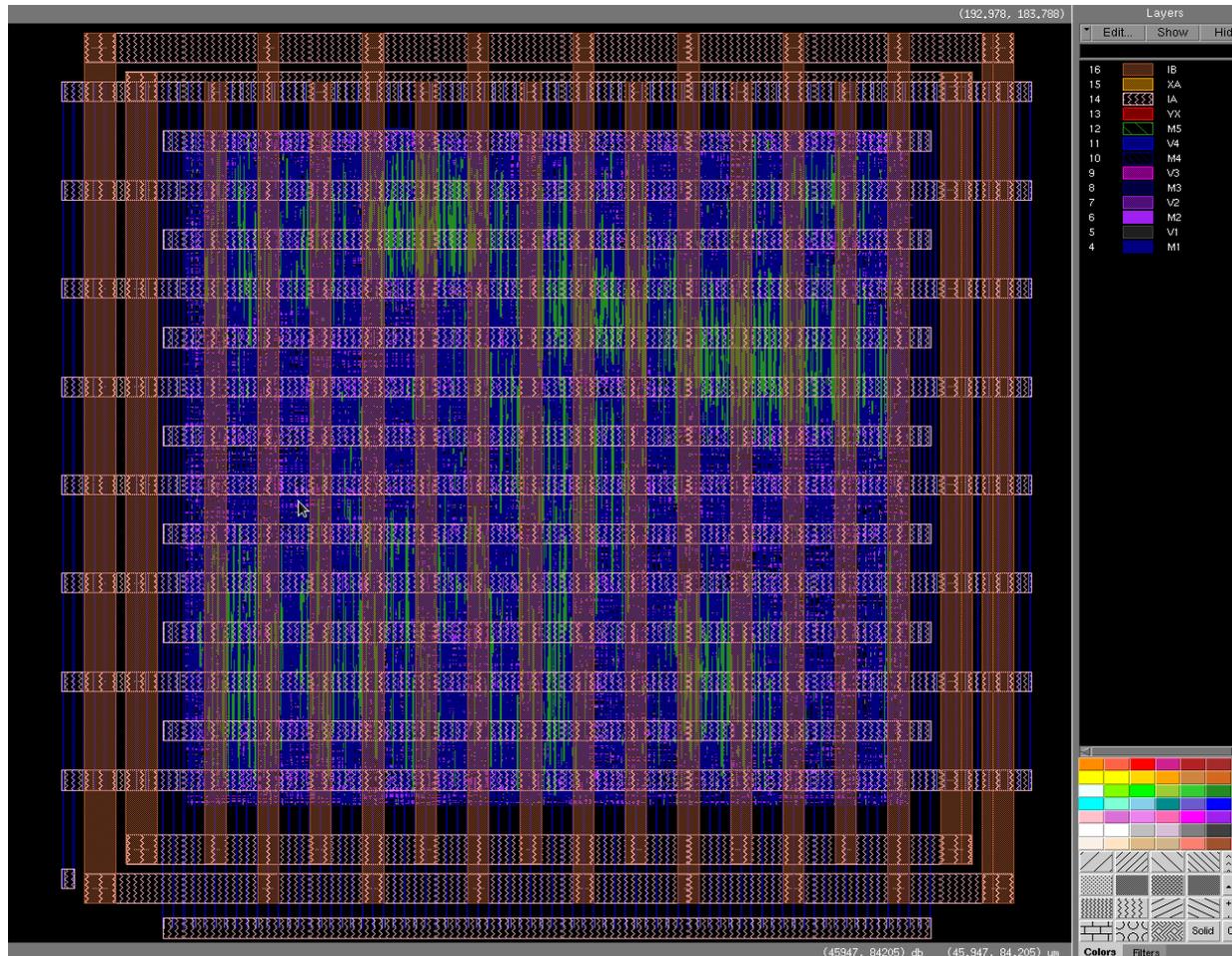
- Design:
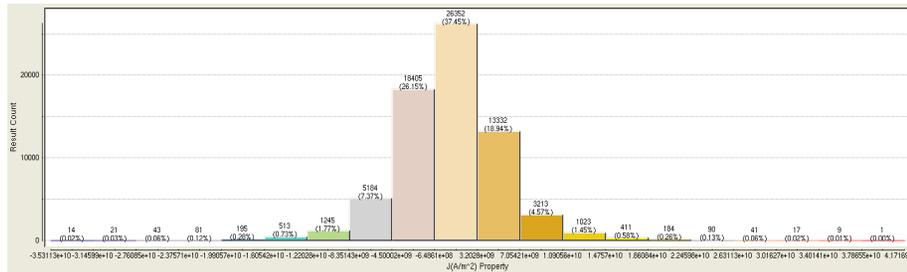- 7-metal layer
- 32nm
- Dimension:184um × 184um

Layer number	Name
3	Contact
4	M1
5	V1
6	M2
7	V2
8	M3
9	V3
10	M4
11	V4
12	M5
13	YX(V5)
14	IA(M6 wide)
15	XA(V6)
16	IB(M7 wide)

Initial current density and initial IR-drop

-power net, M1 layer

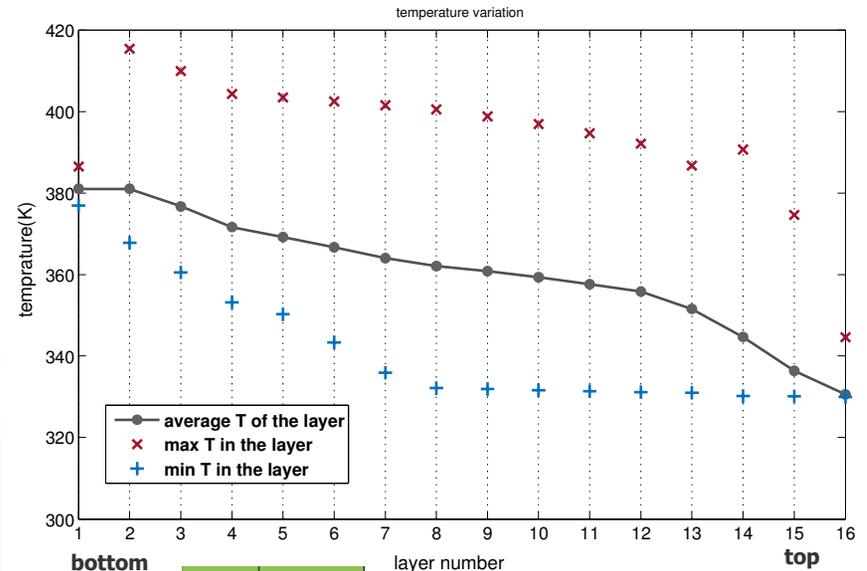# Initial hydrostatic stress

-power net, M1 layer

$\sigma_{crit} = 500\text{Mpa}$
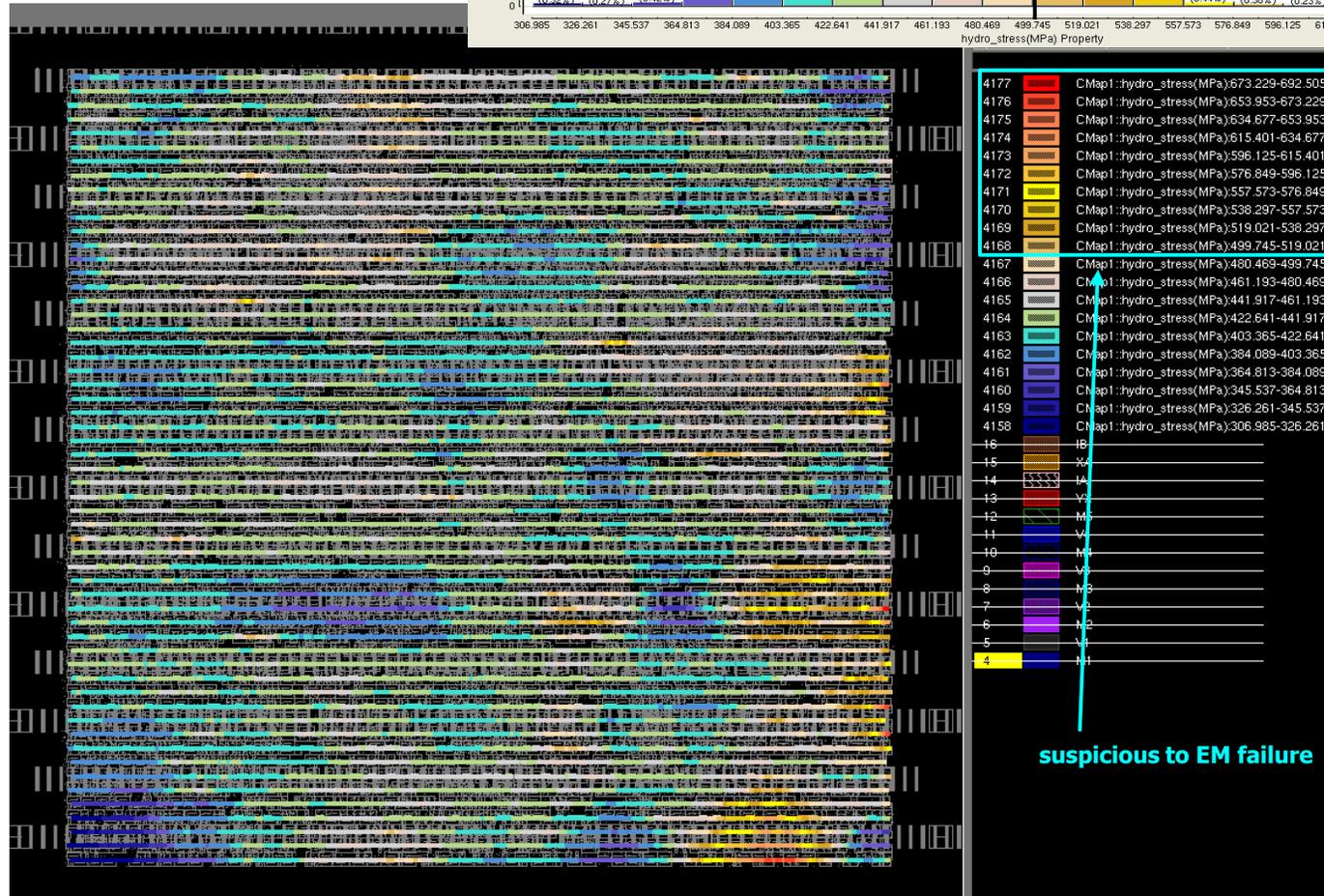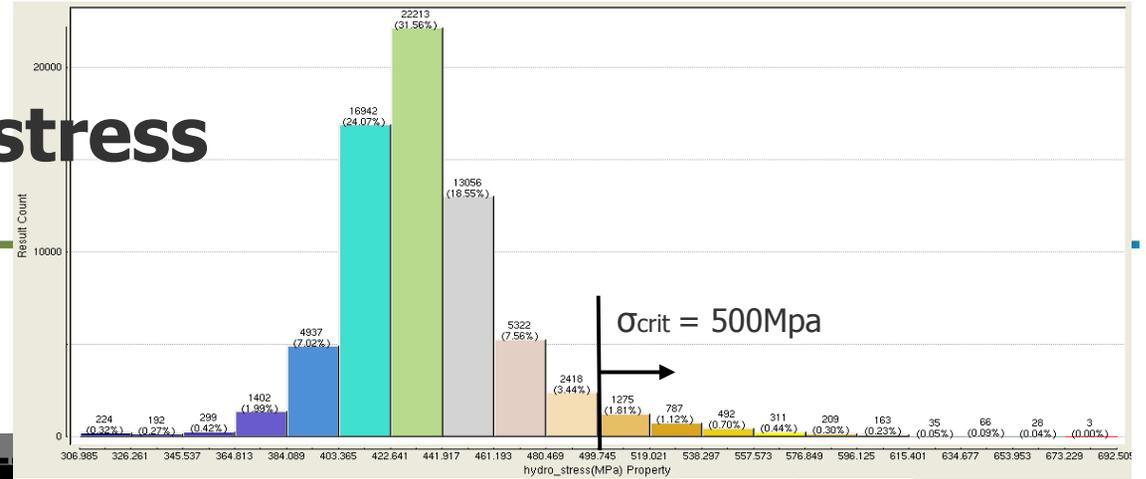
suspicious to EM failure

Temperature distribution

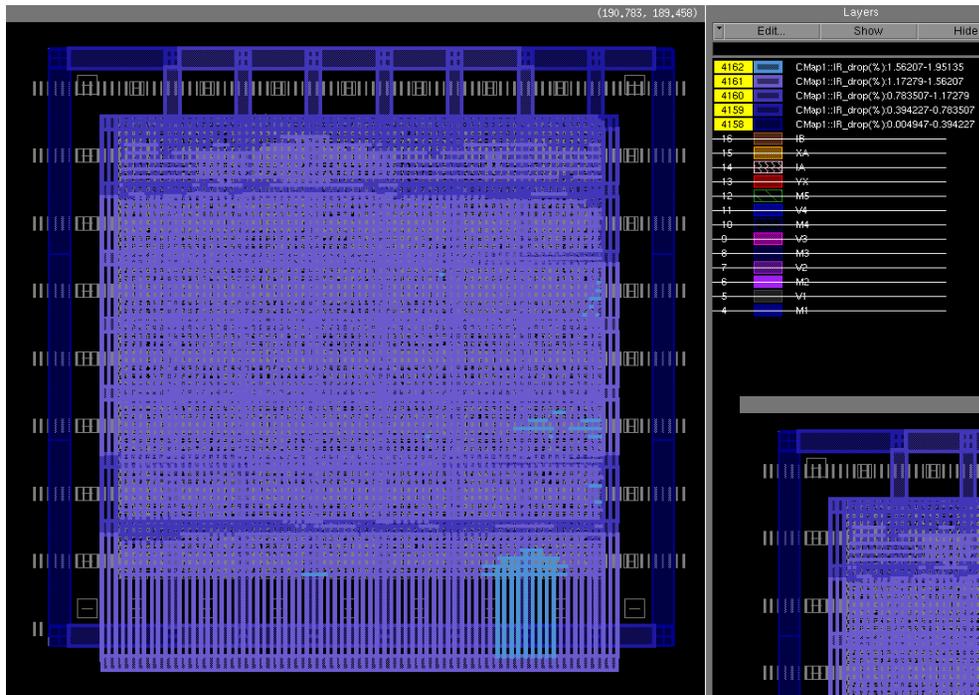## Metal 1 layer

M. Chew, A. Aslyan, J.-H. Choy, X. Huang, "Accurate Full-Chip Estimation of Power Map, Current Densities and Temperature for EM Assessment", in *Computer-Aided Design (ICCAD), 2014 IEEE/ACM International Conference on*, pp. 440–445, 2014.
FCMN2015, Dresden
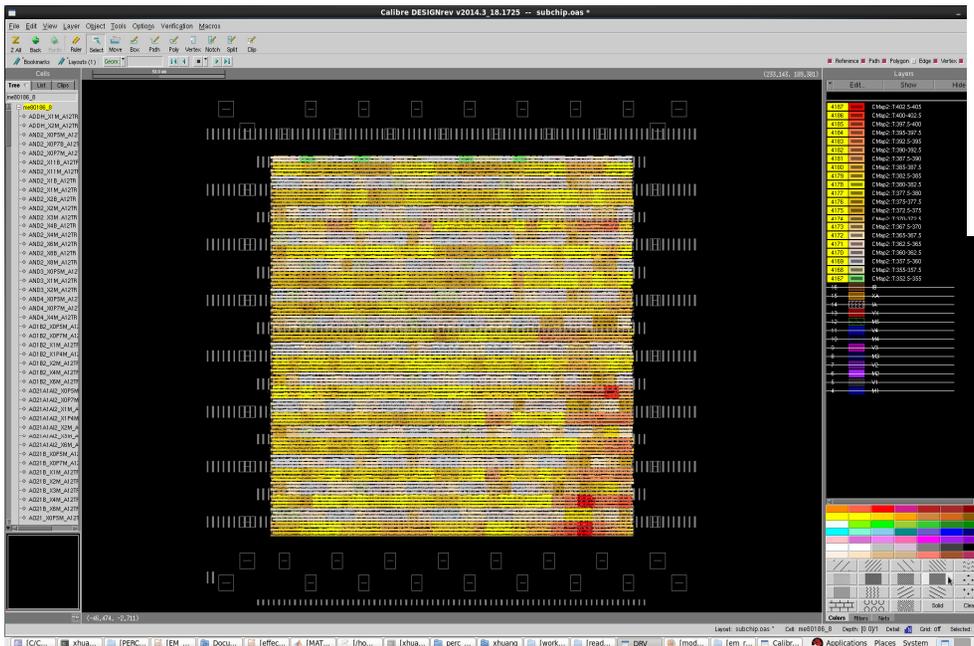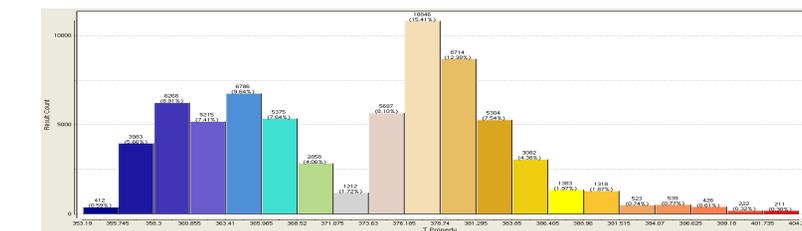
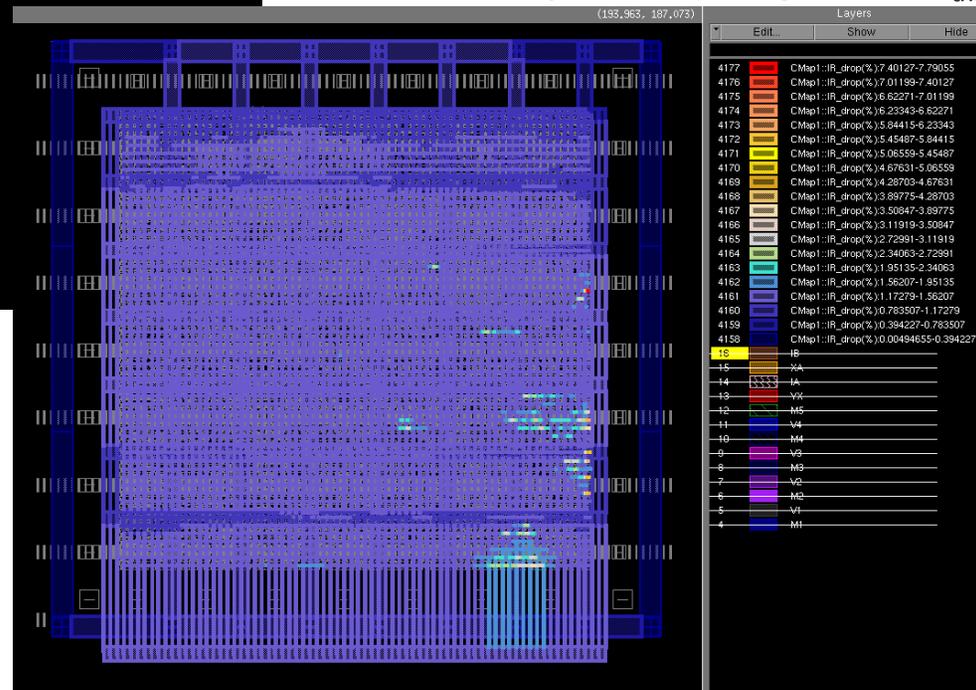| Layer	Layer number
Si	1
Si_device	2
Contact	3
M1	4
V1	5
M2	6
V2	7
M3	8
V3	9
M4	10
V4	11
M5	12
YX	13
IA(8x)	14
XA	15
IB(8x)	16

EM induced IR drop change
- power net

Initial IR drop distribution

Final IR drop distribution (at lifetime$_{th}$)

- ◆ Significant IR drop changes in M1 layer

Mentor Graphics

EM induced IR drop change
- power net

Branches with voids
- power net

Voids mainly locate in M1 layer, some voids locate in M3 layer

EM induced IR drop change
- power net

Chip fails when the maximum IR drop > threshold level

CALIBRATION/VALIDATION

# How to calibrate/validate verification tools?

- **Both types of tools predicting the effect of CPI on chip performance and chip reliability need as inputs:**
    - Measured foundry and process dependent thermal-mechanical properties of the involved materials.
    - Calibrated compact models employed for calculation of the stresses and temperature across a device layer and across the whole chip.
    - Calibrated models for calculating effective thermal-mechanical properties of all composite layers (BEoL and RDL interconnects, underfill with C4 and u-bumps, silicon bulk with TSVs, etc.).

- **Both types of tools need to be validated by a direct comparison between the predicted characteristics and measured:**
    - Comparing the measured characteristics of individual transistors and predicted by verification tools is a validation of the CPI effect on chip performance.
    - **What kind of test-structures should be used to validate the effect of CPI on chip reliability (EM as an example)?**

Calibration of the models for effective thermal-mechanical properties

- ❑ New approach to determine CTE for Cu/ULK for a partially de-processed 3DIC, by combination of FIB cutting and SEM (heating stage holder).
  - isolate a bar
  - separate into two bars of same length, and measure the gap in the middle as a function of temperature up to 250° C
- ❑ Layout file (GDSII & Oasis) allows to calculate all three components of the effective CTE for different bin sizes.
- ❑ Following FEA simulation could allow to calibrate the effective CTE model.

- ❑ Similar approach can be employed for calibration of the models for effective Young's modulus and Poisson factor.
- ❑ There is a need in experimental methodology for calibrating the models for thermal properties of on-chip interconnects and other composite layers.
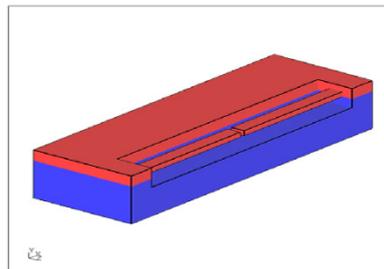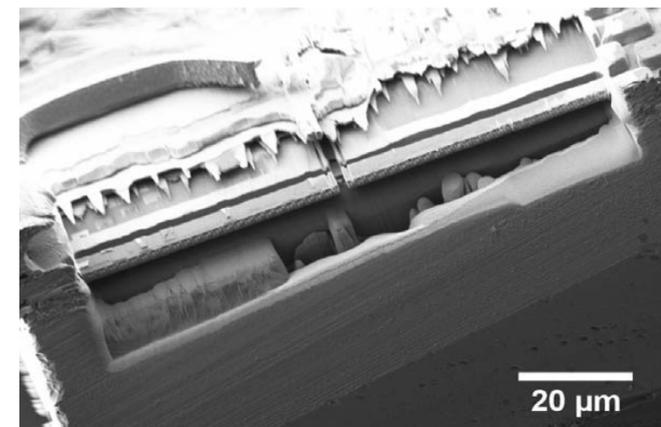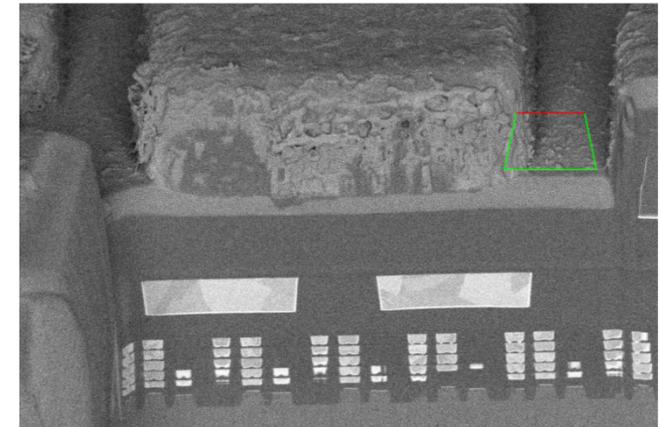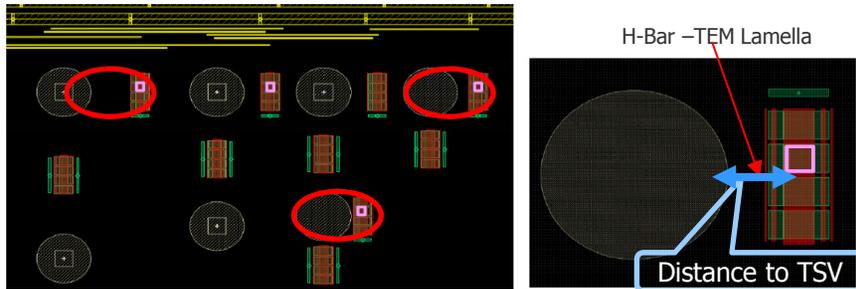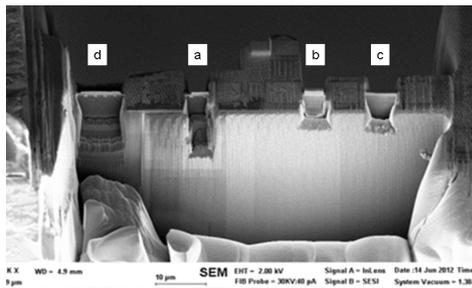

20 µm

R. Radojcic, E. Zschech, V. Sukharev, "Managing the Effects of Mechanical Stress on Performance of Modern SoCS", iMAPS 2013, Hand-out for Tutorial T7.

QCthermal.fbd

Proof Electrical vs. Mechanical

MECHANICAL DOMAIN

H-Bar –TEM Lamella

Distance to TSV

TEM CBED measurement of strain

Calibrating ε_{th} :

$$\sigma_x = -\sigma_y = \frac{E_{Si}\varepsilon_{th}}{1 - 2v_{Si}} \frac{D_{TSV}^2}{4r^2} \cos 2\theta$$

Reconstructive FEA simulation

After FIB processing   Before FIB processing

Strain distribution in lamella
(— after FIB, — before FIB)
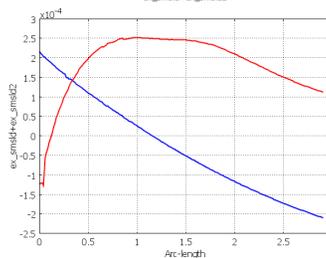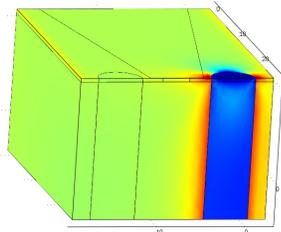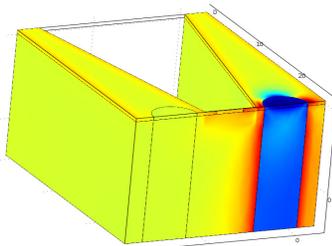
ELECTRICAL DOMAIN
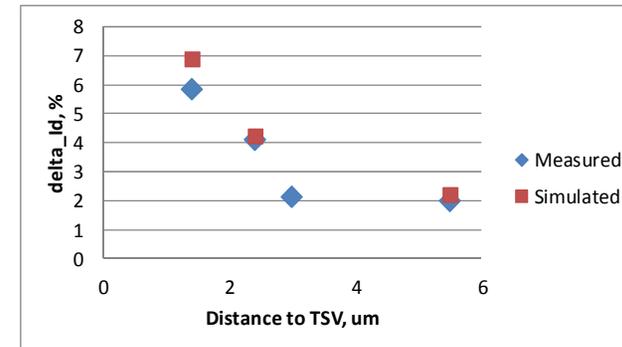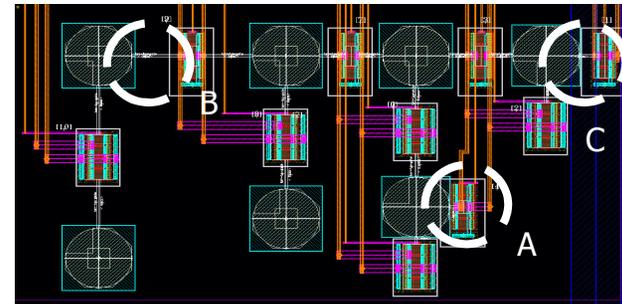
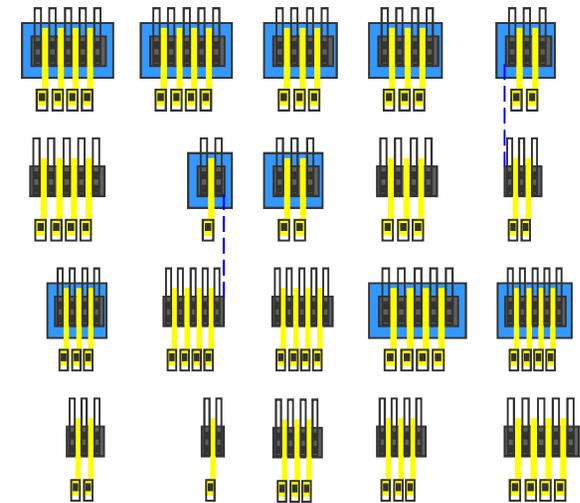$$\Delta I^{simul} = -\left(\pi_x^I \sigma_x + \pi_y^I \sigma_y + \pi_z^I \sigma_z\right) I^{SPICE}$$
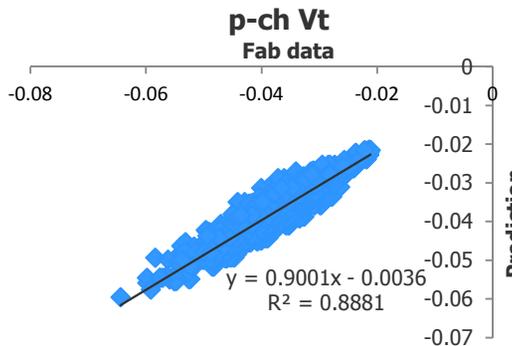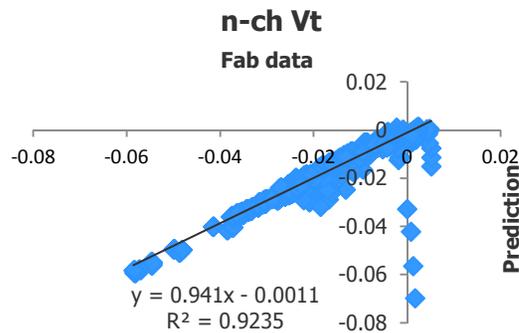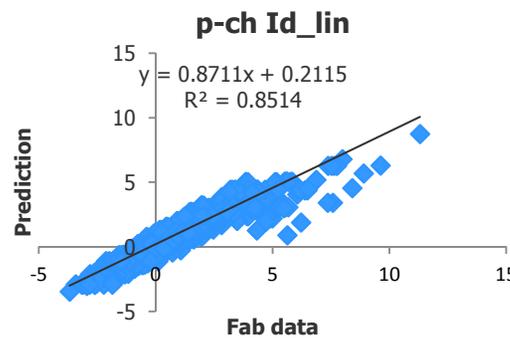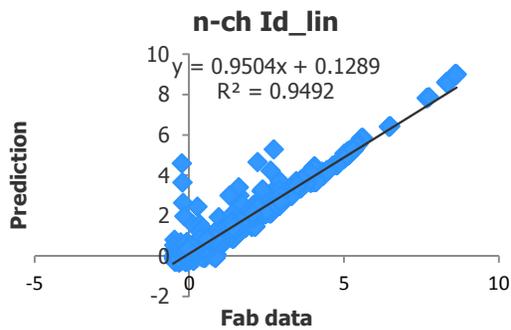
Good fit between simulated and measured electrical characteristics of transistors located at different distances from TSV allows to calibrate the developed tool with relatively easy accessible electrical data.

R. Radojcic, E. Zschech, V. Sukharev, "Managing the Effects of Mechanical Stress on Performance of Modern SoCS", iMAPS 2013, Hand-out for Tutorial T7.

Validation with the Foundry calibrated Model

Calibration was performed on ~100 gates
Prediction was made for all (~4000) gates

Test-chip segment

n-ch Id_lin

$y = 0.9504x + 0.1289$
$R^2 = 0.9492$

Prediction (y-axis), Fab data (x-axis)

p-ch Id_lin

$y = 0.8711x + 0.2115$
$R^2 = 0.8514$

Prediction (y-axis), Fab data (x-axis)

n-ch Vt

Fab data

$y = 0.941x - 0.0011$
$R^2 = 0.9235$

p-ch Vt

Fab data

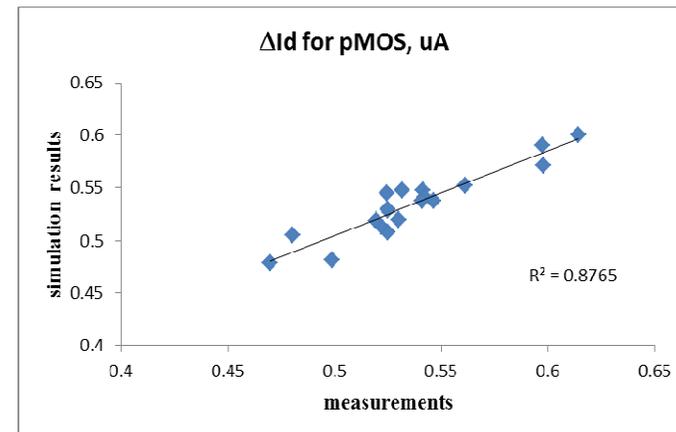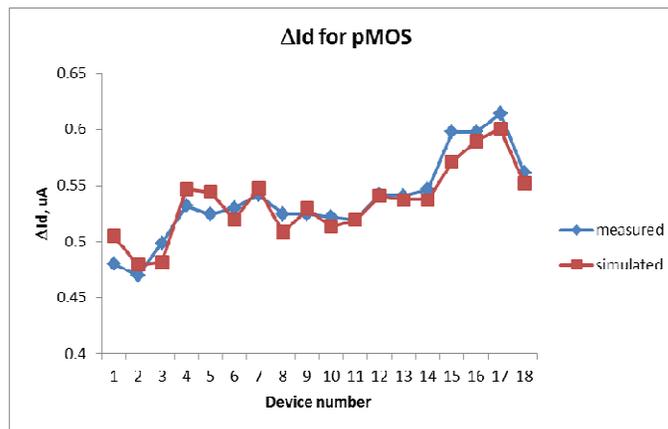$y = 0.9001x - 0.0036$
$R^2 = 0.8881$

Prediction (y-axis)

V. Sukharev et al., "Multi-scale simulation methodology for stress assessment in 3D IC: effect of die stacking on device performance," J. Electron. Test. 28(1), 63–72 (2012).

Mentor Graphics

Die Corner Array: Test-chip 28nm node
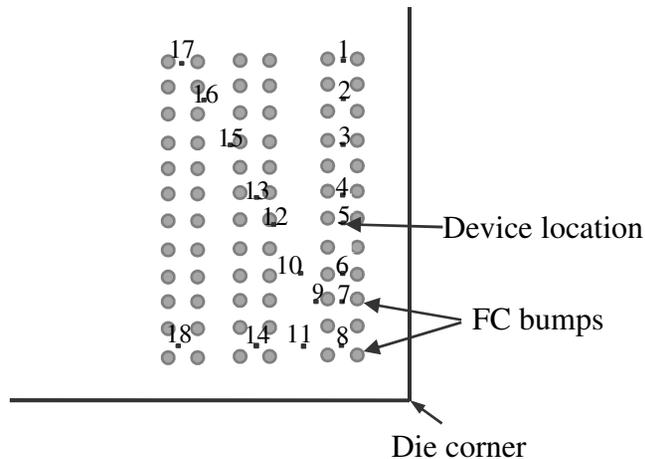
Schematics of the test structures used for model calibration: die corner

R. Radojcic, E. Zschech, V. Sukharev, "Managing the Effects of Mechanical Stress on Performance of Modern SoCS", iMAPS 2013, Hand-out for Tutorial T7.

Validation related tasks

- **How can we validate the predicted stress distribution inside the interconnect metal of the die stacked by 3D IC technology?**

- **How can we validate the distribution of the EM- or SM-induced voids inside BEoL interconnect?**

- **How can we monitor the accelerated kinetics of IR-drop degradation? What kind of test-structures should be developed?**

- **Test-chips with the temperature sensors?**

- **Itc., etc.**

CONCLUSIONS

A NOVEL METHODOLOGY FOR FULL-CHIP POWER/GROUND NETS REDUNDANCY-AWARE EM ASSESSMENT BASED ON IR-DROP ANALYSIS WAS DEVELOPED.

PHYSICS-BASED MODEL FOR TEMPERATURE- AND RESIDUAL STRESS-AWARE VOID NUCLEATION AND GROWTH WAS DEVELOPED AND IMPLEMENTED IN THE FLOW.

A DEVELOPED TECHNIQUE FOR CALCULATING THE HYDROSTATIC STRESS DISTRIBUTION INSIDE A MULTI BRANCH INTERCONNECT TREE ALLOWS TO AVOID OVER OPTIMISTIC PREDICTION OF THE TIME TO FAILURE MADE WITH THE BLECH-BLACK ANALYSIS OF INDIVIDUAL BRANCHES OF INTERCONNECT SEGMENT.