Economies of CMOS Scaling

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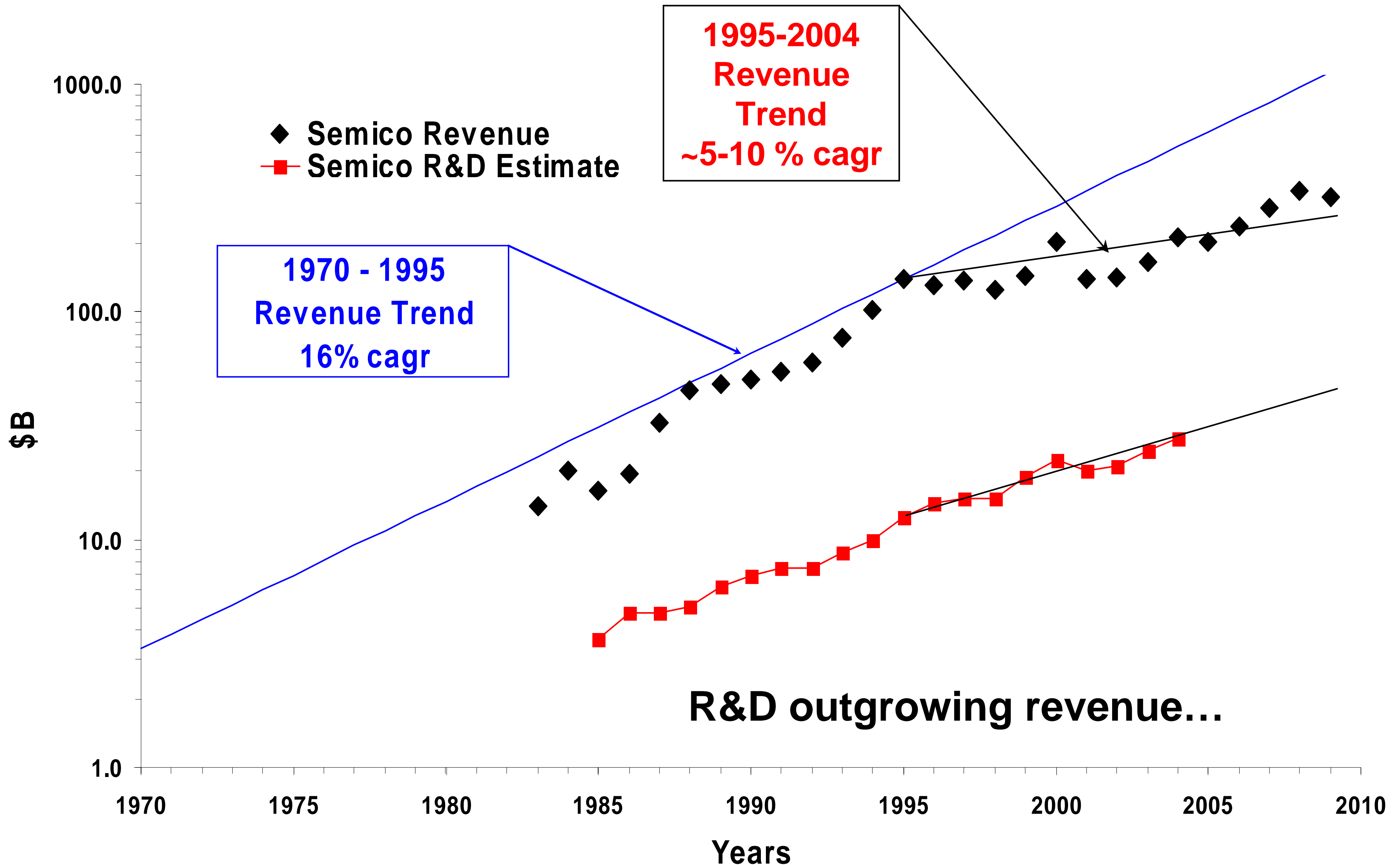
Revenue and R&D Forecasting



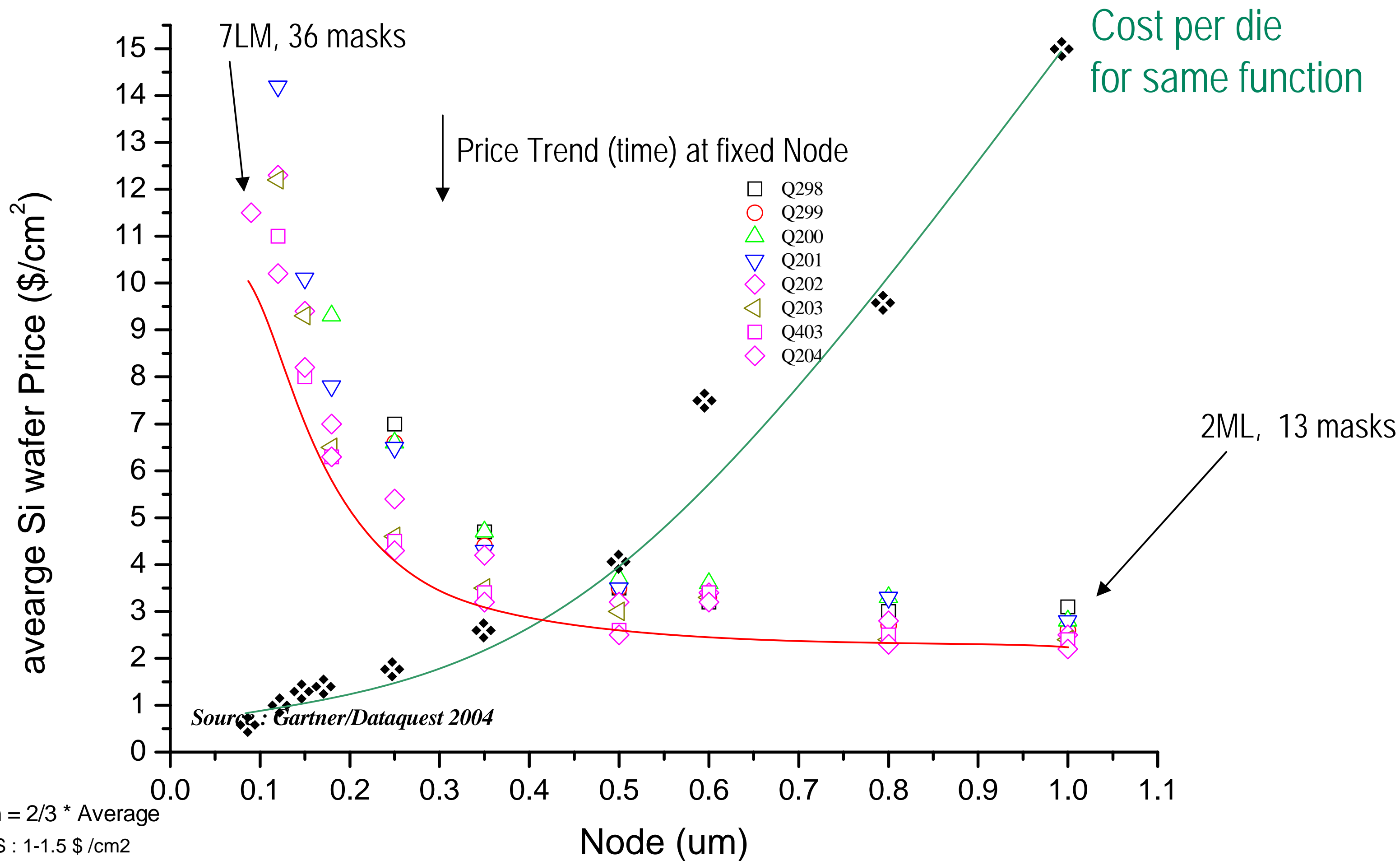
Increasing Investment in R&D

- New process development > $ 300M
  - Time to revenue > 4 years
- New wafer fab > $ 2B
  - Time to revenue > 2-3 years
- New product development > $ 10M **x 100**
  - Time to revenue > 1.5 years

- High risks with long cash flow
  - Volatile market
  - Difficult execution
  - Rapid innovation cycles

Pricetrend Baseline CMOS

Foundry Data



Min = 2/3 * Average

LTPS : 1-1.5 $ /cm2

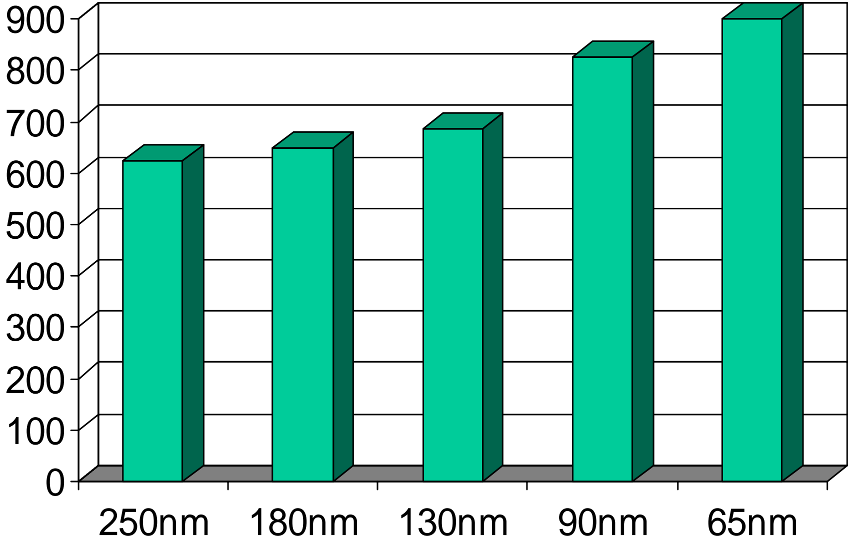
Source: [2004] Carel van der Poel, Philips Research

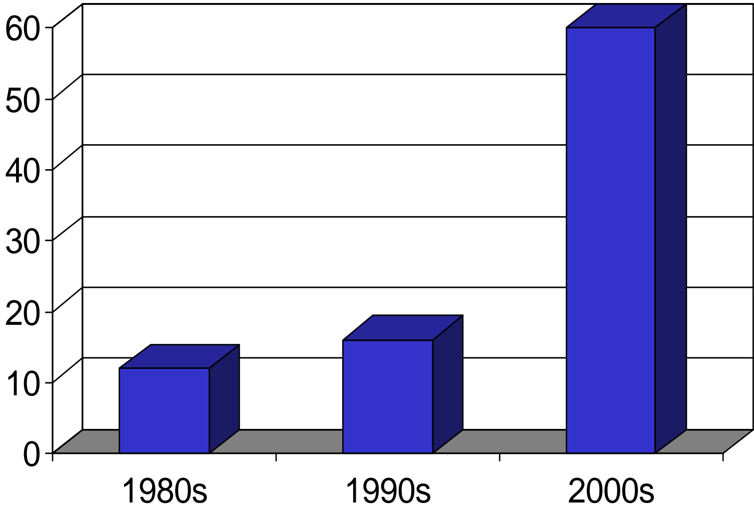
Next Generation CMOS Challenges

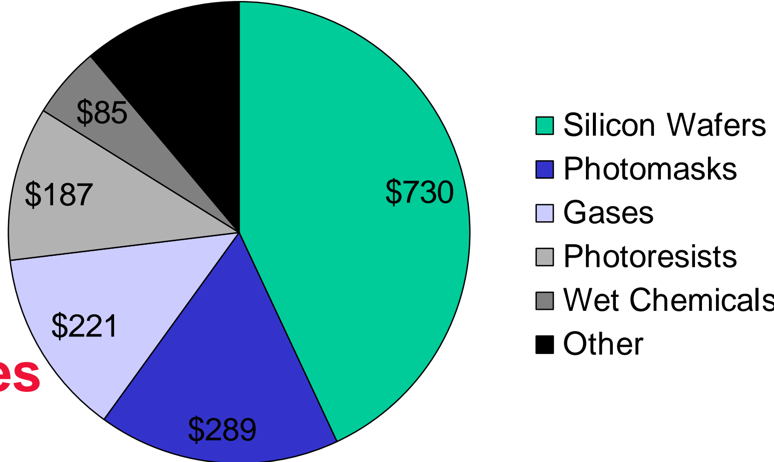
- Immersion 193 lithography with extensive RET
- Low leakage and high performance sub 40nm CMOS transistors
  - Strain engineering
  - High-k gate dielectric and metal gate
- Cu interconnect with ultra low-k dielectrics

- Power Management
- Analog and RF integration on the driver product
- Process development on 300mm

Complexities







Limited market opportunity for consumables

Sources: IBM, SEMI and WaferNews

RET Progression

Increasingly complex
Increasingly expensive

0.25um
- size adjusts
- iso/dense selective size adjusts for poly
- line end extension

0.18um
- size adjusts
- iso/dense selective size adjusts on multiple layers
- hammerheads and serifs
- model based OPC for SRAM poly

130 nm
- size adjusts
- iso/dense selective size adjusts (SSA)
- hammerheads and serifs
- model based OPC for active and poly
- attenuated PS for holes and poly
- vector e-beam reticle write for active and poly

90 nm
- size adjusts
- model-based iso/dense SSA
- hammerheads and serifs
- model based OPC for active, poly and metal
- attenuated PS for holes
- alternating PS for poly
- advanced OPC strategies
- vector e-beam reticle write for all critical levels

65 nm
- size adjusts
- model-based iso/dense SSA
- hammerheads and serifs
- model based OPC for active, poly, contacts and metal
- attenuated PS for holes
- alternating PS for poly
- vector e-beam reticle write for all critical levels
- Scattering bars for multiple levels

Complexity of Contact SRAFs

Single Isolated Contact:

Requires sub-resolution assist features to print

Nearby Contact:

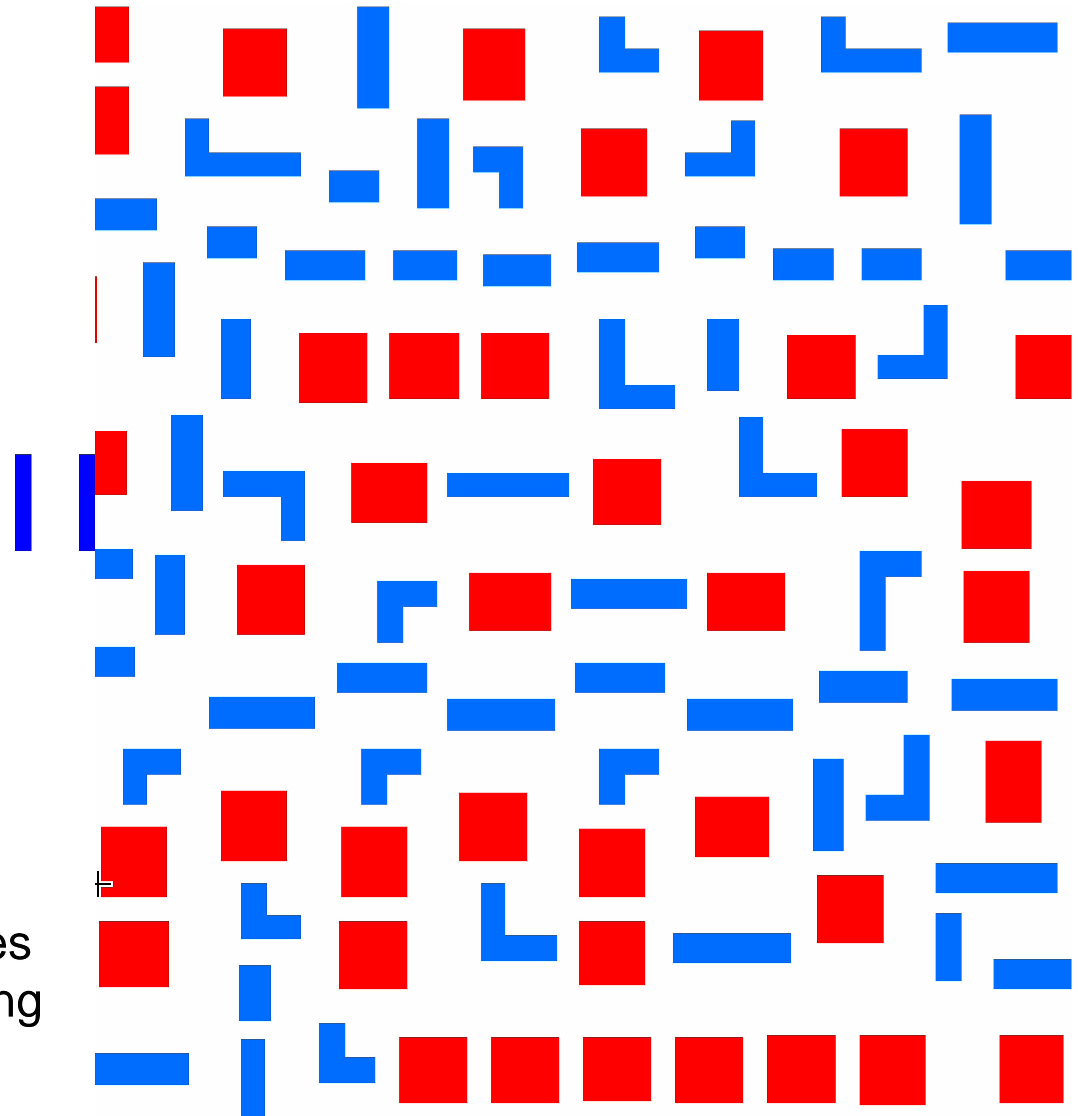
Requires sharing of sub-resolution assist features

Multiple Contacts

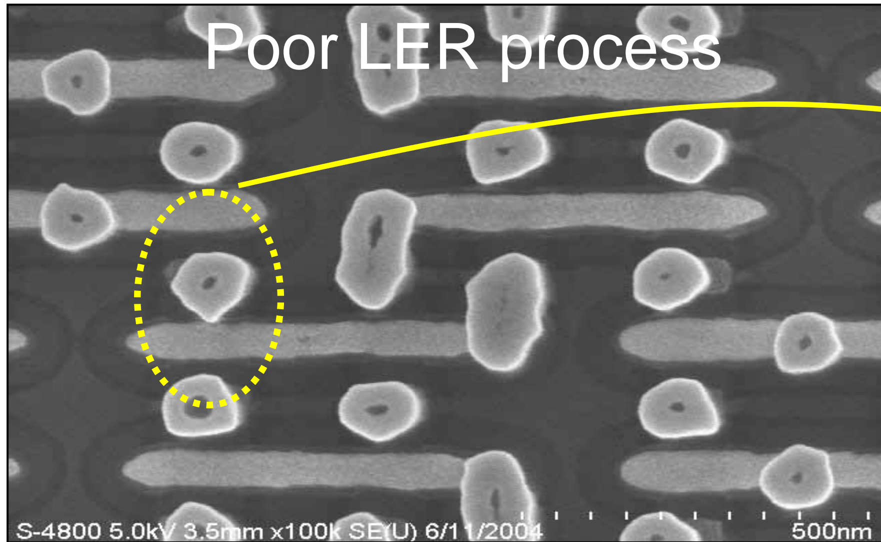
Conflicts require complicated conflict resolution code

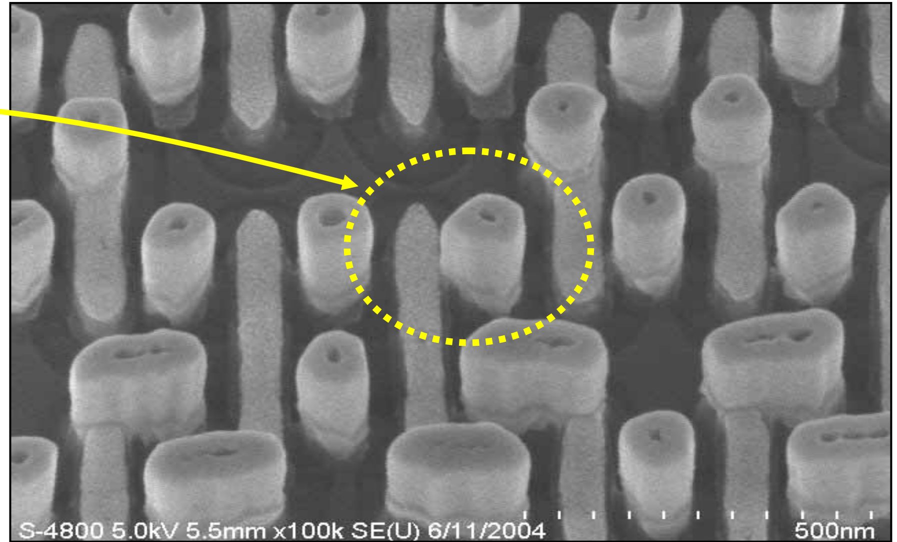
Production Layouts

Millions of SRAF compromises followed by model based sizing of every contact



Tighter Design Rules





- **Contact patterning is no. 1 lithography challenge for 65nm**
- **Tight gate-to-contact spacing results in little margin for contact edge roughness or deformation, or for alignment**
- **Significant work needed for OPC, to optimize photo and etch processes**

Strained Silicon

PMD liner

Capped poly

Raised S/D

Recess S/D epi (SiGe)

Implant S/D strain

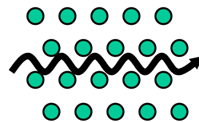
STI liner

Strained channel

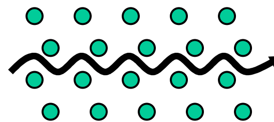
Substrate orientation

Active area epi

Normal Si lattice



Strained Si lattice



Improved mobility

Holes in [110] Uniaxially Compressed Si

Si

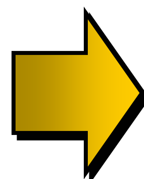
[110]

k_y

$| p_x,p_y>$

k_x

Unstrained Heavy Hole (HH)



LH,HH

HH_S

LH_S

⊥ *Mobility Degrades*

|| *Mobility Improves*

k_y

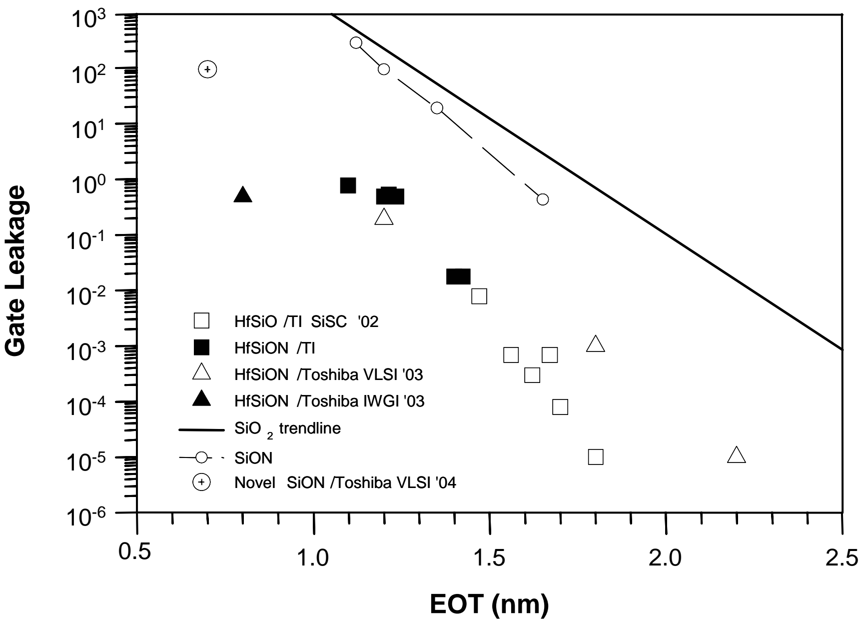
$| s,p_x,p_y ,p_z>$

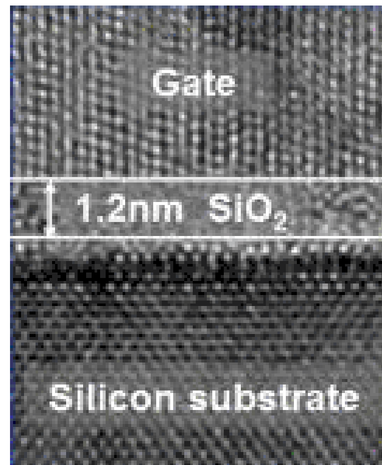
k_x

Strained Heavy Hole (HHS)

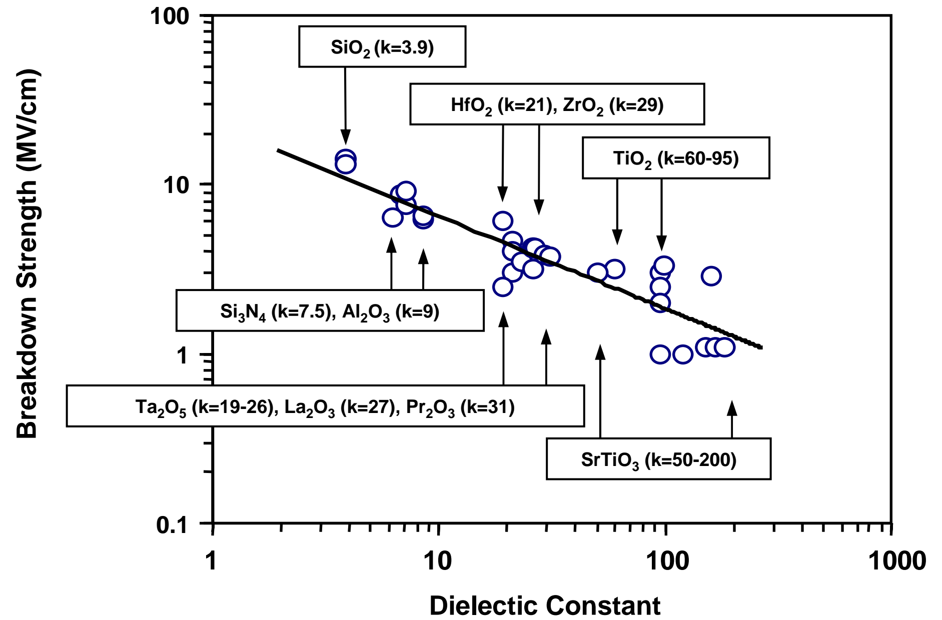
Gate Insulator

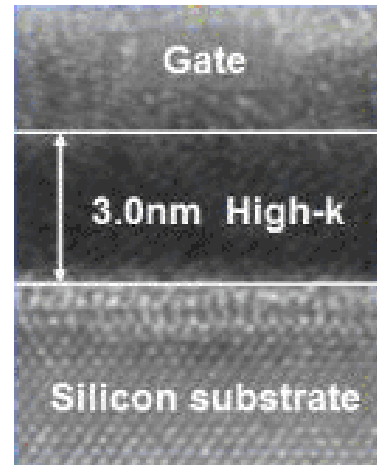
Good News



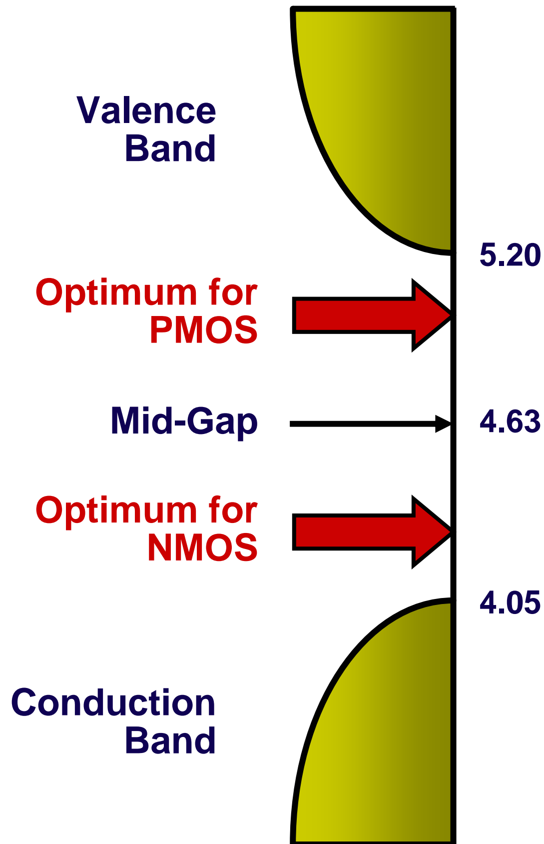


Bad News





Metal Gate

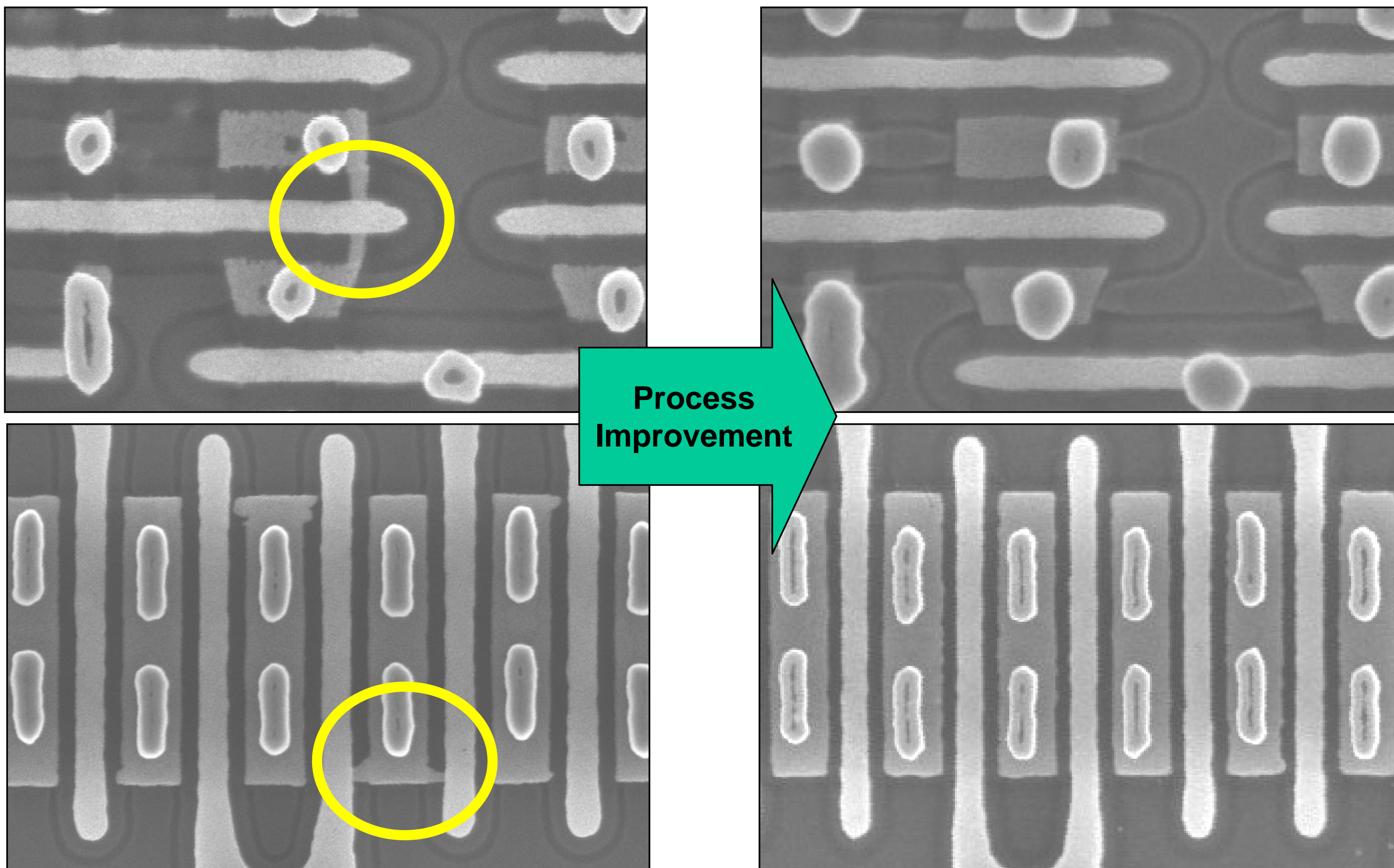


Work Function (eV)

6.0
5.5
5.0
4.5
4.0
3.5
3.0

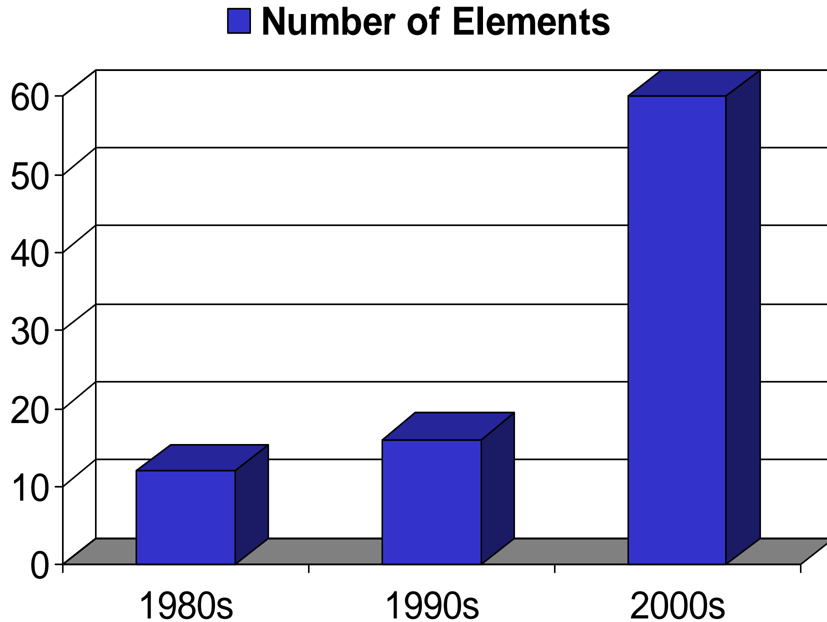
La Hf Ta Zr In Cd Ag Al Nb V Zn Sn Cr W Mo Ru Ti Os Re Rh Ir Pt

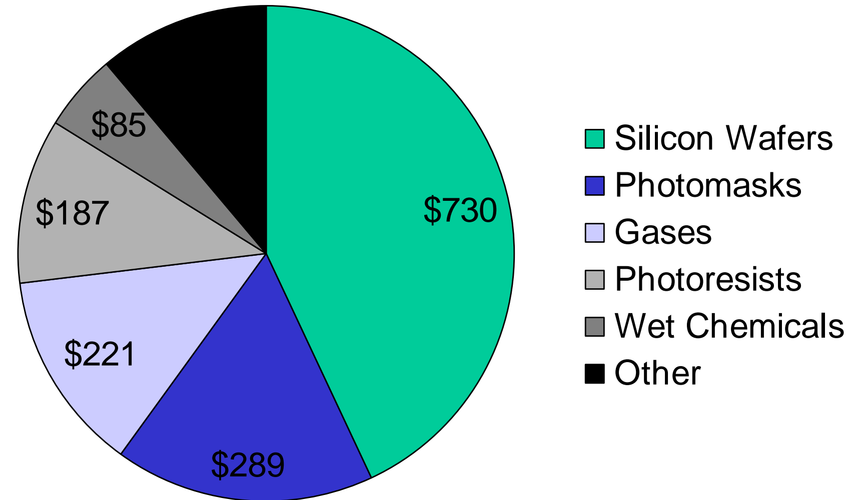
New Silicide: NiSi



Ni moves into the silicon; affected by strain

New Materials and Markets

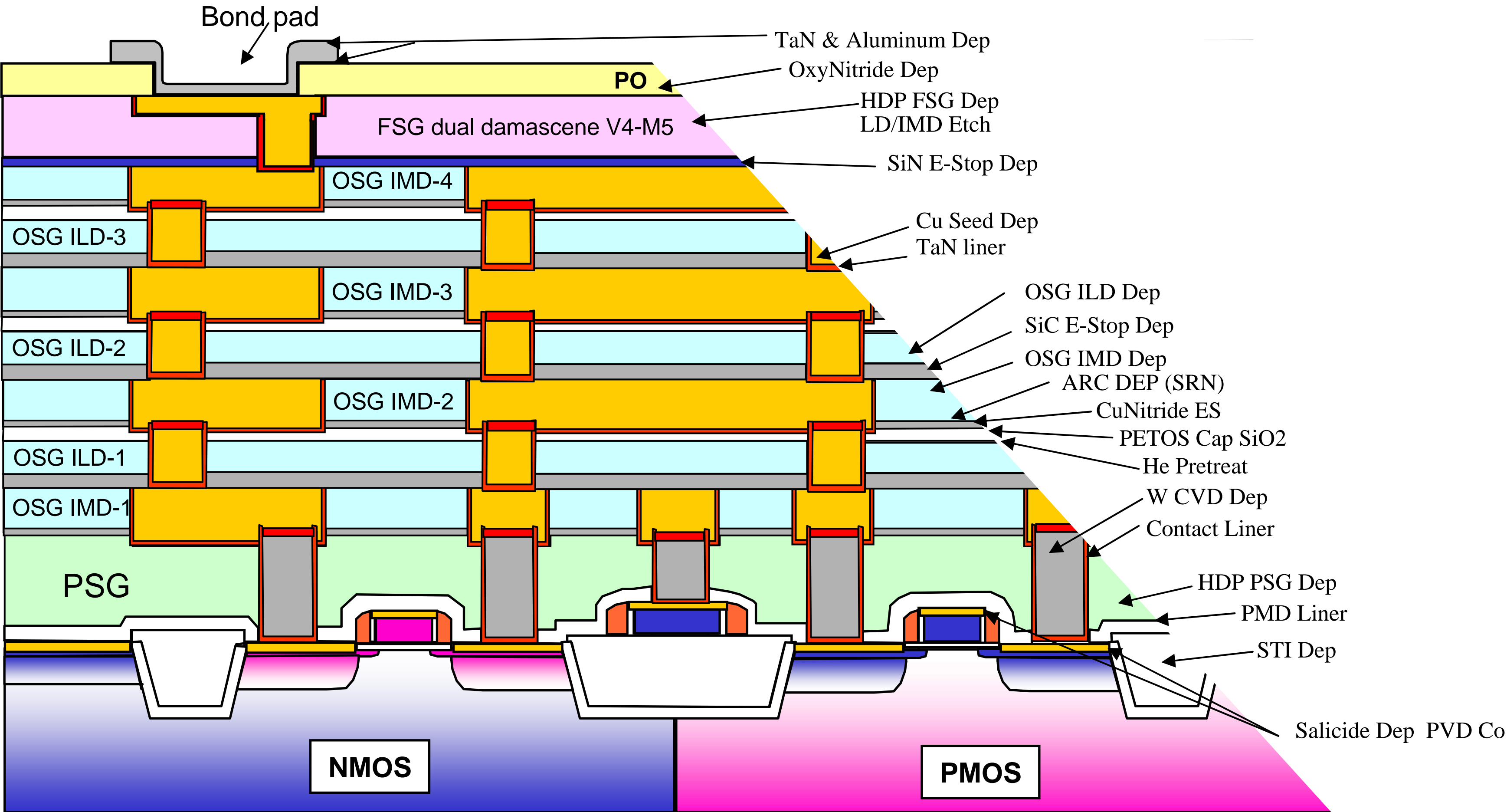




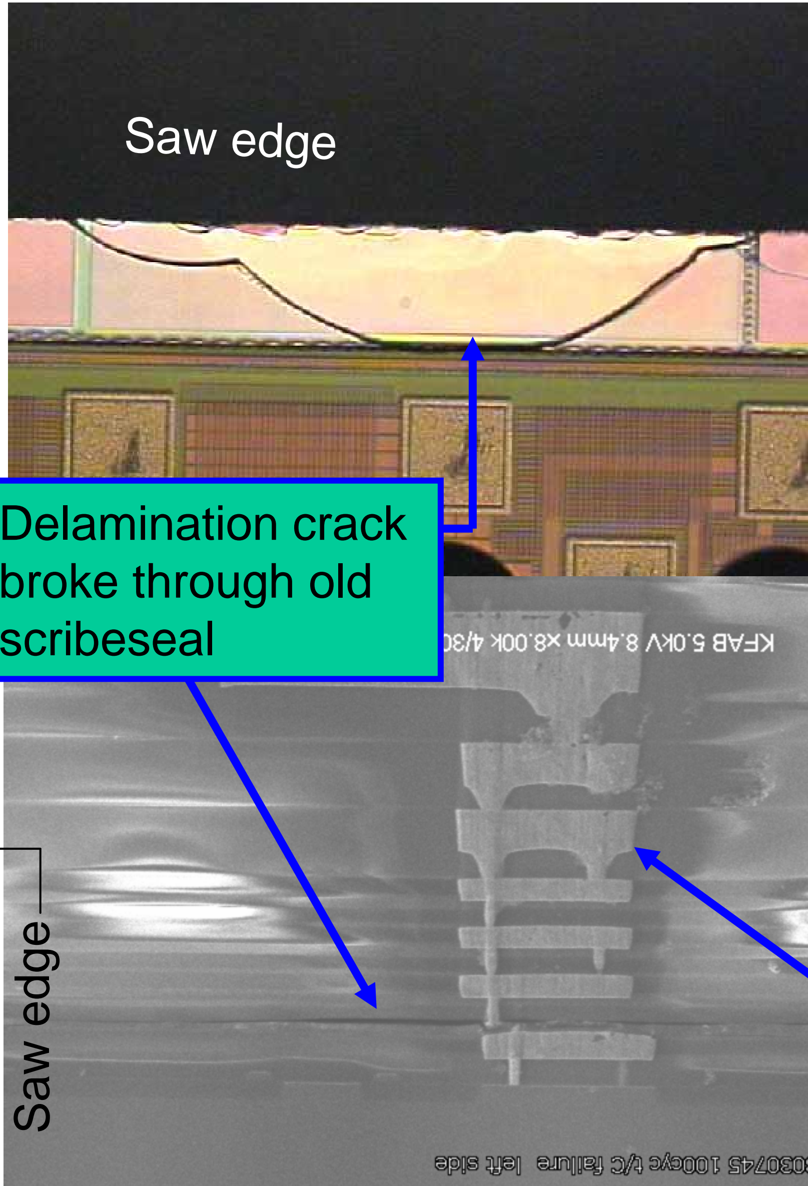
Limited market opportunity for consumables

Sources: SEMI and WaferNews

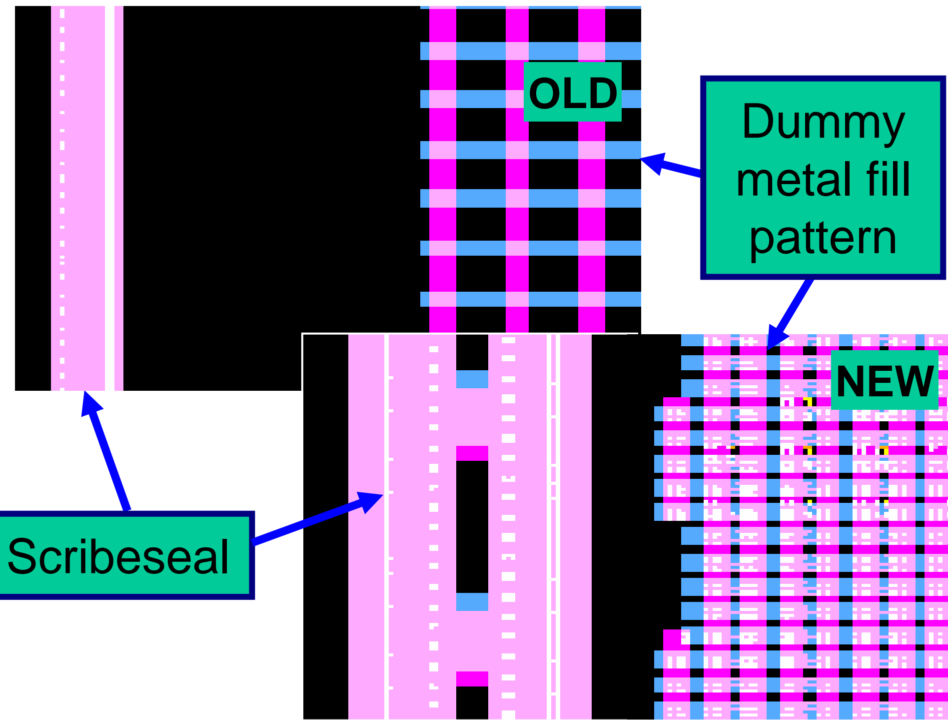
Interconnect Integration



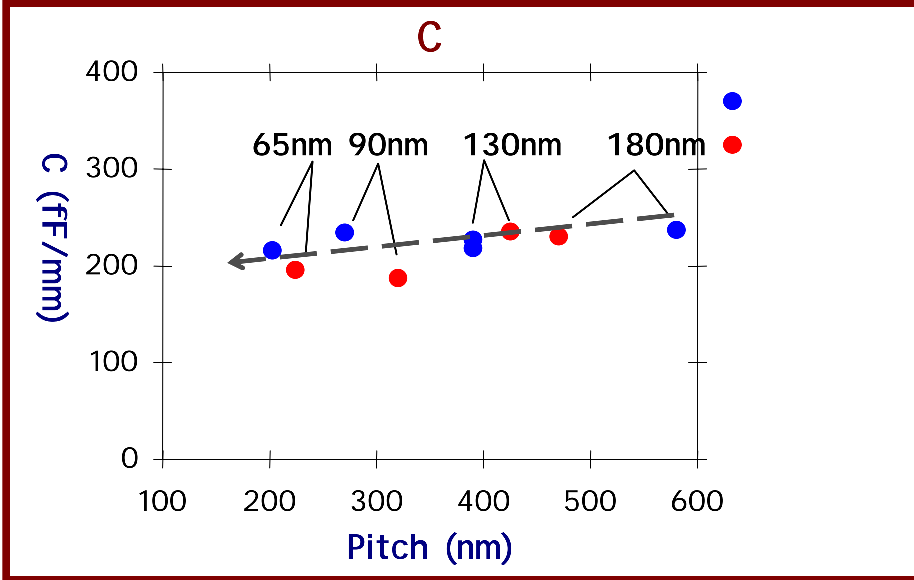
Low k Dielectric Cracking

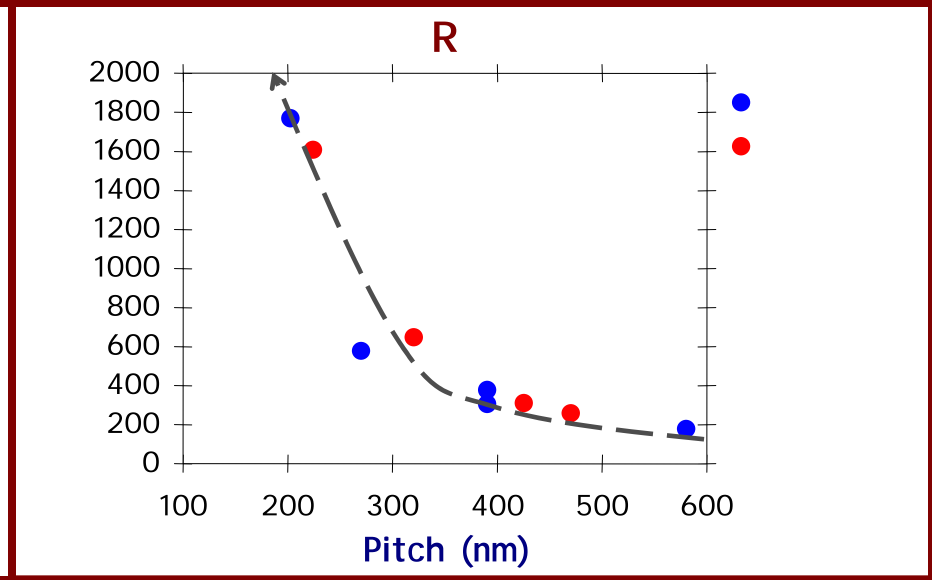


- Crack propagation from die saw edge into the die
- Interface engineering
- Optimization of dummy fill structures

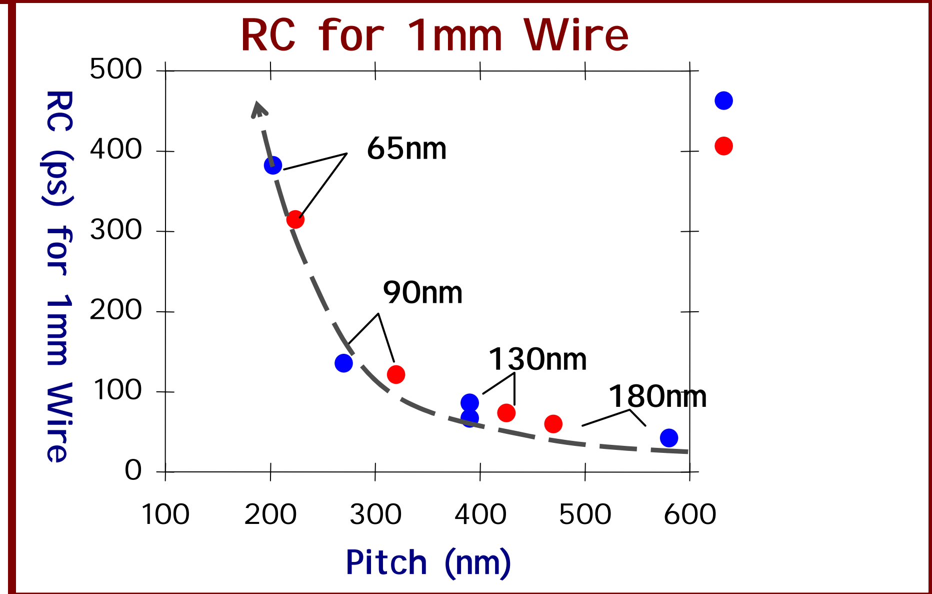


Interconnect RC trends

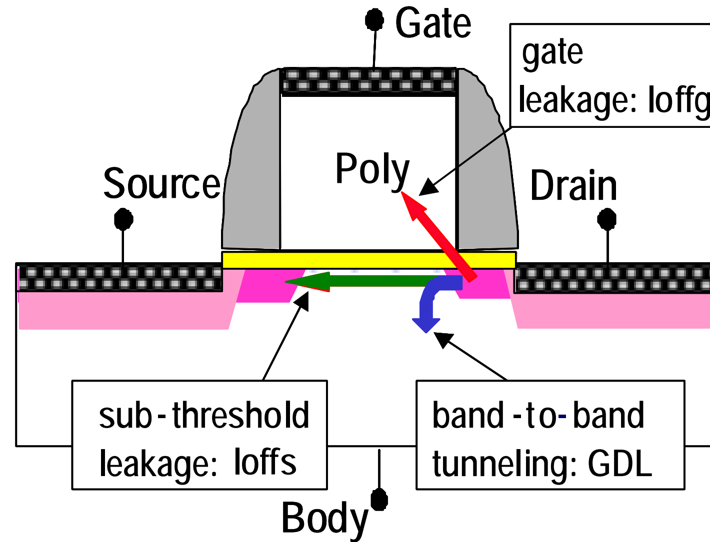




- Capacitance continues to decrease linearly
- Resistance is increasing on a steep exponential for minimum pitch lines due to boundary scattering
- For fixed pitch line lengths (1000x) R increase swamps C decrease node-to-node

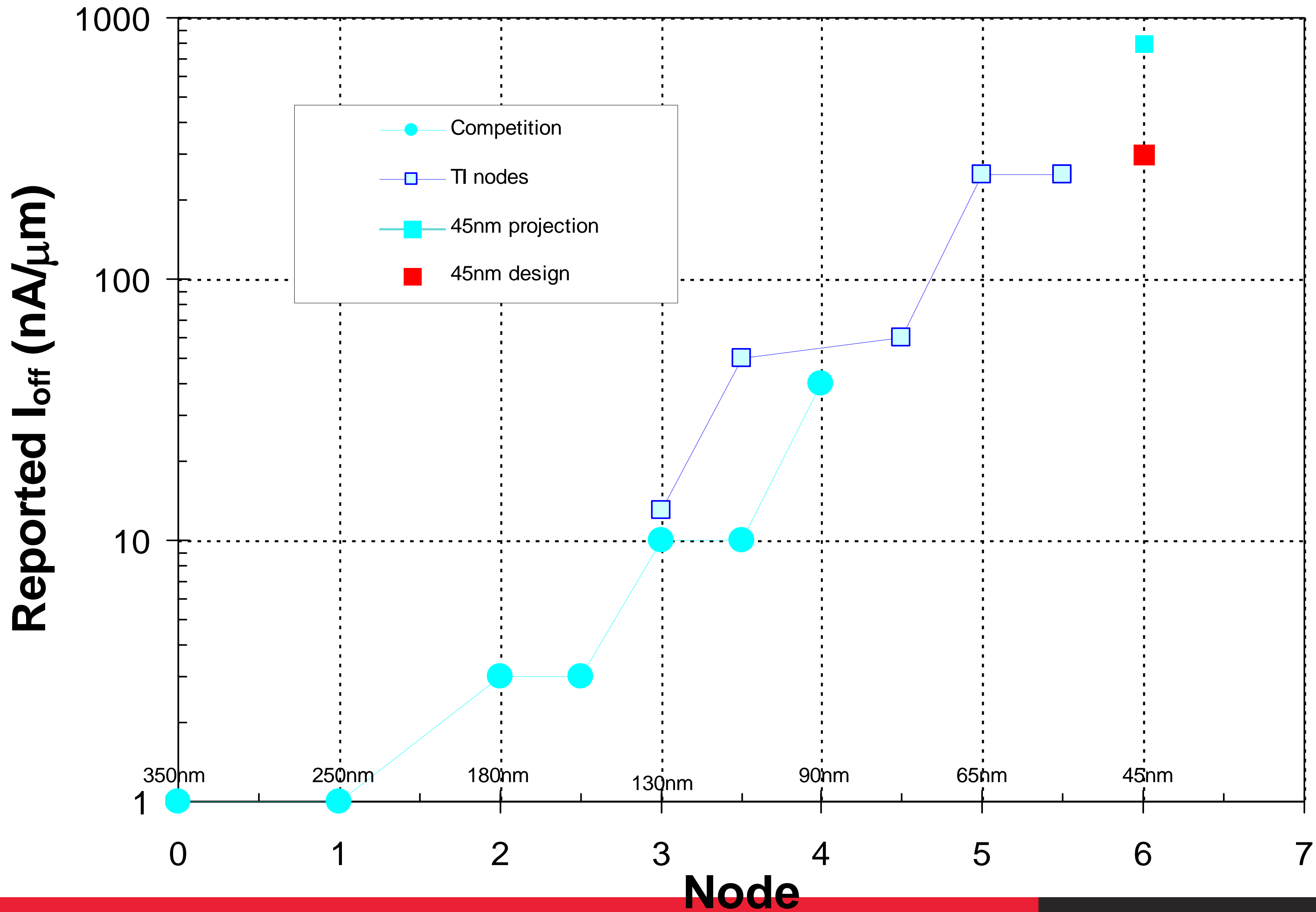


From Switch to Dimmer



1) Subthreshold Leakage – traditional component
   - Shorter channel lengths
   - Higher channel doping
   - Threshold Voltage not scaling as fast as Vdd
2) Gate Oxide Leakage or Tunneling Current
   - As oxide thins, leakage increases exponentially
3) Gate Induced Diode Leakage (GIDL)
   - Band to band tunneling
   - Shallow junctions
   - Higher doping of Source & Drain

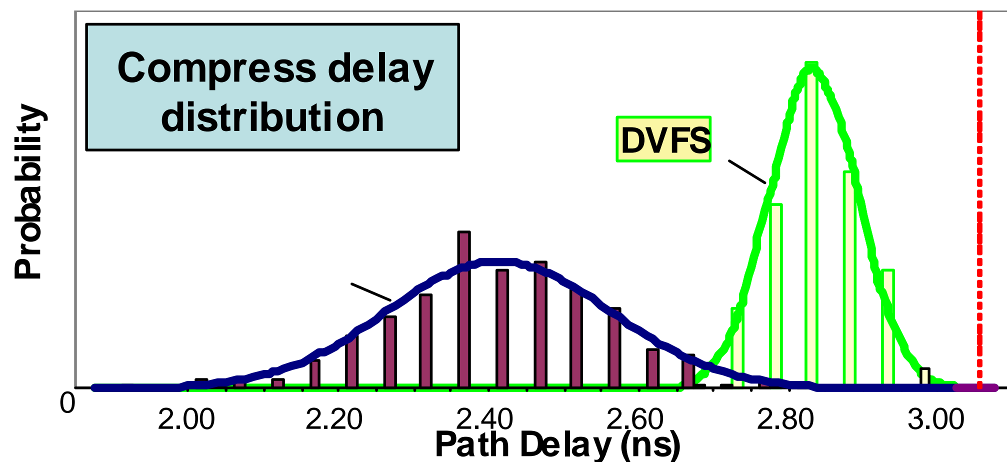
Off-Current vs Node

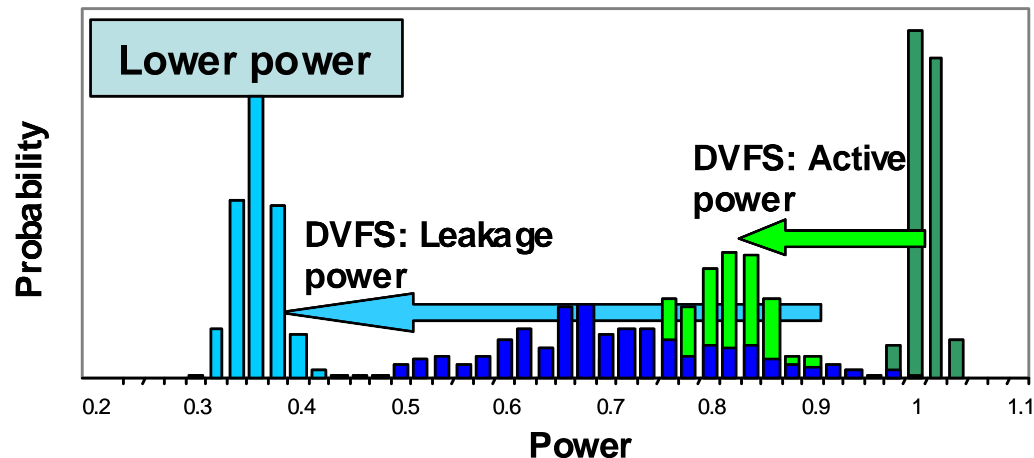


Product Power Management

Power Management Strategies:

- ***Dynamic Voltage & Frequency Scaling***
- **Multiple Voltage Domains**
- **Multiple Vt Libraries**
- **Sleep modes**
- **Drowsy modes**
- **Substrate biasing**
- **Tapered metal routers**
- **Non-orthogonal Place & Route**

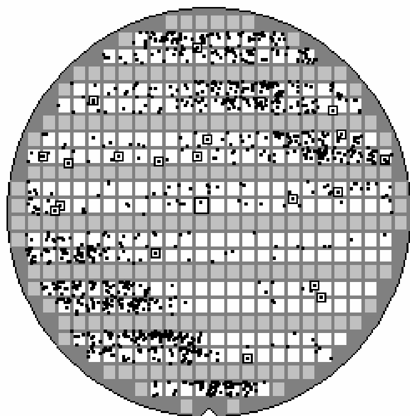


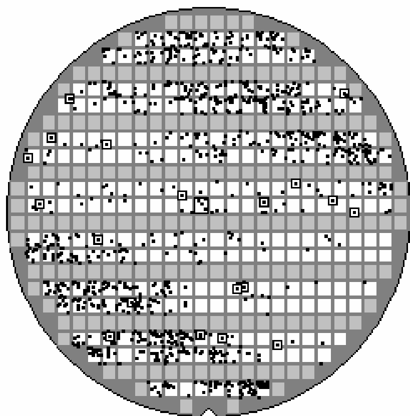


Manufacturing

- The science of manufacturing is finding all the relevant (systematic and random) defects and eliminate them, in parallel
  - Yield is no longer limited by manufacturing: design greatly affects yield -> DFM
- The business of manufacturing is to maximize the scalability of capacity, taking advantage of the upturns and reducing the impact of the downturns
  - Processes and designs have to be portable between fabs

Signal to Noise in Defect Metrology





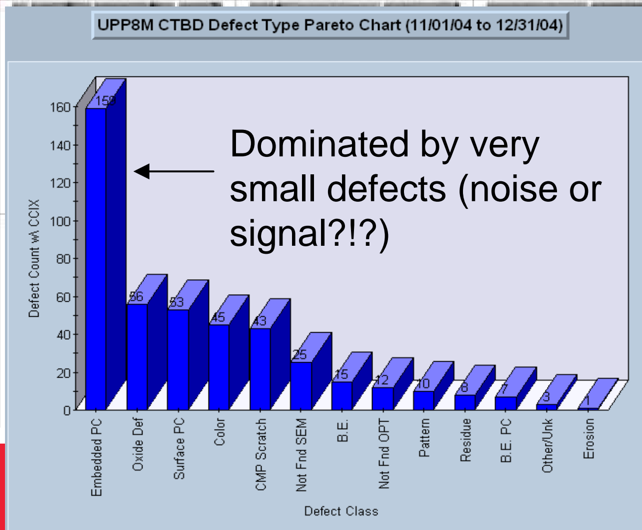
Today's highly sensitive defect metrology finds "everything"

Challenge:

- How do we know which of these defects are Yield killers?

Even Bigger Challenge:

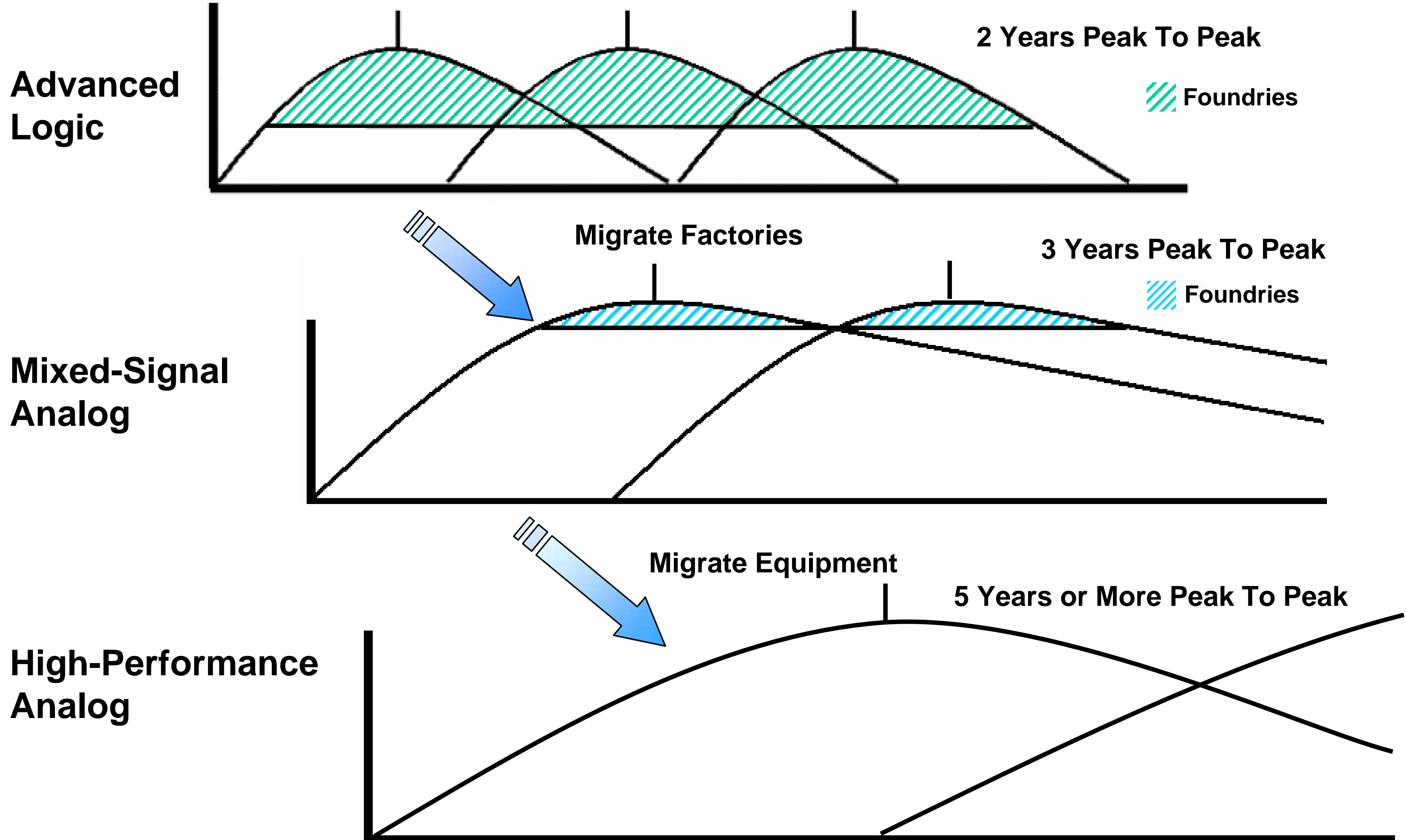
- How do we know which of these defects are reliability issues?



Statistics Of
Whole Data Set
Current Node

Lots : 23
Wafers with Defects : 46
Inspections : 23
Inspected Wafers : 46
Inspectors : 2
Steps : 1
Scan Tools : XD17K, XD16
Defects : 346026
Inspected Area(SqCm) : 10164.987
Inspection Time From : 11/01/04 14:
Inspection Time To : 12/31/04 03:

Improving ROIC



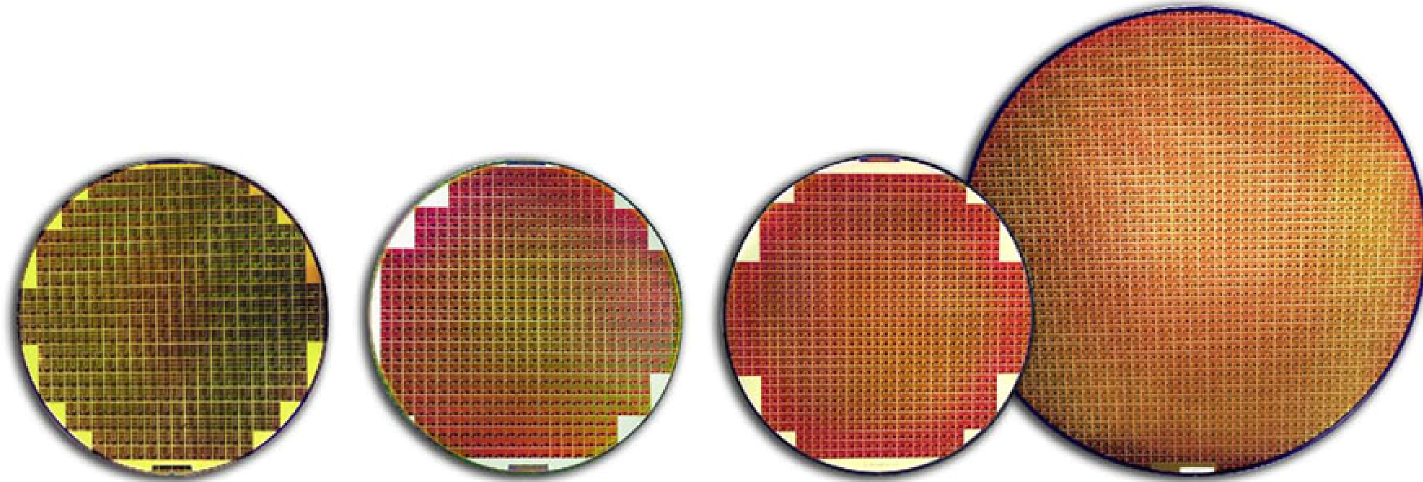
Sub 100nm CMOS is Different

- Many new materials and processes to keep the physics going
  - Cu, Low-k, NiSi, SiGe, HfSiON, FUSI, etc
  - Immersion litho, millisecond annealing, constant angle implant, strain engineering, etc.
- Leakage has reached the ceiling
  - Easiest way to increase current drive
  - Several new components: gate dielectric & junction tunneling
- Interconnect not scaling
  - Makes up half the delay in a critical path
  - Capacitance is materials and integration limited
  - Resistivity increasing for narrow lines
- Increased variances; design for manufacturing
  - Doping fluctuations, supply-threshold voltage reduction, interconnect R&C
  - Physical design affects process yield
- Product requirements go beyond digital
  - High voltage I/O, mixed signal, analog, RF integration, non-volatile memory

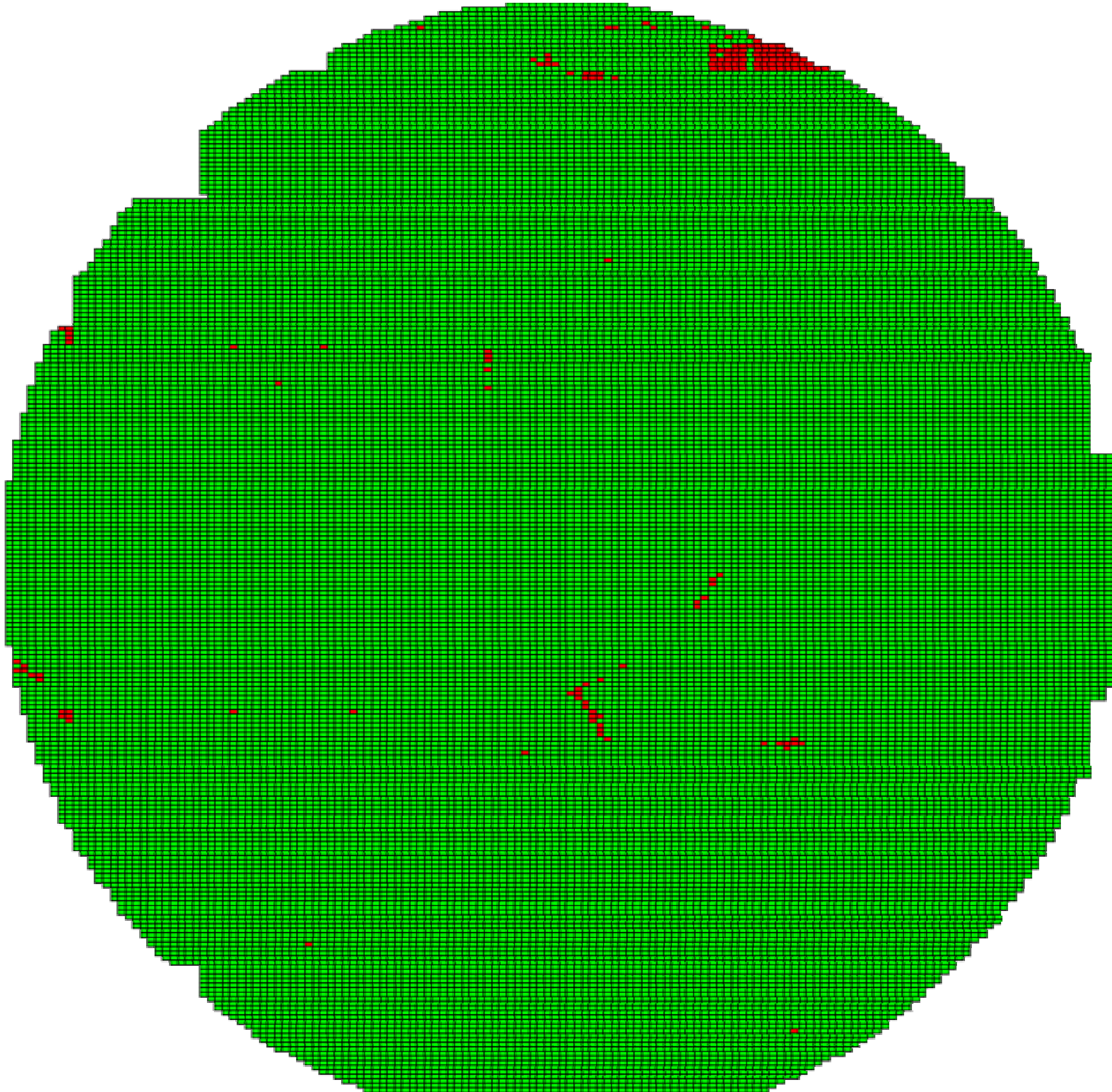
Summary

- The major challenges to sustain CMOS scaling are
  - Economics/Complexity of new materials and processes
  - Cost/Complexity of physical design
- Product Innovation will be enhanced by
  - Analog, RF, High Voltage integration
  - Package contributions
  - Architecture differentiation

Technolog Scaling



Advanced 200mm Analog



HPA07
High Performance
OP AMP
.25 Pitch
29000 Chips/Wafer

99% Yield