

Solid-State Fingerprint Scanners

A Survey of Technologies

Philip D. Wasserman

Guest Researcher, NIST, Gaithersburg MD

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Objectives

- Review solid state fingerprint scanner technologies
 - Emphasize forensic requirements
 - Present emerging, as well currently available technologies
- Discuss the future of solid-state fingerprint scanners

Solid-State Fingerprint Scanner Technologies

- A live-scan fingerprint scanner measures some physical property of a fingerprint and converts it to a digitized ridge-valley image
- Many technologies have been applied. A few (with a representative vendor) include the following.
 - Capacitance (UPEK)
 - RF (Authentec)
 - Thermal (Atmel)
 - PiezoResistive (Fidelica)
 - Ultrasonic (Ultrascan)
 - Piezoelectric (Fraunhofer with Crossmatch)
 - MEMS

Scanner Configurations

➤ Sweep scanner

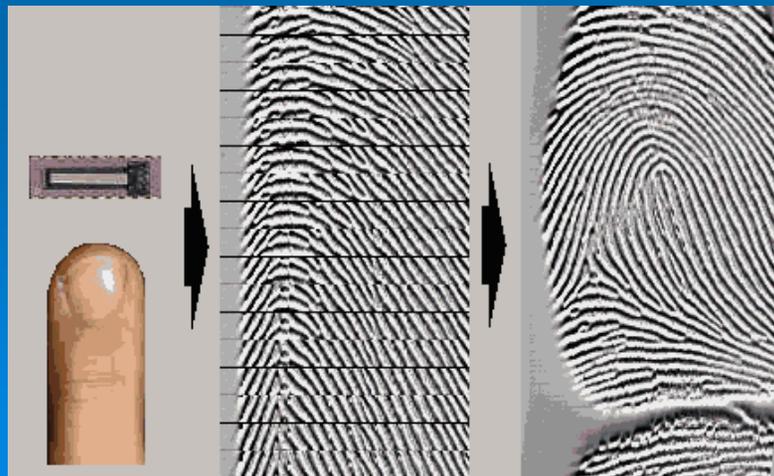
- User sweeps finger across a narrow row of sensors.

➤ Area scanner

- Contains an array of sensors which substantially cover the user's fingerprint
- Cost is higher than "sweep" scanners due to larger sensor area.

Sweep Scanners

- Single row (or a few rows) of sensor elements; low cost, size, and power. Intended for cell-phone, PDA and laptop computer security.
- User sweeps finger across line of sensors; fingerprint is stitched together in software
- Speed and direction of sweep must be within limits
 - Naïve user may not produce usable prints
- **Software stitching process may produce artifacts**
 - **which are unacceptable in forensic quality fingerprints**



Area Scanners

- Captures one or more fingerprints from a single impression.
 - Usually flat, but rolled impressions can be simulated by stitching multiple images in software.
- Image size must be sufficient to satisfy comparison accuracy requirements.

Fingerprint Size

- The NIST study NISTIR 7201, *Effect of Image Size and Compression on One-to-One Fingerprint Matching* concludes:
 - “...*image cropping quickly degrades matcher performance*”
 - “*The conclusion from this study is that Image sizes below 320 pixels by 320 pixels should not be used.*”
- Relating to PIV requirements, **NIST Special Publication 800-76, section 4.1** states: “The device shall be capable of imaging an area of at least 16.5 mm in both the horizontal and vertical directions.
- No commercially available single-finger solid state scanner meets these image size requirements.
 - Upek TCS1CD is the largest; 256 x 360 pixels at 508 dpi

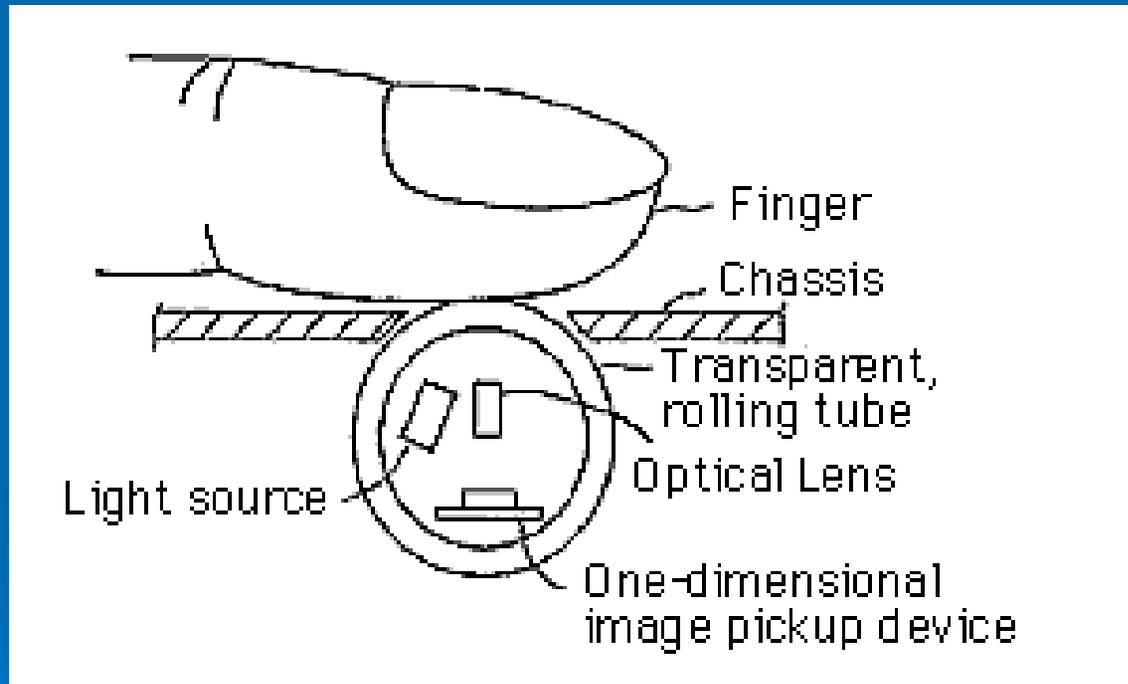
3.2" x 3" Silicon Fingerprint Scanner is Technically possible

- Silicon CCD scanners as large as 4.24" x 3.38" have been produced.
 - Cost is now high
 - Historically, demand and technology have rapidly and dramatically reduced integrated circuit costs
- No commercially available solid state scanner meets the 3.2" x 3" size requirement for multi-finger scanners
 - *Homeland Security 10-Print Capture User Group Scanner & Software Requirements Version 0.9 – DRAFT – September 29, 2005*

Single-Finger Solid State Scanners

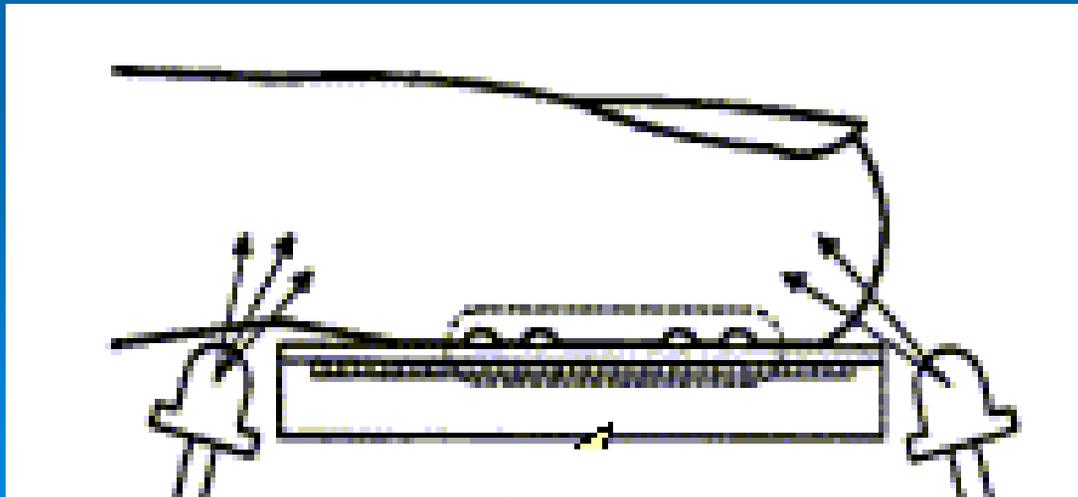
- All solid-state scanner products now available are of the single-finger type
 - Targeted market is cell phones, PDAs, personal computers, access control, ...

Optical Rolling-Tube Scanner (Mitsumi)



Direct Optical Scanner (NEC)

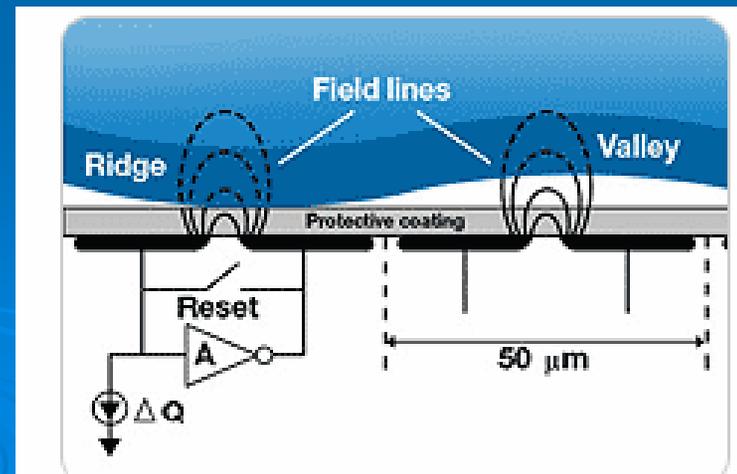
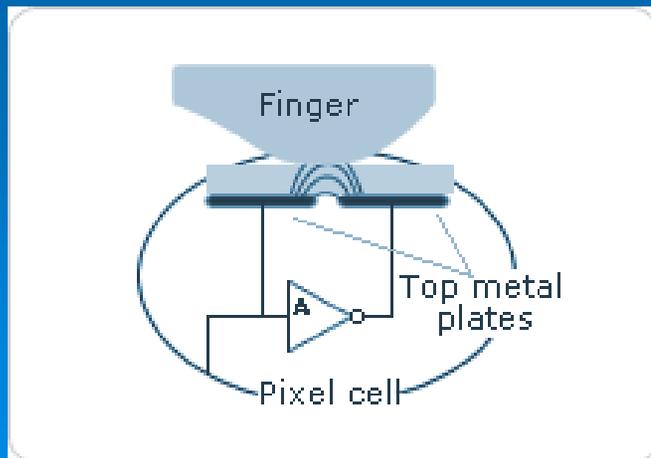
- The finger interior is illuminated from LEDs around its periphery
- A fiber-optic light guide couples the image to a CMOS camera the size of the finger.
- Mitsumi proposes the same technology in a sweep scanner.



Active Capacitive Scanners (UPEK)

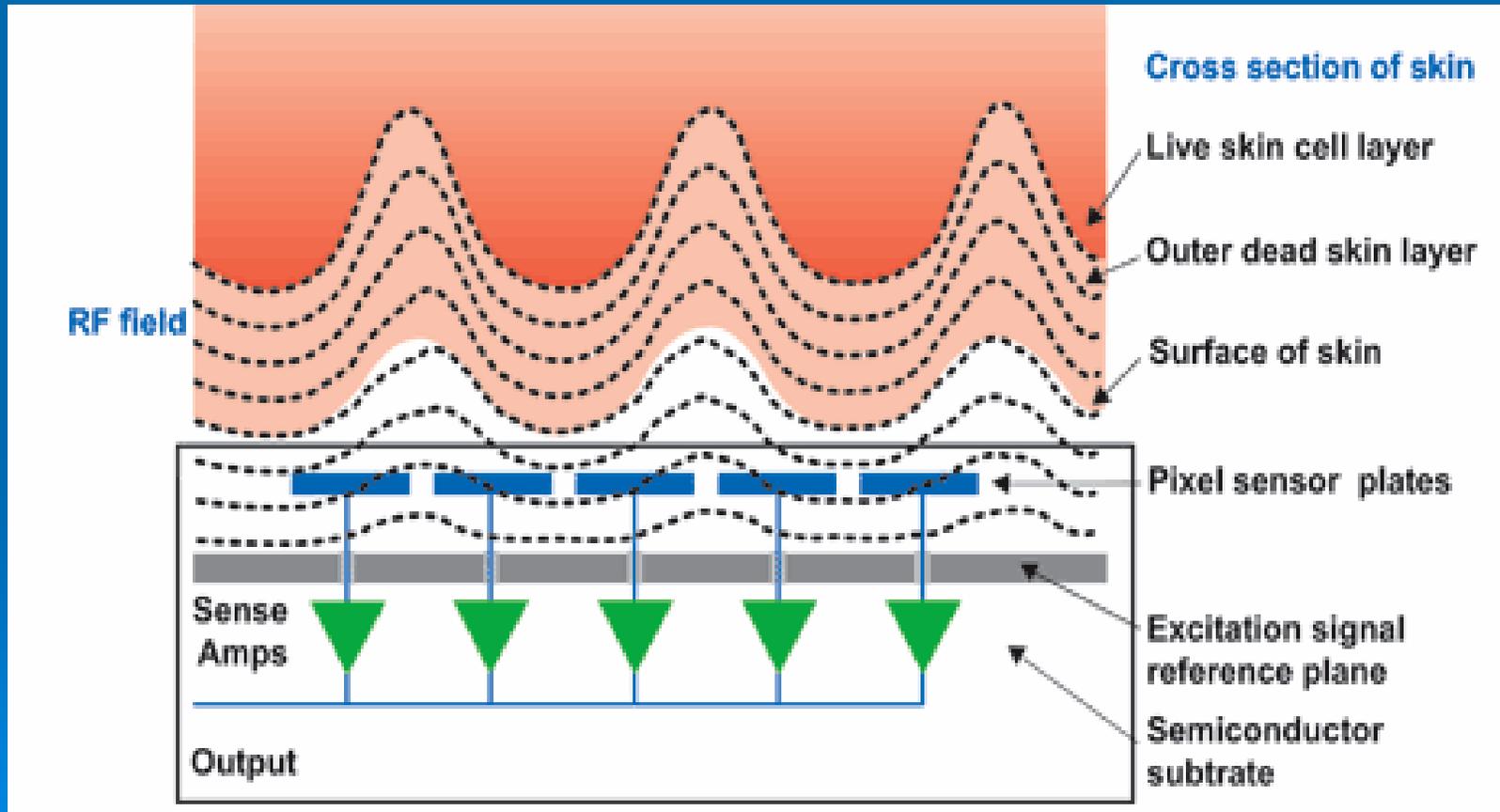
US Patent 5,973,623 (Assigned to STM)

- Each sensor cell (pixel) contains an active capacitive feedback circuit whose effective capacitance is decreased by the presence of live skin close to the surface of the scanner.
 - A ridge intercepts fringing field lines between plates, thereby reducing the capacitance between them.
- The amplifier operates as an integrator
 - Reset during phase 1 by shorting feedback capacitor
 - During phase 2, integrator receives a fixed increment of charge ΔQ
 - This produces an output voltage $E = \Delta Q / C_f$, where C_f is the capacitance between top metal plates, as determined by skin proximity (ridge or valley).



RF Scanners (Authentec)

- Sensor amps respond to RF coupled through capacitance from finger to the sensor plate



Non-Linearity of Solid State Scanners

- Many solid state sensor technologies have a non-linear response to the fingerprint property being measured.
- Capacitive sensors respond to finger-sensor capacitance, a non-linear function of finger-sensor distance.

Thermal Sensors (Atmel)

- Measures the temperature difference between ridge and valley.
 - Temperature difference is transitory (lasts approx. 100ms)
- Consists of a silicon die tiled by pixels of pyro-electric material sensitive to temperature differences.
- The temperature difference appearing at the pyro-electric layer is transformed into electrical charges. These are amplified and measured by the underlying silicon circuitry
- Only four bit gray scale from sensor

Pressure Scanners

- Piezo-electric Fraunhofer IKTS (Crossmatch)
 - From Fraunhofer web site: “Realization of 1-3 piezocomposites with ca. 25,000 individual elements (diameter: 75 μm , pitch: 103 μm , height: 280 μm) and demonstration of applicability in fingerprint scanners (Cross Match and FI)”
- U.S. Patents (Assigned to Cross Match)
 - 6,720,712 Scott , et al. April 13, 2004
 - 6,812,621 Scott November 2, 2004
 - 6,844,660 Scott January 18, 2005

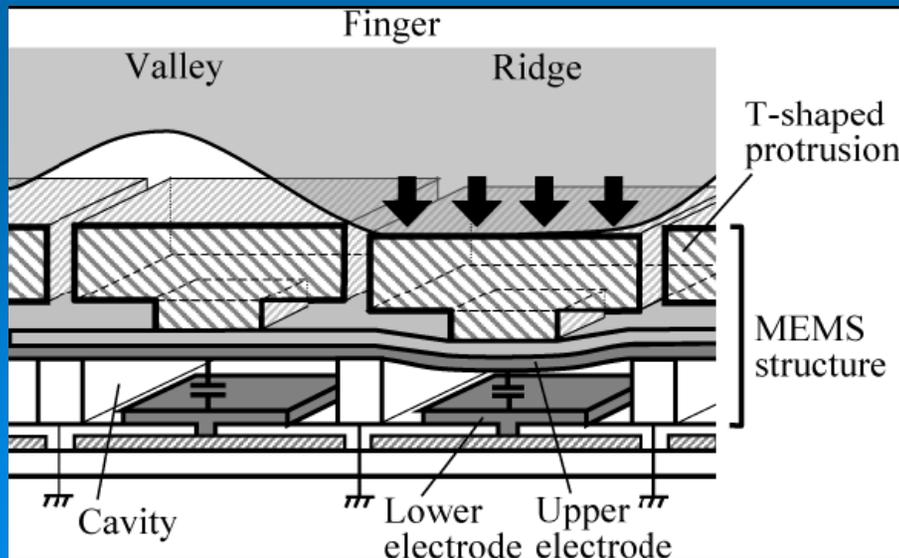
Micro-electro-mechanical Systems (MEMS)

- MEMS are mechanical devices such as sensors, embedded in semiconductor chips.
 - Integrated circuits with moving parts.
- Low potential cost due to semiconductor mass processing methods.
- A variety of technologies used to produce arrays of MEMS for fingerprint sensors
 - pressure sensitive contacts
 - variable capacitance
 - piezoelectric
 - piezoresistive
 - pyroelectric (thermal)

MEMS Capacitive Fingerprint Sensor

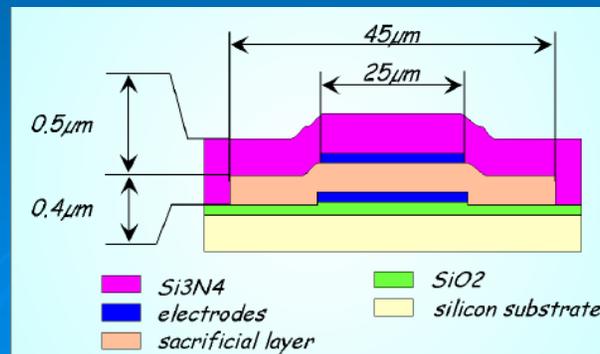
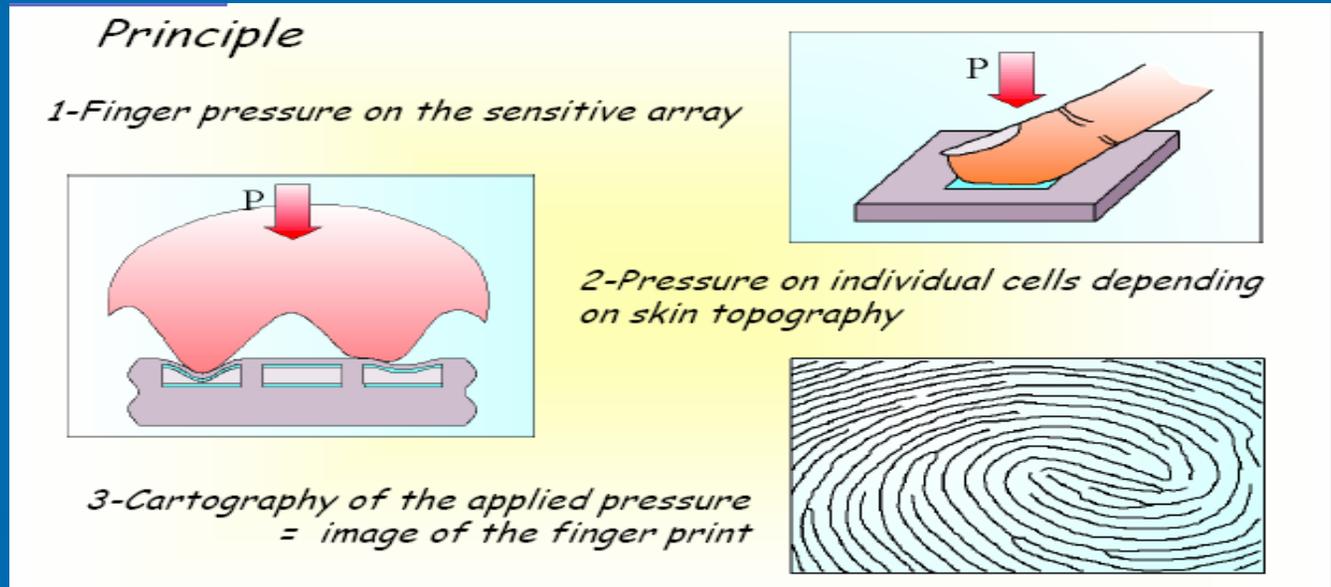
<http://mtlweb.mit.edu/researchgroups/mems-salon/Sato-%20Surface%20structure%20and%20fabrication%20for%20MEMS%20fingerprinting%20sensor.pdf>

Experimental sensor has an array of 57 000 pixels 50- μ m in the area of 11.2 12.8 mm . Each pixel is a capacitive pressure sensor that has a MEMS cavity structure stacked on a CMOS LSI. A sensing circuit is located just below each MEMS cavity structure



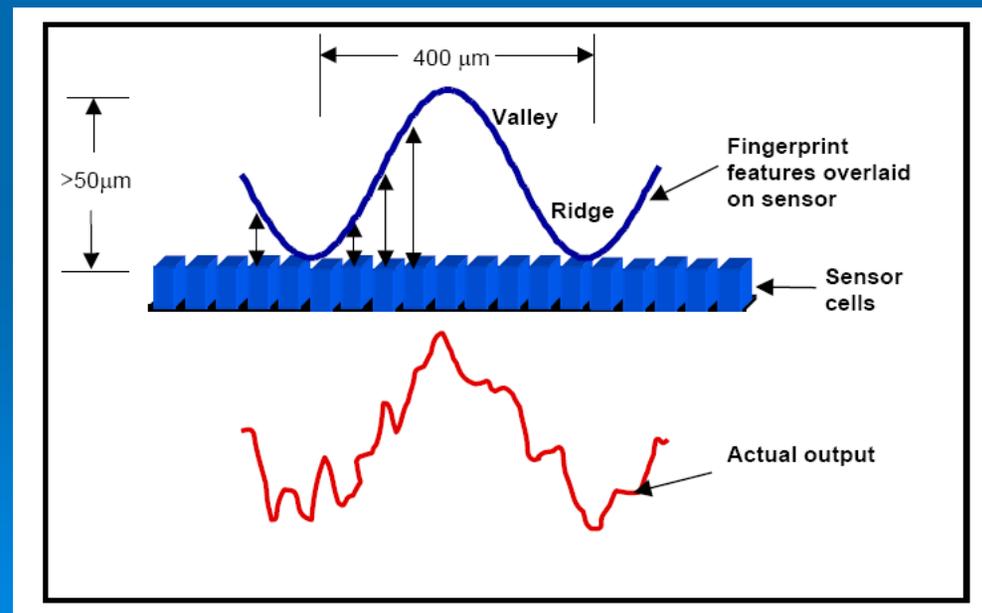
MEMS Capacitive Pressure Sensor On Silicon (LITI)

<http://www-leti.cea.fr/commun/AR-2002/09-mems%20%26%20microsensors/09-3-rey.pdf>



MEMS Resistive Sensor Fidelica

- A resistive network and MEMS structure at each cell location.
- Upon the application of a fingerprint, the structures under the ridges of the fingerprint experience a deflection, producing a resistance change



No Fully Acceptable Solution for Four-Finger Live Scan

- As stated in *Homeland Security 10-Print Capture User Group Scanner & Software Requirements Version 0.9 – DRAFT – September 29, 2005*
- “The size of the Scanner, power requirements, and speed of both the Software and Scanner will have critical impacts on current facilities and operations. Although **we are not aware of any technology existing today that is able to meet these parameters ...**”
- Solid-state scanners provide the potential for satisfying these requirements

Can Multiple Smaller Scanner Chips be Tiled to Simulate a Larger One?

Proposed by Michael Garris, NIST

- Costs could be reduced if a multi-finger scanner could be implemented as a tiled array of small fingerprint scanner chips
- There will be gaps between chips therefore, insensitive regions will exist.
- The gaps can be filled by shifting the sensor array in X and Y
 - Capture three images
 - Combine them in software
- While retaining sensitivity, It is possible to cover a capacitive sensor array with a thin layer of plastic, preferably Teflon, to reduce the coefficient of friction.
 - US Patent # 6,512,381B2

Shifting the Sensor Array

- Capture a fingerprint image at a initial location,
- Shift sensor array in X so image covers the X gap. Capture a second image.
- Returning array to original position in X, shift in Y. Capture a third image.
- Piezoelectric or magnetic actuators could be used to move the sensor array.
- There are many questions about this approach.
 - Can the sensors be made to slide smoothly under the plastic cover despite the finger pressure on top?
 - Would the plastic cover excessively reduce sensitivity or resolution of the image?
 - Can the scanner be made durable?
 - Research will be required to answer these and other questions.

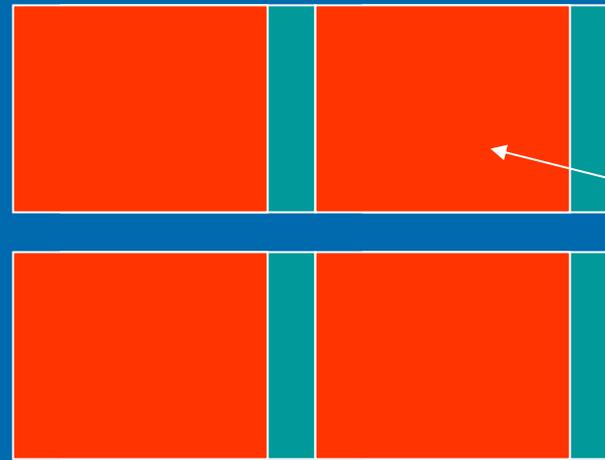
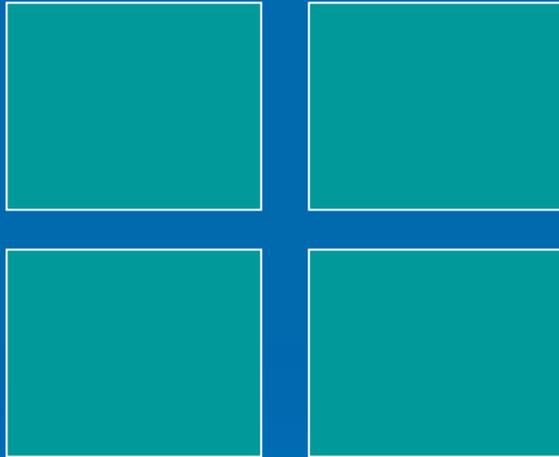
Connecting Multiple Scanner Chips

- The top surface or the array of scanner chips must be planer and smooth if the cover is to slide easily.
 - Common lead bonding could not be used.
- Flip-chip techniques to connect the front-side circuitry to the substrate will allow the chips to be placed more closely, reducing the required shift.
- Through-hole vias can connect the circuitry on the front of the chip to capacitive sensing plates on the back.

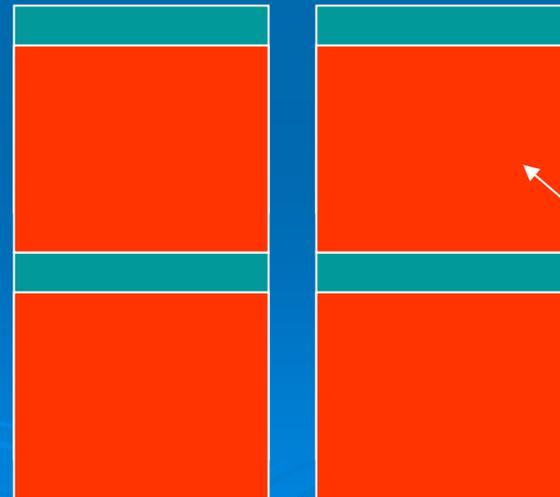
<http://retina.et.tudelft.nl/data/artwork/publication/mems/520763576.pdf>

Array Shifts To Cover Gaps

Starting Position

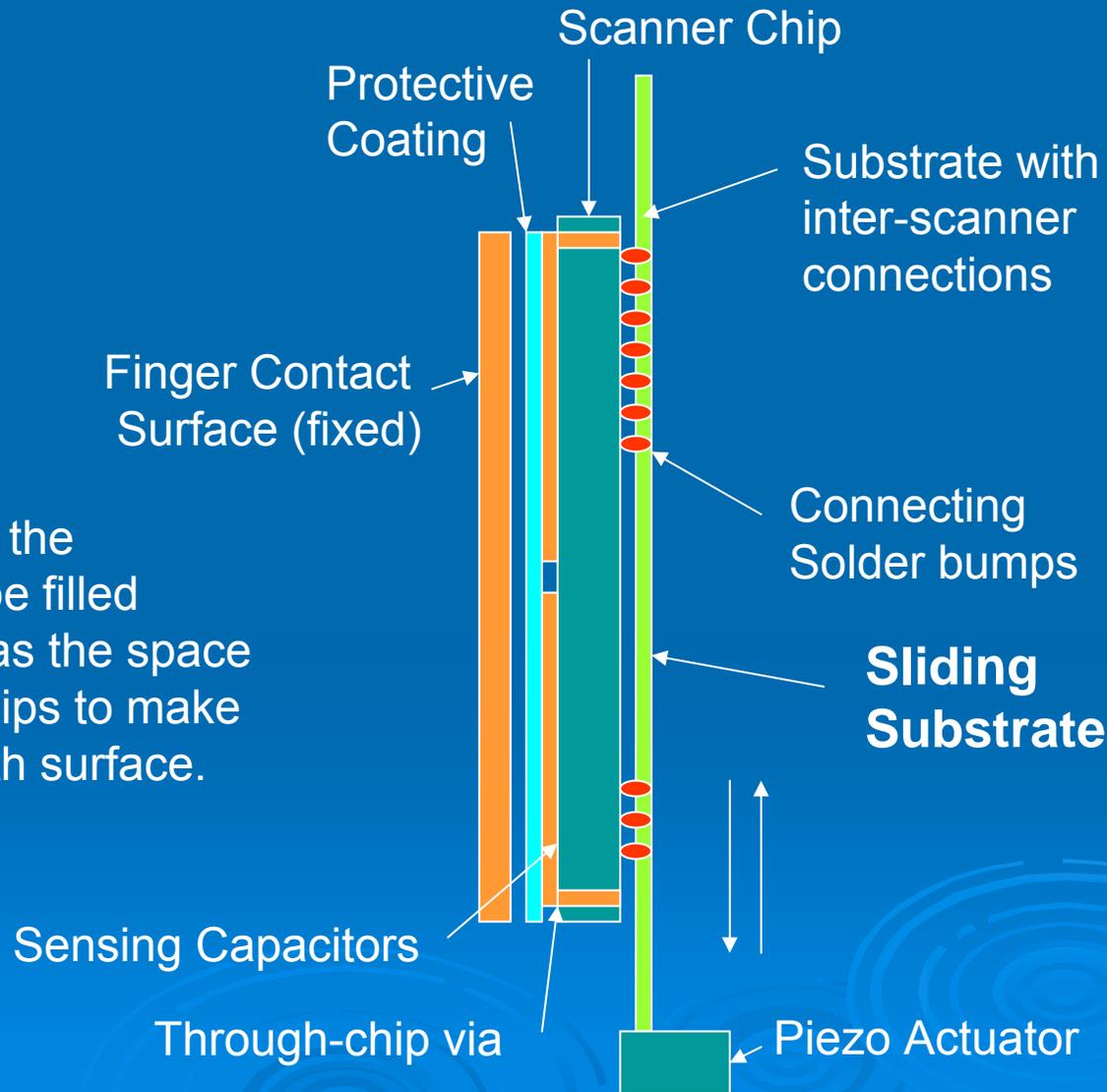


Shifted in X



Shifted in Y

Flip-Chip Structure



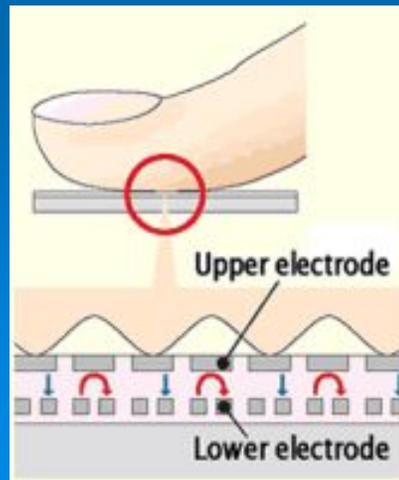
The region between the solder bumps may be filled with epoxy. as well as the space between scanner chips to make a fully planar, smooth surface.

Flat Panel Display Technology

- Large feature size and substrate suggests flat panel display technology.
 - Flat panel displays are now above 50" diagonal
 - Greatly reduced cost per square inch for glass compared to silicon.
 - Highly refined manufacturing process
- Thin-film photo-detectors on glass.
 - Could be capacitive for fingerprint sensor.
- Organic photo-detectors printed on plastic (Nanoident)

Capacitive Sensor With TFT Flat Panel Technology (Mitsubishi)

- Flat panel thin-film transistor technology on glass rather than single-crystal silicon
- Potential for low cost, large area scanners
- Still in laboratory stage
- A Capacitive Fingerprint Sensor with Low-Temperature Poly-Si TFTs
http://ieeexplore.ieee.org/xpl/abs_free.jsp?arNumber=1175508



Firms Developing Thin-Film Transistor Fingerprint Sensors on Glass Substrates

- Casio
- SiliconImageWorks
- Silicon Display Technology
- Alps Electric
- Mitsubishi

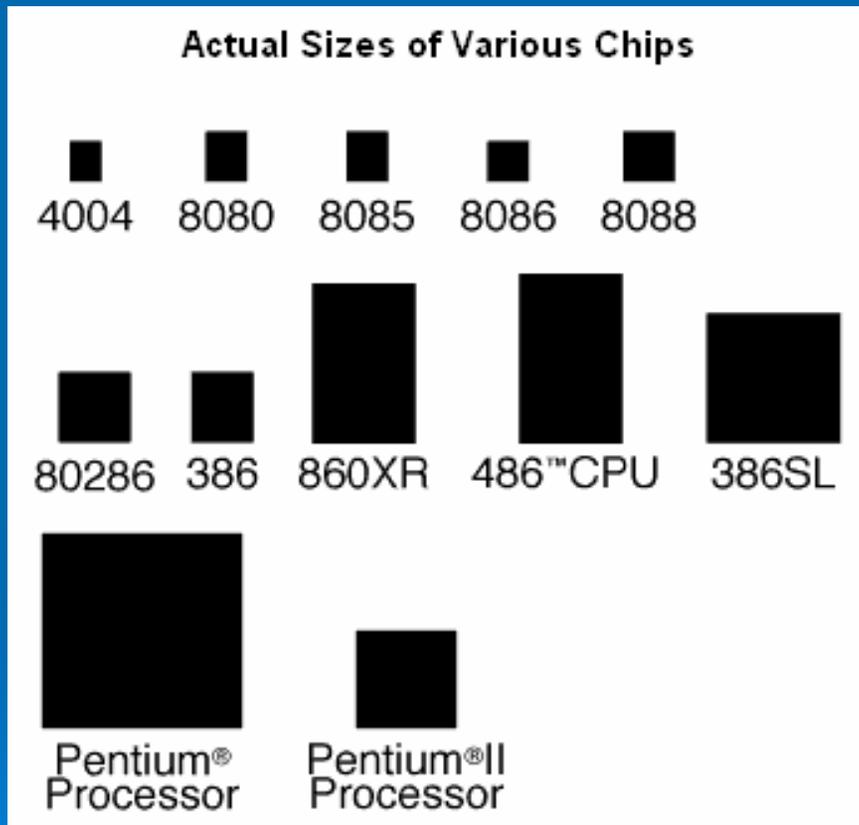
Silicon Integrated Circuit Die Size

- As a semiconductor chip becomes larger, yield goes down due to the defect density.
- Costs go up exponentially above a critical die size.
- This critical die size has been increasing steadily
 - Improved manufacturing processes have reduced defect density.
- Increased complexity has become possible because of increased die size, and reduced feature size.

Silicon Integrated Circuits and Moore's Law

- In the mid-1960s, Intel co-founder Gordon Moore noticed that, largely as a result of **feature size shrinkage**, chip processing power was roughly doubling every 18 months, with a concurrent reduction in cost.
- He extrapolated this trend in what proved to be a remarkably accurate estimate of semiconductor industry progress. The so-called “Moore's Law” curve of industry progress is one of the standards of the chip making world,

Silicon Chip Size and Complexity vs. Time (source INTEL)



Year	Processor name	Transistor count	Minimum feature size
1971	4004	2300	10 micron
1972	8008	3500	10 micron
1974	8080	6000	6 micron
1976	8085	6500	3 micron
1978	8086	29000	3 micron
1982	80286	134,000	1.5 micron
1985	80386	275,000	1.5 micron
1989	Intel486	1.2 million	1 micron
1993	Pentium	3.1 million	800 nanometer
1997	Pentium II	7.5 million	350 nanometer
1999 (Feb.)	Pentium III	9.5 million	250 nanometer
1999 (Oct.)	Pentium III	28 million	180 nanometer

Roadmap, Semiconductor Industry Association, 2004

Semiconductor Industry Association Roadmap (1993)							
		1992	1995	1998	2001	2004	2007
Feature size (μm)		0.5	0.35	0.25	0.18	0.12	0.1
Bits/Chip	DRAM	16M	64M	256M	1G	4G	16G
	SRAM	4M	16M	64M	256M	1G	4G
Chip size (mm^2)	Logic / microprocessor	250	400	600	800	1000	1250
	DRAM	132	200	320	500	700	1000
Performance (MHz)	on chip	120	200	350	500	700	1000
	off chip	60	100	175	250	350	500
Maximum power (W/chip)	high performance	10	15	30	40	40-120	40-200
	portable	3	4	4	4	4	4
Power supply voltage (V)	desktop	5	3.3	2.2	2.2	1.5	1.5
	portable	3.3	2.2	2.2	1.5	1.5	1.5
No. of interconnect levels - logic		3	4.5	5	5-6	6	6-7
Number of I/Os		500	750	1500	2000	3500	5000
Wafer processing cost ($\\$/\text{cm}^2$)		\$4.00	\$3.90	\$3.80	\$3.70	\$3.60	\$3.50
Wafer diameter (mm)		200	200	200-400	200-400	200-400	200-400
Defect density (defects/cm^2)		0.1	0.05	0.03	0.01	0.004	0.002

Feasibility of 3.2" x 3.0" Chip (81.3mm x 76.2mm, 6200 mm²)

➤ Cost

- 2004
 - \$ 115
- 2007
 - \$ 112

➤ Chip Size

- **Required chip area is 6200 mm²**
- Maximum chip area according to EIA
 - 1000 mm² now
 - 1250 mm² in 2007
- This has already been exceeded
 - Kodak 1737 mm²
 - Dalsa 4032 mm²
 - **Phillips 9246 mm²**
 -

Large Silicon Integrated Circuits

All CCD (Charge Coupled Device) Image Scanners.
Convertible to capacitive scanners by replacing the photodiodes with capacitor plates.

- 3.2" x 3" Fingerprint Sensor would require **9.6 in²** chip
- Kodak 39 megapixels, 6.8 micron pixel size, 39mm x 50.7mm image area, 1.54" x 2.0", **3.08 in.²**
- DALSA Inc., 26 megapixels, 2.5" x 2.5", **6.25 in²**
- Philips, 66.236 megapixels, 12 micron pixel size, 4.24" x 3.38", **14.36 in.²**
- Pixel Size
 - CCD < 20 micron
 - Fingerprint Sensor at 500dpi, pixel size 50.8 micron

Conclusions

- It is now technically feasible to make a silicon fingerprint scanner 3.2" x 3.0"
 - Current price could be competitive with comparable optical scanners.
 - Can be linear extension of well developed capacitive scanner technology
- Glass substrates and thin-film transistors are another promising technology.
 - Based on flat-panel display technology
 - Substrate and processing costs much lower than for silicon
 - Quality of transistors is poor
 - No commercial product to date

Suppliers of Solid State Fingerprint Scanners (A partial listing)

- Alps Electric
- Atmel
- Atrua
- Authentec
- BMF
- Casio
- Casio + Alps
- Cecrop, KSI, Sannaedle
- Delsy
- Digital Persona
- Ethentica
- Fidelica
- Fingerprint Cards
- Fujitsu
- Idex
- Infineon (Siemens, discontinued)
- Melfas
- Mitsumi
- NEC
- NTT
- Nanoident
- Silicon Display Technology
- Sony
- Symwave
- TesTech
- TST touchless
- Ultrascan
- Upek
- Validity