UNITED STATES DEPARTMENT OF COMMERCE
National Institute of Standards and Technology
Gaithersburg, Maryland 20899

Semiconductor Metrology Research & Development: Workshop 2

April 20, 2022 – April 21, 2022

April 20, 2022: Panel Discussion Sessions

Workshop Facilitators: Anita Balachandra (NIST) & George Orji (NIST)

10:00 am – 10:15 am (EDT)	**Welcome and Opening Remarks**	Eric Lin (NIST)
10:15 am – 10:45 am (EDT)	**CHIPS Act Overview**	Michael Molnar (NIST)
10:45 am – 11:25 am (EDT)	**Plenary Speaker**	E. Jan Vardaman (TechSearch Intl., Inc.)

11:30 am – 12:30 pm (EDT) **Panel 1 – Novel Metrologies for Advanced Packaging**

Discuss the future of advanced packaging related, but not limited to, the metrology needs of electrical, thermal, and mechanical performance, as well as its effects on power consumption and efficiency.

Moderator: Carol Handwerker (Purdue University)

Panelists: Mike Hill (Intel), Amy Marconnet (Purdue University), Pilin Liu (Intel), and Bongtae Han (University of Maryland)

12:30 pm – 1:00 pm (EDT) **Break for Lunch**

1:00 pm – 2:00 pm (EDT) **Panel 2 – Critical Areas for the Future of Advanced Packaging**

Discuss key supply chain areas where metrology needs exist and must be strengthened for a holistic approach in developing a successful manufacturing strategy for advanced packaging in the United States.

Moderators: E. Jan Vardaman (TechSearch Intl., Inc.), Matt Kelly (IPC)

Panelists: Deepak Kulkarni (AMD), Dale Lee (Plexus Corporation), Raj Kumar (TTM Technologies), Gerard John (Amkor), Dale C. McHerron (IBM Research)

2:00 pm – 3:00 pm (EDT) **Panel 3 – Materials and Devices: Characterization, Modeling, and Design**

Discuss materials and device characterization for modeling and design, particularly for novel technologies and first pass design success.

Moderator: James Booth (NIST), Jerome Cheron (NIST)

Panelists: Peter Aaen (Colorado School of Mines), Michael Shröter (Technical University of Dresden), Norman Chang (ANSYS), Bill Deal (Northrop Grumman Corp, Space Systems)

3:15 pm – 4:15 pm (EDT) **Panel 4 – Security and Trust Across Semiconductor Development and Supply Chain**

Discuss collaboration among government agencies, industry, and academia to build techniques, guidance, best practices, support research, and manage security risks and vulnerabilities in design, development, integration, and post-deployment use of semiconductor devices.

Moderator: Laurie Giandomenico (MITRE)

Panelists: Mark Tehranipoor (University of Florida), Matthew Areno (Intel), Serge Leef (Microsoft), Bill Tonti (IEEE Future Direction)

4:15 pm – 4:20 pm (EDT) **Closing Remarks** George Orji (NIST)

4:30 pm – 6:00pm (EDT) **RFI: National Advanced Packaging and Manufacturing Program Questions**

Moderators: Robert Rudnitsky (NIST), Dave Seiler (NIST)

April 21, 2022: Breakout Discussion Sessions

Breakout Session Lead Facilitator: Joan Pellegrino (Energetics)

10:00 am – 10:05 am (EDT) **Welcome**

10:05 am – 10:50 am (EDT) **Keynote Speaker** Suman Datta (University of Notre Dame)

"The Era of Hyper-scaling in Electronics"

10:50 am – 10:55 am (EDT **Introduction to Breakouts**

10:55 am – 12:10 pm (EDT) **Panel 1 Breakout – Novel Metrologies for Advanced Packaging**

12:10 pm – 12:40 pm (EDT) **Break for Lunch**

12:40 pm – 1:55 pm (EDT) **Panel 2 Breakout – Critical Areas for the Future of Advanced Packaging**

2:05 pm – 3:20 pm (EDT) **Panel 3 Breakout – Materials and Devices: Characterization, Modeling, and Design**

3:30 pm – 4:45 pm (EDT) **Panel 4 Breakout – Security and Trust Across Semiconductor Development and Supply Chain**

4:55 pm – 5:00 pm (EDT) **Closing Remarks**

April 20, 2022 Workshop Speaker and Moderator Bio's

Workshop Facilitator: Anita Balachandra (NIST) - Anita Balachandra is a Resource Manager with the Hollings Manufacturing Extension Partnership. Her portfolio includes the manufacturing extension Centers in Hawaii, Oregon, Arizona, Kansas, Missouri, Minnesota and Mississippi. Prior to joining NIST, Ms. Balachandra spent many years as a private-sector consultant, where she worked extensively with the semiconductor industry.

Workshop Facilitator: George Orji (NIST) - George Orji is currently with the NIST Program Coordination office. He is a project leader in the Microsystems and Nanotechnology Division of the Physical Measurement laboratory at NIST, where he works on nanoscale dimensional and optical metrology, calibration methods, traceability, and uncertainty analysis in dimensional metrology.

Plenary Speaker: E. Jan Vardaman (TechSearch International, Inc.) - E. Jan Vardaman is president and founder of TechSearch International, Inc., which has provided market research and technology trend analysis in semiconductor packaging since 1987. She is the author of numerous publications on emerging trends in semiconductor packaging and assembly. She is a senior member of IEEE EPS and is an IEEE EPS Distinguished Lecturer. She received the IMAPS GBC Partnership award in 2012, the Daniel C. Hughes, Jr. Memorial Award in 2018, the Sidney J. Stein International Award in 2019, and she is an IMAPS Fellow. She is a member of MEPTEC, SMTA, and SEMI. Before founding TechSearch International, she served on the corporate staff of Microelectronics and Computer Technology Corporation (MCC), the electronics industry's first pre-competitive research consortium.

Panel 1 – Novel Metrologies for Advanced Packaging

Panel Moderator: Carol Handwerker (Purdue University) - Carol Handwerker is the Reinhardt Schuhmann, Jr. Professor of Materials Engineering and Environmental and Ecological Engineering at Purdue University, West Lafayette. Before joining Purdue in 2005, she served for 9 years as the Chief of the NIST Metallurgy Division where she started her career as an NRC Postdoctoral Fellow following her Ph.D. in materials science and engineering from MIT. She is a co-PI in SCALE, a national DOD program led by Purdue on workforce development for advanced microelectronics. She co-leads the thrust in heterogeneous integration and advanced packaging. She is a Fellow of TMS, ASM, MRS, and the American Ceramics Society, and received the TMS Leadership Award, TMS Applications to Practice Award, and the TMS/FMD John Bardeen Award.

Michael J. Hill (Intel Corporation) - Michael J. Hill is a Principal Engineer at Intel Corporation in Chandler, Arizona. His work includes the development of new tools and techniques to allow precise characterization of substrate electrical performance metrics spanning power delivery, highspeed I/O and RF applications. He holds B.S., M.S., and Ph.D. degrees in Electrical Engineering from the University of Arizona.

Amy Marconnet (Purdue University) - Amy Marconnet is an associate professor of Mechanical Engineering and a Perry Academic Excellence Scholar at Purdue University. She received a B.S. in Mechanical Engineering from the University of Wisconsin – Madison in 2007, and an M.S. and a PhD in Mechanical Engineering at Stanford University in 2009 and 2012, respectively. Research in her lab intersects heat transfer, energy conversion, and materials science to enable advances in technologies where energy conversion and thermal transport are key factors in performance. In particular, much of her work focuses on developing new innovative measurement techniques for probing thermal transport properties of emerging materials and systems.

Pilin Liu (Intel Corporation) - Pilin Liu completed his Ph. D in Materials Science and Engineering from University of Illinois at Urban-Champaign in 2004 and he is currently a Sr. staff engineer in Failure Analysis Labs at Intel. His responsibilities include failure analysis, defect and material characterizations of pathfinding advanced packaging, failure mechanism understanding of interconnects and solder joint reliabilities. He has published 50+ papers in academic journals and conferences.

Bongtae Han (University of Maryland) - Bongtae Han is a Keystone Professor at the University of Maryland. He was named the 2016 American Society of Mechanical Engineering (ASME) Mechanics Award winner in Electronic and Photonic Packaging Division for his contributions to structural mechanics of electronic systems. He served as an Associate Technical Editor for various journals, and he is currently serving as a Co-Editor-in-Chief for Microelectronics Reliability. He was elected a Fellow of SEM (Society for Experimental Mechanics) and ASME in 2006 and 2007, respectively

Panel 2 – Critical Areas for the Future of Advanced Packaging

Panel Moderator: E. Jan Vardaman (TechSearch International, Inc.) - E. Jan Vardaman is president and founder of TechSearch International, Inc., which has provided market research and technology trend analysis in semiconductor packaging since 1987. She is the author of numerous publications on emerging trends in semiconductor packaging and assembly. She is a senior member of IEEE EPS and is an IEEE EPS Distinguished Lecturer. She received the IMAPS GBC Partnership award in 2012, the Daniel C. Hughes, Jr. Memorial Award in 2018, the Sidney J. Stein International Award in 2019, and she is an IMAPS Fellow. She is a member of MEPTEC, SMTA, and SEMI. Before founding TechSearch International, she served on the corporate staff of Microelectronics and Computer Technology Corporation (MCC), the electronics industry's first pre-competitive research consortium.

Panel Moderator: Matt Kelly (IPC) - Matt Kelly is Chief Technologist at IPC and is focused on driving next generation technology advancements and supply chain transformation across the electronics industry. He works within the association's executive leadership team to identify and develop new strategic initiatives, meeting member and industry needs. He delivers influential thought leadership, research, and advocacy to industry and governments. Matt comes to IPC following a 15-year career at IBM Corporation, holding several senior technology and engineering leadership positions within IBM Systems Division. He is a licensed Professional Engineer with a degree in Chemical Engineering from McMaster University and holds an MBA in Strategic Management from Sir Wilfrid Laurier University.

Deepak Kulkarni (AMD) - Deepak Kulkarni is a Fellow, Advanced Packaging at AMD. Deepak has over 15 years of experience in packaging technology development. Over the years, he has held several leadership positions driving substrate technology development and yield improvement. Prior to joining AMD, Deepak was Senior Director of packaging yield at Intel Corporation. He holds eight patents and nineteen publications on various aspects of packaging such as 2.5D/3D architectures, DFM/DFY and AI techniques applied to yield management. His contributions to the semiconductor industry have been recognized by an Intel Achievement Award, Next 5% award (AMD) and best paper award (ITHERM). Deepak holds a PhD from the University of Illinois Urbana-Champaign with a major in mechanical engineering and a minor in computational science.

Dale Lee (Plexus Corporation) - Dale Lee is a Senior Staff DFX Strategy Engineer with Plexus Corporation primarily involved with DFX analysis, root cause failure analysis and definition/correlation of design, process and tooling impacts on assembly processes and manufacturing yields. He has been involved in surface mount design, package & process development and production for over thirty years in various technical and managerial positions. He has authored multiple technical articles and papers and is a frequent instructor/presenter globally on topics including PCB and SMT design, assembly, cleaning, and DFM/DFX and is a past recipient of the Surface Mount Technology Association's "Excellence in Leadership" award and IPC's "President's Award".

Raj Kumar (TTM Technologies) - Raj Kumar is currently serving as the VP Technology Solutions, AMI&I BU (Automotive Medical Industrial & Instrumentations Business Unit) for TTM Technologies. He has over 38 years of experience in the field of Printed Circuit Board and BGA substrate fabrication. His area of expertise is in Conceptual Engineering, Process Engineering, Product Development, and Research & Development that spans across a wide array of products such as High Layer Count & High-Density Rigid PCBs, Flex & Rigid-Flex, Embedded Metal Core, Flip-Chip BGAs and Multi-Chip Module-Laminate (MCM-L) substrates. His educational background includes a BS in Mechanical Engineering & BS in Chemistry. Raj has 11 patents and is actively engaged in IPC standards development.

Gerard John (Amkor) - Gerard John joined Amkor in 2005, and currently manages the FCBGA product portfolio for customers in Europe, Israel and South Korea. He previously served as an advanced test technical expert for MEMS, wafer probe and advanced packaging. Prior to joining Amkor, Gerard worked in various semiconductor test positions for Conexant Systems, Flarion Technologies (acquired by Qualcomm) and Motorola. He holds a BS degree in electronics and telecommunications engineering from Osmania University and an MBA from Gainey School of Business in Michigan and is pursuing a MSEE from the University of New Mexico.

Dale McHerron (IBM Research) - Dale McHerron is currently Senior Manager at IBM Research based in Albany, NY with responsibility for IBM's Heterogeneous Integration Research Program and project leader in the IBM AI Hardware Research Center. Dale received his PhD in chemical engineering from Virginia Tech and started his career at IBM in 1992 in the IBM Microelectronics Advanced Packaging Development Group where he developed thin film interconnect technology for multichip modules in IBM mainframe and server products. Over his career Dale has held various technical, managerial, and business development positions in both advanced packaging and silicon logic R&D. In 2007, he transitioned to the IBM Albany Research lab where he has initiated and led research projects in logic scaling and heterogeneous integration and has played a key role developing the IBM collaborative research ecosystem in Albany.

Panel 3 – Materials and Devices: Characterization, Modeling, and Design

Panel Moderator: James Booth (NIST) - James C. Booth joined the National Institute of Standards and Technology as a physicist in 1996, and currently leads the Guided Wave Electromagnetics Group within the Communications Technology Laboratory. He received the Ph.D. degree in Physics from the University of Maryland. Research interests at NIST include material and component measurements for advanced wireless communications; on-wafer measurements and standards for advanced microelectronics and hardware security applications; and novel microfluidic chip-based techniques exploiting electromagnetic effects for chemistry and biochemistry.

Panel Moderator: Jerome Cheron (NIST) - Jerome Cheron received the Ph.D. degree in electrical engineering from the University of Limoges, France, in 2011. Before joining the National Institute of Standards and Technology (Boulder CO, USA) in 2013, he worked with the Fraunhofer Institute for Applied Solid State Physics (Freiburg, Germany). His current research interests include the characterization, modeling and design of microwave, millimeter-wave and terahertz active-circuits in III-V technologies.

Peter Aaen (Colorado School of Mines) - Peter H. Aaen (Senior Member, IEEE) received the B.A.Sc. degree in engineering science and the M.A.Sc. degree in electrical engineering from the University of Toronto, Toronto, ON, Canada, in 1995 and 1997, respectively, and the Ph.D. degree in electrical engineering from Arizona State University, Tempe, AZ, USA, in 2005. In 2019, he joined the Colorado School of Mines as a Professor and the Head of the Electrical Engineering Department. He is a member of the Microwave Theory and Techniques and Electron Device Societies, served as an Executive Committee Member and the Vice-President of the Automatic RF Techniques Group, and formerly was the Chair of the IEEE Technical Committee (MTT-1) on Computer-Aided Design.

Michael Shröter (Technical University of Dresden) - Michael Schröter has held engineering and management positions at Nortel/BNR in Ottawa, Canada, and at Rockwell/Conexant and RFNano in Newport Beach (CA), USA. Since 1999, he has been a Full Professor at Technical University Dresden, Germany, and head of the Chair for Electron Devices and Integrated Circuits. Among his many accomplishments, he was the initiator and Technical Project Manager for the EU projects DOTFIVE and DOTSEVEN that led to SiGe HBT technologies with world-record performance and is the author of the industry standard compact bipolar transistor model HICUM. He has co-authored two textbooks and over 270 peer reviewed publications.

Norman Chang (ANSYS) - Norman Chang co-founded Apache Design Solutions in February 2001 and currently serves as Ansys Fellow and Chief Technologist at Electronics and Semiconductor BU, ANSYS, Inc. He is also currently leading AI/ML and security initiatives at ANSYS. Dr. Chang received his Ph.D. in Electrical Engineering and Computer Sciences from University of California, Berkeley. He holds twenty patents and has co-authored over 50 technical papers and a popular book on "Interconnect Analysis and Synthesis". He is a Senior Member of IEEE.

William Deal (Northrop Grumman Corp, Space Systems) - William R. Deal (Fellow, IEEE) received the B. S. degree in electrical engineering from the University of Virginia, Charlottesville, VA, USA, in 1996, the M.S. and Ph.D. degrees from the University of California, Los Angeles, CA, USA, in 1998 and 2000, respectively., Currently, he is a Consulting Engineer with Northrop Grumman's RF Product and Mixed Signal Center in Redondo Beach, CA, USA. He leads a variety of efforts related to developing submillimeter wave technology and inserting submillimeter wave technology into applications. He has authored and co-authored more than 150 journal and conference papers, as well as five book chapters.

Panel 4 – Security and Trust Across Semiconductor Development and Supply Chain

Panel Moderator: Laurie Giandomenico (MITRE) - Laurie Giandomenico is vice president and chief acceleration officer at MITRE. In this role, she leads MITRE's Accelerator and launched MITRE Engenuity, MITRE's tech foundation that works with the private sector for public good. Last year, her team launched the Semiconductor Alliance – an industry R&D collaboration focused on building a neutrally-led, industry alliance that is creating a semiconductor strategy, governance model, investment fund and workforce plan for CHIPS Act funding to revitalize the US semiconductor industry. Giandomenico has a BS in electrical engineering from the University of Connecticut, an MA in anthropology and archeology from Cornell University, and a Ph.D. in nutritional sciences with a focus on science and technology studies and organizational development, also from Cornell University.

Mark Tehranipoor (University of Florida) - Mark M. Tehranipoor is currently the Intel Charles E. Young Preeminence Endowed Chair Professor in Cybersecurity at the University of Florida. His current research projects include: hardware security and trust, supply chain security, IoT security, VLSI design, test and reliability. He co-founded the IEEE International Symposium on Hardware-Oriented Security and Trust (HOST), IEEE International Conference on Physical Assurance and Inspection of Electronics (PAINE). He serves on the program committee of more than a dozen leading conferences and workshops. He is currently serving as a founding director for Florida Institute for Cybersecurity Research (FICS) and a number of other centers with focus on microelectronics security. Dr. Tehranipoor is a Fellow of the IEEE, a Fellow of the ACM, a Golden Core Member of IEEE CS, and Member of ACM SIGDA.

Matthew Areno (Intel) - Matthew (Matt) Areno is a Senior Principal Engineer and Senior Director of Security Assurance and Cryptography at Intel Corporation. Having worked previously at Sandia National Laboratories and Raytheon Cyber Security Innovations, Dr Areno has a long history of both offensive and defensive work with extensive experience with threats against supply chain security.

Serge Leef (Microsoft) - Serge Leef joined Microsoft Azure in March of 2022 as the Head of Azure for Secure Microelectronics. For the prior 4 years, he was a program manager at DARPA's Microsystems Technology Office (MTO) focusing on computer architecture, chip design tools, simulation, synthesis, semiconductor intellectual property (IP), cyber-physical modeling, distributed systems, secure design flows, and supply chain management. Serge received his Bachelor of Science degree in electrical engineering and Master of Science degree in computer science from Arizona State University. He has served on corporate, state, and academic advisory boards, delivered numerous public speeches, and holds patents in hardware Trojan detection and Internet of Things (loT) infrastructure.

Bill Tonti (IEEE Future Direction) - Tonti holds a BSEE from Northeastern University, an MSEE and a Ph.D. from the University of Vermont, and an MBA from St. Michael's College. He worked for over 30 years at IBM in the area of semiconductor technology research. Dr. Tonti holds 297 issued patents, and has been recognized as an IBM master inventor, and as one of the world's top patent family holders. His 250'th patent issue has been transcribed into the U.S. Congressional Record. Dr. Tonti has produced over 350 publications and invited talks throughout his career. Dr. Tonti is a Fellow of the IEEE a past IEEE Reliability Society President, a recipient of the IEEE Reliability Engineer of the Year award, and the IEEE 3'rd Millennium medal. Dr. Tonti currently is a Senior Director at the IEEE leading its Future Technology Directions. Dr. Tonti is a past IEEE IRPS and IEEE IRW General Chair.

RFI - National Semiconductor Technology Center Questions

Moderator: Robert Rudnitsky (NIST) - Robert Rudnitsky is a Physicist and Associate Director in the NIST Office of Advanced Manufacturing, where he develops planning for the CHIPS Advanced Packaging Manufacturing Program and the Manufacturing USA program. His research experience includes microelectromechanical systems, device fabrication, microfluidics, and sensors. He received a Ph.D. in Applied Physics from Stanford University, where he was a Hertz Fellow, and a B.A. from Yale University. Robert was the founding chair of the international Organisation for Economic Cooperation and Development (OECD) Working Party on Nanotechnology, and has chaired the U.S. National Nanotechnology Initiative International Working Group, and the NATO Science for Peace and Security Advisory Committee. Prior to coming to NIST, he worked at the State Department, as an investment banker specializing in acquisitions, and as president of a small company.

Moderator: Dave Seiler (NIST) - David Seiler is a Microelectronics Senior Advisor at the National Institute of Standards and Technology (NIST) Office of Advanced Manufacturing (OAM). He has a Ph.D. in physics from Purdue University and has authored more than 140 invited and contributed papers and given over 200 talks at national and international meetings. He is a Fellow of the American Physical Society and the Institute of Electrical and Electronic Engineers. Prior to joining OAM, David had over 20 years of experience as Chief of the Semiconductor Electronics and Engineering Physics Divisions at NIST, working with industry to provide innovative measurement science research and standards. Dr. Seiler has been involved in a wide variety of important activities for the semiconductor community which include: serving on the ITRS Roadmap activities, the IEEE Electron Device Society's Semiconductor Manufacturing Committee, the IEEE's Corporate Innovation Award Committee, and the Governing Council of the Nanoelectronics Research Initiative (a model for industry-driven consortia seeking a new paradigm beyond CMOS devices).

April 21, 2022 Workshop Keynote Speaker

Suman Datta (University of Notre Dame) - Suman Datta is the Stinson Professor of Nanotechnology in the Electrical Engineering Department at the University of Notre Dame. He is Adjunct Professor of School of Electrical and Computer Engineering at Georgia Institute of Technology. Prior to that, he was a Professor of Electrical Engineering at The Pennsylvania State University, University Park, from 2007 to 2011. From 1999 till 2007, he was in the Advanced Transistor Group at Intel Corporation, Hillsboro, where he developed several generations of high-performance logic transistor technologies including high-k/metal gate, Tri-gate and non-silicon channel CMOS transistor technologies. His research group focuses on emerging device concepts that enable new computational models. He is a Fellow of IEEE and the National Academy of Inventors (NAI). He has published over 400 journal and refereed conference papers and holds 187 patents related to advanced device technologies. He is the Director of a multi-university advanced microelectronics research center, the ASCENT, funded by the Semiconductor Research Corporation (SRC) and the Defense Advanced Research Projects Agency (DARPA).