Nanoelectronics Landscape In Europe: New Opportunities for Research and Innovation

Gisele Roesems

Deputy Head of Unit Nanoelectronics

European Commission, DG Information Society and Media

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Presentation Outline

- R&D Infrastructure and Production sites in Europe
- European R&D Programmes FP7, ENIAC and Catrene
- Metrology and Characterization –Project examples
- Summary and conclusion

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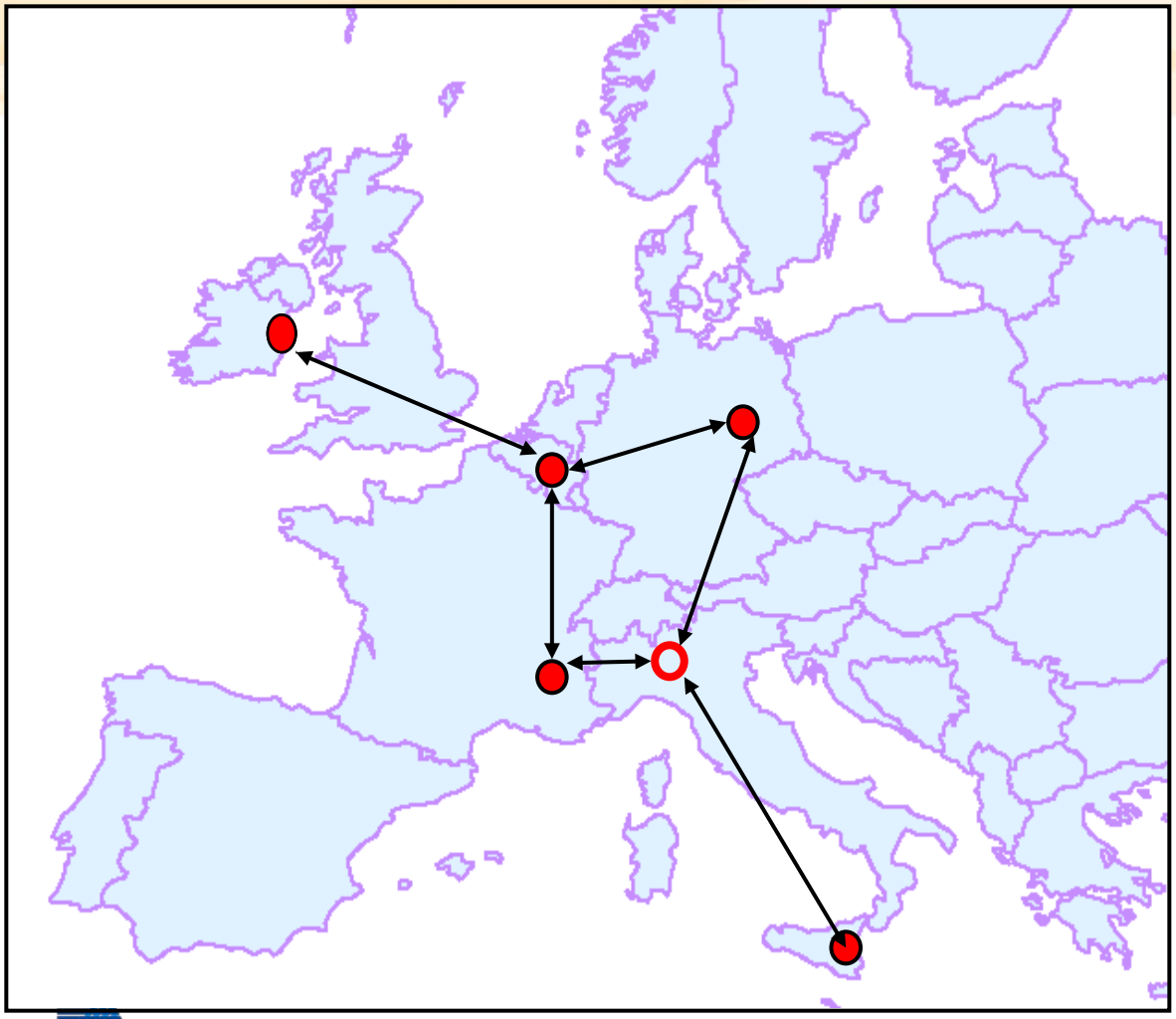
Eco-zones for research and development

- A decade of clustering in semiconductor leading-edge technologies has generated jobs, economic growth and leadership in innovation
- Best practice of collaboration between industry, research institutes and academia
- Extensive partnerships to gain critical mass and leverage investments
- "local" sourcing for systems suppliers with respect to equipment, services, materials and knowledge
- Many spin-off companies
- Establishment of local branches of non-European high-tech industries
- Attracting specific support from local government

European Nano-electronics eco-zones:
Industry,Research institutes, academia, and public authorities working together



300mm research infrastructures in Europe:

- Dresden (D)
- Leuven/Eindhoven (B, NL)
- Grenoble (F)
- Catania (I)
- Dublin (IRL)

Specializing on different subjects, with partial overlap.

Providing access to researchers working on the field in all Europe.

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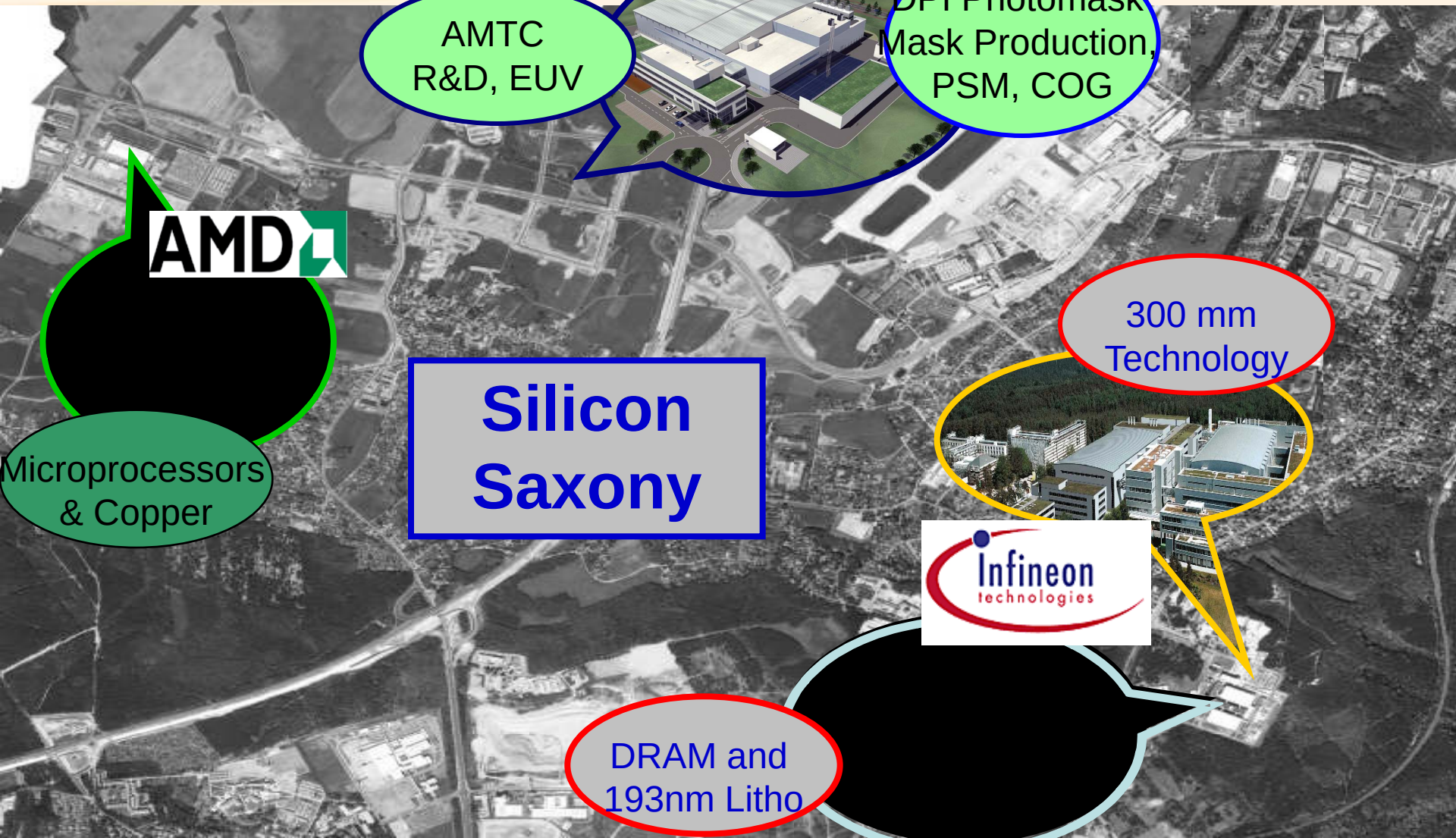
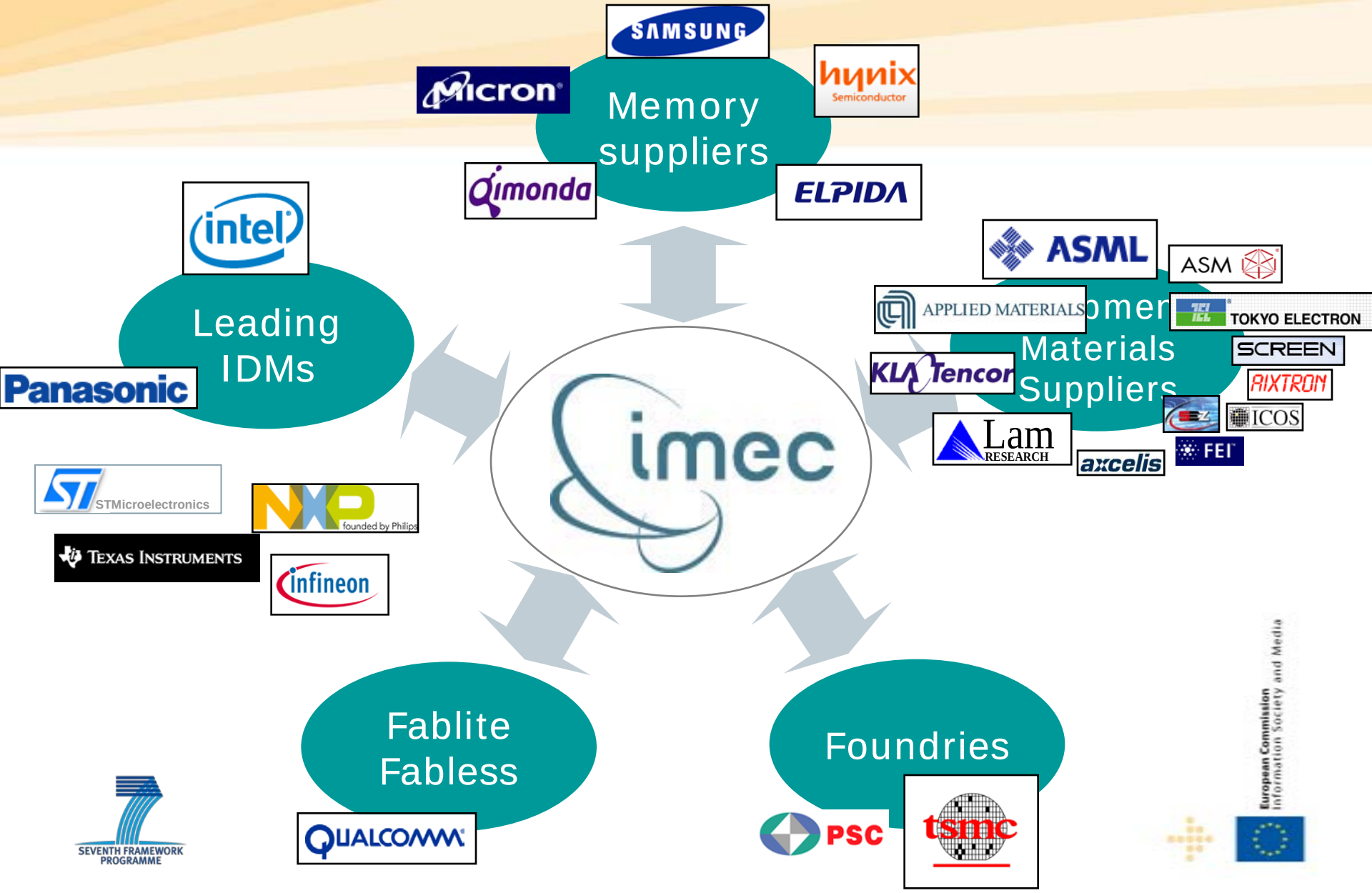
Dresden, Silicon Saxony, Germany



Partnering for Cost-effective Research

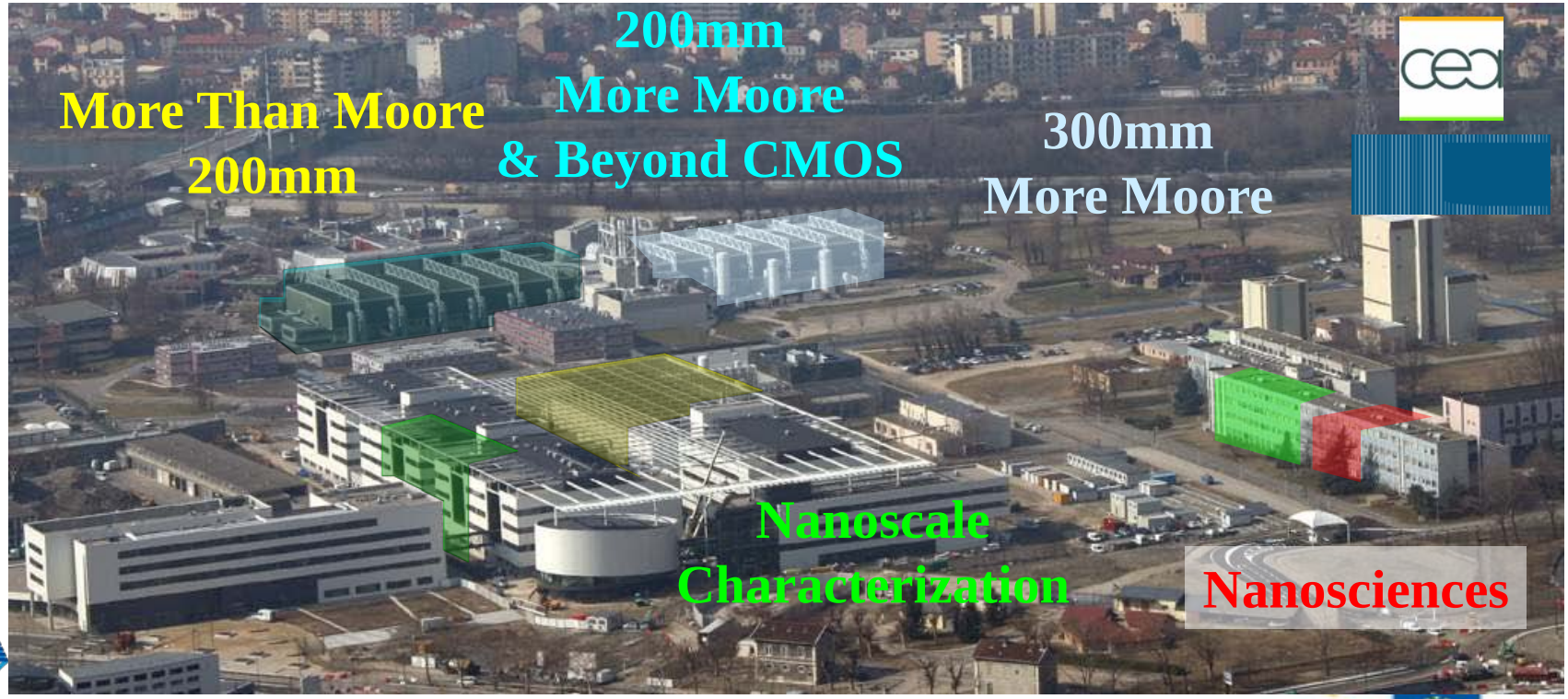


A complete set of research platforms

From advanced concepts to pilot lines

Short loops with industrial sites

Cooperative with academia and industry



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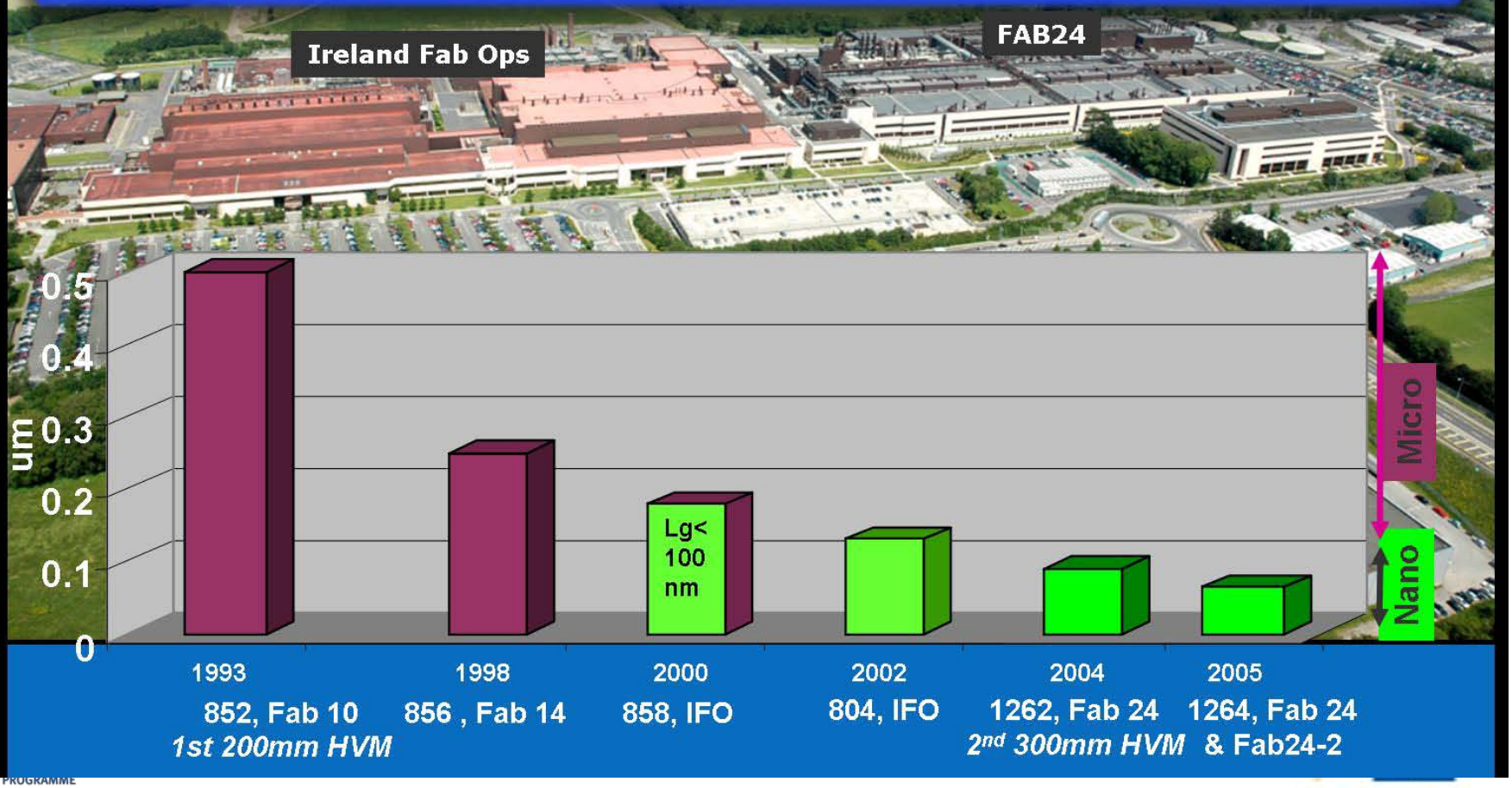
Intel in Ireland

Moore's Law in action !
6 major technology transfers from 0.5um to 65nm
wafer transition from 200 to 300mm
$7 billion has been invested to date, approximately 5000 direct & indirect employees, 344k m² of buildings!



Nanoelectronics: An Industry in Movement

Increasing cost for advanced mega fabs & for R&D for next technology node & private equity involvement trigger major changes:

- ***Globalisation of Semiconductor R&D and Manufacturing***

Global alliances, emerging markets

- ***Changing Business Models and Consolidation***

from IDM to foundry – fab lite - fab less

handshake between design, product, technology and manufacturing; solutions rather than technology;

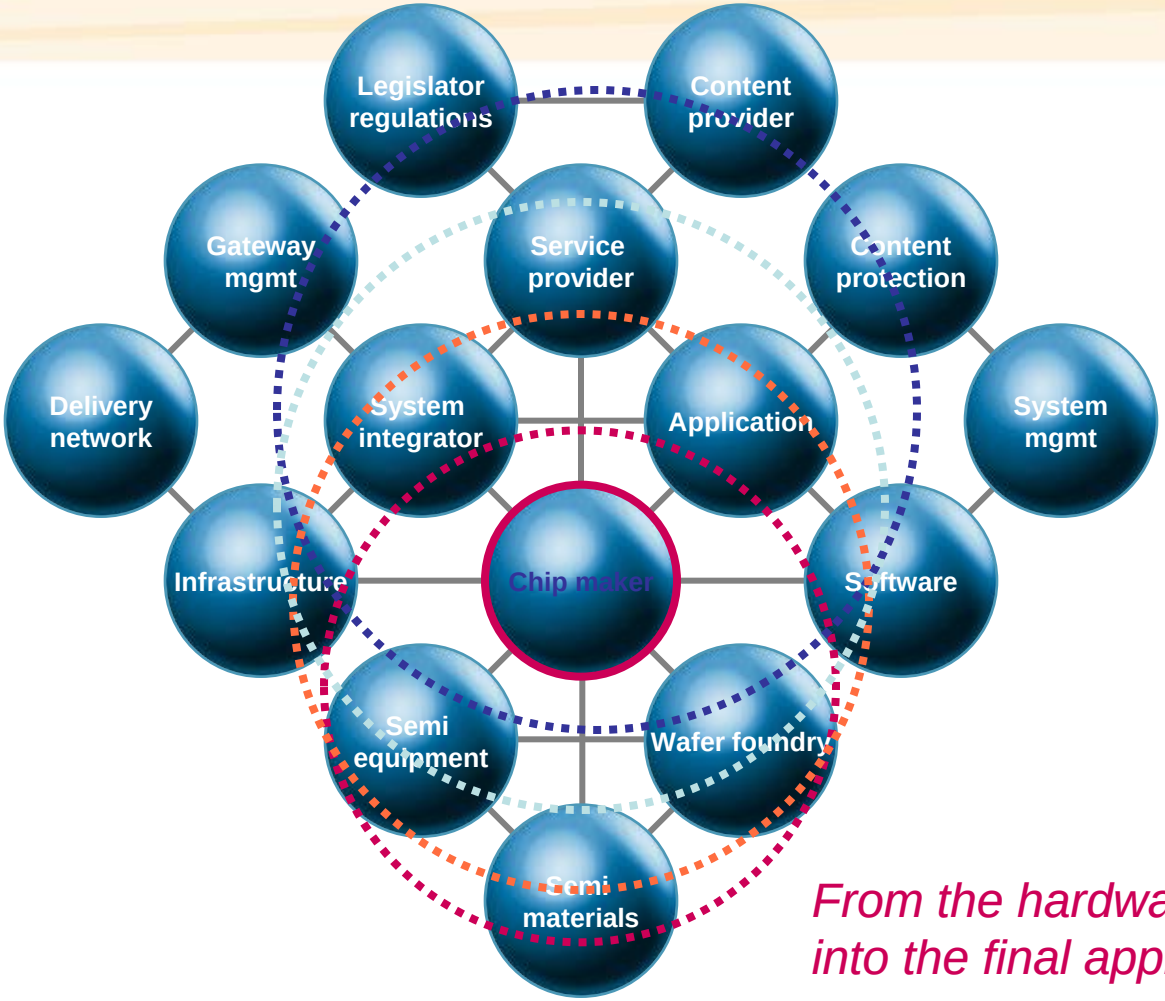
- ***Changing R&D Models***

Global alliances for process R&D; in-house more application R&D and system integration; cost of infrastructure, multi-disciplinarity, complexity

- ***4 Generations to Go ? - What is Next ?***

« Alternative » solutions to replace and extend the lifetime of traditional CMOS;

European Chip makers are moving up the value chain



From the hardware supply side into the final application

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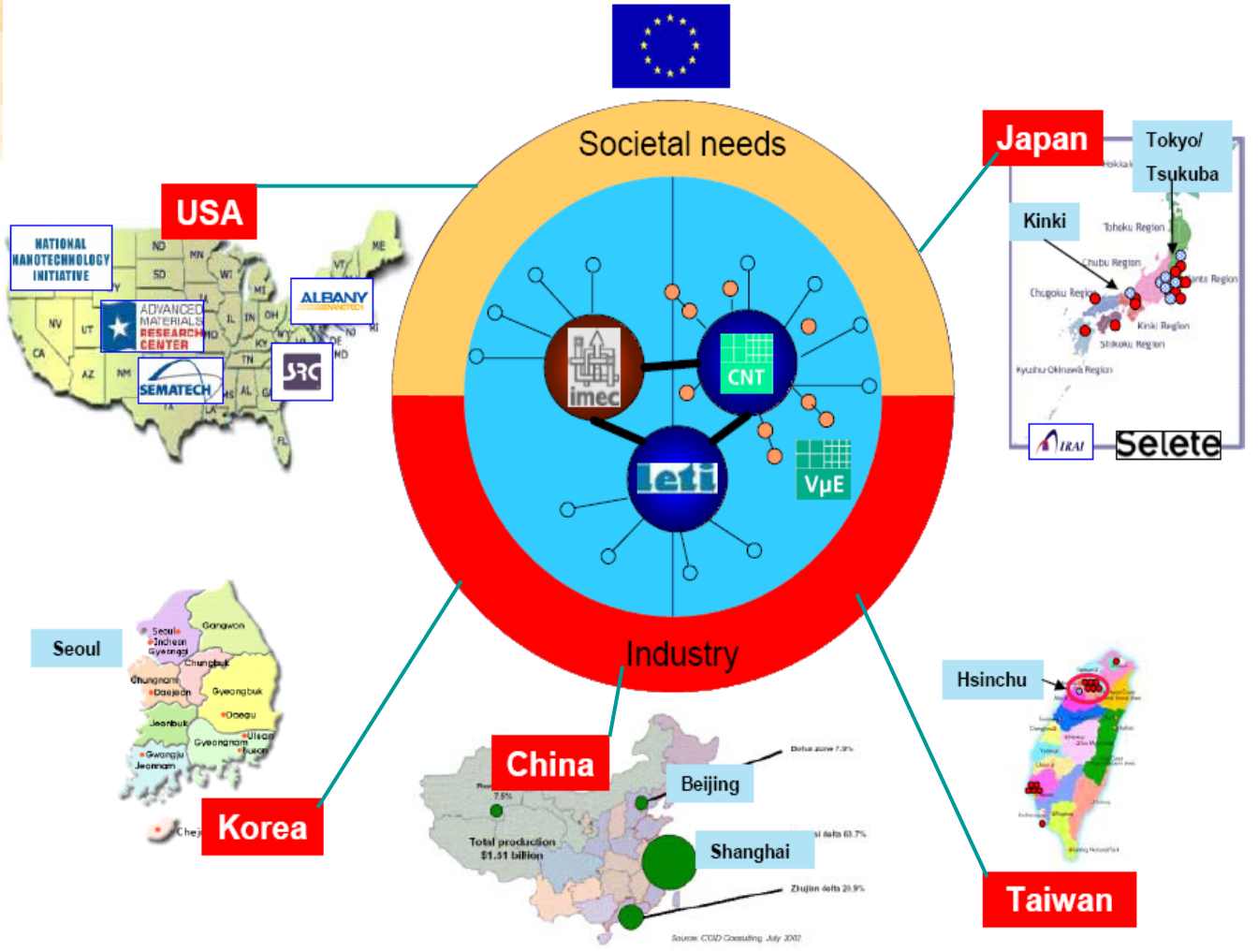
Global Cooperations in International Networks



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Building up a European strategy for publicly funded cooperative research

Public Authorities

MEDEA+ System Innovation on Silicon

CATRENE

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i2010

ENIAC JTI

Research Projects

Industrial association

AENEAS

Technology Platform

niac

The Report of the High Level Group (2003-2004)

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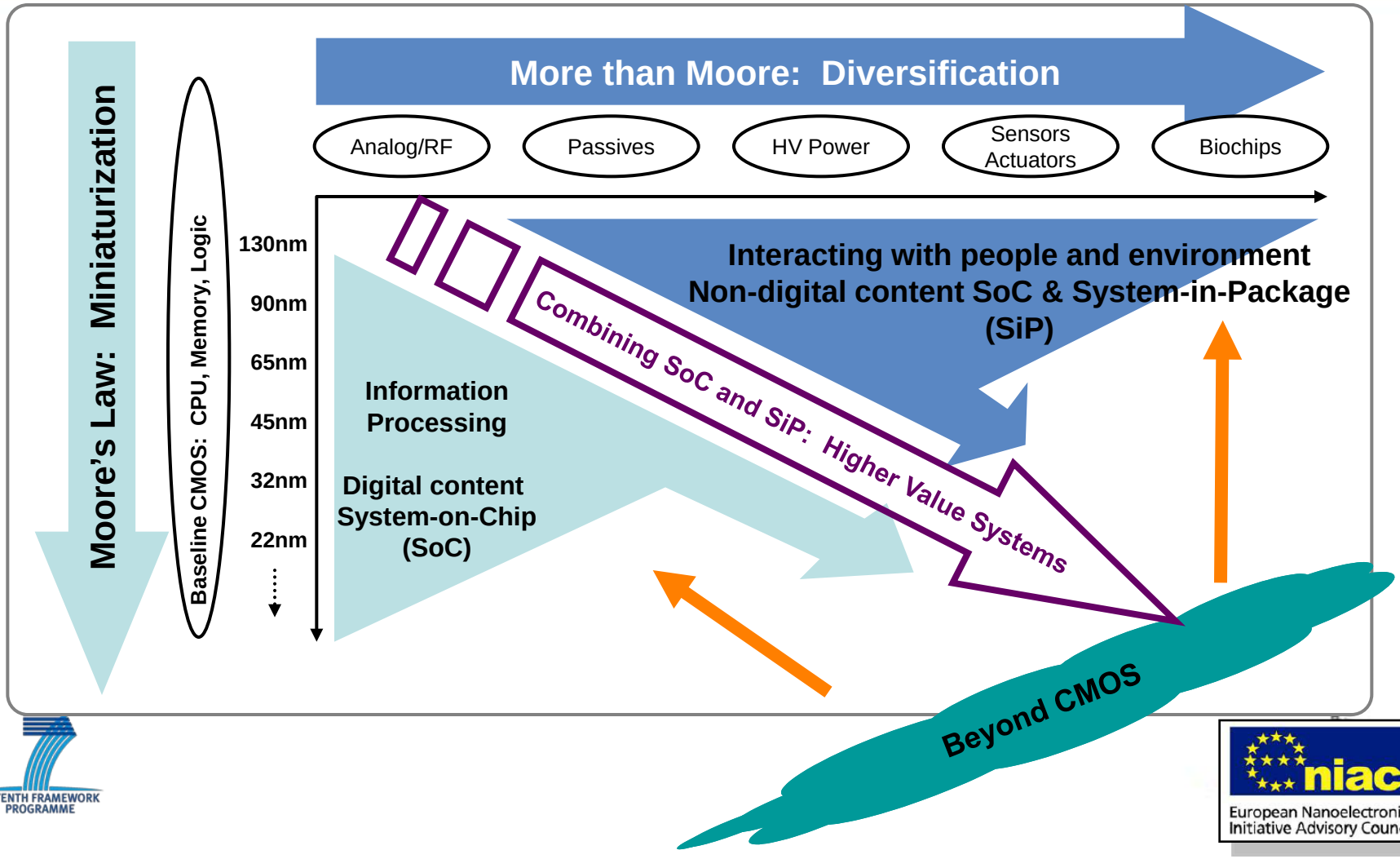
European Roadmap for Nanoelectronics



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niac
European Nanoelectronics Initiative Advisory Council

ENIAC SRA implementation

ENIAC

Industry-driven long-term vision

Beyond CMOS

Design Automation

'More Moore'

'More than Moore'

Equipment and Materials, Manufacturing

Heterogeneous Integration

5+ €bn

Coordination

FP7
(ICT-NMP)
WP 2009-2010
WP 2011-2013

Joint Technology Initiative

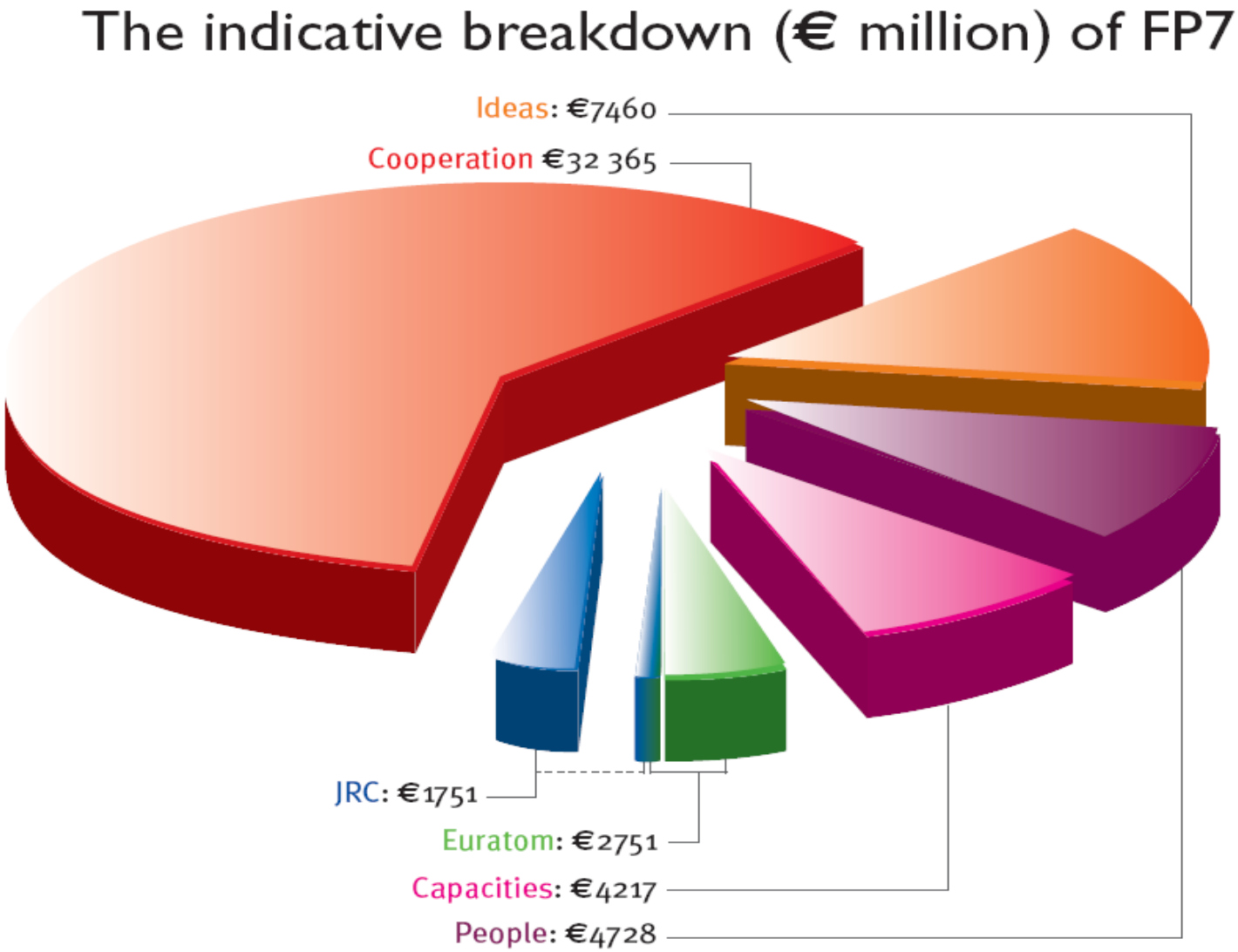
Multi-Annual Strategic Plan

Annual Work Programme

Eureka
(Catrene)
White Book

National / regional programmes

Framework Programme 7 (2007-13)



FP7 Cooperation Programme: Themes

1. Indicative budget [M€]

1.	Health	6,000	
2.	Food, Agriculture & Biotechnology	1,935	
3.	Information & Communication Technologies	9,120	(28%)
4.	Nanosciences, Nanotechnologies, Materials & new Production Technologies	3,505	
5.	Energy	2,300	
6.	Environment (including Climate Change)	1,900	
7.	Transport (including Aeronautics)	4,195	
8.	Socio-Economic Sciences & the Humanities	610	
9.	Space	1,430	
10.	Security	1,320	
		32,315	

... including

- ***Joint Technology Initiatives***
- ***ERA-Nets***
- ***International Co-operation***

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FP ICT WP Structure

- A WP structured around a limited set of "Challenges" that should be addressed

- A Challenge is
  - Focused on concrete goals that require effort at Community level and where collaboration is needed
  - Ambitious and strategic proposing a European vision on ICT for the next 10 to 15 years
  - Described in terms of the set of ***outcomes targeted*** and their ***expected impact*** on industrial competitiveness and on addressing policy and socio-economic goals

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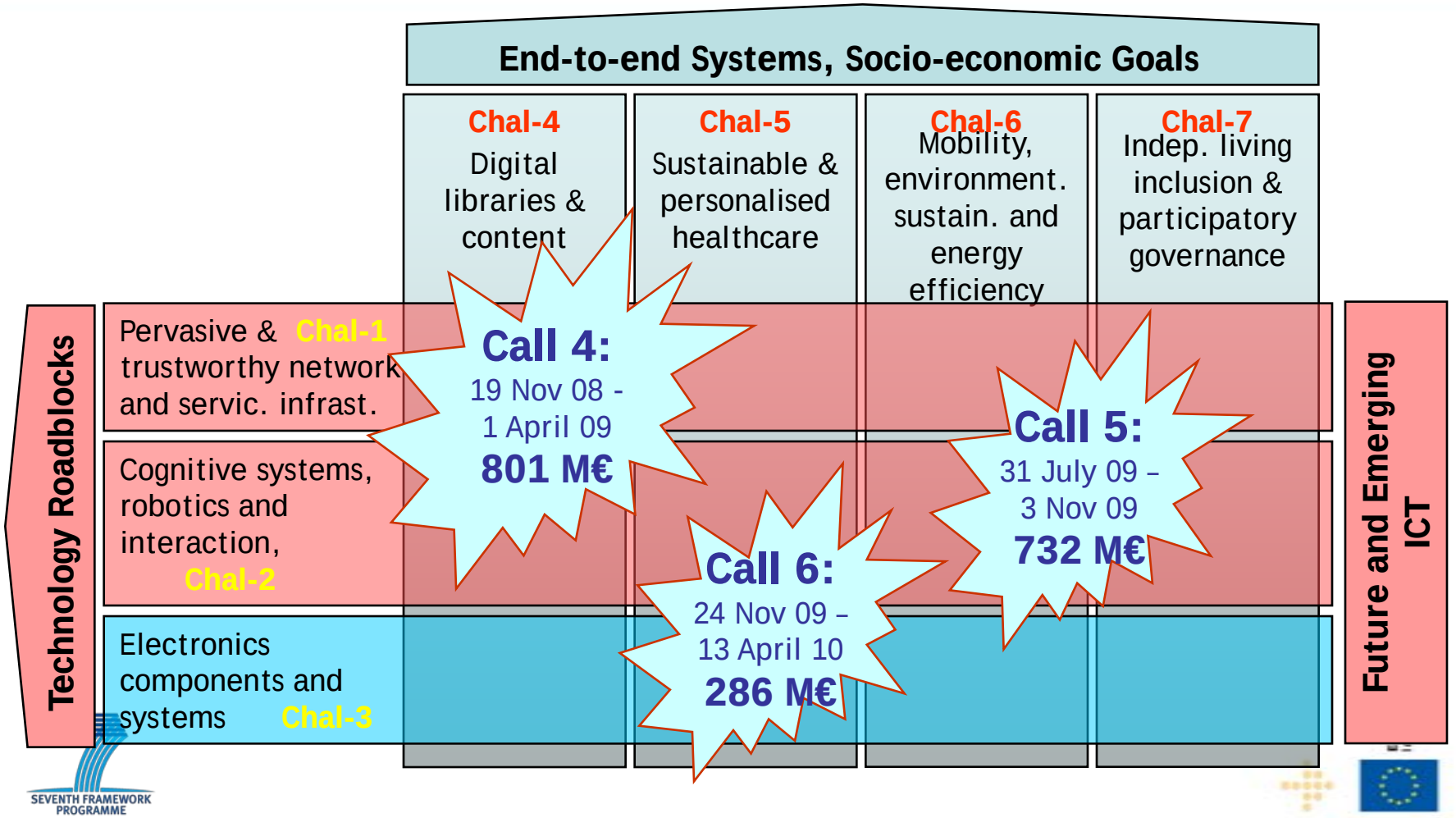
ICT Work Programme 2009-10



European Economic Recovery Plan

- Adopted by the EC on 26 Nov 2008 and endorsed by the EU Council on 11-12 Dec 2008
- "*To support innovation in manufacturing, construction and in the automobile sector, which have recently seen demand plummet as a result of the crisis and which face significant challenges in the transition to the green economy.*"
- 3 Public-Private Partnerships (PPPs) to promote the convergence of **public interest** with **industrial** commitment and leadership in determining strategic research activities

  - Green cars (Transport, ICT, Energy, NMP, Environment)
  - Energy efficient buildings (NMP, Energy, ICT, Environment)
  - Factories of the future (NMP, ICT)

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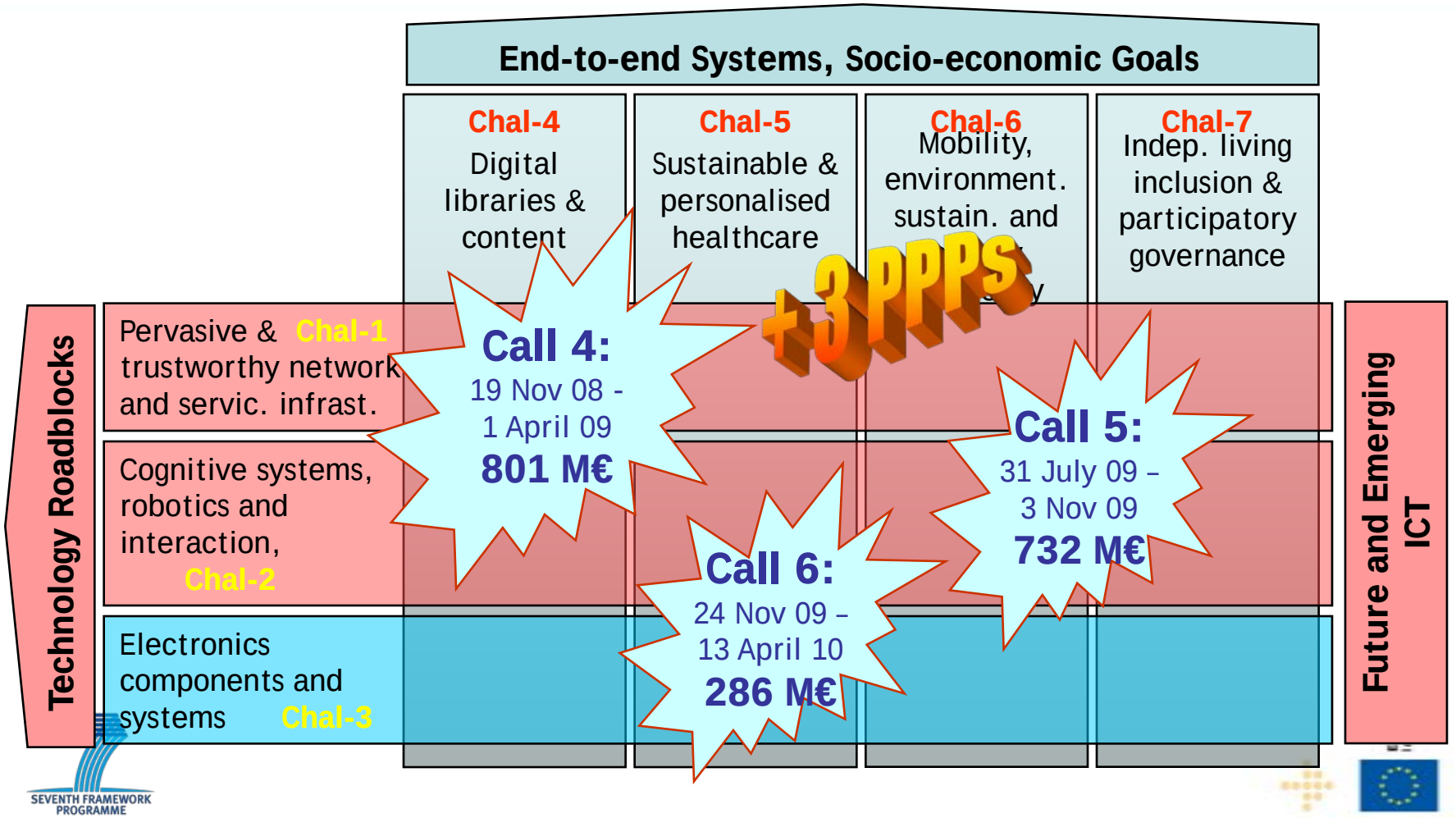
ICT Work Programme 2009-10



FP ICT WP Update

- ICT WP 2010
  - Contribution of ICT Theme to Public Private Partnerships for R&D in the European Economic Recovery Plan:

    Cross thematic calls
    - Factories of the Future: 35 M€ (ICT contribution)
    - Energy-efficient buildings: 15 M€
    - Green cars: 20 M€

  - Additional objectives aimed at strengthening cooperation in ICT R/D in an enlarged Europe: 15 M€

- ICT WP 2011-2012: reinforced support for PPPs

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FP7 ICT : Overview

- **ICT Call 4 (closed)**
  - 19 November 2008 - 1 April 2009
  - Indicative budget 801 M€
  - Objective 3.2: Design of Semiconductor Components and Electronic-based Miniaturised Systems (25 M€)
  - Remote evaluation ongoing; Consensus meetings and panel meeting: week 20; Hearings: week 23
  - ESRs => proposers: end of June

- **ICT Call 5**
  - **31 July 2009 – 3 November 2009**
  - **Indicative budget 732 M€**
  - **Objective 3.1 Nanoelectronics Technology**

+3 Cross thematic calls

- **ICT Call 6**
  - 24 November 2009 - 13 April 2010
  - Indicative budget 286 M€

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International Cooperation in FP7/ICT Objectives

- To jointly respond to major global technological challenges by developing interoperable solutions and standards
- To jointly develop ICT solutions to major global societal challenges
- To improve scientific and technological cooperation for mutual benefit

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Countries participating in FP7

- EU Member States and Associated Countries
- International Cooperation Partner Countries/ICPC, including Brazil/Latin America (receive funding)
- Other countries (e.g. US) funding only exceptionally
- International partners in addition to minimum number

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3.1 Nanoelectronics technology (1)

- Miniaturisation and functionalisation

  - Process variability, physical and reliability limitations of devices and interconnects
  - New circuit architectures, metrology and characterisation techniques
  - Interface and system integration =>SoC, SiP
  - New device structures (non-Si and Si)
  - Disruptive technologies and functional devices: Beyond CMOS
  - Electromagnetic interference, heat dissipation, energy consumption

3.1 Nanoelectronics technology (2)

- Manufacturing technologies
  - New manufacturing approaches, processes and tools
  - Joint assessments of novel process/metrology equipment and materials
  - Supporting 200/300mm wafer integration platform
  - Process, metrology, equipment metrics, test wafers, carriers and physical interfaces to prepare for 450mm wafer processing

3.1 Nanoelectronics technology (3)

- Support measures
  - Roadmaps, benchmarks, selection criteria for the industrial use of 'Beyond CMOS'
  - Access to state-of-the-art technologies for prototyping and low volume and to design expertise and commercial tools
  - Stimulation of interest of young people, training and education
  - Linking of R&D strategies and stimulation of International Cooperation in particular with US, ...
  - Support and coordination of preparatory work for 450 mm processing and equipment

ENIAC SRA implementation

ENIAC

Industry-driven long-term vision

Beyond CMOS

Design Automation

'More Moore'

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5+ €bn

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(Catrene)
White Book

National / regional programmes

ENIAC Joint Technology Initiative

- What? **Industrial R&D programme with coordinated public support**
- Why? **Boosting the competitiveness of EU industry whilst building the European Research Area**
- How?

Pioneering approach **in pooling public and private efforts:**

- Public-Private Partnership: **industry, Member States and Commission**
- Common objectives and strategy
- Single evaluation, selection and project monitoring processes
- First time ever: large scale co-funding of R&D by Community and Member States

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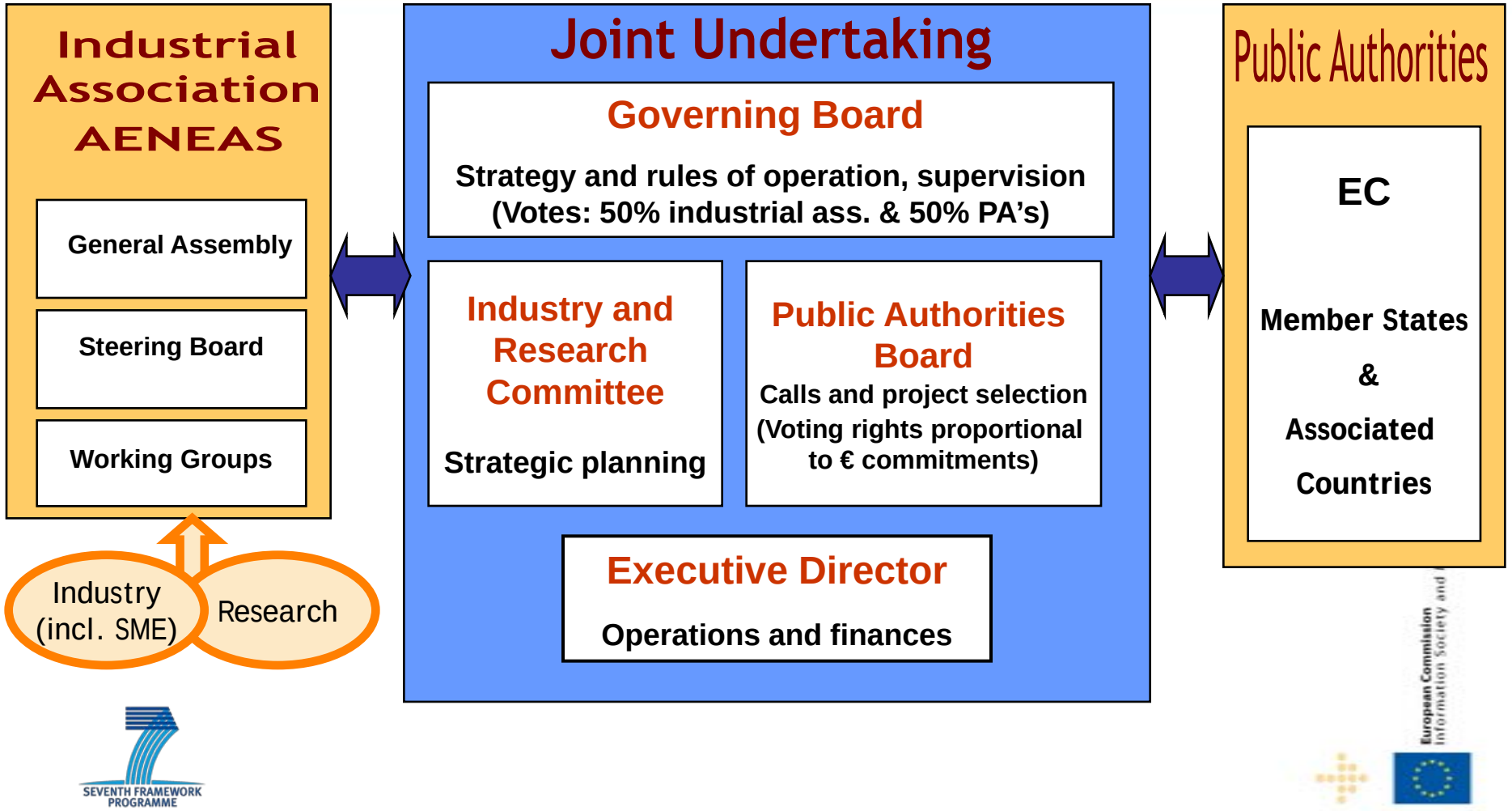
Implementing the JTI: ENIAC Joint Undertaking



Budget of ENIAC Joint Undertaking 2008-2017

Total R&D budget:

- Community: up to €440 million (FP7: 2008-2013)
- States: > 1.8 x Community contribution
- R&D actors: in-kind > 50% of costs

~ €3 billion invested in nanoelectronics R&D activities

Calls for Proposals open to all participants

from EU and Associated Countries

Total JU running costs: max €30 million

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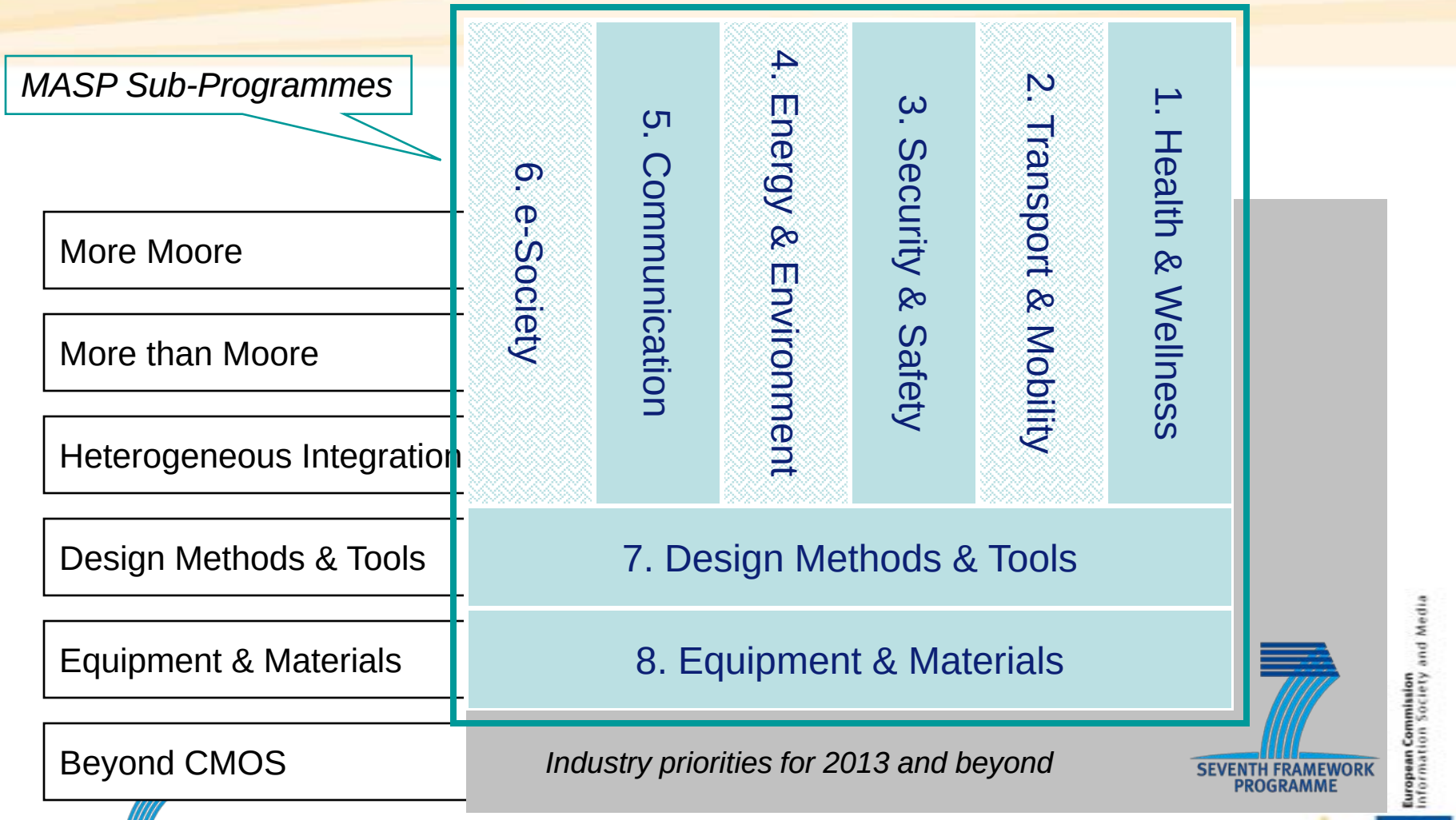
Technological scope follows the ENIAC SRA



Summary of Progress

- Set up of Joint Undertaking largely completed
  - Most internal rules and procedures established
  - Rules and guidelines for Calls for Proposals published
  - Administrative Agreements signed with all funding authorities
  - JU is fully operational …but in transitory period
  - JU autonomy expected in mid-2009
  - Ongoing recruitment of staff

- Call 1 (2008) completed
  - Published in May; deadline in September
  - Evaluation, selection and project negotiation completed
- Call 2 (2009)
  - Published 19 March;
  - Deadline for submission of project outline: May 6th
  - Deadline for submission of full project proposal: September 3rd

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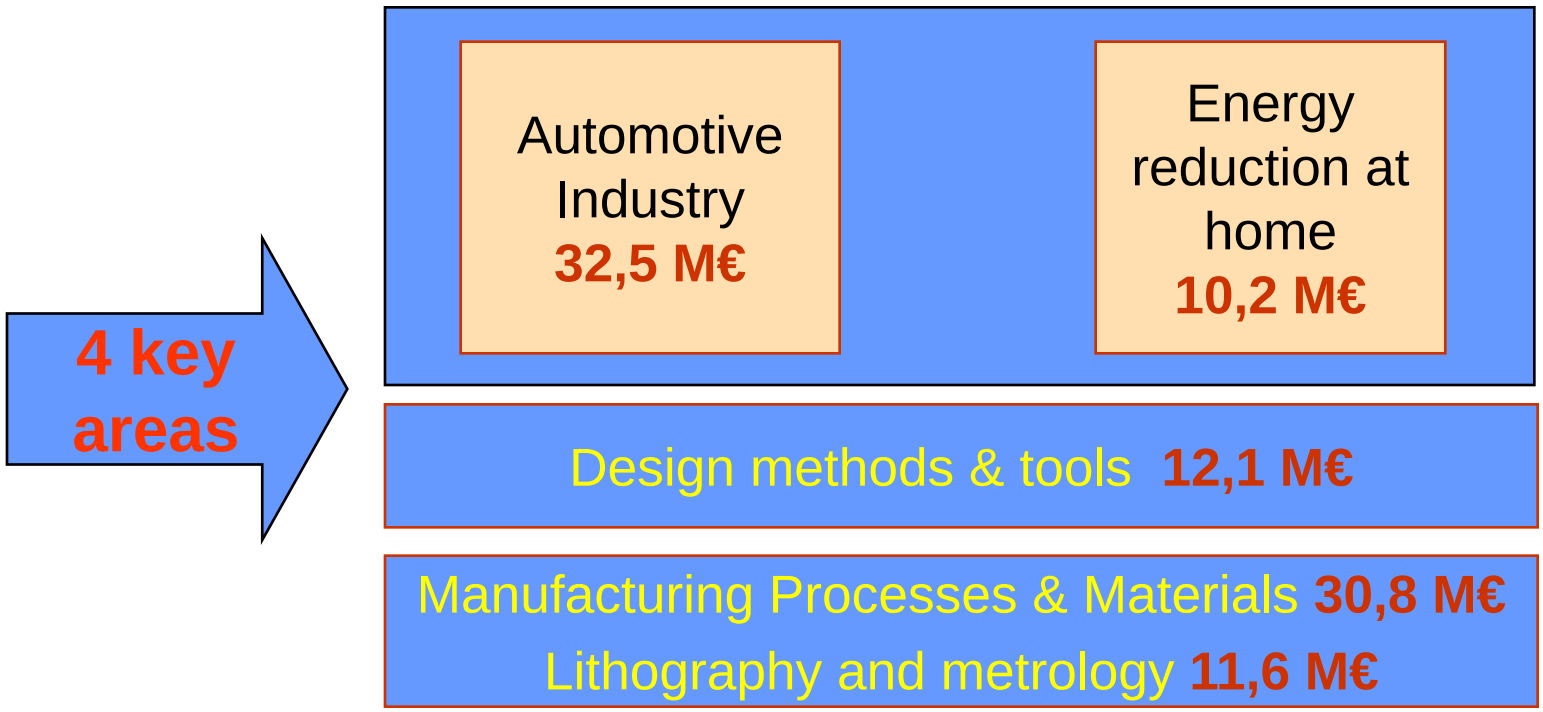
ENIAC Call 1 – Results

- 8 projects currently starting (funding):



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Call 2 2009 Budget

	2008 (M€)	2009 (M€)
Austria	4	4
Belgium	1,500	2,500
Czech Republic	1,500	1,500
Estonia	0	0,300
France	8	7
Germany	15	21
Greece	0,500	1,500
Hungary	1,320	1,320
Ireland	1	1
Italy	10	12
Latvia	-	0
Netherlands	10	7
Norway	1,500	1,500
Poland	1	1
Portugal	0,500	0,500
Slovak Republic	-	0,500
Spain	1	2,250
Sweden	1	1
United Kingdom	0	1,500
Total	57,820	67,370

Total:
104,420 M€

EC commitment:
37,053 M€

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The ENIAC JTI tomorrow: delivering on its promises

- Public Authorities should keep to their commitment, even during difficult times

	Agreed annual R&D budget plan					
	2008	2009	2010	2011	2012-3	Total R&D
ENIAC MS	75,45 M€	100 M€	124,55 M€	154,55 M€	345,45 M€	800 M€
ENIAC JU	41,5 M€	55 M€	68,5 M€	85 M€	190 M€	440 M€

97,2

104,4

55%

- Industry should show a clear overall strategy and present proposals of sufficient quality

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ENIAC

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Nanoelectronics Vision / CATRENE

JESSI (1989-1996)	**helped European companies to be back in the race in Technology**
MEDEA (1997-2000)	**strengthened R&D cooperation of System suppliers and Semiconductor manufacturers**
MEDEA+ (2001-2008)	**helped Europe to conquer leading domains in System Innovation on Silicon**
CATRENE (2008-2011)	**focuses to deliver Nanoelectronic Solutions**

**responding to the needs of society at large,
improving the economic prosperity of Europe,
reinforcing industry's ability to be at the forefront of the global competition**

thus effecting Technological Leadership for a competitive European ICT industry

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CATRENE: Application and Technology Research on Nanoelectronics

The ambition: **to provide industrial solutions that address lead markets responding to the needs of society at large and to create the ability of global European leadership in these new market segments.**

Concept of lighthouse projects addressing large and global socio-economic needs and that create critical mass, address the complete value chain and get support from public authorities

Ex.: Secure Communications and trusted information
Transportation (autonomous vehicles)
Healthcare, aging society (ubiquitous health monitoring and treatment)
Energy saving and Environment
High quality media and entertainment (mobile TV)
Next generation equipment and materials

Catrene is a 4 year (4 year extendable) program started 1/2008,
6 Billion Euro for extended programme, first call evaluated now

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R & D

www.semiconductors.co.uk

Suppliers

Users

European strength!

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Challenges for Metrology and Characterization

- **In the sub-45nm region, well known challenges gain new quality *):**
  - Scaling of MOSFETs to half-pitch of 32nm and below
  - New device architectures
  - New materials (low-k for metallization, high-k for gate-stack and memory, …)
  - Control of critical dimensions (CD), overlay control
  - Measurement on product wafers
  - Understanding and controlling of dimensions, materials properties, and defects towards atomic level
- **Transition to 450 mm wafer size**

*) ITRS 2005, short-term challenges through 2013

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450 mm transition process (1)

- Debate on transition to 450mm wafer processing launched in May 2008
  - Intel, Samsung Electronics and TSMC
  - Target starting transition in 2012
  - Cooperative approach to minimize risks and costs
- Of interest to limited number of IC makers
- But whole foodchain linked to them affected
- Financial and economical crisis =>
  transition yes, but timeline unclear

450 mm transition process (2)

- Several European research institutes and equipment and material suppliers are already exploring and developing their first 450 mm technologies
- Europe is preparing a coordinated approach => single voice of European players in the transition process => Set up of a European 450 mm E&M initiative
- Interest of the EC to stimulate global cooperation of European companies in the field of semiconductor manufacturing (not only 450 mm transition)
- EU financial support (call 5) for European E&M suppliers for preparatoy R&D work and linking with upcoming global activities
- Europe wants to participate in global initiatives, offering its competence and contributing to the critical mass

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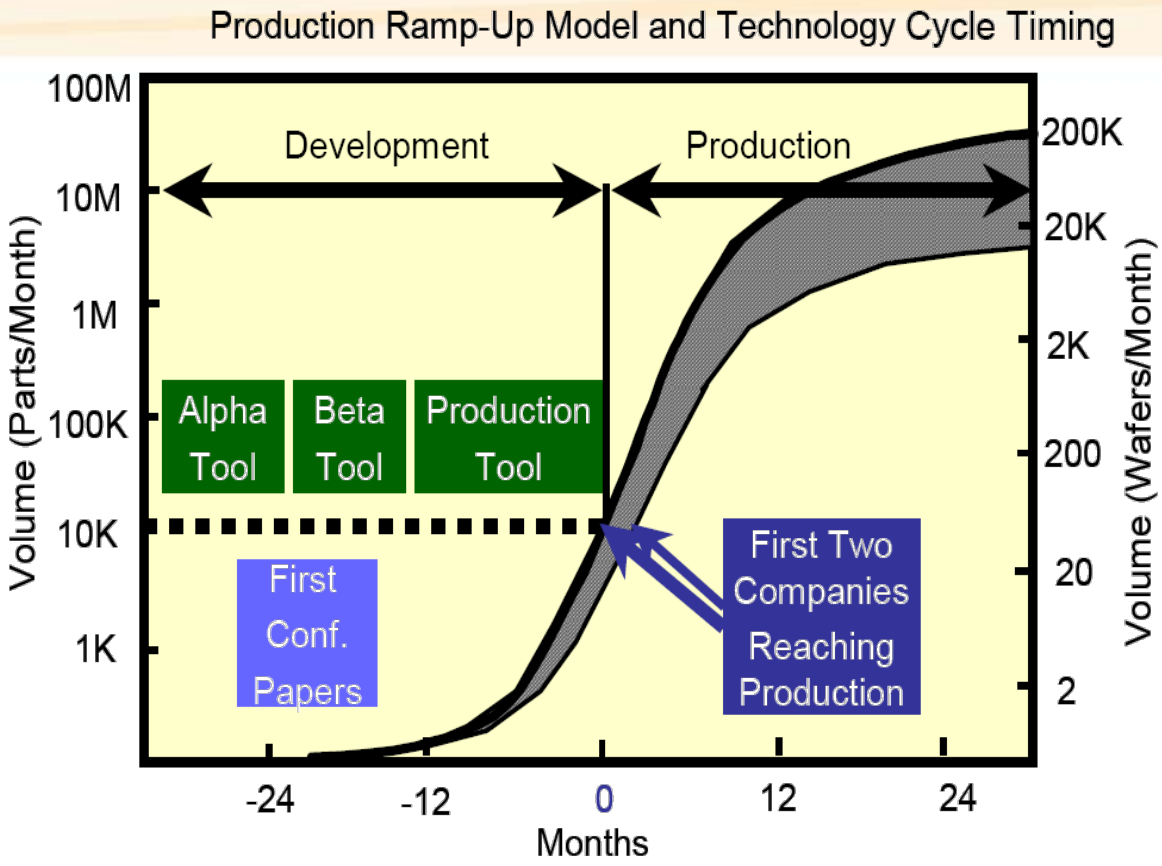
Metrology for Process Development and Process Control



Metrology and characterization techniques in Process development, Fab ramp-up and Production

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Fraunhofer IISB

European R&D and Support Activities for Metrology (selection)

- **ANNA** – FP6 project, 2007-2010
  - Integrate and enhance European analytical resources
  - Create a centre of excellence of analysis for nanotechnologies and a multi-site laboratory
- **SEA-NET** – FP6 project, 2006-2009
  - Validate emerging semiconductor manufacturing equipment for advanced process requirements at 65nm and below
  - Follow-up of this successful approach in FP7
- **Equipment Forums** – as part of integrated projects
  - Connect equipment suppliers to technology oriented projects
  - Relay results and knowledge to equipment companies, to foster the development of enhanced or novel equipment
  - Equipment forums implemented in:
    - PULLNANO – FP6 project, 2006-2008
    - IMPROVE – ENIAC project, 2009-2011

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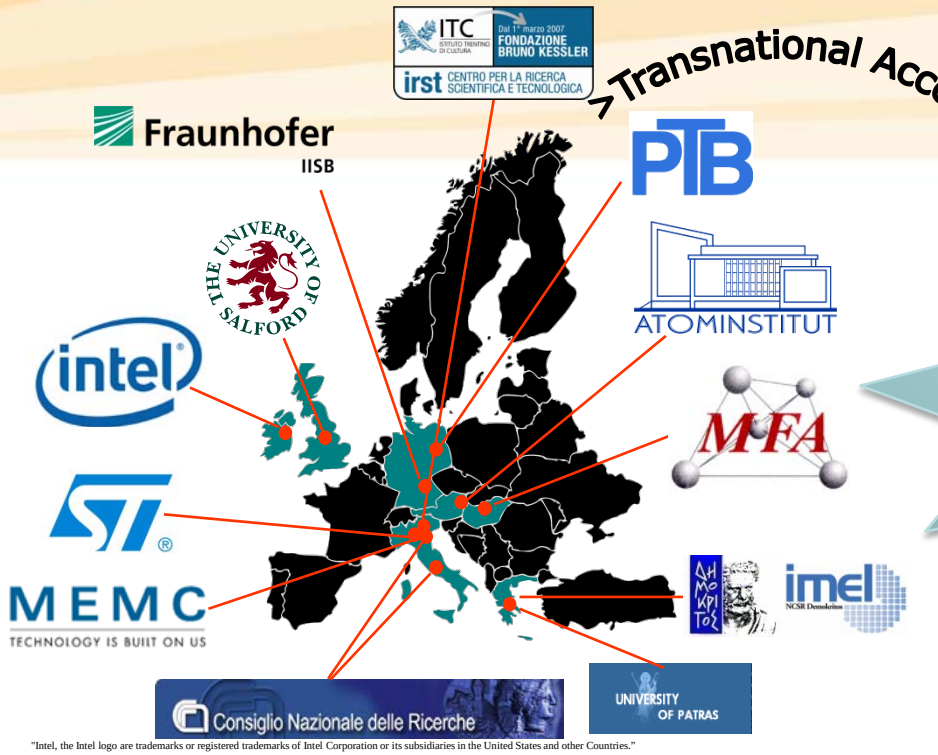
Results

Fraunhofer IISB

www.anna-i3.org

ANNA



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→ Transnational Access →→

Services
Reference Labs
Characterization
Analysis
Samples

ANNA - European Integrated Activity of Excellence and Networking for Nano and Micro- Electronics Analysis

Networking

→ standardization
→ establishment of certified reference laboratories

Transnational Access
access to laboratories of research institutes and universities (samples, characterization and analysis)

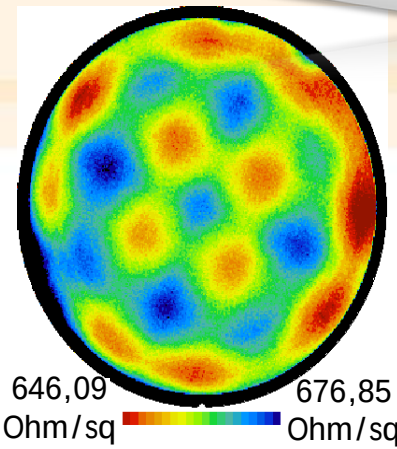
Joint Research
→ enhancement and extension of the methodologies
→ development of competencies

Results from SEA-NET: „LEAD-IT“

www.sea-net.info

LEAD-IT
Low Energy and Dose Implant Test

Use of junction photo-voltage to measure sheet resistance; capacitive pick-up electrodes measure the lateral voltage drop in implanted or epi layers



Sheet resistivity pattern of implanted layer

Benefits of LEAD-IT

- Fully automated 300 mm metrology tool for the measurement of sheet resistivity
- Non-contact metrology
- Non-destructive
- High speed
- High resolution

Partners: Semilab, Fraunhofer IISB, ST Microelectronics Crolles II, NXP Crolles R&D

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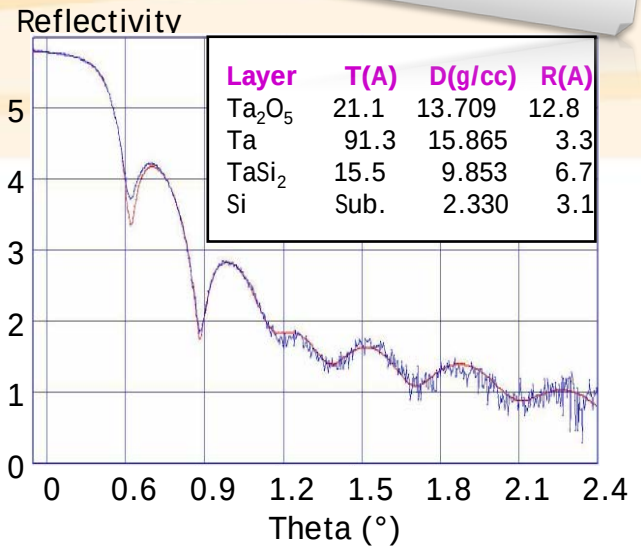
Results from SEA-NET: „MUXT“

www.sea-net.info

MUXT (“GIX tool”)
Metrology using X-Ray techniques

Gathering XRR and GI-SAXS in one metrology platform will allow the whole monitoring of Cu/low k interconnects



Reflectivity spectrum of a layer stack

Benefits of MUXT

- Fast and fully automated metrology techniques for thickness, density (porosity) and texture monitoring of thick and thin:
- Metallic layers: Cu, TaN, TiN, …
- Dielectric films: high k, low k

Partners: Jordan Valley, CEA-LETI, STMicroelectronics Crolles II, NXP Crolles R&D

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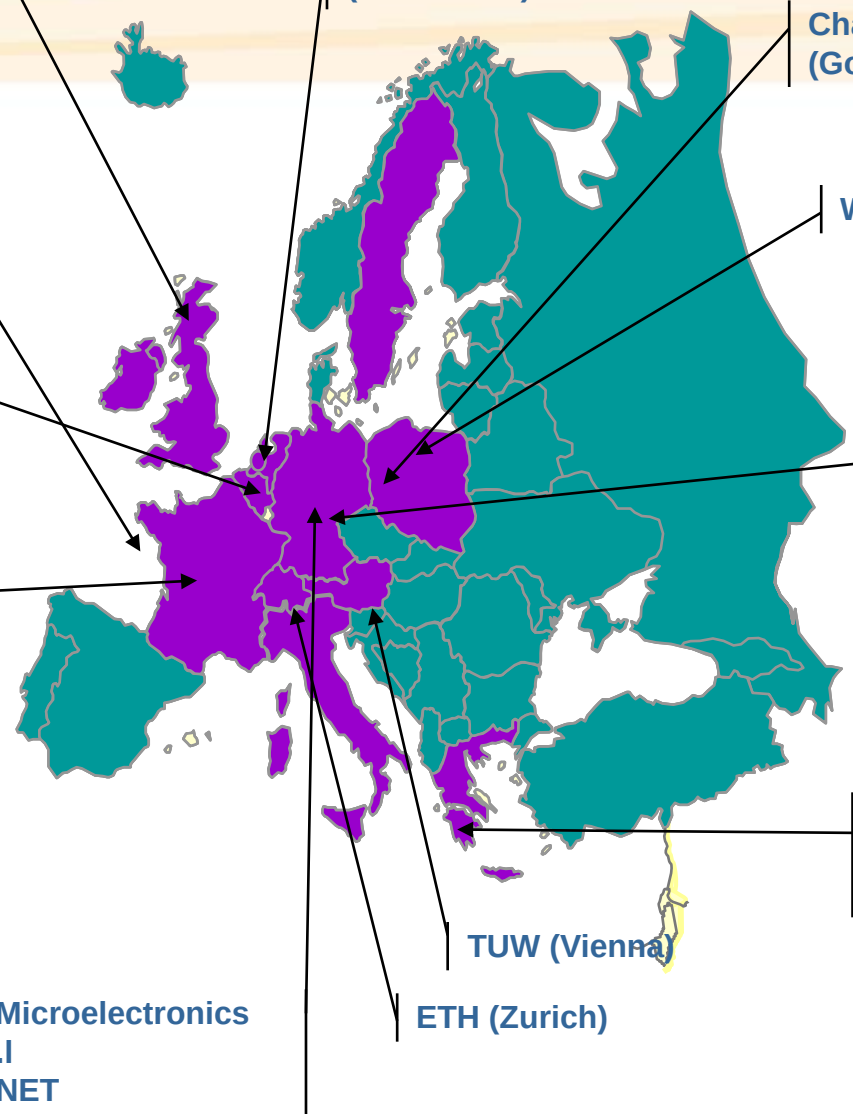
Industry, Academia, and Public Authorities Working Together

PullNano



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University of GLASGOW
University of LIVERPOOL
University of WARWICK
University of SURREY

PHILIPS (Eindhoven)

Chalmers University (Goteborg)

Tyndall Institute (U of Cork)

Warsaw University

PHILIPS Research
IMEC
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MAGWEL

Infineon
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AMO
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STMicroelectronics SA & SAS
Philips Semiconductors
Freescale Semiconductors
ESRF
CEA/LETI
CNRS(10 laboratories)
LACH (Universite de Savoie)
Ion Beam Services
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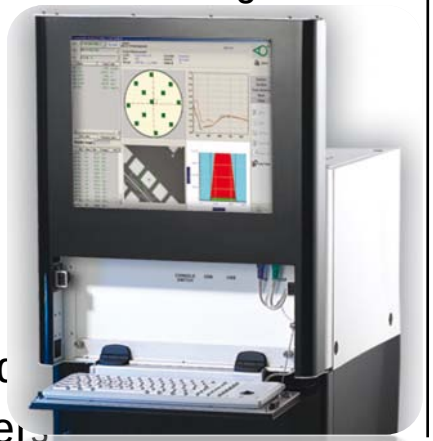
Results from Equipment Forum in PULLNANO

- **Scatterometry for Characterization of Sidewall Plasma Damage of Low-K Materials**
- Feasibility test of non-destructive characterization method of sidewall plasma damage, carried out on patterned product wafers without affecting the wafer flow
- **Partners**
- NOVA, IMEC

Result

- Characterization of plasma damaged sidewall low-k layers successfully demonstrated



Novel Integrated Flatness Metrology for CMP

Improve optical setups from NANOCMOS project for flatness measurement
(focus: improve lateral/vertical resolution)

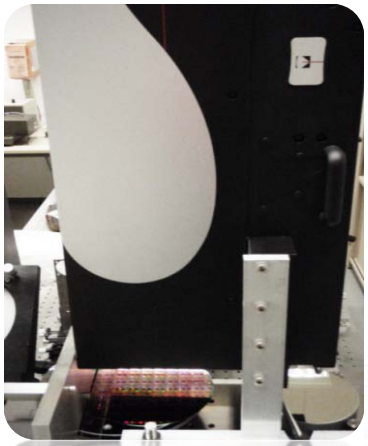
Partners

Imagine Optic
Fraunhofer IISB

Results

Drastically enhanced lateral/vertical resolution

Filtering software developed



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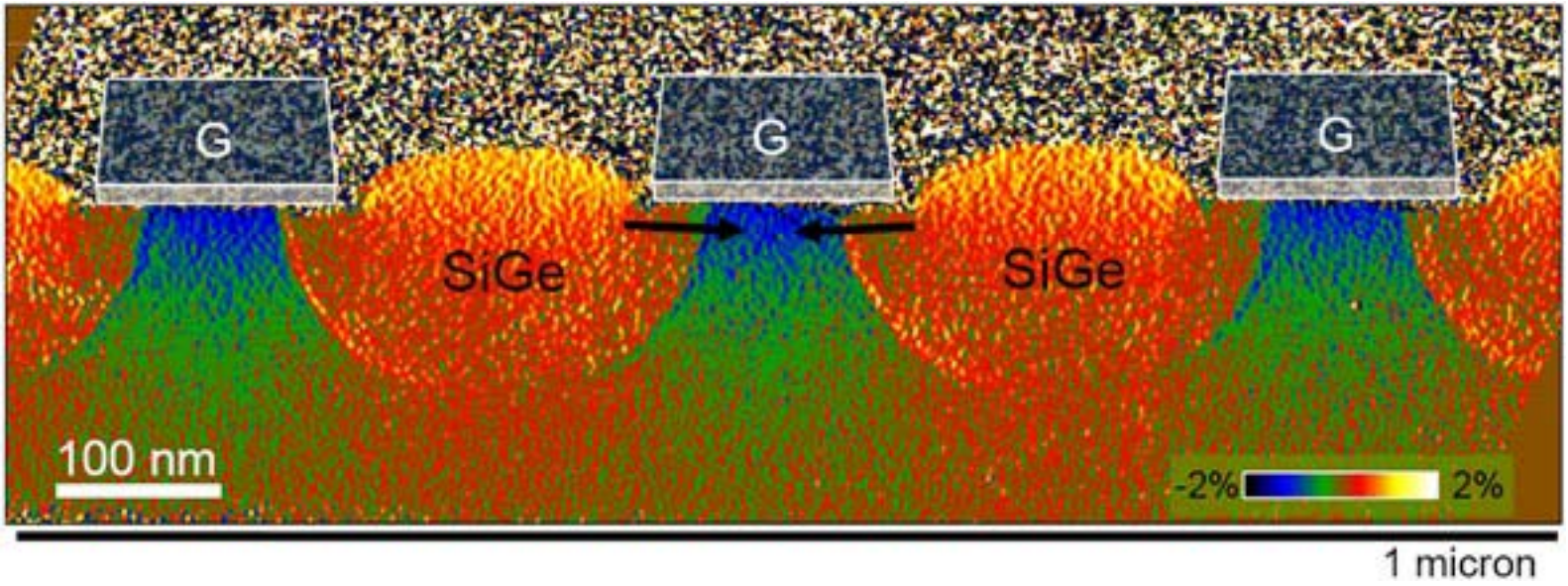
Breakthrough in strain metrology



Presentation Outline

- R&D Infrastructure and Production sites in Europe
- European R&D Programmes FP7, ENIAC and Catrene
- Metrology and Characterization –Project examples
- Summary and conclusion

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Summary (1)

- **Current and future challenges for metrology and characterisation (Sub-32 nm, new materials, 450mm)**

- **Europe has to cope with the changing industrial structure of its industry, wants to safeguard major European competences on European soil and wants to optimise the transfer of research results in innovation for economic leadership and socio-economic purposes**

- **Lining up all available resources, funding and mechanisms (FP7 – JTI – Eureka – national (poles de competitivité)) towards a common global European vision supported by industry, targeting major holistic initiatives will be a powerful approach to increase the competitivity of European industry at large and to generate extra high quality jobs**

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Summary (2)

- **The European Commission will invest in nanoelectronics:**

*** (500 +) MEuro funding from regular FP7,**

*** contribute to a 3BEuro worth Program in Public Private Partnership with industry and Member States (420 MEuro FP7; 820 MEuro from Member States, rest from industry)**

*** coordinate / cooperate with other Eureka, Member States or Regional Initiatives (incl. education and infrastructure) and internationally to fulfil (part of) the European Strategic Research Agenda for cooperative RTD in nanoelectronics**

- **Europe has embarked on a strategy to be a player in global cooperation and to compete on excellence where possible**

- **Mega-fabs may be locating in Asia; smaller, more flexible fabs will continue to prosper in Europe**

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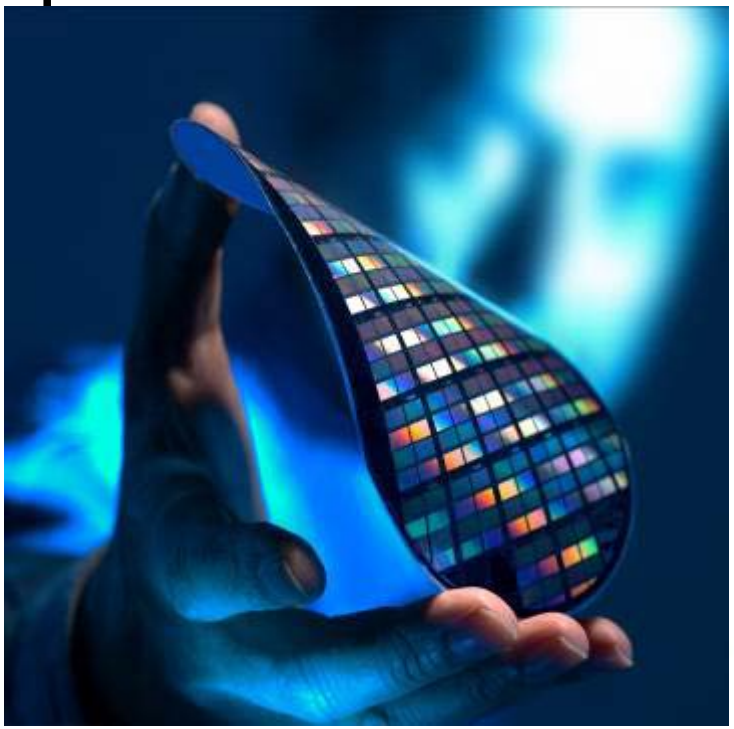
Conclusion

Europe has something to offer:

High technology material and equipment companies, innovative system integrators, continued contributions from research consortia such as IMEC, LETI, Fhg and Tyndall and universities, contribution from innovation regions (poles de competitivité) and initiatives like ENIAC, CATRENE and the Framework have to keep Europe in the centre of innovation in nanoelectronics.



Courtesy Fraunhofer IZM

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Contact:

Gisele.Roesems@ec.europa.eu

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