Examination of Advanced Technologies in Characterization, Diagnostics, and Verification at Different Stages in the Manufacturing Lifecycle of Packaged IC Devices

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Agenda

- Mold thickness metrology
- Fault isolation
- System level test

Corporate Overview

Founded:	1954, Tokyo, Japan
U.S. Head Office:	San Jose, CA
Europe Head Office:	Munich, Germany
Other Major Subsidiaries:	Singapore, South Korea, Taiwan, China
Business:	Semiconductor ATE Mechatronics Systems Services, Support & Others
Publicly Traded:	Tokyo Stock Exchange (6857)
Capital:	32.4 Billion Yen
Consolidated Sales:	162.1 Billion Yen (FY2015)
No. of Employees:	4,494 Worldwide (as of March 2016)

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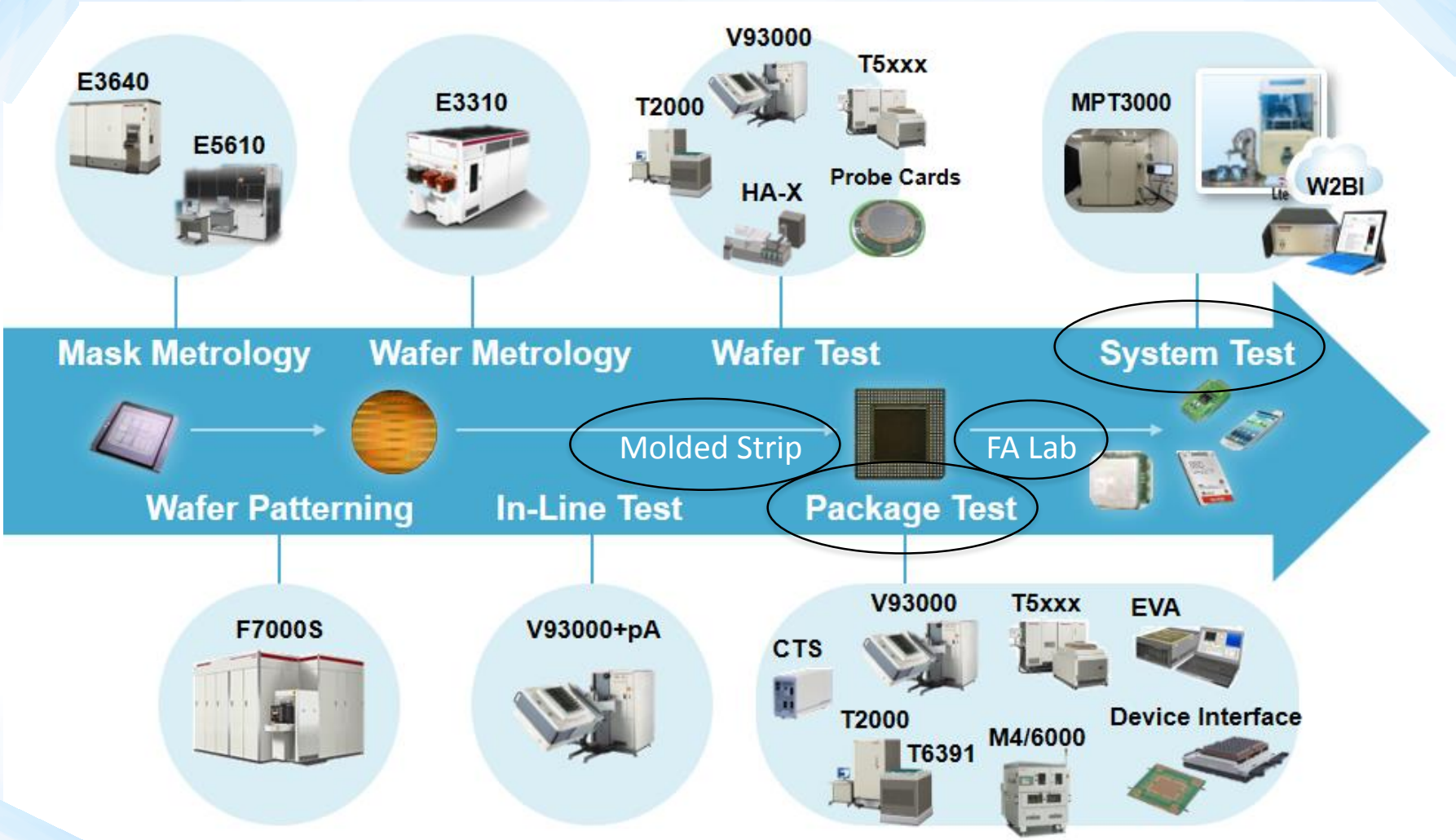
Advantest in Semiconductor Manufacturing



Nondestructive Mold Thickness Metrology for Characterization of Mobile Devices

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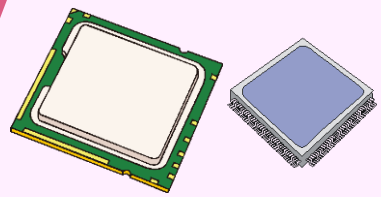
Trouble with mold quality

Mobile phone

Tablet

Thin laptop PC



IC chip needs

- *much smaller*
- *much thinner*
- *Higher density mounting*

Thin and high strength molding is necessary

- Molding of chip must have:
  - thin layer with high strength
  - no warps, no bend
- Chip molding defects result in:
  - damage to die and wiring
  - impact to yield

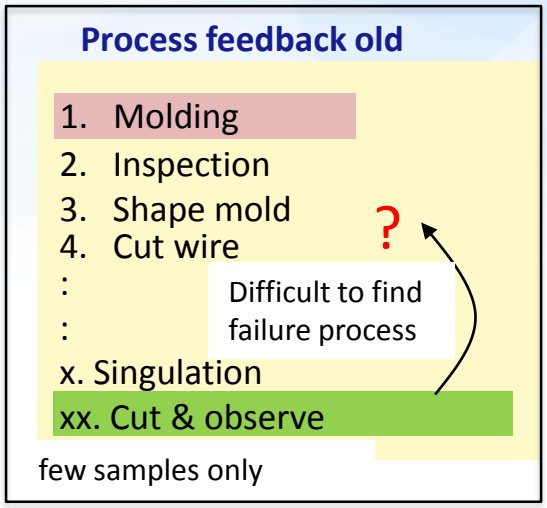
Quality of molding for protecting die and wires is important

Methodology of mold thickness analysis

In present method :

Cut device and observe edge by microscope

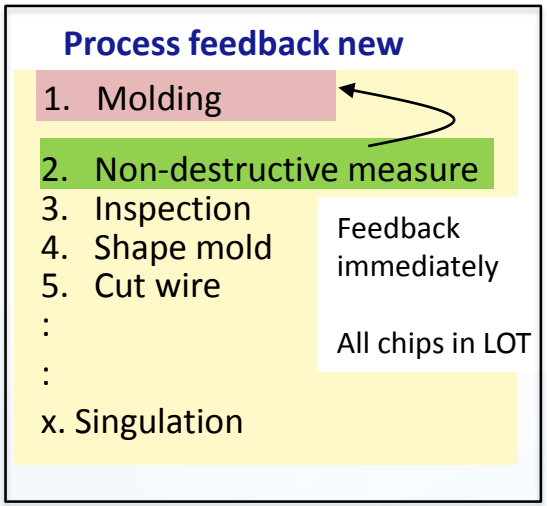
- Limited sample count
- Difficult to understand trends of mold defects in lots
- Difficult to feedback defect info to molding process



In new method :

Non-destructive measurement

- High volume measurement possible
- Understand trend of defects on strip in each lot
- Fix problems much earlier in the process



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Needed mold thickness measurement solution

- Non-Destructive
  - Non-ionizing, non-heating - does not affect the sample in any way
- Fast high speed measurement for high volume
  - Suitable for volume samples in production environment
  - 250 units/hour, multiple points per device, automatic measurements
- Highly reliable
  - Accuracy roughly 1% at 500um
  - Near zero bias

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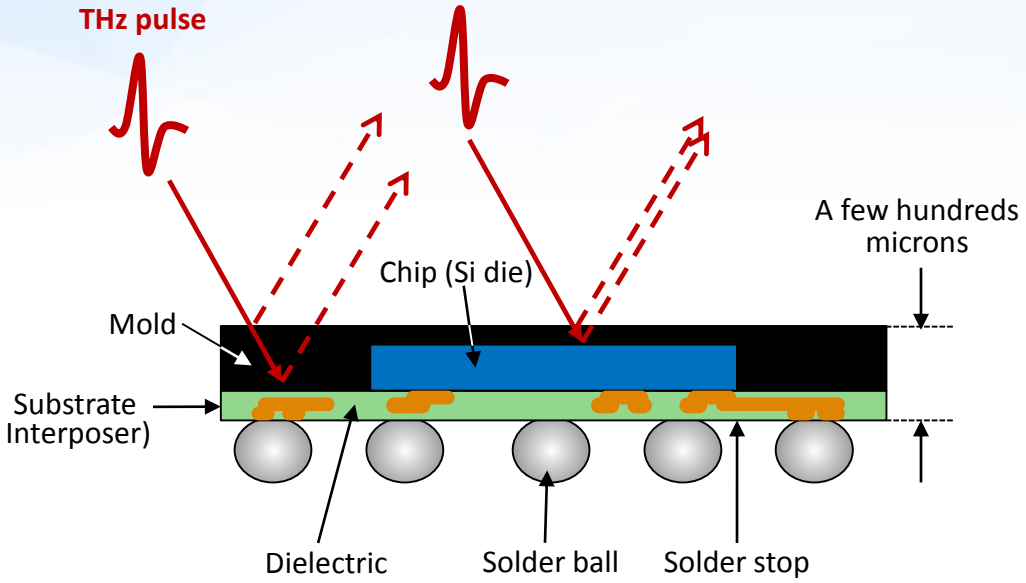
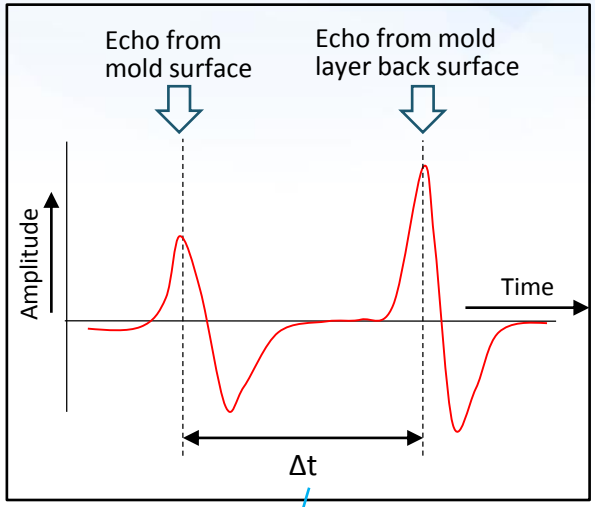
Applying THz wave to mold layer thickness metrology

❑ Applying THz time of flight (TOF) to mold thickness metrology



Reflected terahertz wave



THz TOF is a promising metrology method

☺ Mold material (plastic) is transparent for THz wave

☺ Adequate mold thickness range
- 30 μm to several hundred microns

☺ Obvious refractive index differences between:
- mold and Si die
- mold and substrate

$$\text{thickness} = \frac{\Delta t \, c \cos\theta}{2n}$$

Δt : time delay
θ : Incident angle of terahertz wave
c : Speed of light
n : refractive index of mold

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Mold thickness analysis setup

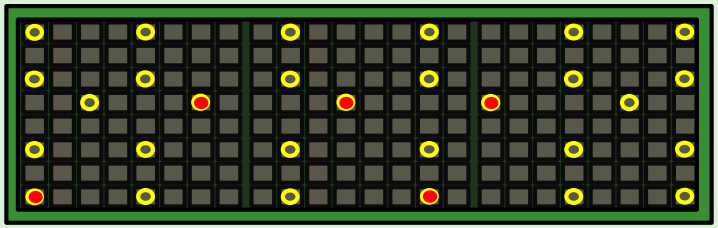
Features

- **Nondestructive mold thickness testing using THz TOF method.**
- **Automated multiple point measurement on singulated chips on JEDEC trays or strips**
  - **250 units per hour**
  - **Multiple points measurement on each unit**
- **Precise and robust operation**
  - **Precision: ±3 µm**

Example of mold thickness test result

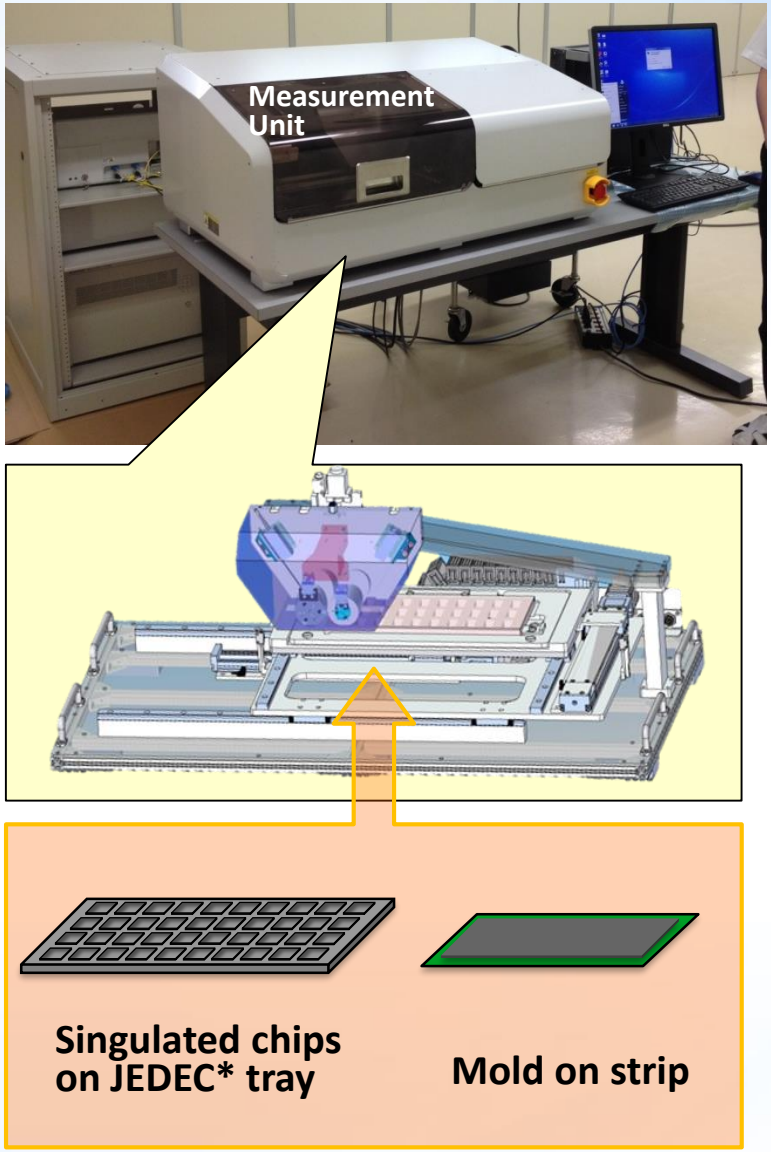
Pass

Fail



Thickness data

	A	C	E	G	I	K	M	O	Q	S	U	W
1	250.3		251.3		249.3		251.0		250.3		250.3	
3	247.2		249.2		246.3		250.3		247.2		250.2	
4		248.4		255.3		254.8		254.2		248.4		248.4
6	252.4		253.1		251.9		253.0		252.0		252.1	
8	253.8		250.1		250.9		254.2		251.4		251.1	



*** Joint Electron Device Engineering Council**

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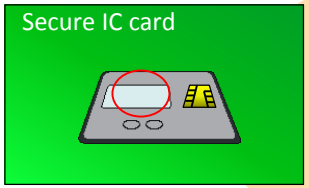
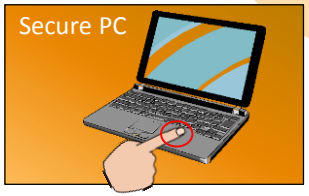
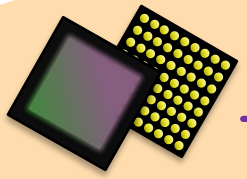
Fingerprint Sensor Example – Mold Thickness

- Mold thickness distribution must be flat/evenly distributed on array for error free finger print sensing
- Must be measured within few micrometer order accurate for thickness quality control.

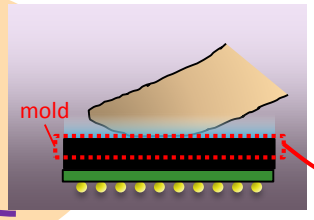


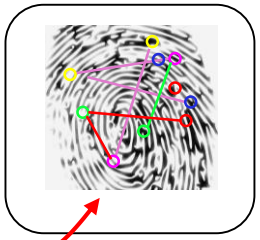


Small & thin FPS production is increasing
Thinner packaging is necessary for mounting in very small spaces
Thinner molding is required for smaller packages



Finger Print Sensor Device



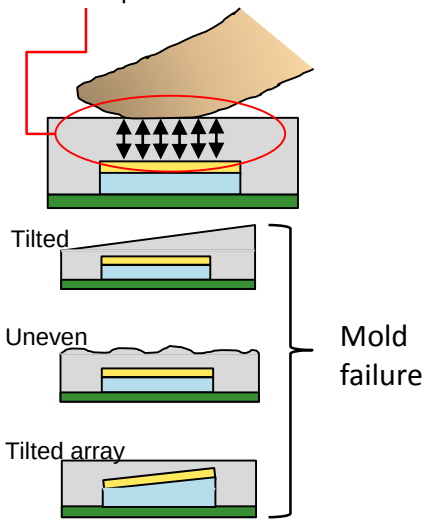


Unevenness of mold on array
Causes pattern reading error

Mold layer thickness must be distributed in flat, evenly, no tilt, for the error free fingerprint pattern capturing

Need high accurate measurement system in production for better quality control.

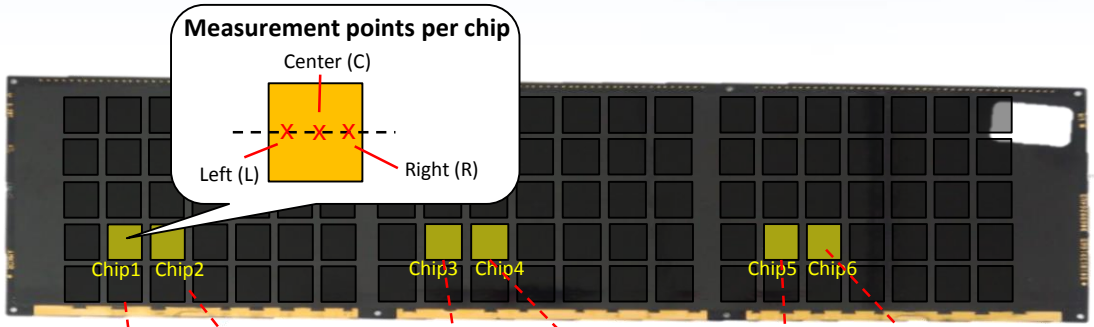
Read pattern on array is charge difference
→ mold layer must be flat within around 50µm.



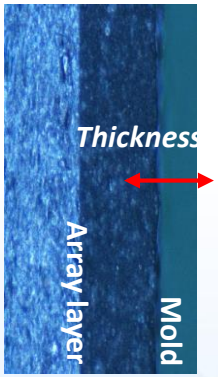
FPS Mold thickness measurement example

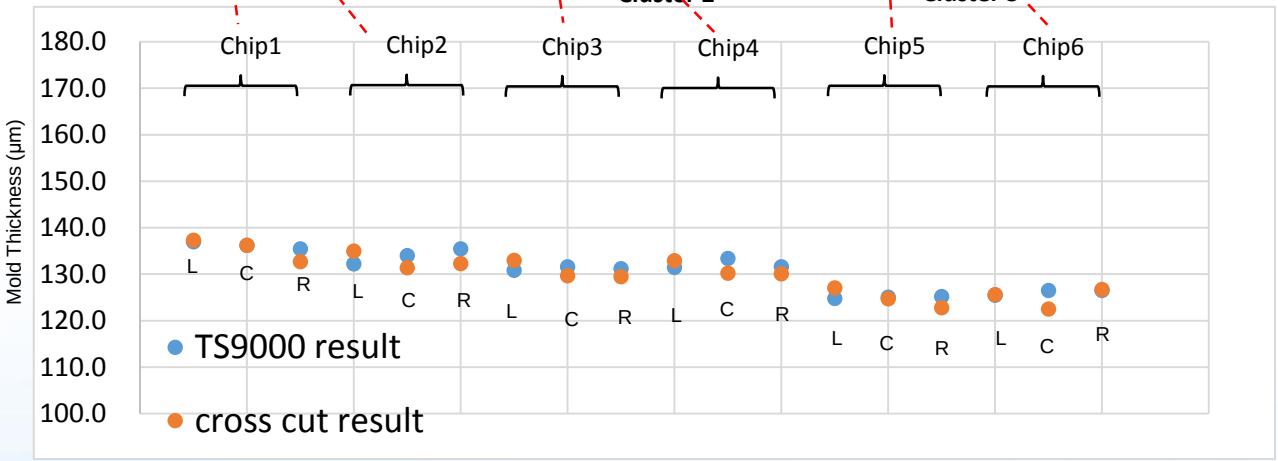
Sample: Static capacitance type FPS, 160x160 pixels chips.
Experiment: Thickness data comparison with cut view observed result.
Result: All thickness difference to cut view are within <±5 µm.

FPS sample (singulated)



Cross sectional view (Microscope)





High Resolution TDR Tool for Diagnostic Failure Investigation in Complex IC Devices

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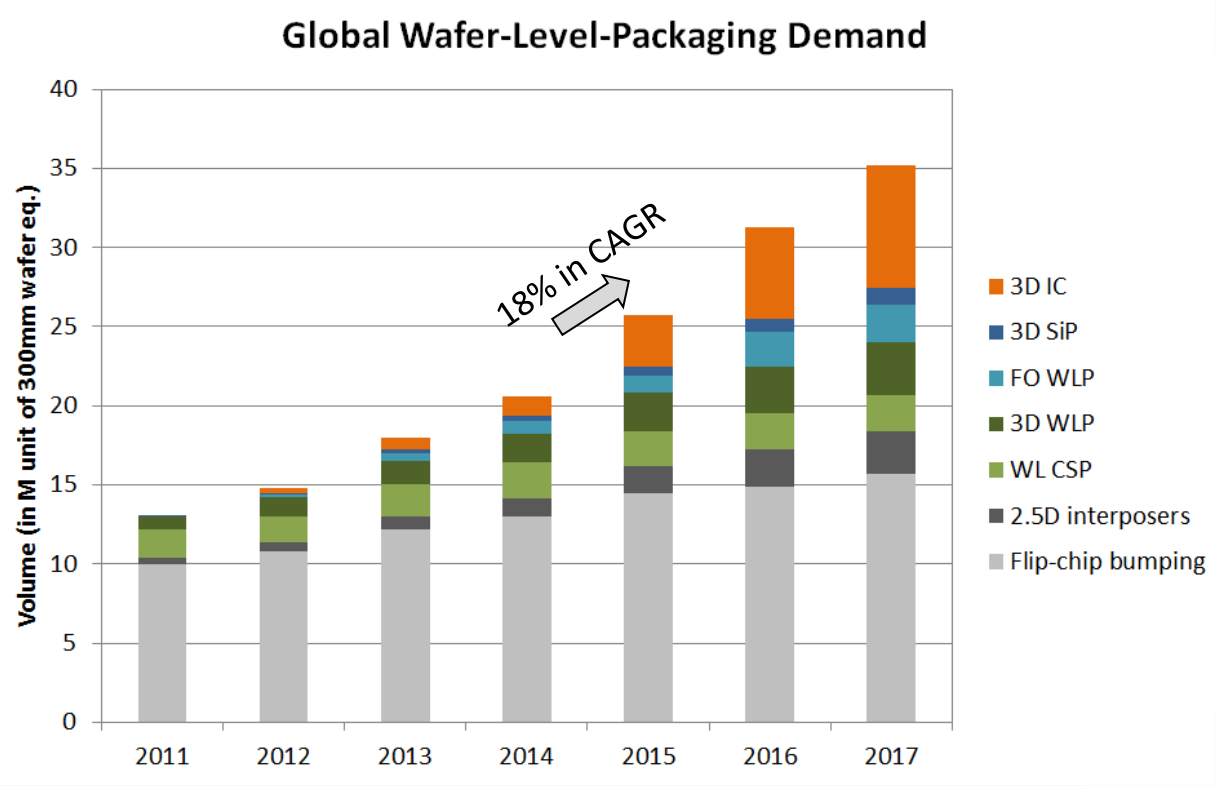
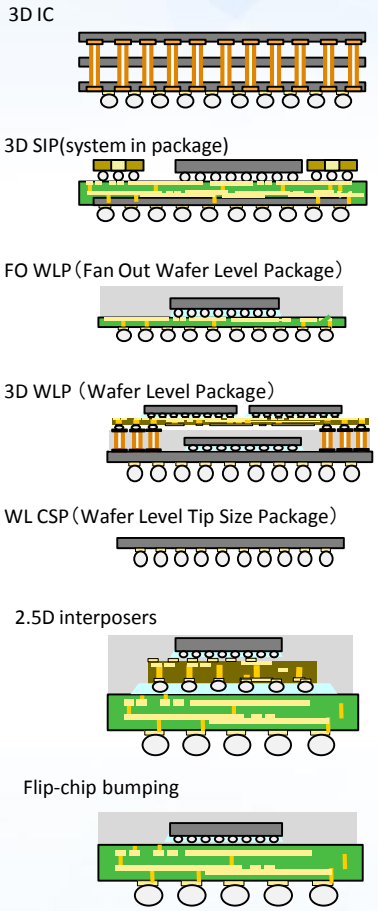
3D integrated semiconductor device trend

2.5D and 3D integration technologies are driving the integration of devices with extremely high interconnect densities and taking place of conventional flip chip bumping technology.





Source : Yole development 2013, “Packaging Key for System Integration,” http: //www.semi.org/eu/sites/semi.org/files/docs

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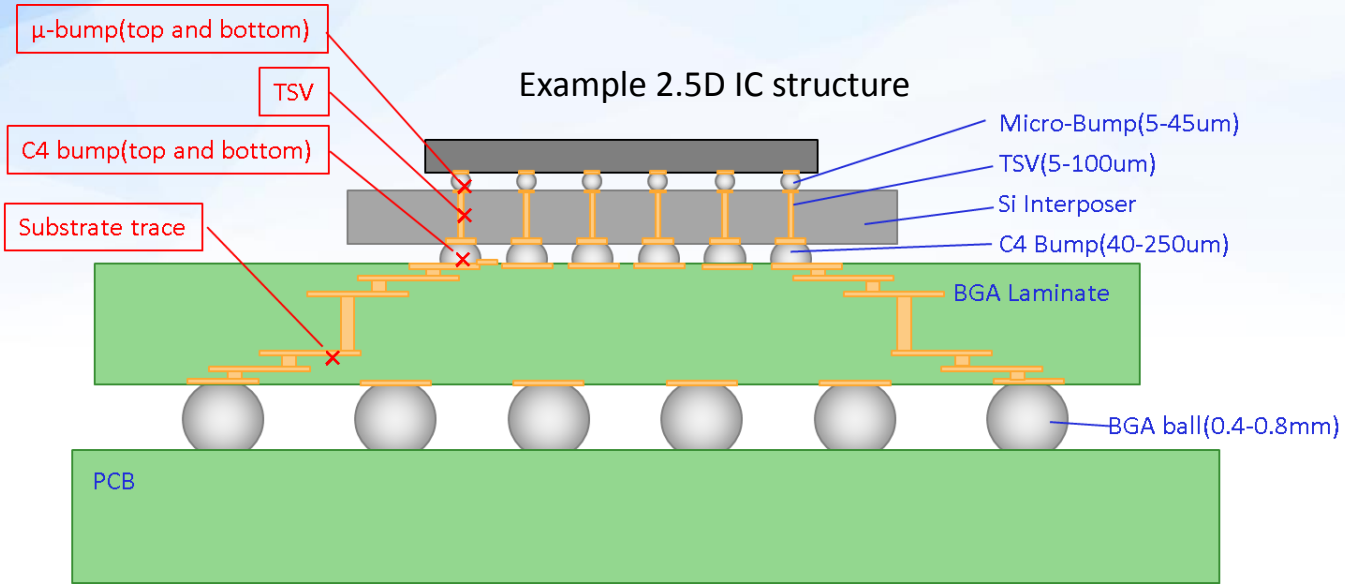
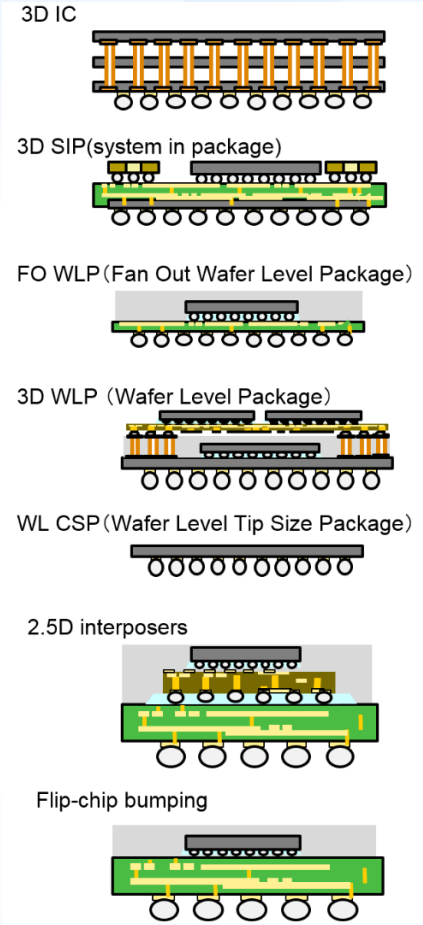
TDR Measurement Needed for 3D Integrated Substrates



Many Package Types



- **Present method (oscilloscope)**
  - Poor spatial resolution due to large rise time and high jitter
  - Resolution limit: Hundreds of µm
- **Needed capabilities:**
  - Detect failures to 5µm → highly accurate failure point location
  - Wider length 300mm → measure long propagation lines
  - Software → analysis to help find failure location

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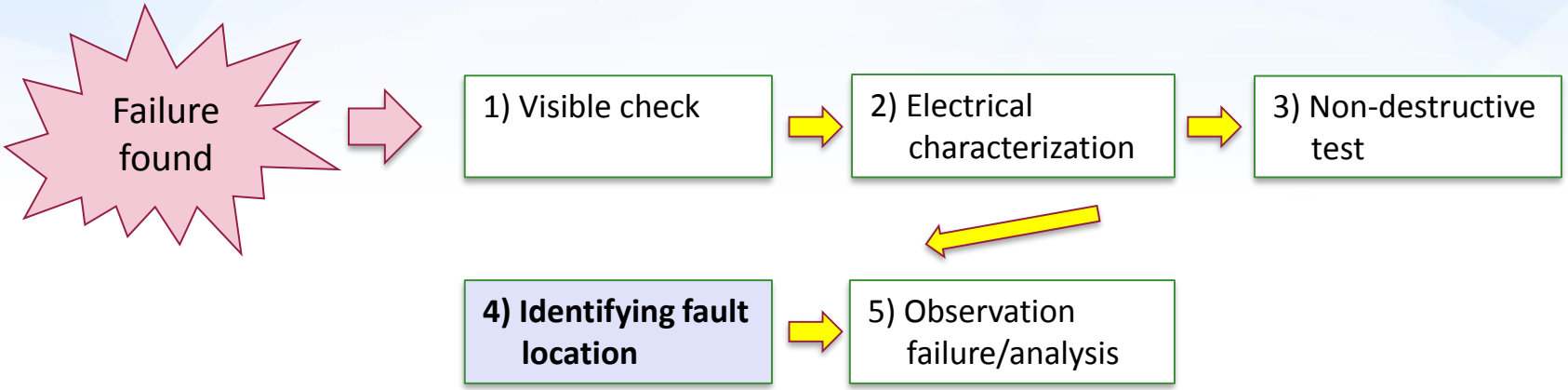
Semiconductor device failure analysis flow

- To identify failure points, emission microscope or oscilloscope TDR are used as usual, however, these methods are limited in identifying OPEN/SHORT fails with high resolution.



Process	Analysis items	Analysis method
1) Visible check	Delamination/lack	Scanning acoustic microscope(SAM), Scanning acoustic tomography (SAT), transmit X ray, X ray CT
2) Electrical characteristics	Logic and analog functional/structure test	LSI test system, oscilloscope, network analyzer
3) Non-destructive test 4) Identifying failure points	Line connection fail (SHORT failure)	Emission microscope (EMS) ⇒OPEN failure can not be detect
	Line connection fail (OPEN failure)	Oscilloscope TDR ⇒ Less resolution (less than a few hundreds μm)
5) Observation of failure and analysis	Observe cut view(3D_CT)	Transmission X ray, X ray CT
	Observe surface(nano-scale)	Scanning Electron Microscope (SEM)
	Crystal particle observe(nano-scale)	Transmission Electron Microscope (TEM)
	Surface roughness test (nano-scale)	Atomic force Microscope (AFM), scanning probe microscope (SPM)

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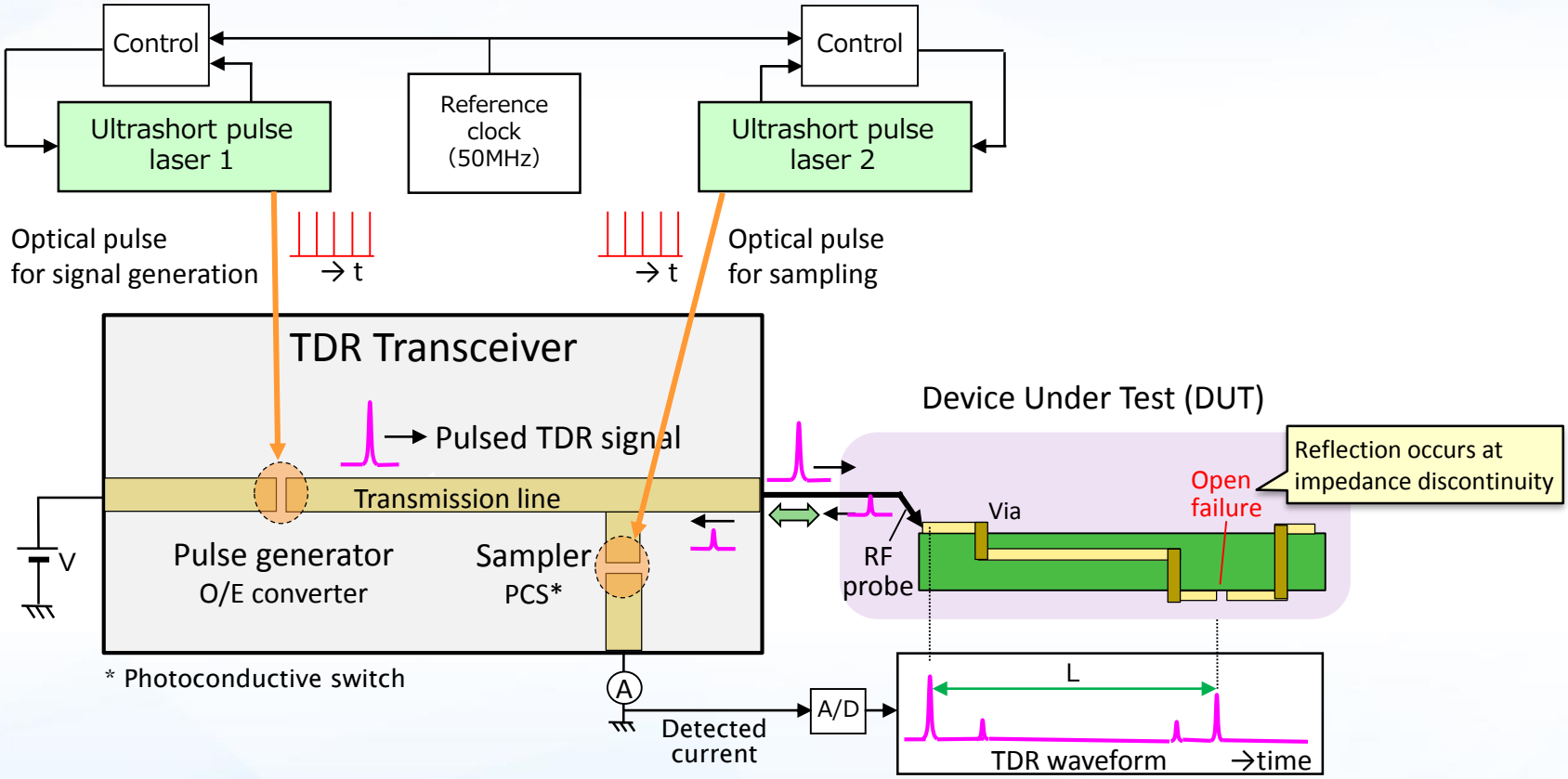
Solution to achieve high-resolution fault isolation

Time domain reflectometry (TDR) with ultrafast pulse

- Developed TDR transceiver, consisting of optical based ultrafast pulse generator and sampler.
- The generated pulse includes ultra-broad frequency component from sub-millimeter to sub-terahertz range



Excellent pulse quality of low jitter (< 40 fs) and ultrafast rise time (< 12 ps) gives high resolution fault isolation capability.

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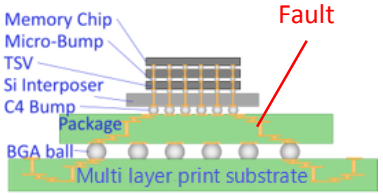
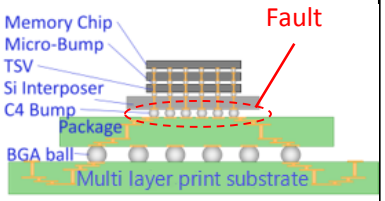
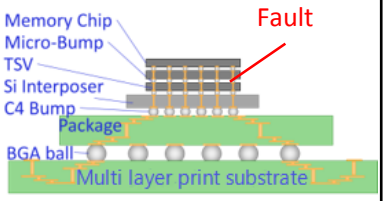
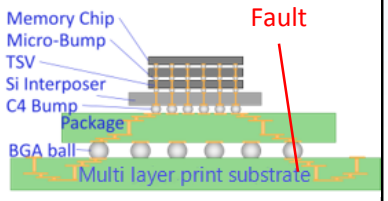
FI/FA capability comparison: pulsed TDR vs. conv. TDR

Case #	1			2			3			4		
Fault analysis target portion in the package	Wiring in the package 			Si interposer (C4 bump) 			Multi layer memory (TSV, Micro-bump) 			Wiring failure in printed circuit board 		
Necessary performance	Ideal	Conv. TDR	TS9000	Ideal	Conv. TDR	TS9000	Ideal	Conv. TDR	TS9000	Ideal	Conv. TDR	TS9000
Distance-to-fault resolution (µm)	< 100	✓/×	✓ **<5**	< 100	✓/×	✓ **<5**	< 30	×	✓ **< 5**	< 100	✓/×	✓ **< 5**
Near end dead zone (µm)	< 200	×	✓ **< 200**	< 200	×	✓ **< 200**	< 30	×	✓	< 200	×	✓ **< 200**
Maximum measurable distance (mm)	300	✓ **> 300**	✓ **> 300**	10	✓ **> 300**	✓ **> 300**	10	✓ **> 300**	✓ **> 300**	300	✓ **> 300**	✓ **> 300**
Repeatability of contact (µm)	< 30	×	✓ **< 10**	< 15	×	✓ **< 10**	<10	×	✓ **< 10**	< 30	×	✓ **< 10**

- High resolution analysis capability of TS9000 enables failure analysis on high-dense 3D/2.5D semiconductor packages.

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TDR/TDT Setup

System configuration

Probe Station

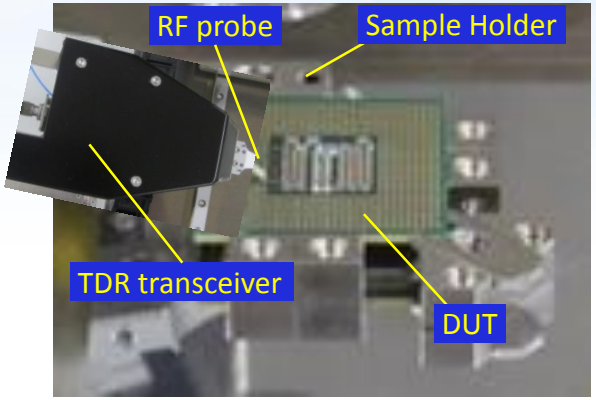
Measurement Unit

Optical Delay Unit

Analysis Unit

System Controller

Probe contact in the probe station



Performance/functions

Items	function		specification
TDR/TDT capability	Measurement mode		TDR, TDT (optional)
	Distance-to-fault resolution		< 5 µm
	Rise time (Tr)		12 ps （6 ps and 25 ps are optional)
	Maximum measurable distance	TDR	> 300 mm@ε_{eff} = 3
		TDT	> 600 mm@ε_{eff} = 3
Analysis function	TDR/TDT Analyzer		• View subtraction of sample and reference as the known-good device data. • Peak search/multiple reflection marking
	CAD Data Link (optional)		• Estimated fault location view at each CAD layer trace.
Measurement support function	Auto probing		• Soft touch down preventing from probe damage.

1. Fully automated touchdown and probing
2. Recipe-based sequential measurement
3. Software analysis
4. Failure location estimation and indication on CAD drawing

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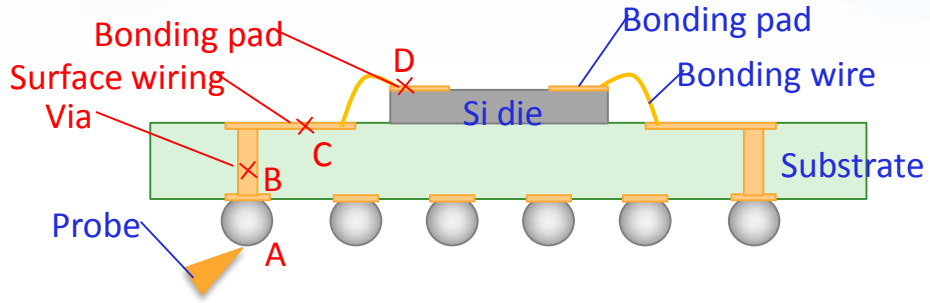
Failure analysis case: Small BGA package

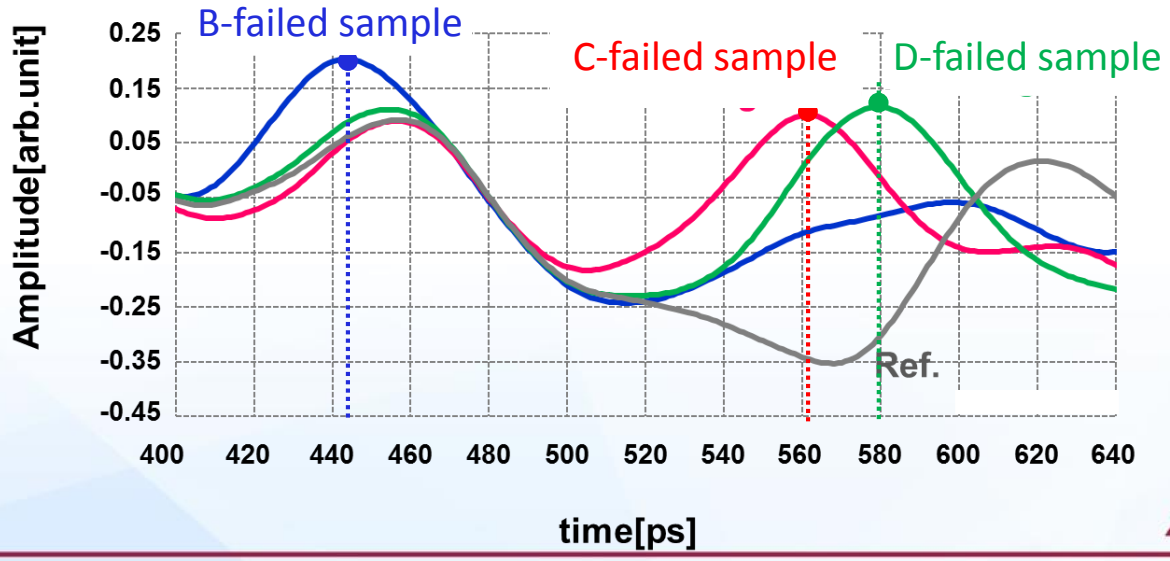
- Small-BGA has more complexed structure than QFP package
- Failures (via, surface wiring and bonding pad) were made intentionally.

⇒ **Failure locations were significantly discriminated by reflected pulse position**

Small-BGA sample structure



TDR measurement result



Thermal Challenges in Endurance vs. Production SSD Testing

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Endurance vs. Production Test Thermal Challenges

- Endurance Test (or RDT) ensures the device design and manufacturing process meets reliability claims
  - Tight control of test conditions needed to prove results are statistically valid
  - ±5 deg. C per JEDEC (JESD218A)
- Production test ensures that a particular drive was manufactured successfully to specification
  - Devices need to be stressed above the test threshold

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Why Thermal Stress Test

- For endurance testing, thermal stress accelerates the time to fail (greatly shortening test time)
- Acceleration adheres to the Arrhenius equation

Arrhenius Equation

Predicting Temperature Dependence on Time to Fail

$$t_f = Ae^{E_A/kT}$$

t_f: time to fail **A**: acceleration factor **E_A**: activation energy;
T: temperature k: Boltzmann's constant

- This covers many failure modes of electronics

but not, for example, failures causes by mechanical fatigue

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Temperature, Test Time Relationship During Endurance Testing

$$\textbf{Stress Test Time} \propto \frac{1}{\textbf{Stress Temperature}}$$

JEDEC Standard 218 uses the Arrhenius Equation in this form for calculations of temperature-accelerated stress times:

$$t_S\left[FH_S Ae^{E_A/kT_{S.H}} + (1 - FH_S)Ae^{E_A/kT_{S.L}}\right] \leq t_U\left[FH_U Ae^{E_A/kT_{U.H}} + (1 - FH_U)Ae^{E_A/kT_{U.L}}\right]$$

From JESD218A Annex B assumes no added delays

Or to show the stress test time:

$$t_S \leq t_U \frac{FH_U Ae^{E_A/kT_{U.H}} + (1 - FH_U)Ae^{E_A/kT_{U.L}}}{FH_S Ae^{E_A/kT_{S.H}} + (1 - FH_S)Ae^{E_A/kT_{S.L}}}$$

Relevant to us $t_S \leq F(T_{S,H})$

A = constant scaling factor (this drops out of the calculations)
t = time (in any units as long as all t values are in the same units)
T = Température in ^{o}K
E_A = Activation energy, assumed to be 1.1 eV
k = Boltzmann's constant, 8.6171·10-5 eV/^{o}K
FH = Fraction of time spent at high temperature
$_S$ = Subscript denoting the endurance stress itself
$_U$ = Subscript denoting the use condition (enterprise vs. client)
$_H$ = Subscript denoting the high temperature of interest
$_L$ = Subscript denoting the low temperature of interest

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Factors Affecting Thermal Consistency in Multiple DUT Chamber

- Chamber Performance Factors
  - Total air flow and temperature
  - Air guides and baffles
  - DUT count, locations, and spacing
- DUT power consumption
  - Power generated = heat; heat must be removed
  - Worst case is with all DUTs at full power
  - New PCIe 3.0 DUTs can be 25W compared to <10W for SATA

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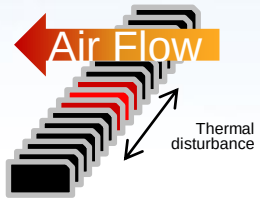
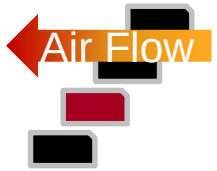
Multi-DUT Chamber Considerations
DUT Spacing

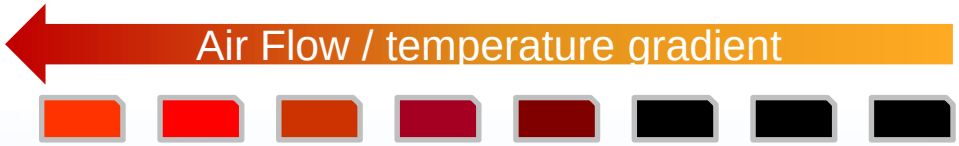
= 1 DUT

- DUTs positioning perpendicular to airflow
  - Too close: thermal disturbance between DUTs
  - Too far apart: more expensive (floorspace)
  - Need to balance spacing with airflow and air temperature





- DUT positioning inline with air flow
  - A gradient in temperature will occur
  - Need to balance airflow and number of DUTs in series



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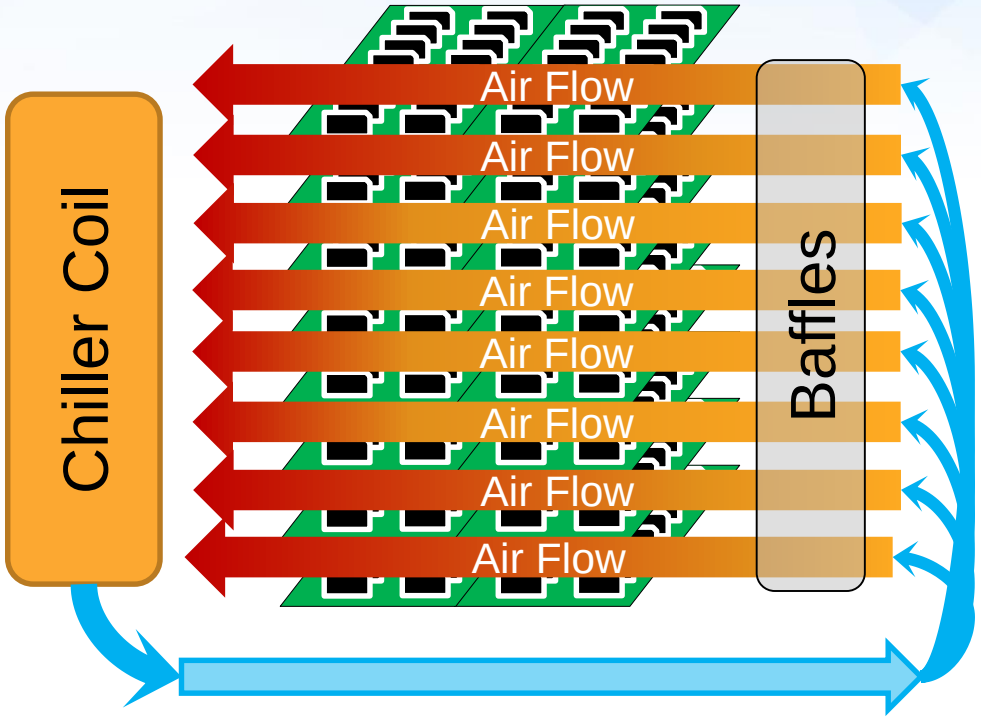
Multi-DUT Chamber Considerations Vertical Positioning

- Airflow loops through chamber to the compressor
- Baffles are needed to guide air into the chamber evenly
- Here is one scenario for 25W DUTs to meet ±5oC
  - 4 levels per chamber
  - 8 DUTs deep
  - 4 DUTs long
- Note: two chambers per 256 DUT system



Poor baffling or too many vertical layers in a single chamber causes vertical temperature gradient

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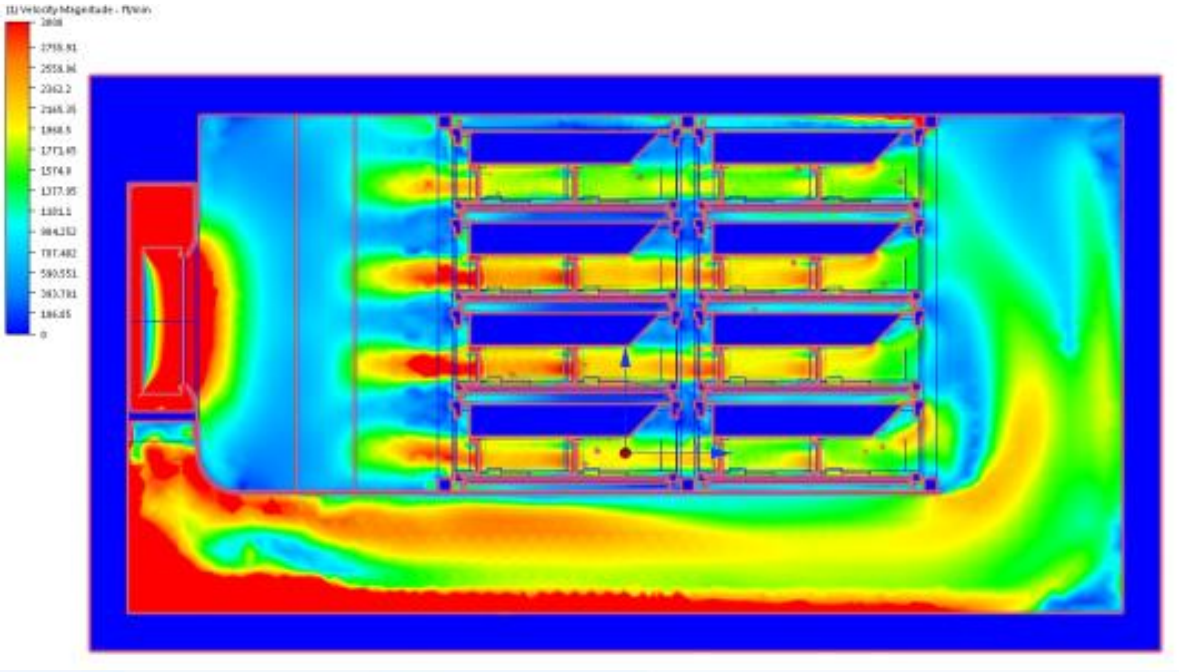
Multi-DUT Thermal Chamber Design

- Air flow is complex,
  - Sophisticated simulation, including baffles and DUT form factors is necessary to aid chamber design including baffles and DUT form factors



Thermal chamber airflow simulation

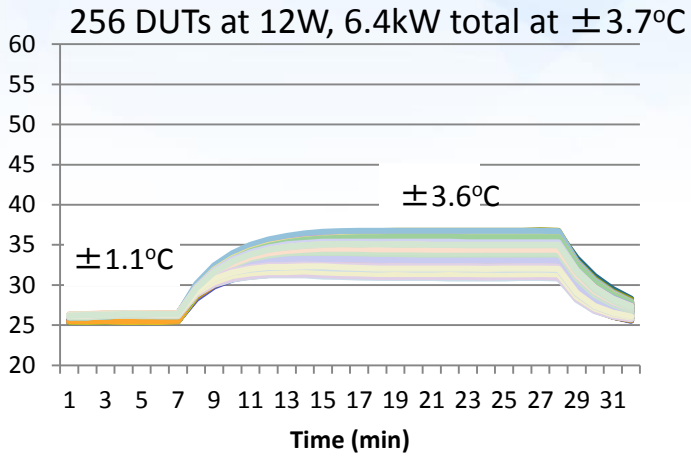
DUT Power Sensitivity

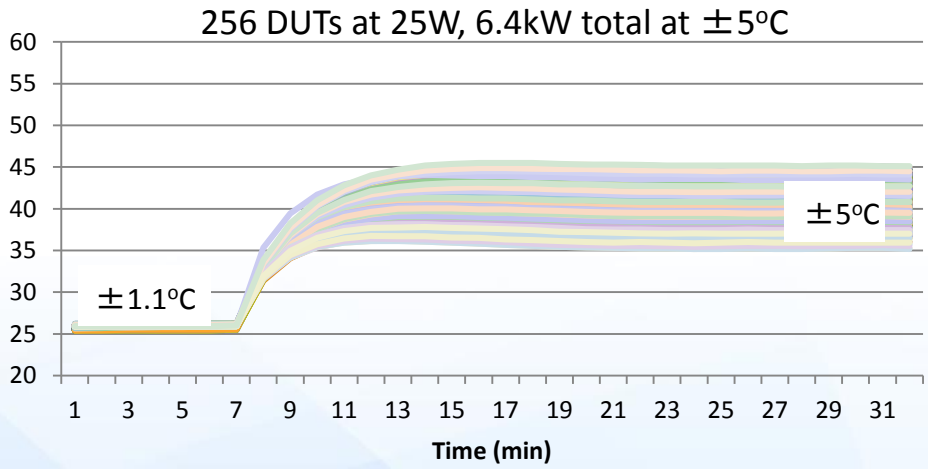
DUT Power vs. Thermal Consistency

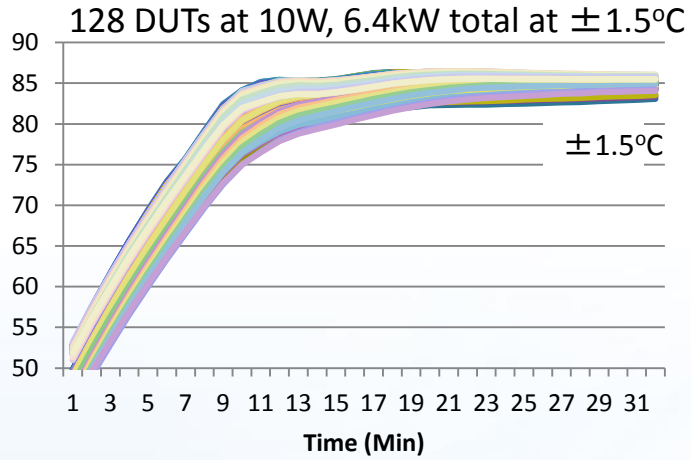
- 256 @0W +/-1.1C
- 128 @10W +/- 1.5C
- 256 @12W +/- 3.6C
- 256 @25W +/- 5.0C

  Set point does not affect consistency (in operating range)

  Set point is air temp, device temp is much higher







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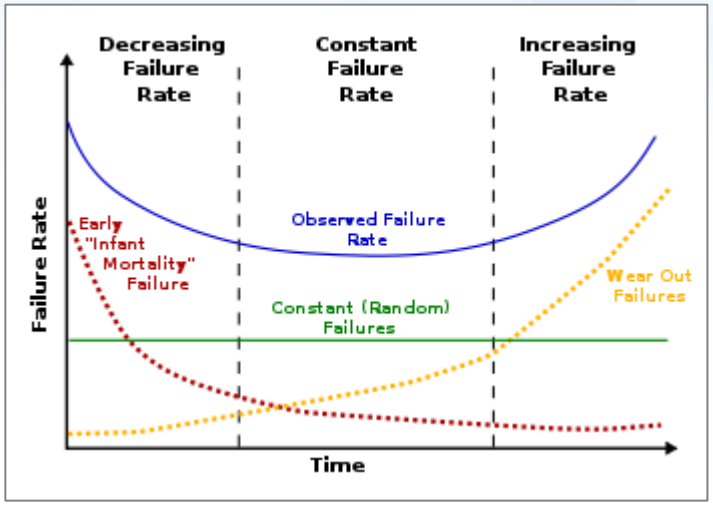
Production Test

- Bathtub curve
- Need to reach a minimum threshold temp to trigger an infant failures
- Lower temp may allow escapes
- Higher temp may cause yield hit, depending on device resilience



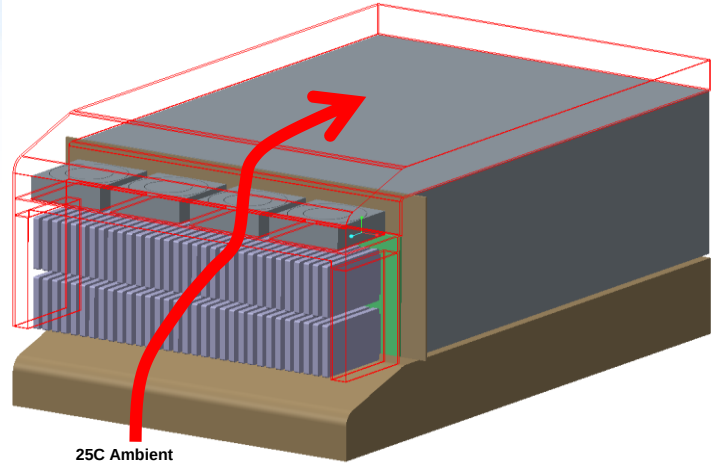
- Therefore
  - Meeting a minimum temperature is required
  - Thermal consistency is an economic question: cost of thermal control/ floor space, etc.
  - Large chambers may prove impractical

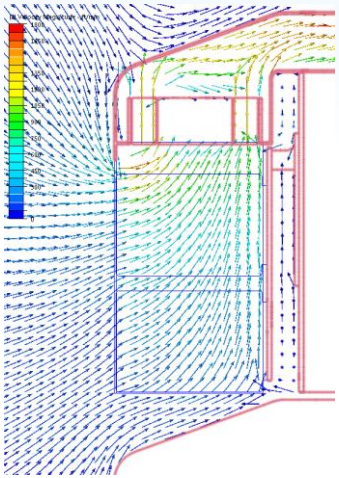
Production Test Approach

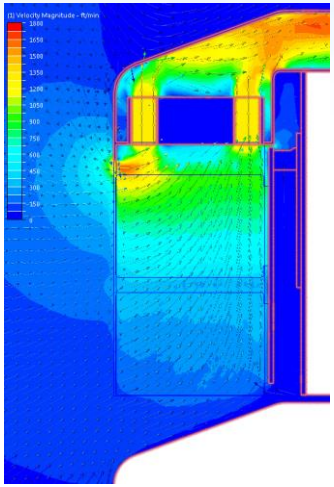
- As production volumes increase, floor space becomes a constraining factor
- Lowest floorspace approach:
  - use ambient air
  - Force air over only 1 or 2 DUTs in parallel
  - Isolate slots with air baffles
  - Used closed-loop control of fan speed

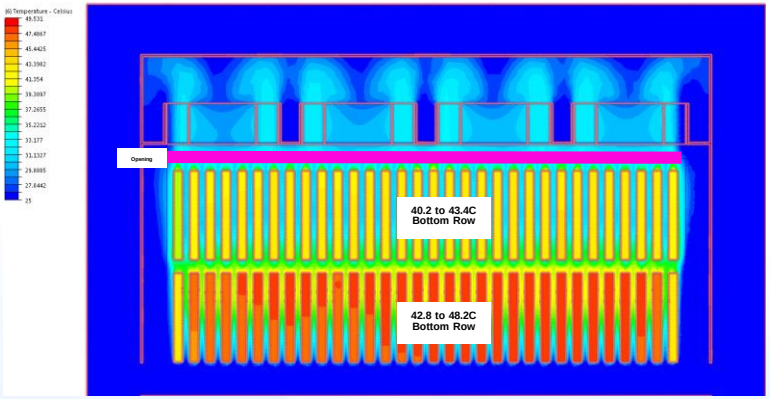
256 SSDs in a 19” Rack

Closed-loop Ambient Thermal Control









Summary

- Endurance test requires both thermal accuracy and consistency
  - A chamber with active cooling is most cost effective
- Production test most critical specification is to meet the minimum high temperature
  - Optimal cost can be achieved with high-density, floorspace-saving ambient air solution with closed-loop thermal control

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Overall Summary

- 3 advanced technologies have been presented for characterization, diagnostics, and verification of IC devices
  - Terahertz wave used in mold thickness metrology
  - Electro-optical pulsed TDR for fault isolation/analysis
  - Thermal analysis-designed System Level Endurance and Production Test

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Thank you for your attention!

And thanks for contributions in learning to various organizations and individuals, including:

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Texas Instruments
Broadcom

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Y. Kobayashi
R. McKay
M. Xie
T. Hemachandar
A. Hooper

And many others

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