# The Limits of CD Metrology

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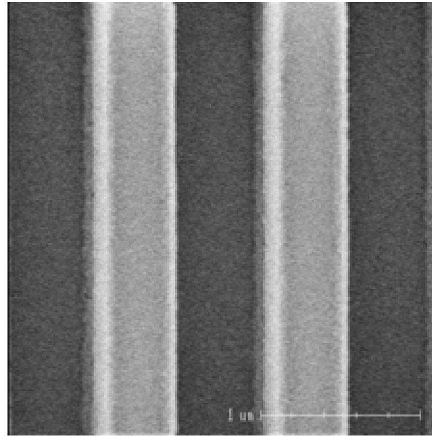
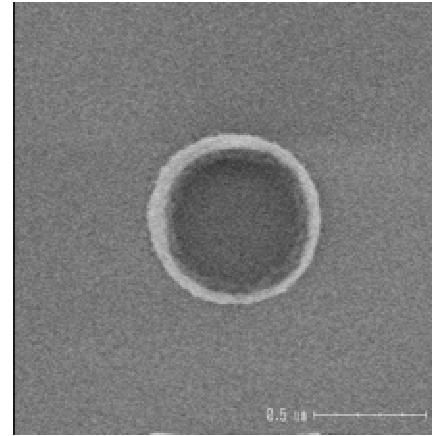
# Outline

- CD Definition
- ITRS CD Metro Requirements
- CXRO Wafers with 32nm+ Node Features
- CD SEM Results
- Scatterometry Results
- Other Technology Results
- Summary and Conclusions

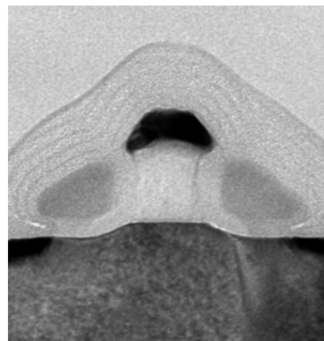
# CD Metrology in the 32 nm node (and beyond)?

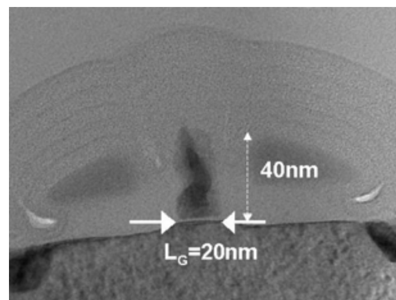
- The good old days: 0.5 ***micron*** lines and holes

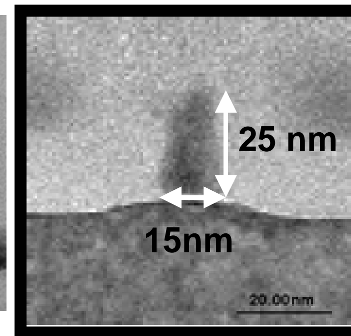


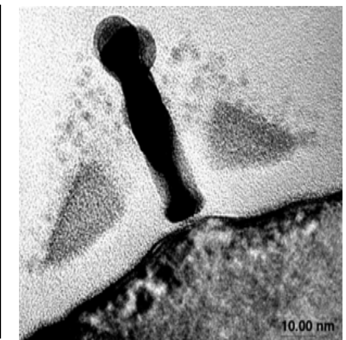


- Today: 50 nm 20 nm 15 nm 10 nm





# CD Definition for in-fab CD Metrology

- The present paper is concerned exclusively with characterizing in-fab CD measurement technologies.
- What do these technologies need to measure? Some combination of technologies must be able to measure all of these:
  - Classic CD (i.e. width), quantitative statistics (mean, sigma, etc)
  - LWR (Line Width Roughness)
  - Profile (sidewall angle for simple cases, curvatures for complex cases)
  - High aspect ratio features (>10:1)
- And must be
  - Non-destructive (i.e. measured part must still operate normally)
  - High throughput (for process control and scanner qual applications)
  - Highly repeatable and reliable
- Over the past few years Intel has evaluated CD SEM, scatterometry, atomic force microscopy, dual incident beam, and HV SEM technologies and has supported experiments with CD-SAXS
- So why has Intel bothered?

# CD Metrology ITRS Roadmap

- The following values are from the International Technology Roadmap for Semiconductors, 2004 Update, Lithography and Metrology sections, with the exception of the rows marked with *

| Year (ITRS) | 2007 | 2010 | 2013 | 2016 |
|---|---|---|---|---|
| *Year (2 Year Roadmap) | Today | 2007 | 2009 | 2011 |
| *Year Tools Needed for Dev. | 2003 | **2005** | **2007** | 2009 |
| *Year Tools Needed for Res. | 2001 | 2003 | **2005** | **2007** |
| Technology Node | 65 nm | 45 nm | 32 nm | 22 nm |
| 1/2 Pitch (nm) | 65 | 45 | 32 | 22 |
| Contact in resist (nm) | 80 | 55 | 40 | 30 |
| Contact post etch (nm) | 70 | 50 | 30 | 21 |
| Aspect ratio | 15:1 | 15:1 | 20:1 | 20:1 |
| Gate in resist (nm) | 35 | 25 | 18 | 13 |
| Gate post etch (nm) | 25 | 18 | 13 | 9 |
| Gate CD control $3\sigma$ (nm) | 2.2 | 1.6 | 1.2 | 0.8 |
| Metro CD $3\sigma$ precision (P/T=0.2) | 0.45 | 0.32 | 0.23 | 0.16 |

- Manufacturable solutions known; Manufacturable solutions not known

# CXRO Wafers

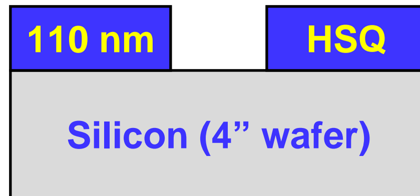
- Intel funded the Center for X-ray Optics at LBNL to create an e-beam writing process capable of producing 32nm node features.
- 4" wafers were patterned by the Nanowriter, a 100keV ebeam writer, to produce nested lines, isolated lines, and contact holes as small as:

| | Size (nm) | Pitch |
|---|---|---|
| Nested Lines | 36 | 1:1, 1:3 |
| Iso Line | 16 | 1:10 |
| Con | 45 | 1:1, 1:2 |

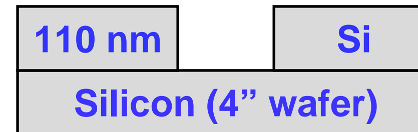
- Both resist and etched substrate wafers were fabricated. Silicon was used for the etched line/space wafers while oxide (HSQ) was used for the etched contact wafers.
- Etch processes were developed specifically to created the etched substrates imaged in this presentation.
- These wafers were used to evaluate the CD SEM and scatterometry technologies and have been supplied for CD-SAXS experimentation

# CXRO Wafer Process Flow

## Line/Space Wafers

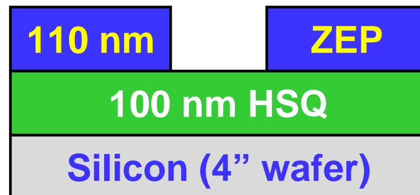



Resist Lines (HSQ used at ebeam-resist)




Etched Silicon Lines/Spaces

## Contact hole Wafers

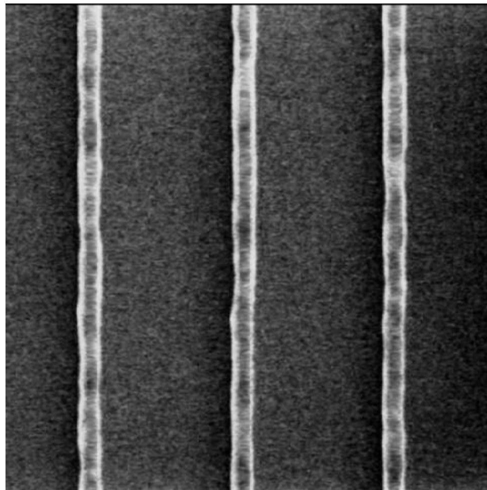


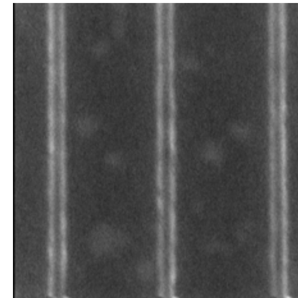

Resist Lines (ZEP ebeam-resist)

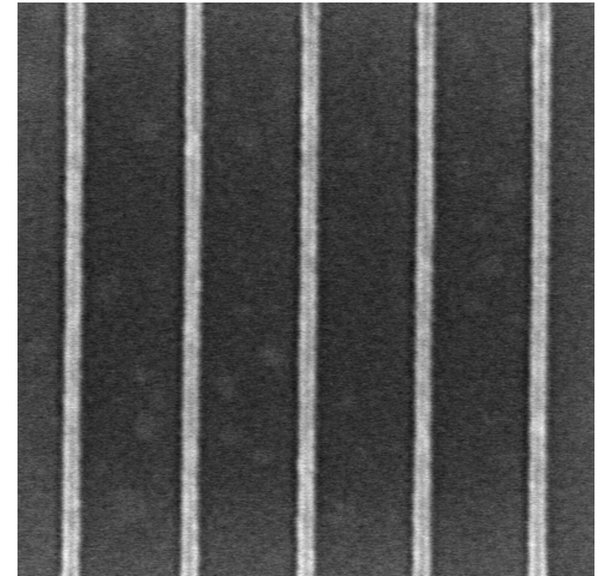
Etched contacts

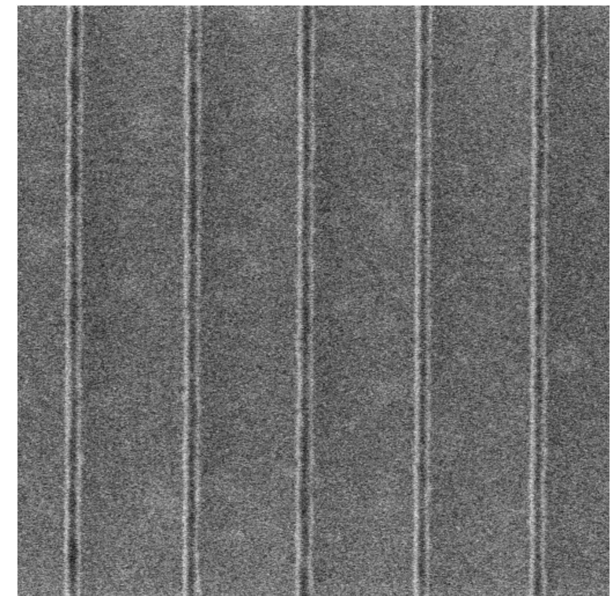
# CD SEM Results – Isolated Resist Lines

- Lines: Nominally 16 nm on a 176 nm pitch.
- Static Repeatability achieved today:
  - ~ 0.2 nm 3$\sigma$









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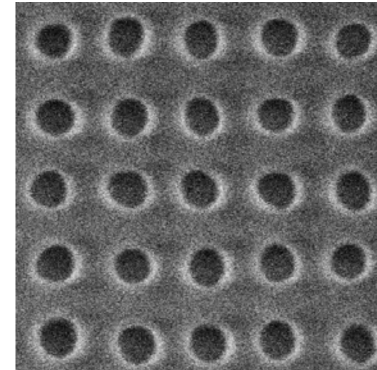
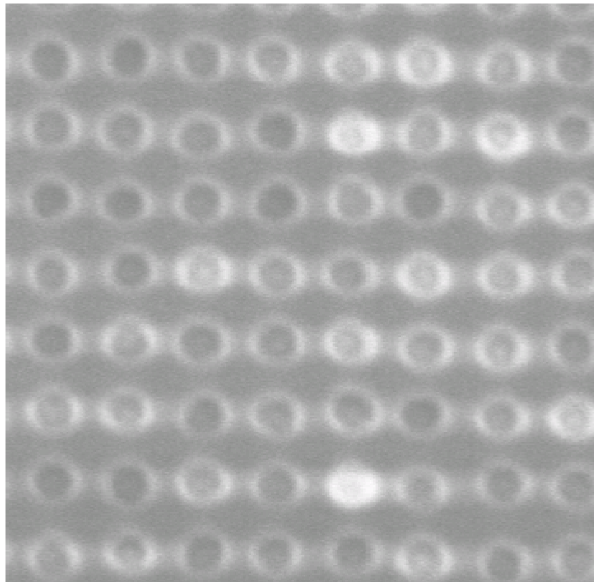
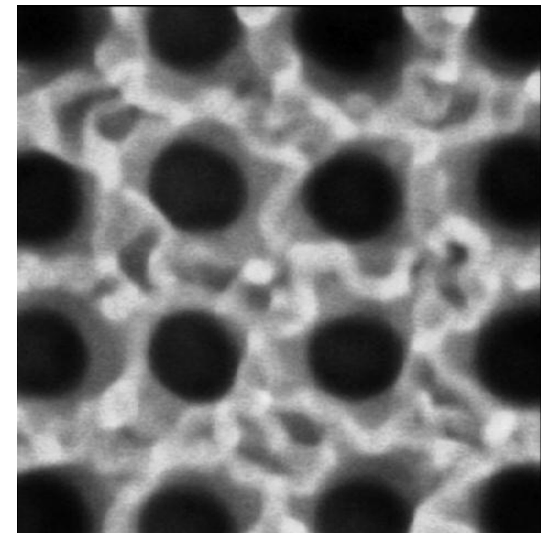
# CD SEM Results – Resist contact holes

- **Contact Holes: Nominally 45 nm on a 1:1 pitch.**
- **Static Repeatability achieved today:**
  - **~ 0.4 nm 3σ**

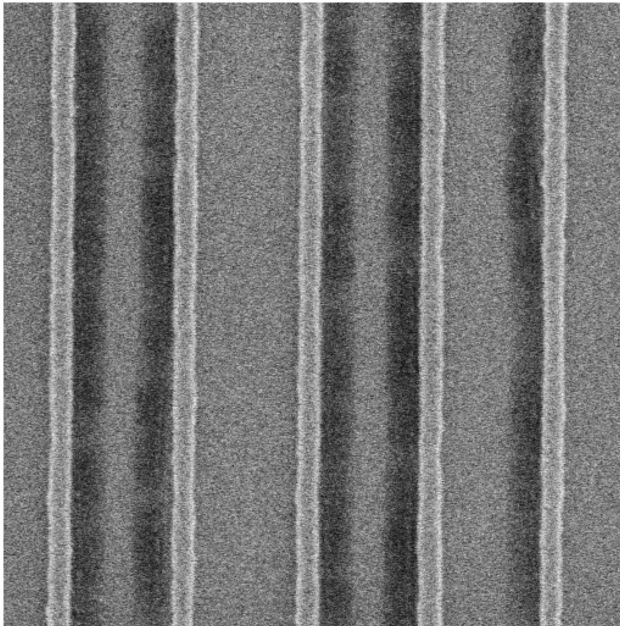


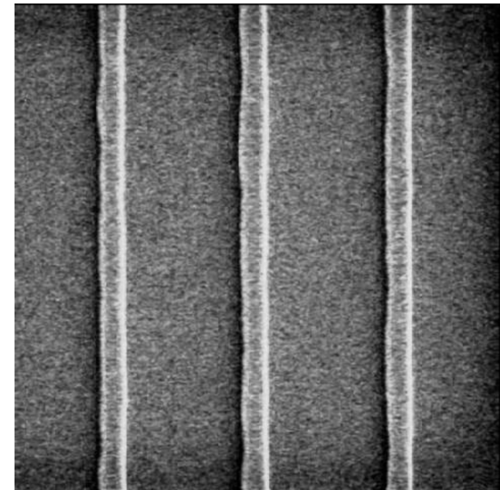




# CD SEM Results – Etched Resist Lines

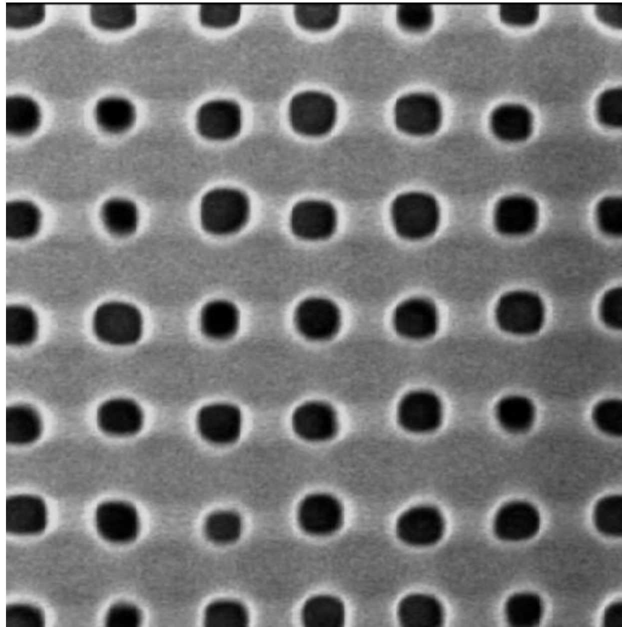
- **Lines: Nominally 16 nm on a 176 nm pitch.**
- **Static Repeatability achieved today:**
  - **~ 0.2 nm 3$\sigma$**

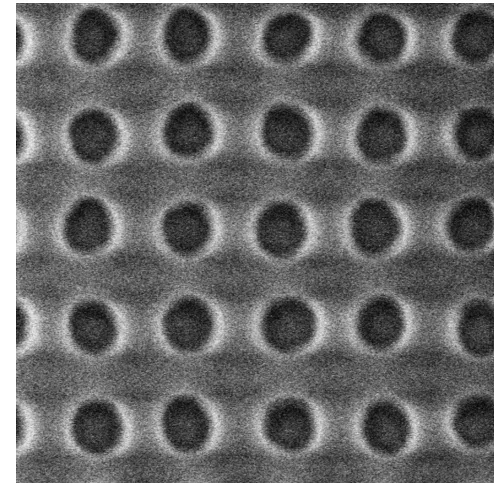




# CD SEM Results – Etched contact holes

- **Contact Holes: Nominally 45 nm on a 1:1 pitch.**
- **Static Repeatability achieved today:**
  - **~0.4 nm 3σ**



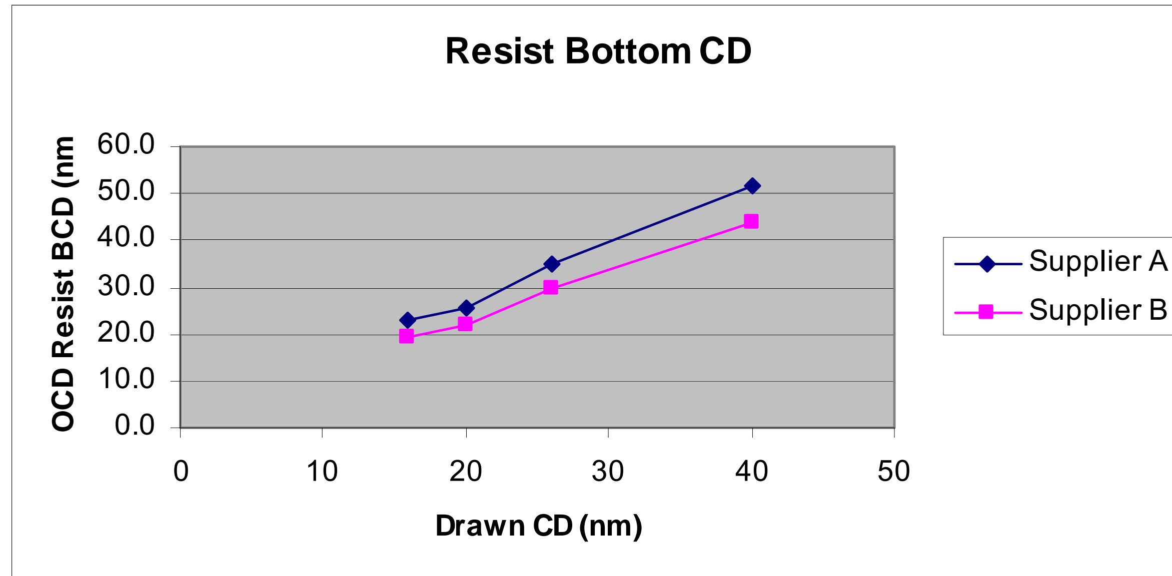


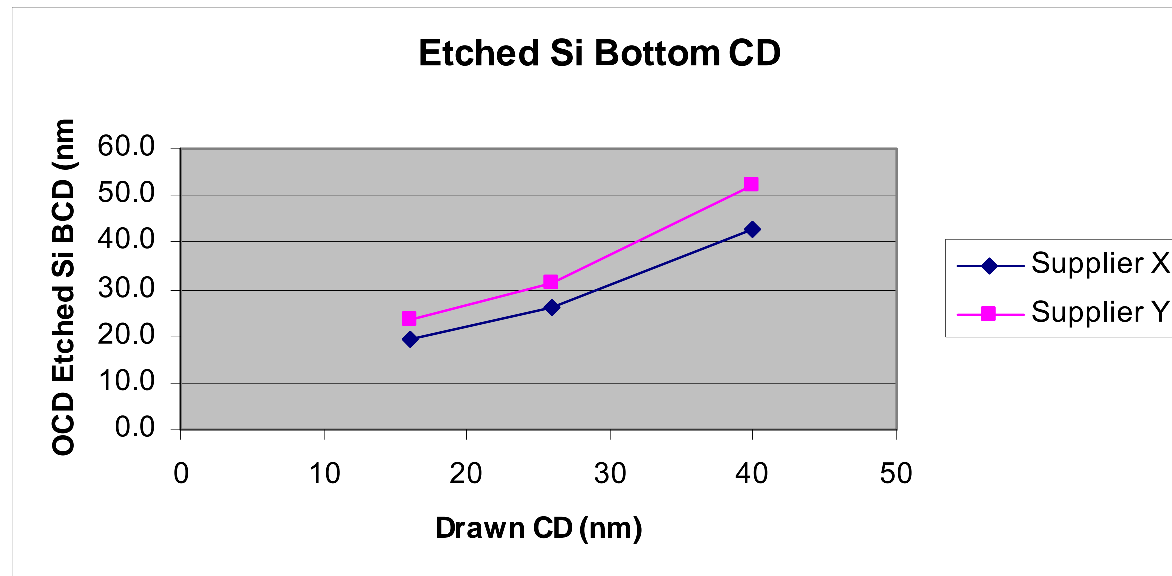
# CD SEM Results

- Demonstrated clear ability to resolve both edges on smallest isolated lines
- CD SEM remains the technique of choice for LWR measurements
- Measurements demonstrated that damage will continue to be an important concern for CD SEM technologies
- **Key Conclusion: CD SEM technology is capable of imaging features at the 32 nm technology node, but the tools must undergo continuous improvement to be ready for HVM in the 32 nm node.**

# Scatterometry results – CD Measurements

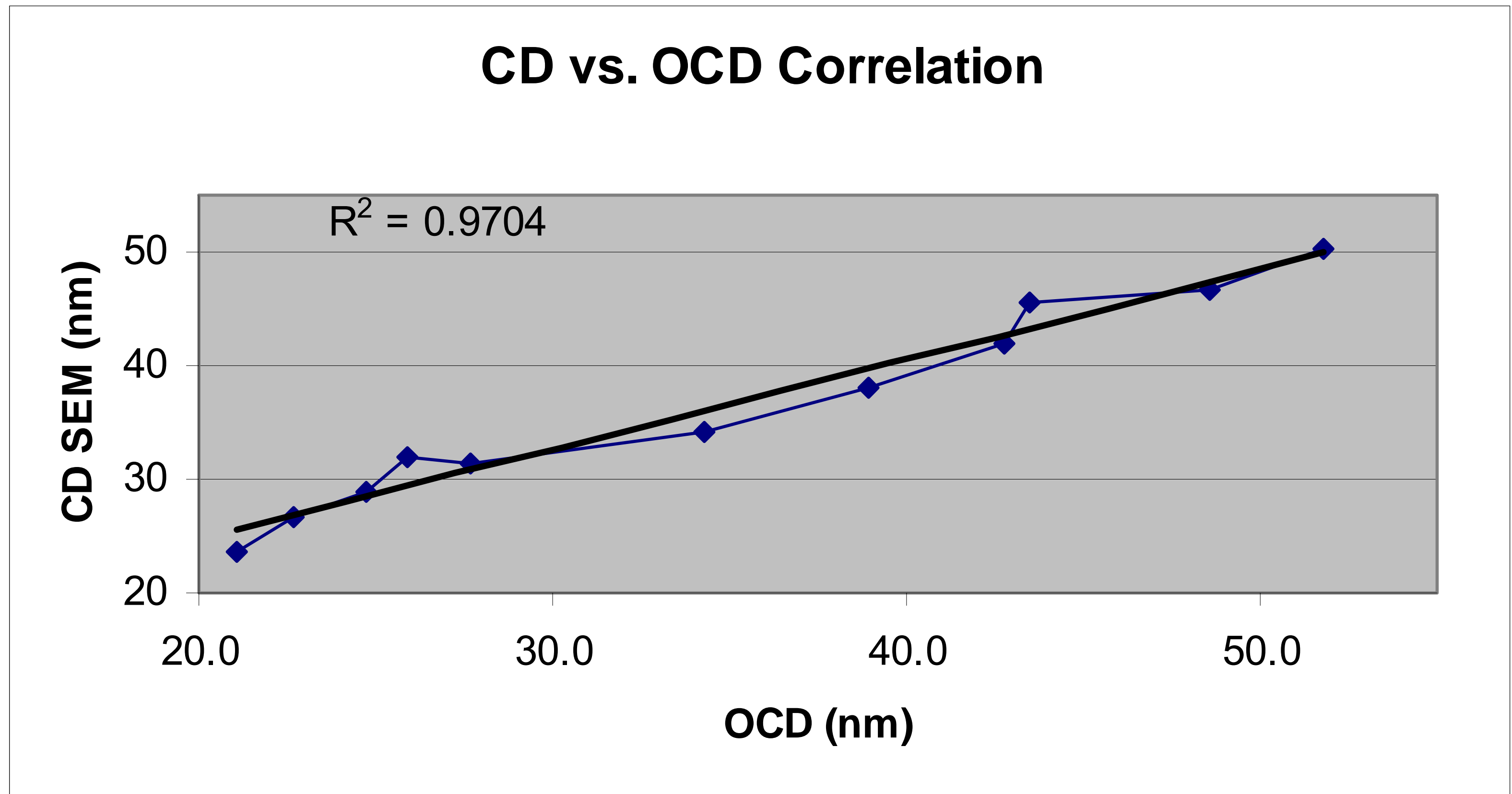
- Line CD's: Multiple suppliers obtained good solutions for the smallest lines (1:10) in patterned resist and etched silicon.
- For resist lines, suppliers accurately predicted straight sidewall profiles.
- For etched silicon lines, all suppliers found poor sidewall angle sensitivity (likely due to small sample volume).



# Scatterometry results – CD SEM Comparison

- Line CD's: In general, scatterometry data (bottom CD shown) correlated extremely well with CD SEM data, even down to 20 nm.



# Scatterometry results – Sematech results

- Ben Bunday presented results at SPIE 2005 of a comprehensive Sematech study of scatterometry tools. His data also suggest scatterometry correlates well with actual CD's, although his data indicate poor OCD accuracy.

Slope of Correlation — slope

Offset — offset

Non-Linearity — N-L

TMU — TMU

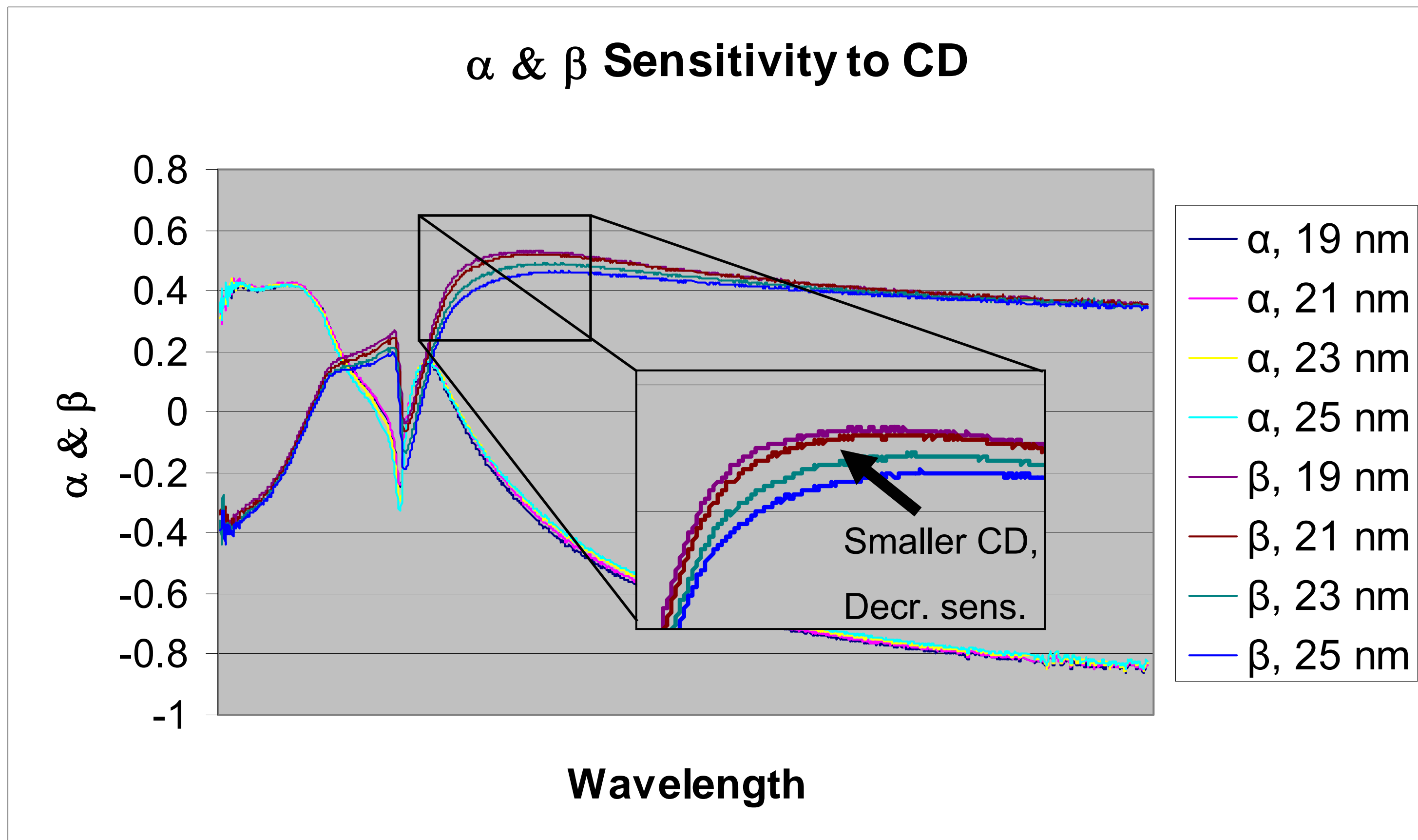
Process Layer / Pitch / Structure: FEM, LWV — Resist, 200nm pitch; Resist, 360nm pitch; Resist, 700nm pitch; Gate, 200nm pitch; Gate, 360nm pitch; Gate, 700nm pitch

- **Gate: slope ~ 1, offset ~ 10 (due to mid-CD), TMU<2nm**
- **Resist: slope > 1, offset ~20 (due to mid-CD), TMU=>2nm**

Ben Bunday et al, SPIE 2005 paper (in press).

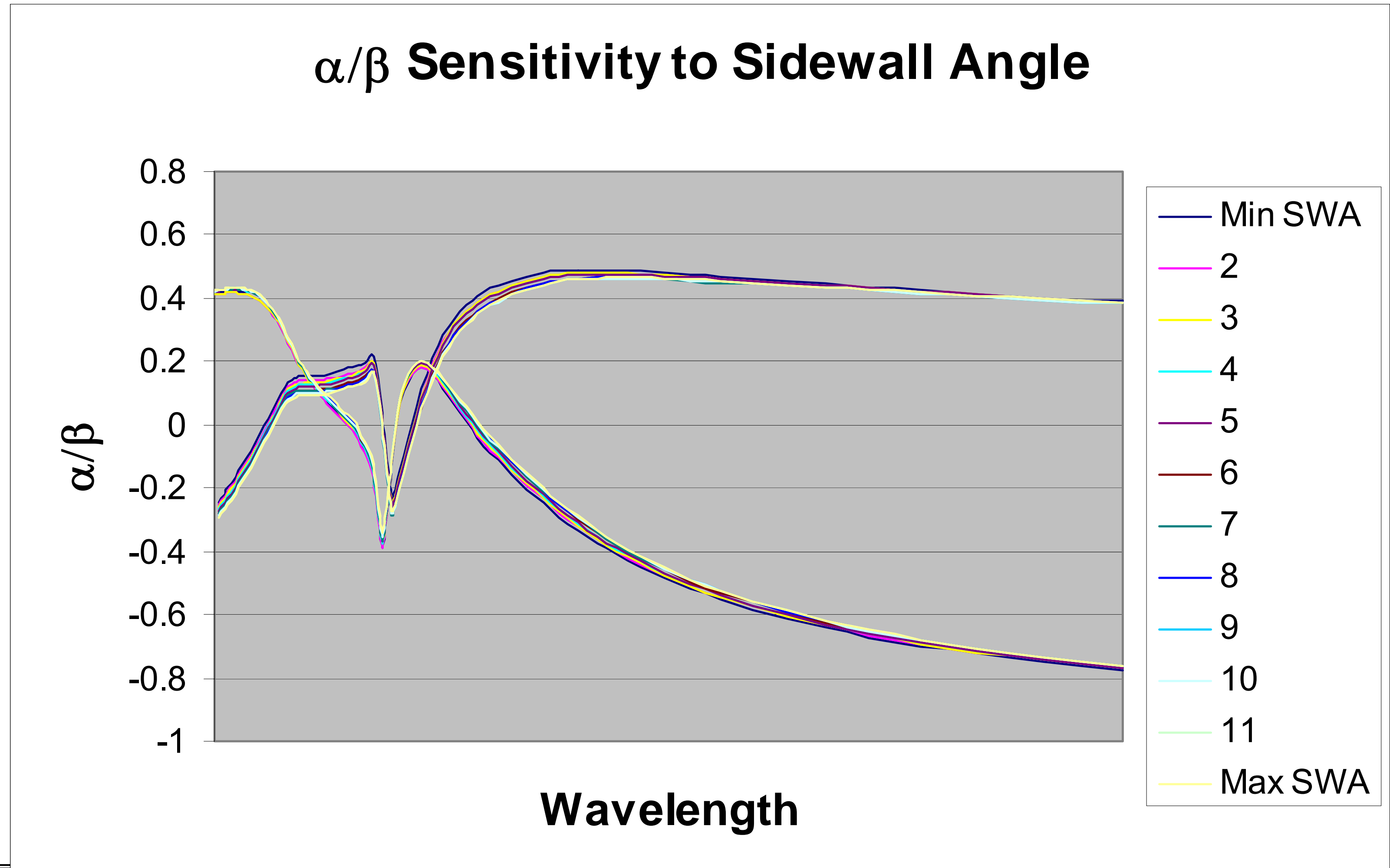
# Scatterometry results – CD Sensitivity

- Scatterometry exhibits some sensitivity to small CD differences even at CD's < 20 nm. (Note: curves below are fits to actual CD data)

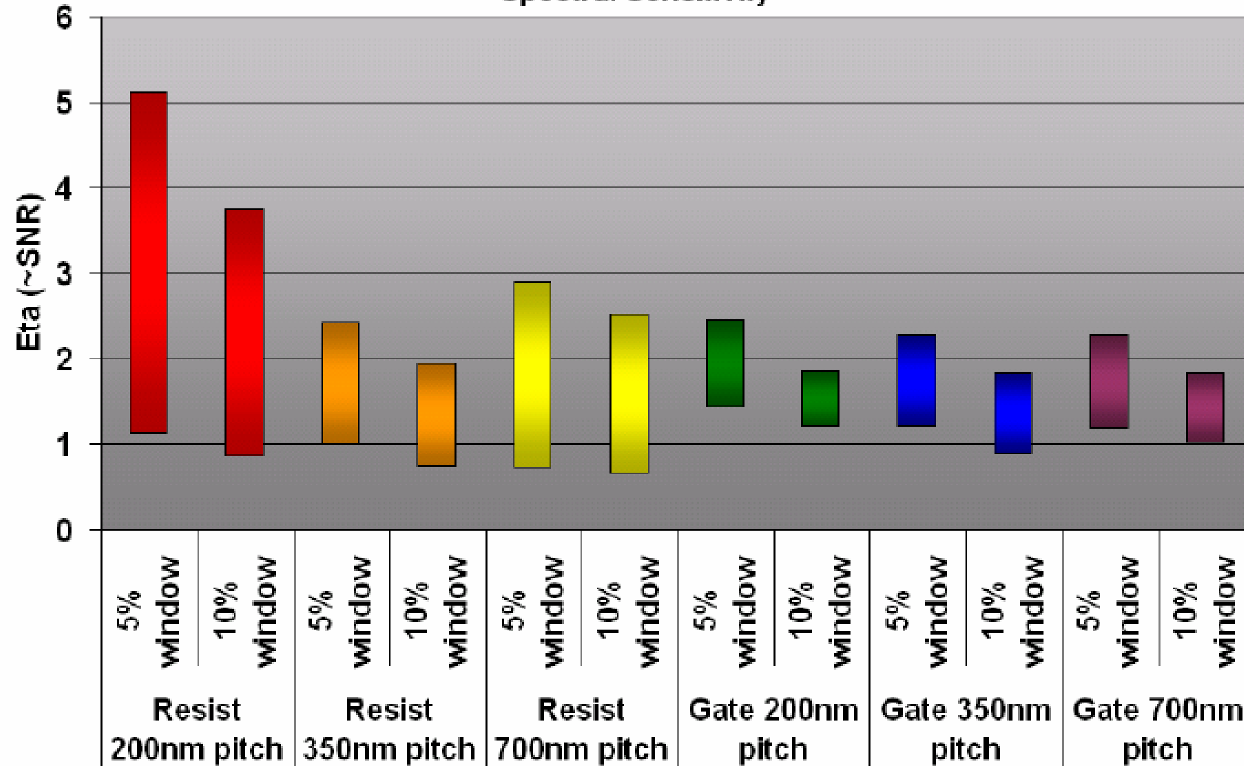


# Scatterometry results – SWA Sensitivity

- Scatterometry exhibits less sensitivity to sidewall angle (SWA) on etched silicon lines with Si height of 30 nm. (Note: curves below are simulations with SWA=68° to 78 °.)



# Spectral Window Sensitivity




- Maximum $\eta$ where all spectra are unique
- Measure of SNR with assumed spectral window

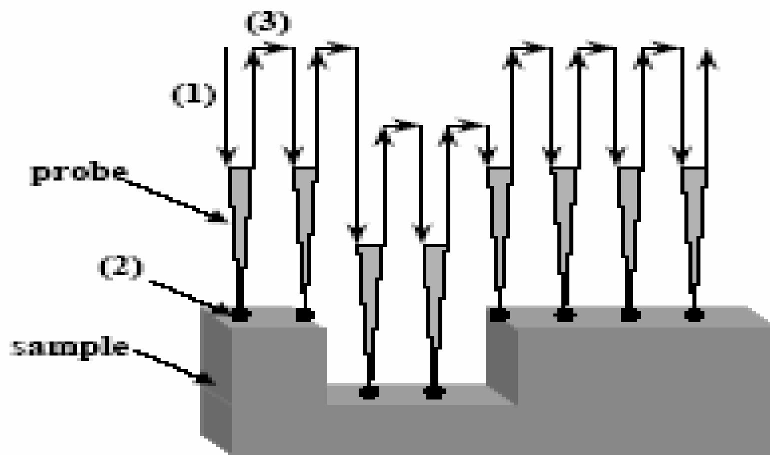
Slide courtesy of Ben Bunday, SPIE 2005, in press.

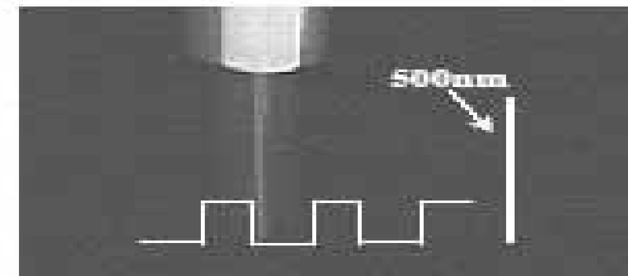
# Scatterometry Results

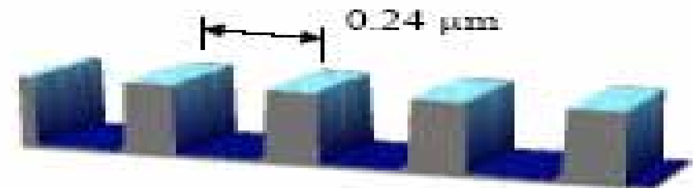
- **Key Result: Scatterometry demonstrated the ability to resolve 32 nm node CD's.**
- Resist profiles were modeled accurately (choice of SWA=90° is corroborated by cross section images).
  - Feature heights for resist generally near 55-100 nm.
- Less success in modeling etched silicon features. Feature height for etched silicon lines was about 30 nm. Feature height WAS accurately modeled, but SWA was generally not accurately modeled.
  - Feature quality was worse for the etched lines than for the resist lines and accounts for some reduction in measurement quality.
- **Key Conclusion**: CD sensitivity to small CD's and SWA sensitivity for thin features must be improved to meet 32 nm HVM targets. If sensitivity solutions are found scatterometry will be the profile measurement standard.

# AFM

- **The capability of atomic force microscopes is primarily dependent upon the tip technology and the control mode.**
- Traditional (C and Si) tip sizes of about 50 nm are currently available; carbon nanotube tips (CNT's) as small as 20 nm have been reported[1].
- Today, in order to measure non-reentrant profiles it is possible to use straight, sharp tips like CNT's. Using a control mode like that proposed in Ref [1], the "Step In" mode, it should be possible to measure 32 nm node features.



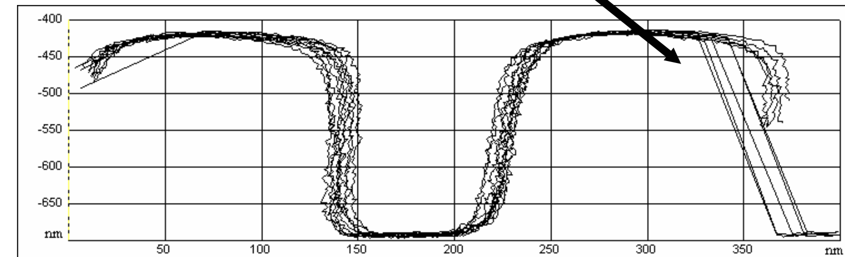



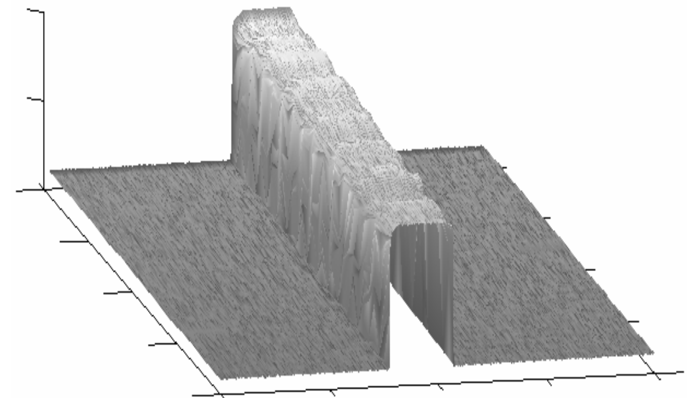

[1]Morimoto et al, Proc SPIE 5038 (2003), pp 636

# AFM Results

- **AFM's primary difficulty arises when measuring reentrant profiles.**
- This requires using a "boot" shaped tip and the "tapping mode" of operation. Contact forces and resonant frequency add additional space requirements of 20-30nm above the physical tip size limiting space/hole capability to ~80 nm.
- **Key Result: AFM can measure P1268 isolated lines today, and provides unmatched 3D profile capability on non-reentrant features, but is not capable of measuring reentrant features from the 65nm node & beyond.**

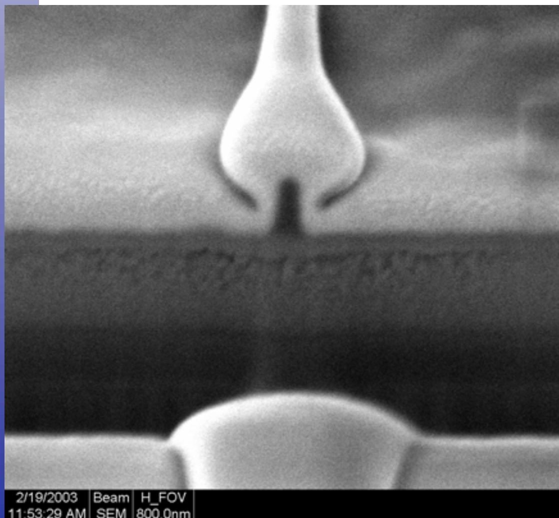
Trace from failed space measurement

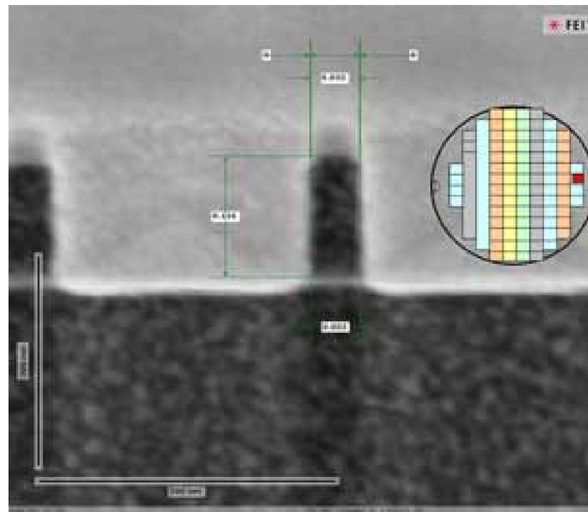


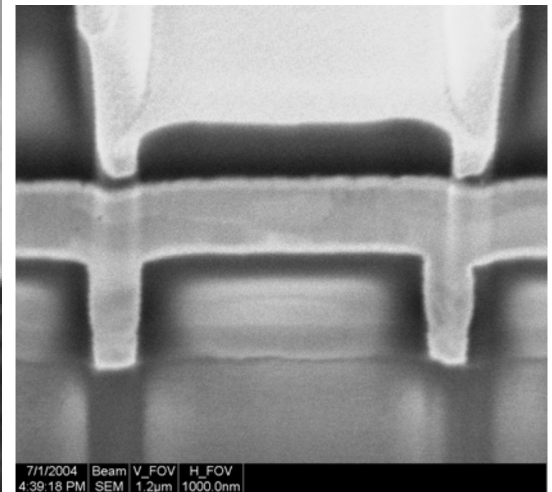



# Dual Beam Results

- **Key Result: Static and Dynamic precisions lag CD SEM precisions.**
- Problems: Difficulty obtaining high fidelity cross-sections of resist features. Ga contamination for front end processes is an issue.
- Advantages: 2-8 minutes per high quality cross sectional image; capable of utilizing full 12” wafers rather than coupons; in situ decoration techniques.
- **Key Result: Dual beam offers promise for low-sample rate inline CD Metro; could replace many current analytical-SEM tasks (and could be in fab). Primary use would be development and inspection.**



# HV SEM

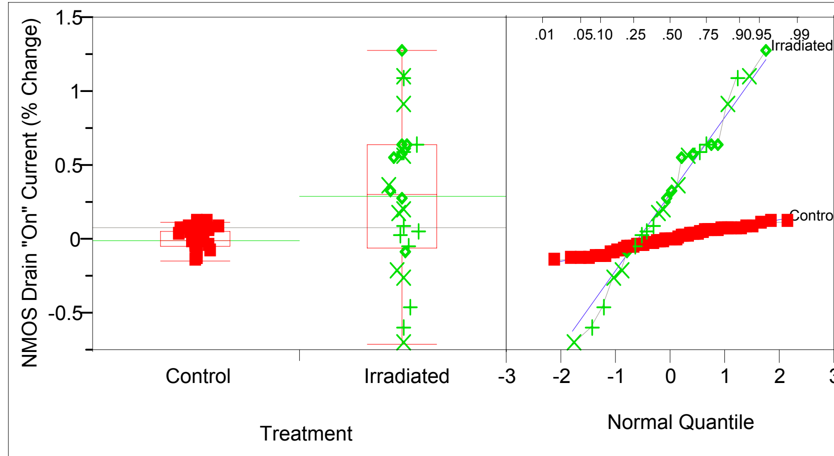
- It was recently proposed[1] that using high energy (50–200 keV) electrons might provide improved imaging compared to the traditional secondary electron (SE) used into today's CD SEM's
- Positives:
  - Little energy deposited in the resist (i.e. no line slimming)
  - Improved resolution compared to SE SEM
- Negatives:
  - Potential for transistor damage
- Intel collaborated with Hitachi High Technologies to determine if transistor damage results from the use of 50-200 keV electrons in an HV SEM
- We irradiated specific transistors on fully integrated Pentium IV processors fabricated using the 0.18 μm process and performed a variety of electrical tests on these devices.
- The wealth of data precludes full description here, so I will only show the drain current results
  - The green data are the control set (no irradiation)
  - The red data are the lump distribution of all irradiated data
  - The vertical axis shows (Post – Pre)/Pre as a %.

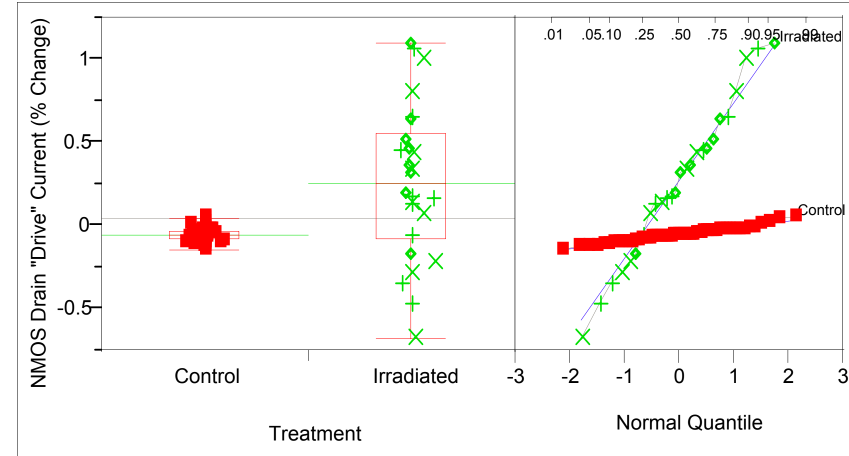
[1] David Joy, SPIE presentation, 2002.

# HV SEM Results by Treatment: Drain Currents

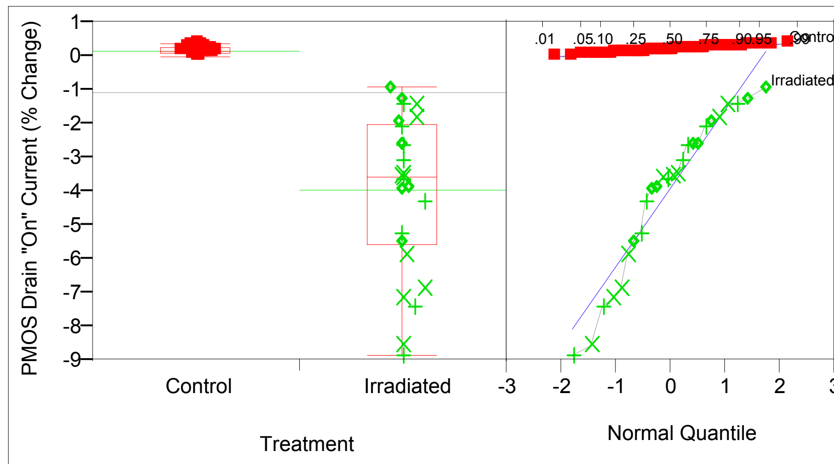
**"On"** **"Drive"**

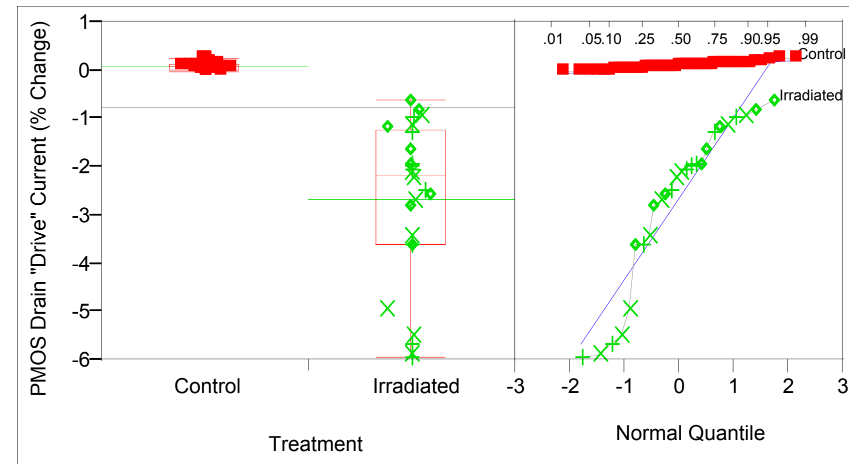
**NMOS**




**PMOS**



# HV SEM Results and Conclusions

- For all doses and energies we found that the devices were affected by irradiation
- The data show a logic device reliability failure issue. No device exposed to these conditions, even the lowest dose, could be sold.
- Significant reduction in dose must be achieved before the primary electron-based SEM may be used for CD metrology on product material.
- Follow-up experiments could determine the maximum allowable dose on logic devices.

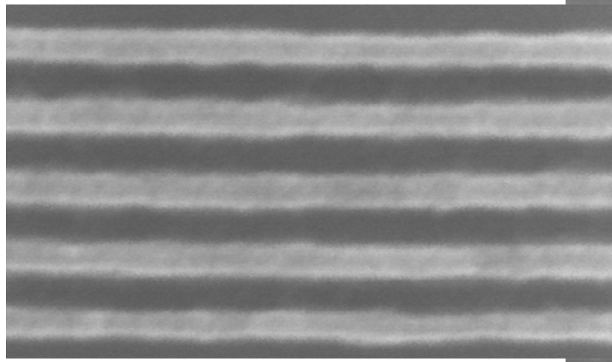
# Summary and Conclusions

- Evaluation of CD Metro technologies at 32 nm node dimensions shows
  - CD SEM continues to be capable at 16 nm lines and 45 nm holes
  - Scatterometry can predict the CD correctly for 16 nm lines, but profile fidelity is still an open question.
  - AFM is not capable of measuring 32 nm node features if they are reentrant.
  - Dual beam has difficulty imaging resist features and is locally destructive, but offers promise for characterization.
  - HV SEM causes damage to devices and is (in its present form) unsuitable for use as a CD metrology solution. A lower dose version might bear revisiting…

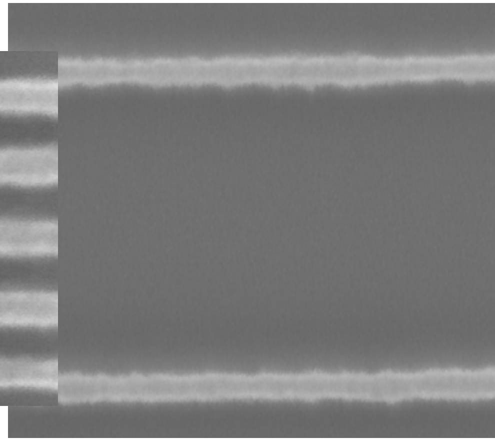
# Future Work

- Technology evaluations with 22 nm node features are planned using EUV lithography and Intel process technologies in 2005-2006 timeframe.  CD SEM and scatterometry evals have already begun on available feature sizes.

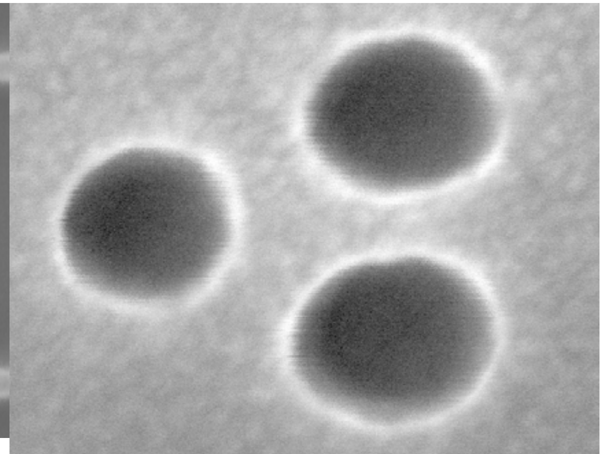
45nm 1:1



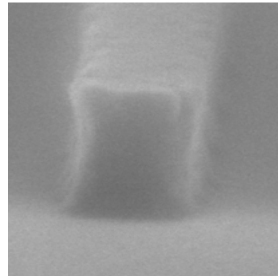
27 nm



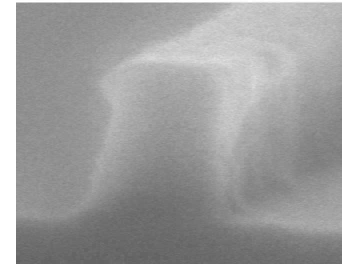
~50 nm



CD = 100 nm, Pitch = 200 nm



CD = 50 nm, Pitch = 550 nm



# Acknowledgements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  - CXRO Lab at LBNL, especially Deirdre Olynik and Alex Liddle
  - Metrology equipment manufacturers (you know who you are!)
  - The device experts are Intel in PTD and CR for the images of their prototype devices
  - David Joy for his ideas on future metro technologies
  - Rex Frost and Brian Coombs for help in creating some of the wafers used in the evaluations
  - Jose Maiz for his help in understanding reliability failures
  - Gary Crays for his help in analyzing e-test data
  - Ben Bunday for allowing me to present some Sematech data