(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
24 July 2025 (24.07.2025)

WIPO | PCT

(10) International Publication Number
WO 2025/155931 A1

(51) International Patent Classification:
G01T 1/24 (2006.01) *G01S 7/4863* (2020.01)
G01J 1/42 (2006.01)

(21) International Application Number:
PCT/US2025/012217

(22) International Filing Date:
17 January 2025 (17.01.2025)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
63/621,856 17 January 2024 (17.01.2024) US

(71) Applicant: **GOVERNMENT OF THE UNITED STATES OF AMERICA, AS REPRESENTED BY THE SECRETARY OF COMMERCE** [US/US]; National Institute of Standards and Technology, 100 Bureau Drive, MS 1052, Gaithersburg, Maryland 20899 (US).

(72) Inventors: **LEVINE, Zachary Howard**; NATIONAL INSTITUTE OF STANDARDS AND TECHNOLOGY, 100 Bureau Drive, MS 1052, Gaithersburg, Maryland 20899 (US). **BIENFANG, Joshua Copeland**; NATIONAL INSTITUTE OF STANDARDS AND TECHNOLOGY, 100 Bureau Drive, MS 1052, Gaithersburg, Maryland 20899 (US). **MIGDALL, Alan Lee**; NATIONAL INSTITUTE OF STANDARDS AND TECHNOLOGY, 100 Bureau Drive, MS 1052, Gaithersburg, Maryland 20899 (US). **ZIMMERMAN, Neil**; NATIONAL INSTITUTE OF STANDARDS AND TECHNOLOGY, 100 Bureau Drive, MS 1052, Gaithersburg, Maryland 20899 (US).

(74) Agent: **JOHNSON, Spencer J.**; National Institute of Standards and Technology, 100 Bureau Drive, MS 1052, Gaithersburg, Maryland 20899 (US).

(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CV, CZ, DE, DJ, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IQ, IR, IS, IT, JM, JO, JP, KE, KG, KH, KN, KP, KR, KW, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, MG, MK, MN, MU, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, ST, SV, SY, TH,

(54) Title: METROLOGICAL PHOTON COUNTER AND METROLOGICALLY COUNTING PHOTONS AT ROOM TEMPERATURE

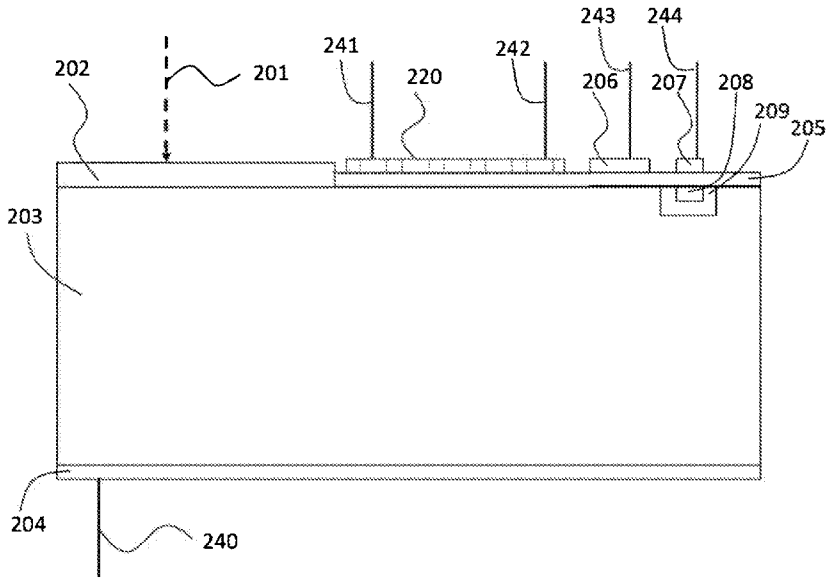


FIG. 1

(57) Abstract: A novel metrological photon counter may be created from an undoped semiconductor material where electrons and/or holes generated by photons are concentrated and guided by electric fields towards a field-effect-transistor. This metrological photon counter can allow for the efficient and accurate measurement of the number of photons in a wide range of environments including at room temperature.

WO 2025/155931 A1

[Continued on next page]

TJ, TM, TN, TR, TT, TZ, UA, UG, US, UY, UZ, VC, VN, WS, ZA, ZM, ZW.

(84) **Designated States** *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, CV, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SC, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, ME, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Published:

— *with international search report (Art. 21(3))*

METROLOGICAL PHOTON COUNTER AND METROLOGICALLY COUNTING PHOTONS AT ROOM TEMPERATURE

STATEMENT REGARDING FEDERALLY SPONSORED RESEARCH

[0001] This invention was made with United States Government support from the National Institute of Standards and Technology (NIST), an agency of the United States Department of Commerce. The Government has certain rights in this invention.

CROSS REFERENCE TO RELATED APPLICATIONS

[0002] This application claims the benefit of U.S. Provisional Patent Application Serial No. 63/621,856 (filed January 17, 2024), which is herein incorporated by reference in its entirety.

BRIEF DESCRIPTION OF THE DRAWINGS

[0003] The following description cannot be considered limiting in any way. Various objectives, features, and advantages of the disclosed subject matter can be more fully appreciated with reference to the following detailed description of the disclosed subject matter when considered in connection with the following drawings, in which like reference numerals identify like elements.

[0004] FIG. 1 shows, according to some embodiments, a cross-section of metrological photon counter 200 that performs photon-number resolving and that counts electrons.

[0005] FIG. 2 shows, according to some embodiments, is a top view of metrological photon counter 200 that counts electrons.

[0006] FIG. 3 shows, according to some embodiments, is a cross-section of metrological photon counter 200 that performs photon number resolving and counts both electrons (on the top) and holes (on the bottom).

[0007] FIG. 4 shows, according to some embodiments, is a metrological photon counter 200.

[0008] FIG. 5 shows, according to some embodiments, is a metrological photon counter 200.

[0009] FIG. 6 shows, according to some embodiments, a graph of relative frequency versus for a metrological photon counter 200.

[0010] FIG. 7 shows, according to some embodiments, is a computing system that provides computational processing, control, or data acquisition with metrological photon counter 200.

[0011] FIG. 8 shows, in one embodiment, one component slab of a floating-gate MOSFET usable in metrological photon counter 200.

[0012] FIG. 9 shows, in one embodiment, a current-voltage (I-V) curve of the MOSFET of FIG. 8.

[0013] FIG. 10 shows, in one embodiment, the increase in detected voltage resulting from the addition of electrons on the floating node of the MOSFET of FIG. 8.

DETAILED DESCRIPTION

[0014] A detailed description of one or more embodiments is presented herein by way of exemplification and not limitation.

[0015] It is difficult to accurately count the number of photons in an optical pulse when that number is larger than 1 or 2, it is very difficult to do so when that number is larger than 10. Moreover, it has likely never been accurately done when that number is larger than 100, wherein accurately refers to being able to distinguish integer photon numbers with less than 10% uncertainty. The challenges are in both efficiency, as in not losing or missing any photons, and accuracy, as in being able to discriminate photon numbers in whatever signal is output (that is, the signal from 15 photons might sometimes look like the signal from 16 or 14 photons).

[0016] A metrological photon counter 200 has been discovered which can count photons with metrological accuracy and determine the number of photons from an input optical signal.

[0017] The disclosed metrological photon counter 200 can metrologically count photons at room temperature. In an embodiment, with reference to FIG. 1, FIG. 2, FIG. 3, FIG. 4, FIG. 5, FIG. 6, and FIG. 7, metrological photon counter 200 includes a bulk (un-doped) semiconductor (203) for the purpose of photon-number resolving detection. A bulk semiconductor has no dopants that create an electric field within the material, so in this

invention an electric field inside the photo-absorptive material (203) is induced by surface electrodes. This electric field separates the electron from the hole that are promoted (the electron to the conduction band and the hole to the valence band of the semiconductor) by the absorption of a photon.

[0018] In an embodiment, metrological photon counter 200 includes a snaking wedge (220) electrode that may be comprised of multiple electrodes and resistors electrically connected in series. This snaking wedge, along with a bottom electrode (204), serve to efficiently gather the photo-generated carriers into a small region located under the final, smallest element in the snaking wedge; the figure envisions 5 electrodes in the snaking wedge so the smallest element is the fifth top-wedge electrode (225). The snaking wedge electrode may be comprised of more or fewer electrodes than 5. The resistive elements are designed so that the electrical voltage is highest at the smallest electrode element of the wedge and decreases in each successively larger electrode element in the wedge. This allows the collection and concentration of charge carriers from a larger volume into a smaller volume with only two externally applied voltage signals applied to wires 241 and 242.

[0019] In an embodiment, metrological photon counter 200 includes the collection and counting of both the electrons and the holes generated by photon absorption. The process used to collect and count electrons can be recreated in a manner suitable for collecting and counting holes in the same device, as illustrated in Fig. 3. Due to the one-to-one correspondence of the number of electrons to holes, this allows the device to make the same measurement (the number of photons absorbed from an incident optical signal) in two ways.

[0020] In an embodiment, metrological photon counter 200, with reference to FIG. 1, is a photon-number resolving (PNR) detector. In its operation, an optical signal (201) comprised of photons incident on the photo-absorptive area of the detector, which is primarily defined by the area of the anti-reflection (AR) coating (202). The anti-reflection coating may be composed of layers of dielectric designed to suppress optical reflection from the surface of the bulk semiconductor (203). The AR coating may be designed for a spectral region of interest and overlaps the absorption spectrum of the bulk semiconductor (203) and is designed for very high transmissivity for the optical wavelengths of interest (>98%). The thickness of the bulk semiconductor (203) is chosen so that photons entering through the AR coating (202) are absorbed within the

semiconductor (203) with very high probability (>98%). The bottom electrode (204) may be composed of a reflective material (e.g., metal) to reflect any unabsorbed photons back through the semiconductor (203). The physical design of the bulk semiconductor (203), the AR coating (202) and the bottom electrode and mirror (204) are designed to have a large photo-sensitive area for the purpose of facilitating the optical coupling (focusing) of light into the detector. Typical dimensions envisioned are diameters of 50 micrometers or more for the AR coating (202) and thicknesses of 10 micrometers or more if the bulk semiconductor (203) is composed of silicon.

[0021] When photons enter the semiconductor, they can be absorbed, promoting an electron to the conduction band and a hole to the valence band of the semiconducting material. An electric field induced by a lower voltage applied to the bottom electrode (204) through wire (240) and a higher voltage applied to the first wire (241) of the top snaking wedge (220) causes the electrons to move towards the snaking wedge and the holes to move down towards the bottom electrode (204).

[0022] The snaking wedge (220) is separated from the semiconductor (203) by a thin insulating or oxide layer (205) that prevents electrons from entering the conductive electrodes of the snaking wedge (220) but allows for effective generation of an electric field within the semiconductor. The snaking wedge may be composed of a series of electrodes (222-225) connected in series with resistive elements (226-229) for the purpose of using only two electrical wire connections (241 and 242) to induce a gradation of increasing electrical voltages from the first electrode to the last electrode in the snaking wedge (220). The number of electrodes and resistors that comprise the snaking wedge (220) may vary. Electrodes (221-225) may be composed of a metal deposited upon the insulating layer or oxide (205), or of polysilicon or another semiconductor material doped in such a manner that it effectively acts like a conductor. The resistors (226-229) may be composed of standard electrically resistive materials known to those experienced in the art, or of doped polysilicon. The position of the first electrode (221) in the snaking wedge (220) relative to the AR coating (202), and the physical dimensions of the electrodes in the snaking wedge (220), and their relative positions with respect to each other are all chosen to maximize the collection of photo-generated charge carriers within the semiconductor (203) and their efficient drift towards the region beneath final electrode (225) in the snaking wedge (220).

[0023] The top well electrode (206) may be composed metal or doped polysilicon or another semiconductor material. An electrical voltage is applied to the top well electrode (206) that is higher than the voltage of the final electrode (225) in the snaking wedge (220). This causes electrons to move from beneath the final electrode (225) in the snaking wedge (220) to beneath the top well electrode (206). The physical dimensions of the top well electrode (206) and its location relative to the final electrode (225) in the snaking wedge (220) is chosen to both maximize the collection of electrons from beneath the snaking wedge (220), to minimize the capacitance between the top well electrode (206) and the top field-effect-transistor (FET) channel (208). Typical values for the capacitance between the top well electrode (206) and the top FET channel (208) are well below 100 attoFarads.

[0024] The top gate electrode (207), the top FET channel (208), and the top insulator/trench isolation (209) form a field-effect transistor with the transistor channel isolated from the bulk semiconductor (203) by the insulator/trench isolation (209), as known in the art. The top gate electrode (207) can be a metal or doped polysilicon conductor and is separated from the channel by the top insulating layer (205). In an alternate configuration the top gate electrode (207) can be a doped semiconductor in contact with the channel (209) as in a junction field-effect transistor (JFET), as known to practitioners in the art. The channel (209) and the top gate (208) are or small dimension (< 100 nm gate length along the channel). This FET, comprised of gate (207), channel (208), isolation (209), top drain electrode (210), and top source electrode (211), is in close proximity to the top well electrode.

[0025] In the PNR detector, capacitance between the top well electrode (206) and the top FET channel (209) is a parameter for consideration. According to the behavior of a capacitor, the voltage change ΔV between the two ports of the capacitor is related to the change in charge ΔQ on the capacitor as $\Delta V = \Delta Q/C$. If the capacitance C is small enough, then the addition of a single electron to the capacitor can cause a significant change in the voltage difference between the electrons under top well electrode (206) and the top FET channel (208) and result in a measurable change in the electrical conductivity of the FET channel (208), as observed as a change in the current flowing through the FET channel (208) from the drain electrode (210) to the source electrode (211). By sampling this current with standard equipment, with and without charge held under the top well electrode (206), the number of electrons under the top well electrode (206) may be determined. The use of electrodes deposited atop an insulating or oxide

layer in this invention is an innovative way to achieve very small capacitance values between the FET channel (208) and the top well electrode (206).

[0026] With reference to FIG. 6, a histogram of current values produced by metrological photon counter 200 can be made for the repeated measurement of pulses of light with a stable Poisson distribution of photon number 3.5. Each peak in the histogram corresponds to a different number of electrons under the top well electrode (206). The change in current due to the addition of a single electron is directly related to the capacitance C between the top well electrode (206) and the FET channel (208). This change in current, along with the variance of the current for each number of electrons, determines the ability to discriminate electron numbers under the top well electrode (206). If the optical losses and the electron losses within the device are low, this PNR detector can provide an accurate measurement of the number of photons incident on the detector.

[0027] With reference to FIG. 7, in one embodiment, the FET used in the metrological photon counter 200 is a floating-gate MOSFET. In this embodiment, one component of the MOSFET is a 25 nm thick conducting slab 400 with a 20 nm oxide layer separating it from a similar slab used as the floating node. The conducting slab has two *n*-type regions used as a source 401 and a drain 402, while the remaining area of the slab is a less heavily doped *p*-type region used as the channel 403. In one embodiment, this slab is 25x300x180 nm, with two 25x50x20 nm *n*-type regions. In one embodiment, the *n*-type region is doped at approximately 10^{17} e^-/cm^3. In another embodiment, the *p*-type channel is doped at approximately 10^{15} e^+/cm^3. In one embodiment, there are ohmic contacts connected with the *n*-type regions, and an electrode for the gate and another for a ground.

[0028] In one embodiment with reference to FIG. 7, the charge in the portion of channel 403 between source 401 and drain 402 is fixed with a uniform density. In one embodiment, when the gate voltage is varied with no external charge and a drain-source voltage of 0.5 V, the current-voltage curve (I-V) is characteristic of a MOSFET with a subthreshold exponential growth in current with voltage and a linear region above threshold, as shown in FIG. 8.

[0029] In one embodiment with reference to the MOSFET partially pictured in FIG. 7, a single electron in the floating node was calculated to change a base current at 5319 nA by 66 nA. This change is over 1% of the base current, and is able to be detected with a very high confidence within 5 ns. These calculations are shown in FIG. 9.

[0030] Metrological photon counter 200 can be made of various elements and components that are microfabricated. Elements of metrological photon counter 200 can be various sizes. Elements of metrological photon counter 200 can be made of a material that is physically or chemically resilient in an environment in which metrological photon counter 200 is disposed. Exemplary materials include a metal, ceramic, thermoplastic, glass, semiconductor, and the like. The elements of metrological photon counter 200 can be made of the same or different material and can be monolithic in a single physical body or can be separate members that are phsycially joined.

[0031] Metrological photon counter 200 can be made in various ways. It should be appreciated that metrological photon counter 200 includes a number of optical, electrical, or mechanical components, wherein such components can be interconnected and placed in communication (e.g., optical communication, electrical communication, mechanical communication, and the like) by physical, chemical, optical, or free-space interconnects. The components can be disposed on mounts that can be disposed on a bulkhead for alignment or physical compartmentalization. As a result, metrological photon counter 200 can be disposed in a terrestrial environment or space environment. Elements of metrological photon counter 200 can be formed from silicon, silicon nitride, and the like although other suitable materials, such ceramic, glass, or metal can be used. According to an embodiment, the elements of metrological photon counter 200 are formed using 3D printing although the elements of metrological photon counter 200 can be formed using other methods, such as injection molding or machining a stock material such as block of material that is subjected to removal of material such as by cutting, laser oblation, and the like. Accordingly, metrological photon counter 200 can be made by additive or subtractive manufacturing. In an embodiment, elements of metrological photon counter 200 are selectively etched to remove various different materials using different etchants and photolithographic masks and procedures. The various layers thus formed can be subjected to joining by bonding to form metrological photon counter 200.

[0032] Metrological photon counter 200 has numerous advantageous and unexpected benefits and uses.

[0033] It is contemplated that metrological photon counter 200 and metrologically counting photons at room temperature can include the properties, functionality, hardware, and process steps described herein and embodied in any of the following non-exhaustive list:

a process (e.g., a computer-implemented method including various steps; or a method carried out by a computer including various steps);

an apparatus, device, or system (e.g., a data processing apparatus, device, or system including means for carrying out such various steps of the process; a data processing apparatus, device, or system including means for carrying out various steps; a data processing apparatus, device, or system including a processor adapted to or configured to perform such various steps of the process);

a computer program product (e.g., a computer program product including instructions which, when the program is executed by a computer, cause the computer to carry out such various steps of the process; a computer program product including instructions which, when the program is executed by a computer, cause the computer to carry out various steps);

computer-readable storage medium or data carrier (e.g., a computer-readable storage medium including instructions which, when executed by a computer, cause the computer to carry out such various steps of the process; a computer-readable storage medium including instructions which, when executed by a computer, cause the computer to carry out various steps; a computer-readable data carrier having stored thereon the computer program product; a data carrier signal carrying the computer program product);

a computer program product including comprising instructions which, when the program is executed by a first computer, cause the first computer to encode data by performing certain steps and to transmit the encoded data to a second computer; or

a computer program product including instructions which, when the program is executed by a second computer, cause the second computer to receive encoded data from a first computer and decode the received data by performing certain steps.

[0034] It should be understood that the calculations, control, and data acquisition or analysis may be performed by any suitable computer system, such as that diagrammatically shown in FIG. 7. Data is entered into system 100 via any suitable type of user interface 116, and may be stored in memory 112, which may be any suitable type of computer readable and programmable memory and is preferably a non-transitory,

computer readable storage medium. Calculations are performed by processor 114, which may be any suitable type of computer processor and may be displayed to the user on display 118, which may be any suitable type of computer display.

[0035] Processor 114 may be associated with, or incorporated into, any suitable type of computing device, for example, a personal computer or a programmable logic controller. The display 118, the processor 114, the memory 112 and any associated computer readable recording media are in communication with one another by any suitable type of data bus, as is well known in the art.

[0036] Examples of computer-readable recording media include non-transitory storage media, a magnetic recording apparatus, an optical disk, a magneto-optical disk, and/or a semiconductor memory (for example, RAM, ROM, etc.). Examples of magnetic recording apparatus that may be used in addition to memory 112, or in place of memory 112, include a hard disk device (HDD), a flexible disk (FD), and a magnetic tape (MT). Examples of the optical disk include a DVD (Digital Versatile Disc), a DVD-RAM, a CD-ROM (Compact Disc-Read Only Memory), and a CD-R (Recordable)/RW. It should be understood that non-transitory computer-readable media include all computer-readable media except for a transitory, propagating signal.

[0037] The processes described herein may be embodied in, and fully automated via, software code modules executed by a computing system that includes one or more general purpose computers or processors. The code modules may be stored in any type of non-transitory computer-readable medium or other computer storage device. Some or all the methods may alternatively be embodied in specialized computer hardware. In addition, the components referred to herein may be implemented in hardware, software, firmware, or a combination thereof.

[0038] Many other variations than those described herein will be apparent from this disclosure. For example, depending on the embodiment, certain acts, events, or functions of any of the algorithms described herein can be performed in a different sequence, can be added, merged, or left out altogether (e.g., not all described acts or events are necessary for the practice of the algorithms). Moreover, in certain embodiments, acts or events can be performed concurrently, e.g., through multi-threaded processing, interrupt processing, or multiple processors or processor cores or on other parallel architectures, rather than sequentially. In addition, different tasks or processes

can be performed by different machines and/or computing systems that can function together.

[0039] Any logical blocks, modules, and algorithm elements described or used in connection with the embodiments disclosed herein can be implemented as electronic hardware, computer software, or combinations of both. To clearly illustrate this interchangeability of hardware and software, various illustrative components, blocks, modules, and elements have been described above generally in terms of their functionality. Whether such functionality is implemented as hardware or software depends upon the particular application and design constraints imposed on the overall system. The described functionality can be implemented in varying ways for each particular application, but such implementation decisions should not be interpreted as causing a departure from the scope of the disclosure.

[0040] The various illustrative logical blocks and modules described or used in connection with the embodiments disclosed herein can be implemented or performed by a machine, such as a processing unit or processor, a digital signal processor (DSP), an application specific integrated circuit (ASIC), a field programmable gate array (FPGA) or other programmable logic device, discrete gate or transistor logic, discrete hardware components, or any combination thereof designed to perform the functions described herein. A processor can be a microprocessor, but in the alternative, the processor can be a controller, microcontroller, or state machine, combinations of the same, or the like. A processor can include electrical circuitry configured to process computer-executable instructions. In another embodiment, a processor includes an FPGA or other programmable device that performs logic operations without processing computer-executable instructions. A processor can also be implemented as a combination of computing devices, e.g., a combination of a DSP and a microprocessor, a plurality of microprocessors, one or more microprocessors in conjunction with a DSP core, or any other such configuration. Although described herein primarily with respect to digital technology, a processor may also include primarily analog components. For example, some or all of the signal processing algorithms described herein may be implemented in analog circuitry or mixed analog and digital circuitry. A computing environment can include any type of computer system, including, but not limited to, a computer system based on a microprocessor, a mainframe computer, a digital signal processor, a portable computing device, a device controller, or a computational engine within an appliance, to name a few.

[0041] The elements of a method, process, or algorithm described in connection with the embodiments disclosed herein can be embodied directly in hardware, in a software module stored in one or more memory devices and executed by one or more processors, or in a combination of the two. A software module can reside in RAM memory, flash memory, ROM memory, EPROM memory, EEPROM memory, registers, hard disk, a removable disk, a CD-ROM, or any other form of non-transitory computer-readable storage medium, media, or physical computer storage known in the art. An example storage medium can be coupled to the processor such that the processor can read information from, and write information to, the storage medium. In the alternative, the storage medium can be integral to the processor. The storage medium can be volatile or nonvolatile.

[0042] While one or more embodiments have been shown and described, modifications and substitutions may be made thereto without departing from the spirit and scope of the invention. Accordingly, it is to be understood that the present invention has been described by way of illustrations and not limitation. Embodiments herein can be used independently or can be combined.

[0043] All ranges disclosed herein are inclusive of the endpoints, and the endpoints are independently combinable with each other. The ranges are continuous and thus contain every value and subset thereof in the range. Unless otherwise stated or contextually inapplicable, all percentages, when expressing a quantity, are weight percentages. The suffix (s) as used herein is intended to include both the singular and the plural of the term that it modifies, thereby including at least one of that term (e.g., the colorant(s) includes at least one colorants). Option, optional, or optionally means that the subsequently described event or circumstance can or cannot occur, and that the description includes instances where the event occurs and instances where it does not. As used herein, combination is inclusive of blends, mixtures, alloys, reaction products, collection of elements, and the like.

[0044] As used herein, a combination thereof refers to a combination comprising at least one of the named constituents, components, compounds, or elements, optionally together with one or more of the same class of constituents, components, compounds, or elements.

[0045] All references are incorporated herein by reference.

[0046] The use of the terms “a,” “an,” and “the” and similar referents in the context of describing the invention (especially in the context of the following claims) are to be construed to cover both the singular and the plural, unless otherwise indicated herein or clearly contradicted by context. It can further be noted that the terms first, second, primary, secondary, and the like herein do not denote any order, quantity, or importance, but rather are used to distinguish one element from another. It will also be understood that, although the terms first, second, etc. are, in some instances, used herein to describe various elements, these elements should not be limited by these terms. For example, a first current could be termed a second current, and, similarly, a second current could be termed a first current, without departing from the scope of the various described embodiments. The first current and the second current are both currents, but they are not the same condition unless explicitly stated as such.

[0047] The modifier about used in connection with a quantity is inclusive of the stated value and has the meaning dictated by the context (e.g., it includes the degree of error associated with measurement of the particular quantity). The conjunction or is used to link objects of a list or alternatives and is not disjunctive; rather the elements can be used separately or can be combined together under appropriate circumstances.

CLAIMS

What is claimed is:

1. A metrological photon counter, the metrological photon counter comprising:

an undoped semiconductor;

an anti-reflection coating on one portion of a first side of the undoped semiconductor;

a thin insulating layer on another portion of the first side of the undoped semiconductor not covered by the anti-reflection coating;

a snaking wedge electrode on the thin insulating layer, comprising: at least two electrodes and at least one resistor electrically connected alternately in series;

a top well electrode on the thin insulating layer; and

a field-effect-transistor on the first side of the undoped semiconductor;

wherein the snaking wedge electrode is positioned in relatively closer proximity to the anti-reflection coating than the top well electrode;

wherein the top well electrode is positioned in relatively closer proximity to the anti-reflection coating than the field-effect-transitor; and

wherein the at least two electrodes of the snaking wedge electrode are arranged in an approximately perpendicular orientation relative to the direction from the anti-reflection coating to the field-effect-transistor.

2. The metrological photon counter of claim 1, additionally comprising a bottom electrode on a second side of the undoped semiconductor, the second side being opposite the first side of the undoped semiconductor.

3. The metrological photon counter of claim 1, additionally comprising:

a second thin insulating layer on a second side of the undoped semiconductor, the second side being opposite the first side of the undoped semiconductor;

a second snaking wedge electrode on the second thin insulating layer, comprising: at least two electrodes and at least one resistor electrically connected alternately in series;

a second top well electrode on the second thin insulating layer; and

a second field-effect-transistor on the second side of the undoped semiconductor;

wherein the snaking wedge electrode is positioned such that it extends from opposite the anti-reflection coating of the first side to being opposite the thing insulating layer of the first side;

wherein the second top well electrode is positioned in approximately opposite the top well electrode of the first side;

wherein the second field-effect-transistor is positioned approximately opposite the field-effect-transistor of the first side; and

wherein the at least two electrodes of the second snaking wedge electrode are arranged in an approximately perpendicular orientation relative to the direction from the anti-reflection coating to the second field-effect-transistor.

4. The metrological photon counter of claim 1, wherein the field-effect transistor is a MOSFET.

5. The metrological photon counter of claim 4, wherein the field-effect transistor is a floating-gate MOSFET.

6. The metrological photon counter of claim 1, wherein the electrodes of the snaking wedge electrode decrease in size as they extend towards the field-effect-transistor, such that the electrode furthest from the field-effect-transistor spans the greatest width of the undoped semiconductor, and such that the electrode closest to the field-effect transistor spans the shortest width of the undoped semiconductor.

7. A method for metrologically counting photons, the method comprising:

exposing a metrological photon counter to a source of photons, the metrological photon counter comprising: an undoped semiconductor with an anti-reflection coating on one portion of a first side of the undoped semiconductor and a thin insulating layer on another portion of the first side of the undoped semiconductor;

creating an electric field near the first surface of the undoped semiconductor underneath the thin insulating layer by applying a current to a snaking wedge electrode on the thin insulating layer;

creating a relatively higher voltage electric field near the first surface of the undoped semiconductor underneath the thin insulating layer by applying a relatively higher voltage to a top well electrode on the thin insulating layer; and

detecting a change in current in a field-effect-transistor on the first side of the undoped semiconductor;

wherein the snaking wedge electrode comprises at least two electrodes and at least one resistor electrically connected alternately in series;

wherein the snaking wedge electrode is positioned in relatively closer proximity to the anti-reflection coating than the top well electrode;

wherein the top well electrode is positioned in relatively closer proximity to the anti-reflection coating than the field-effect-transitor; and

wherein the at least two electrodes of the snaking wedge electrode are arranged in an approximately perpendicular orientation relative to the direction from the anti-reflection coating to the field-effect-transistor.

8. The method of claim 7, wherein the electrodes of the snaking wedge electrode decrease in size as they extend towards the field-effect-transistor, such that the electrode furthest from the field-effect-transistor spans the greatest width of the undoped semiconductor, and such that the electrode closest to the field-effect transistor spans the shortest width of the undoped semiconductor.

9. The method of claim 8, wherein when current is applied to the snaking wedge electrode, the voltage of the smallest electrode in the snaking wedge electrode is highest, and wherein the voltage decreases in each successively larger electrode in the snaking wedge electrode.

10. The method of claim 7, wherein a voltage is applied to a bottom electrode on a second side of the undoped semiconductor, the second side being opposite the first side of the undoped semiconductor.

11. The method of claim 10, wherein the voltage applied to the bottom electrode is selected to attract holes.

12. The method of claim 7, wherein the field-effect-transistor is a floating-gate MOSFET.

13. The method of claim 12, wherein the effect of an electron generated by a photon in the metrological photon counter produces a change in current of greater than 1% over base current when the electron interacts with a floating node of the floating-gate MOSFET.

14. The method of claim 7, wherein metrological photon counter is configured such that the detection of a change in current in the field-effect transistor corresponds to an integer number of photons.

15. The method of claim 7, wherein the metrological photon counter is operated a room temperature.

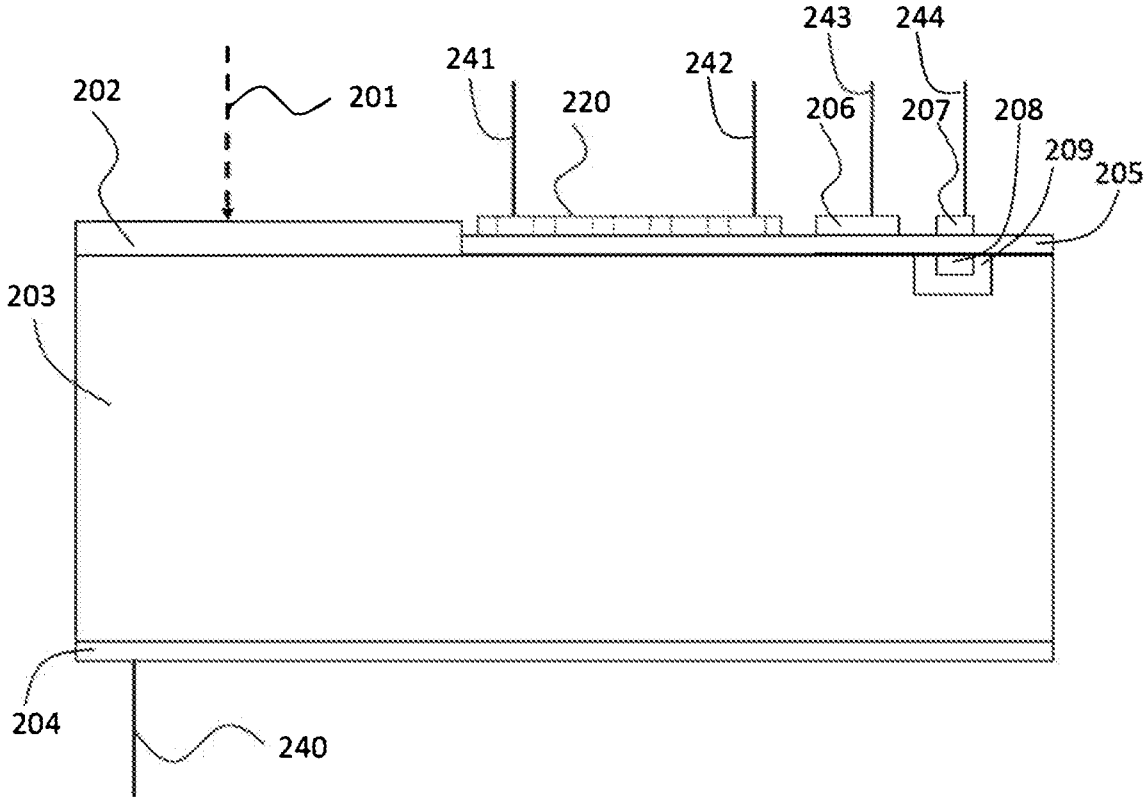


FIG. 1

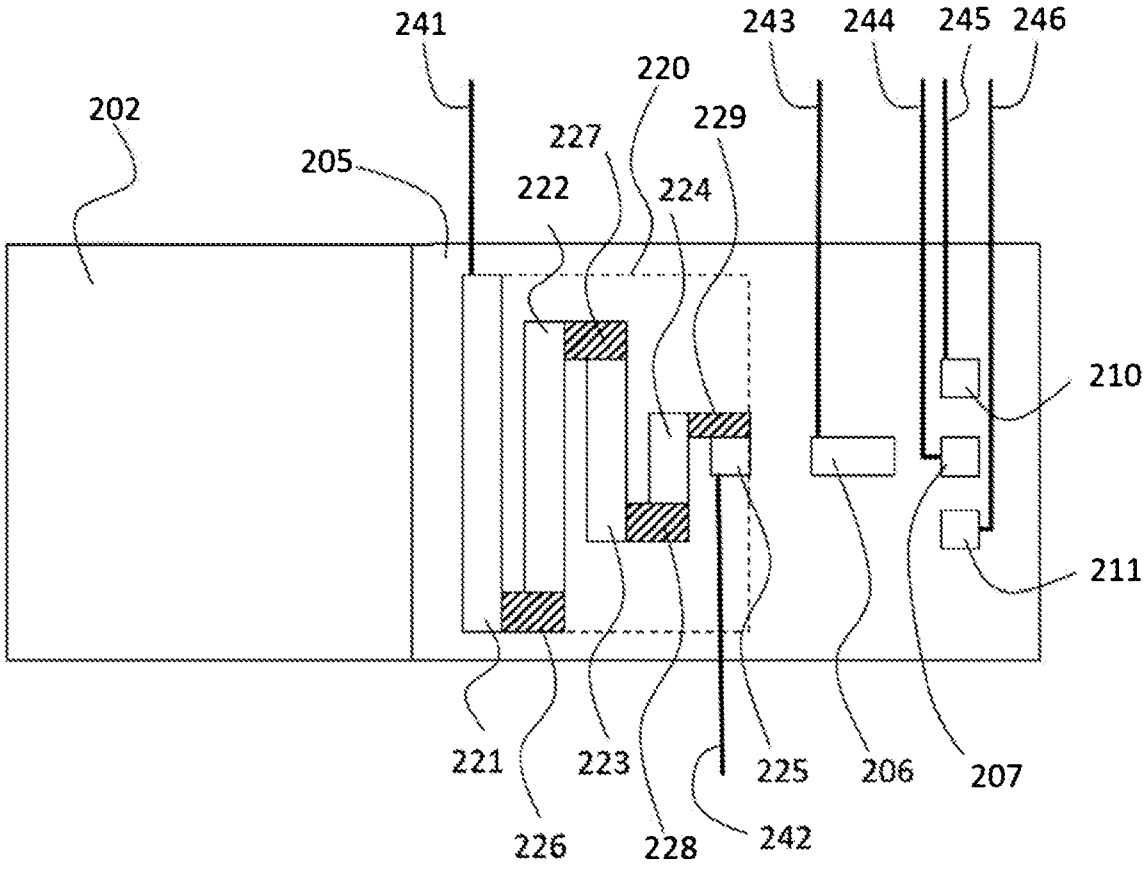

241
243
244
245
246
220
202
227
229
205
222
224
210
211
221
223
225
206
207
226
228
242

FIG. 2

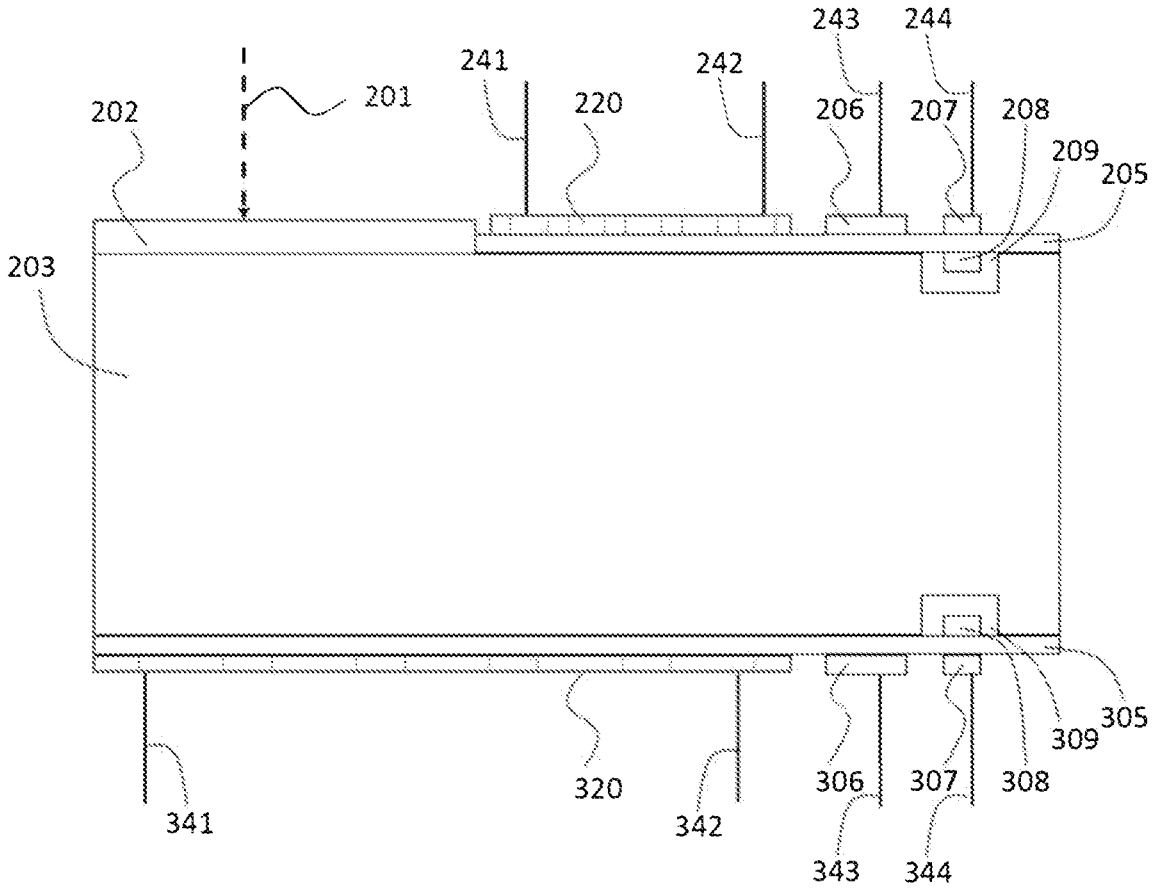

243
244
241
242
201
202
220
206
207
208
209
205
203
305
309
306
307
308
320
341
342
343
344

FIG. 3

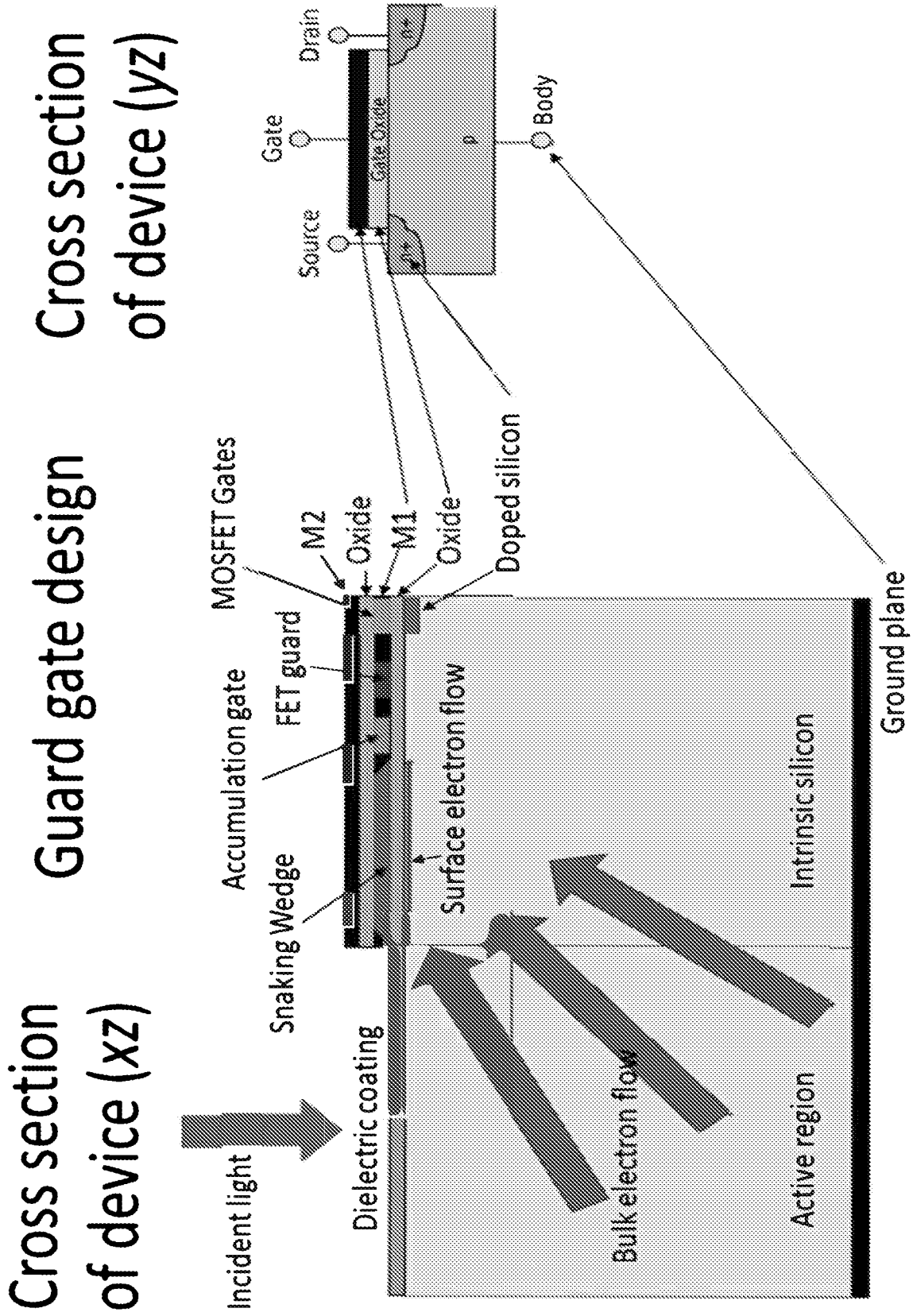

Cross section of device (xz)
Guard gate design
Cross section of device (yz)
Incident light
Dielectric coating
Snaking Wedge
Accumulation gate
FET guard
MOSFET Gates
M2
Oxide
M1
Oxide
Doped silicon
Surface electron flow
Bulk electron flow
Active region
Intrinsic silicon
Ground plane
Source
Gate
Drain
Gate Oxide
Body

FIG. 4

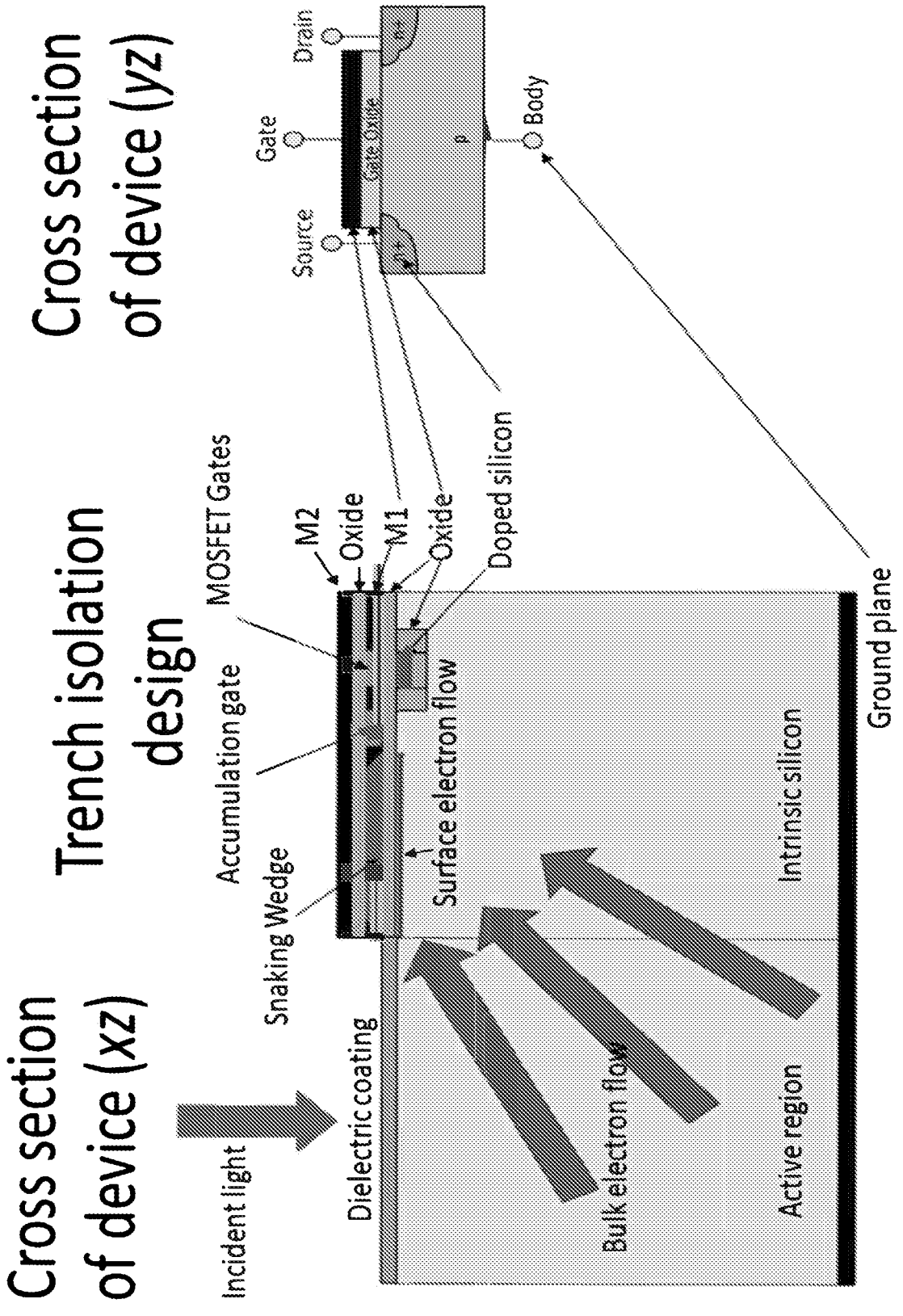

Cross section of device (xz)
Trench isolation design
Cross section of device (yz)
Incident light
Dielectric coating
Snaking Wedge
Accumulation gate
MOSFET Gates
M2
Oxide
M1
Oxide
Doped silicon
Surface electron flow
Bulk electron flow
Active region
Intrinsic silicon
Ground plane
Gate
Drain
Source
Gate Oxide
Body

FIG. 5

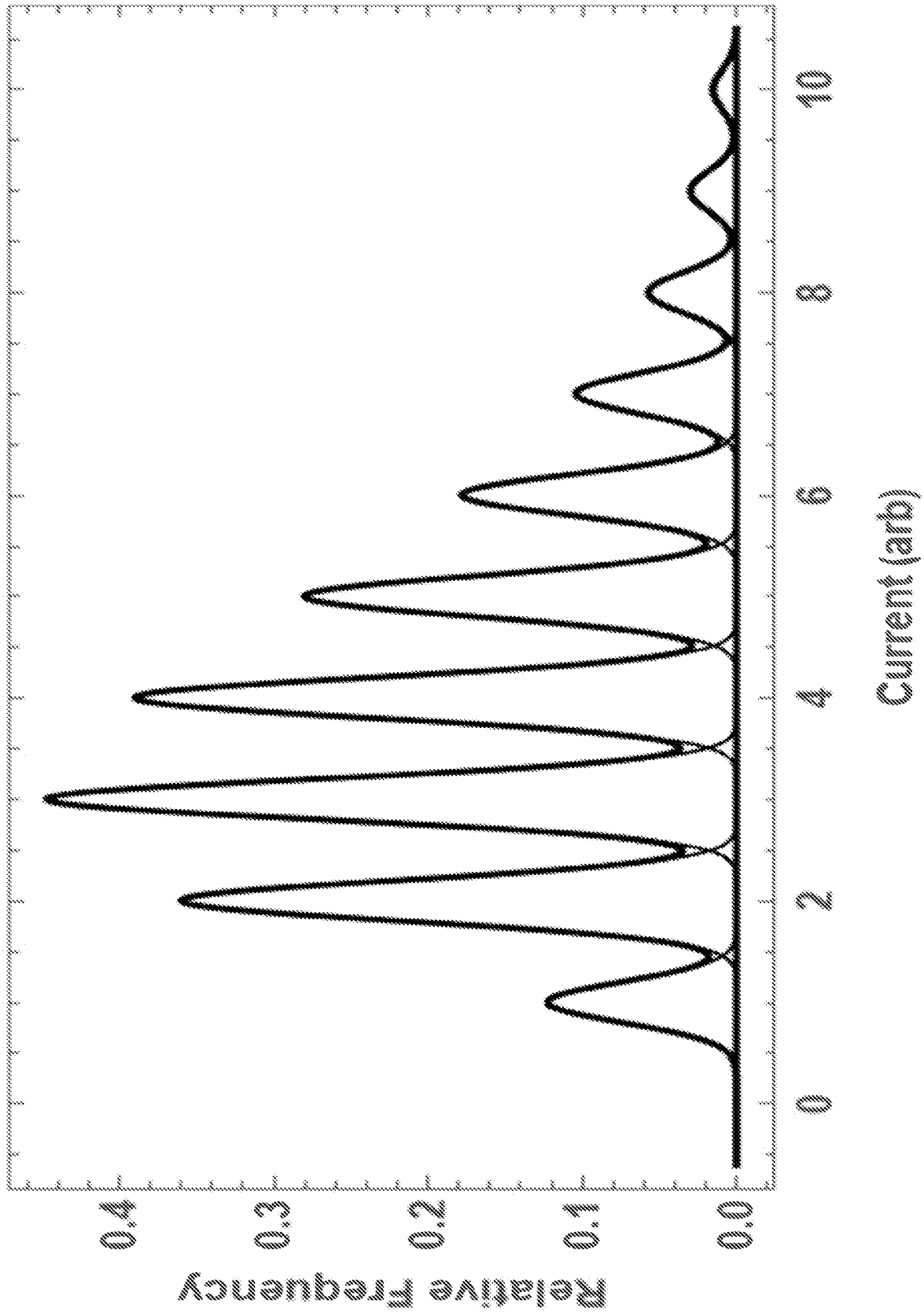


FIG. 6

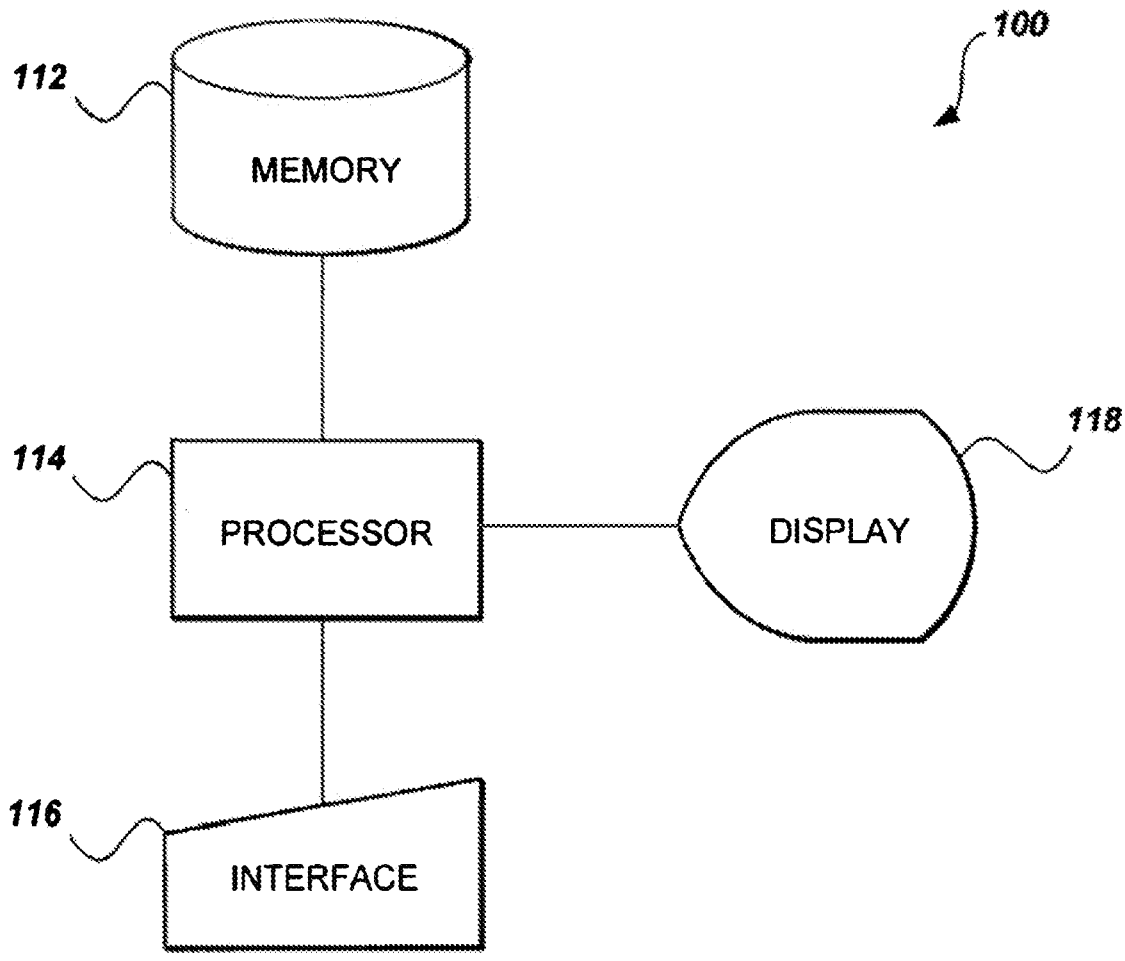


FIG. 7

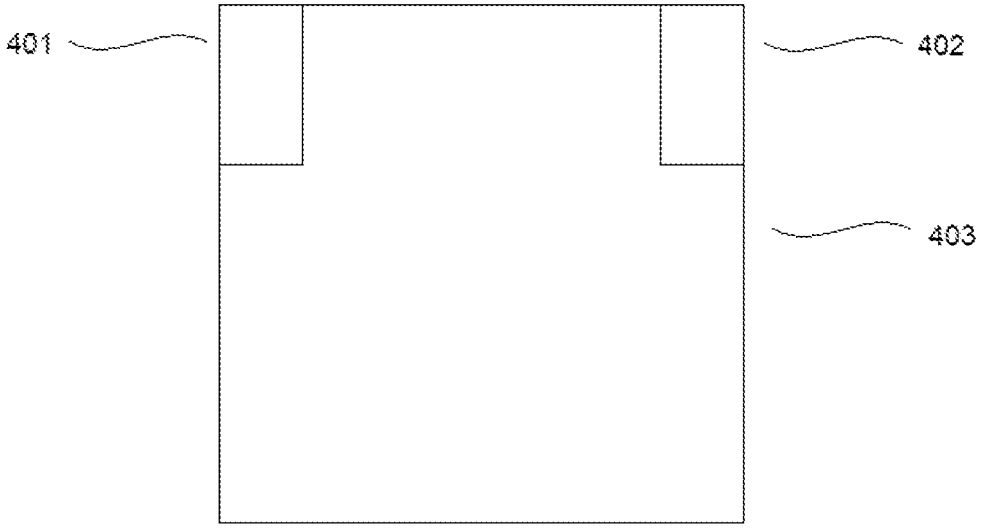


FIG. 8

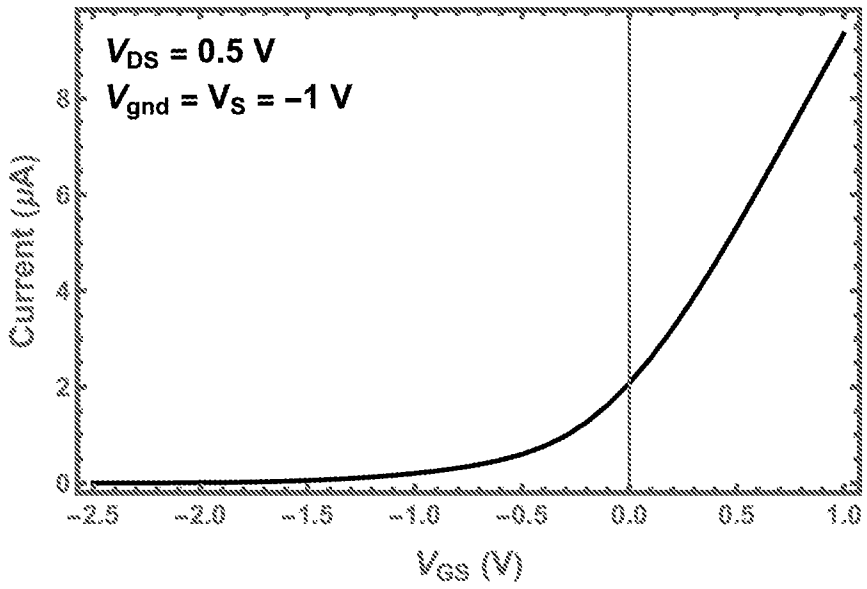

V_{DS} = 0.5 V
V_{gnd} = V_S = –1 V
Current (μA)
0
2
4
6
8
–2.5
–2.0
–1.5
–1.0
–0.5
0.0
0.5
1.0
V_{GS} (V)

FIG. 9

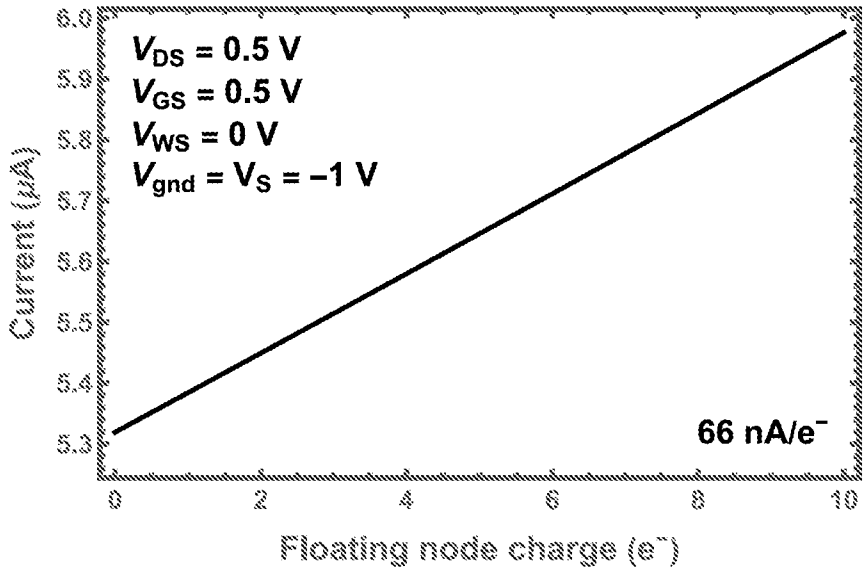

V_{DS} = 0.5 V
V_{GS} = 0.5 V
V_{WS} = 0 V
V_{gnd} = V_S = –1 V
66 nA/e⁻
Current (μA)
5.3
5.4
5.5
5.6
5.7
5.8
5.9
6.0
0
2
4
6
8
10
Floating node charge (e⁻)

FIG. 10

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2025/012217

A. CLASSIFICATION OF SUBJECT MATTER

IPC: ***G01T 1/24*** (2025.01); ***G01J 1/42*** (2025.01); *G01S 7/4863* (2025.01)

CPC: ***G01T 1/241; G01J 1/42;*** *G01S 7/4863*

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

See Search History Document

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

See Search History Document

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

See Search History Document

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2013/0009265 A1 (DAUTET et al.) 10 January 2013 (10.01.2013) entire document	1-15
A	US 2018/0206804 A1 (KABUSHIKI KAISHA TOSHIBA) 26 July 2018 (26.07.2018) entire document	1-15
A	US 2022/0057317 A1 (CAPTL LLC) 24 February 2022 (24.02.2022) entire document	1-15
A	US 2023/0299114 A1 (PANASONIC INTELLECTUAL PROPERTY MANAGEMENT CO. LTD.) 21 September 2023 (21.09.2023) entire document	1-15
A	US 2021/0343762 A1 (SEMIKING LLC) 04 November 2021 (04.11.2021) entire document	1-15
A	US 2023/0358608 A1 (SONY SEMICONDUCTOR SOLUTIONS CORPORATION) 09 November 2023 (09.11.2023) entire document	1-15

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"D" document cited by the applicant in the international application

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
05 March 2025 (05.03.2025)	**10 April 2025 (10.04.2025)**

Name and mailing address of the ISA/US	Authorized officer
COMMISSIONER FOR PATENTS **MAIL STOP PCT, ATTN: ISA/US** **P.O. Box 1450** **Alexandria, VA 22313-1450** **UNITED STATES OF AMERICA**	**TAINA MATOS**
Facsimile No. **571-273-8300**	Telephone No. **571-272-4300**