NANOFAB METROLOGY

CNST Center for Nanoscale Science & Technology

Monolithic Silicon Wafer Line-Width Standards

PROJECT LEADER: Craig McGray (NIST)

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GOAL

To develop nanoscale linewidth standard materials with near-atomically-smooth surfaces in order to improve the traceability of the meter.

KEY ACCOMPLISHMENTS

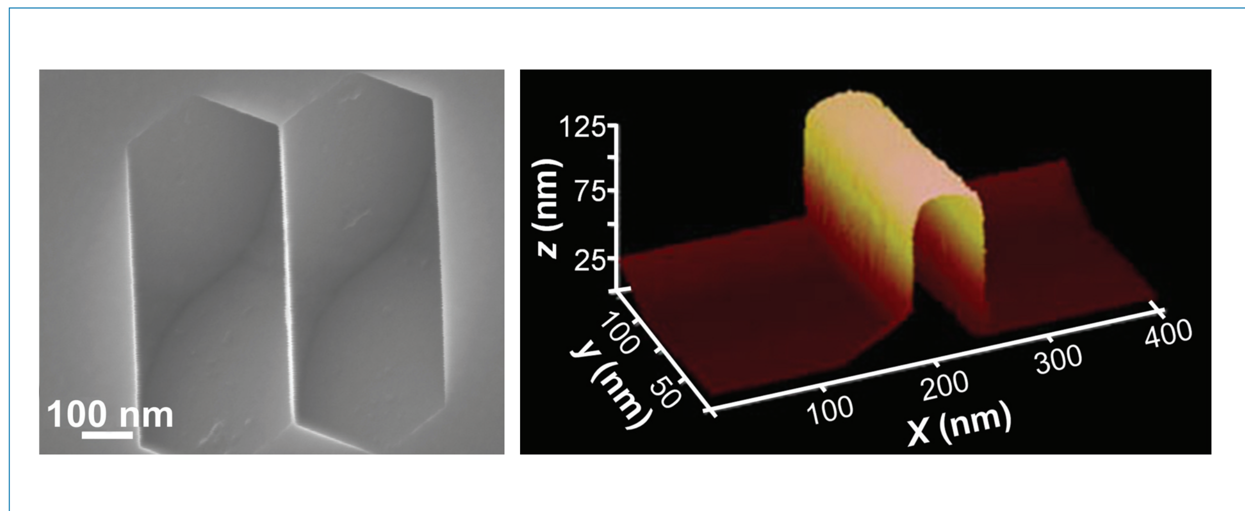
Achieved sidewall roughness as low as 0.6 nm (two atoms).

Fabricated a full range of widths from 200 nm down to 5 nm for linearity assessment.

KEY NANOFAB PROCESS

Electron beam lithography to define lines for chemical etching.

A scanning electron micrograph of a next-generation linewidth standard structure where the center line is defined by the two adjacent crystallographically-etched hexagonal pits. The 3D topography of the central structure as measured by atomic force microscopy.



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