Collaboration: The Semiconductor Industry's Path to Survival and Growth

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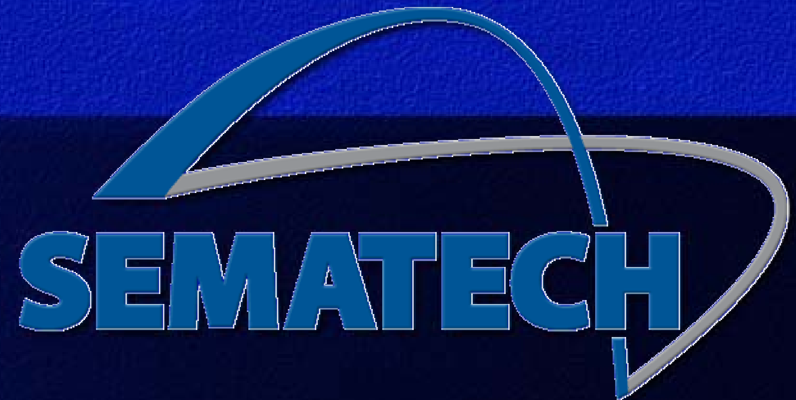
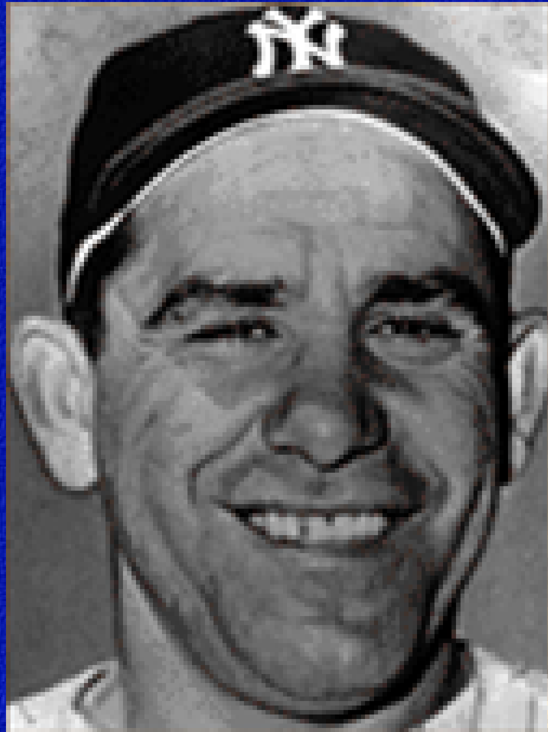
President and CEO
SEMATECH

15 March 2005



Outline

- Environment
  - Economic Challenges
  - Technology Challenges
- Solutions
  - Innovation and Manufacturability through Collaboration
    - SEMATECH examples



“The future ain't what it used to be…”

- Yogi Berra

The Electronics Ecosystem

Global GDP	$36,356T
Electronics	$1,240B
Semiconductors	$213B
Semi. Equipment	$52B
Materials	$28B

2004 data (GDP from 2003) Sources: World Bank, World Semiconductor Trade Statistics, VLSI Research, SIA, SEMI

Making the world

SMALLER

Growth may slow, but will continue…

Sources: Gartner Dataquest and SIA, February 2004

Business Challenges
The new economy for microelectronics

- **Affordability**
  - Increasing costs
    - Capital
    - Manufacturing
    - R&D

- **Manufacturability**
  - Fab and equipment productivity

Accelerating the next technology revolution.

Semiconductor Manufacturing Challenge

Wafer Fab Cost Trend

Year	Cost ($B)
1975	$0.05
1980	$0.1
1985	$0.2
1990	$0.4
1995	$1.0
2000	$1.6
2005E	$2.4
2010E	$3.3

Cost ($B)

Source: IC Insights, Inc. Mclean Report, 2004

Semiconductor R&D Challenge

Chip Making R&D Versus Revenues

Source: VLSI Research Inc., 2004

International Technology Roadmap for Semiconductors

Minimum Feature Size (nm)
(DRAM Half-Pitch)

350
250
180
130
100
70
50
35
22

1994
1997
1998/1999
2000
2001
2003/2004

1995 1997 1999 2001 2003 2005 2007 2009 2011 2013 2015 2017

Accelerating the next technology revolution.

Technology Challenges

Innovation required

Still no known solutions in many areas:

- Lithography
- Front End
- Interconnect
- Metrology

Table 71a Thermal and Thin Film, Doping and Etching Technology Requirements—Near-term UPDATED

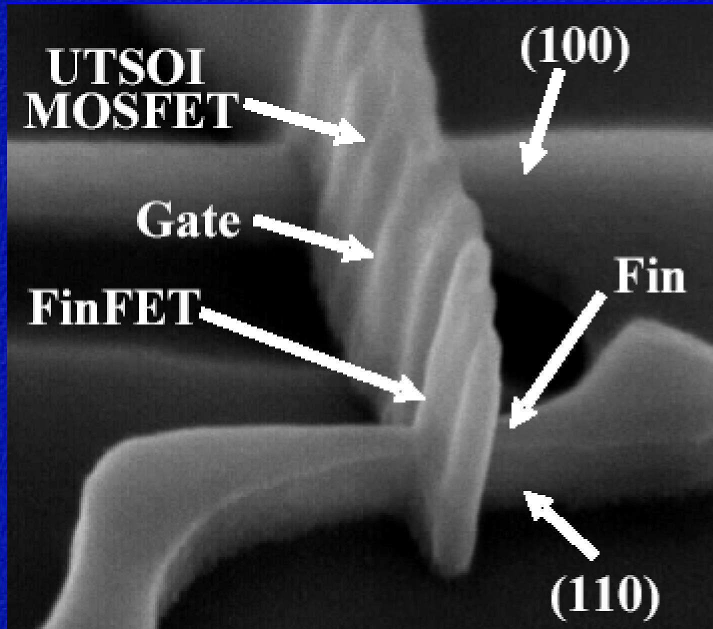
Year of Production	*2003*	*2004*	*2005*	*2006*	*2007*	*2008*	*2009*	*Driver*
Technology Node		*hp90*			*hp65*			
DRAM ½ Pitch (nm)	*100*	*90*	*80*	*70*	*65*	*57*	*50*	*DRAM*
MPU/ASIC ½ Pitch (nm)	*107*	*90*	*80*	*70*	*65*	*57*	*50*	*MPU*
MPU Printed Gate Length (nm)	*65*	*53*	*45*	*40*	*35*	*32*	*28*	*MPU*
MPU Physical Gate Length (nm)	*45*	*37*	*32*	*28*	*25*	*22*	*20*	*MPU*
Equivalent physical oxide thickness for MPU/ASIC T_{ox} (nm) [A, A1]	1.3	1.2	1.1	1	0.9	0.8	0.8	*MPU*
Gate dielectric leakage at 100°C (nA/μm) High-performance [B, B1, B2]	100	170	170	170	230	230	230	*MPU*
Physical gate length low operating power (LOP) (nm)	65	53	45	37	32	28	25	*Low Power*
Physical gate length low standby power (LSTP) (nm)	75	65	53	45	37	32	28	*LSTP*
Equivalent physical oxide thickness for low operating power T_{ox} (nm) [A, A1]	1.6	1.5	1.4	1.3	1.2	1.1	1	*LOP*
Gate dielectric leakage at 100°C (nA/μm) LOP [B,B1, B2]	0.33	1	1	1	1.67	1.67	1.67	*LOP*
Equivalent physical oxide thickness for low standby power T_{ox} (nm) [A, A1]	2.2	2.1	2.1	1.9	1.6	1.5	1.4	*LSTP*
Gate dielectric leakage at 100°C (pA/μm) LSTP [B, B1, B2]	3	3	5	7	8	10	13	*LSTP*
Thickness control EOT (% 3σ) [C]	<±4	<±4	<±4	<±4	<±4	<±4	<±4	*MPU/ASIC*
Gate etch bias (nm) [D]	20	16	14	12	10	10	8	*MPU/ASIC*
L_{gate} 3σ variation (nm) [E]	◆ 4.46	◆ 3.75	◆ 3.15	2.81	2.5	2.2	2	
Total maximum allowable lithography 3σ (nm) [F]	3.99	3.35	2.82	2.51	2.24	1.97	1.79	*MPU/ASIC*
Total maximum allowable etch 3σ (nm), including photoresist trim and gate etch [F]	◆ 1.99	◆ 1.68	◆ 1.41	1.26	1.12	0.98	0.89	*MPU/ASIC*
Resist trim maximum allowable 3σ (nm) [G]	◆ 1.16	◆ 0.97	◆ 0.82	0.73	0.65	0.57	0.52	*MPU/ASIC*
Gate etch maximum allowable 3σ (nm) [G]	1.62	◆ 1.37	◆ 1.15	1.02	0.91	0.8	0.73	*MPU/ASIC*
CD bias between dense and isolated lines [H]	≤15%	◆ ≤15	◆ ≤15	≤15%	≤15%	≤15%	≤15%	*MPU/ASIC*
Minimum measurable gate dielectric remaining (post gate etch clean) [I]	>0	>0	>0	>0	>0	>0	>0	*MPU/ASIC*
Profile control (side wall angle) [J]	>89	90	90	90	90	90	90	*MPU/ASIC*
*PIDS Assumed Device Structure**	Enhanced Planar Bulk CMOS					FDSOI, Elev. Contact *		
Drain extension Xj (nm) [K]	24.8	20.4	17.6	15.4	13.8	8.8	8	*MPU/ASIC*
Maximum drain extension sheet resistance (PMOS) (Ω/sq) [L]	545	663	767	833	884	1739	1800	*MPU/ASIC*
Maximum drain extension sheet resistance (NMOS) (Ω/sq) [L]	255	310	358	389	412	811	840	*MPU/ASIC*
Extension lateral abruptness (nm/decade) [M]	5	4.1	3.5	3.1	2.8	TBD	TBD	*MPU/ASIC*
Contact Xj (nm) [N]	49.5	40.7	35.2	30.8	27.5	NA	NA	*MPU/ASIC*

Source: ITRS 2004

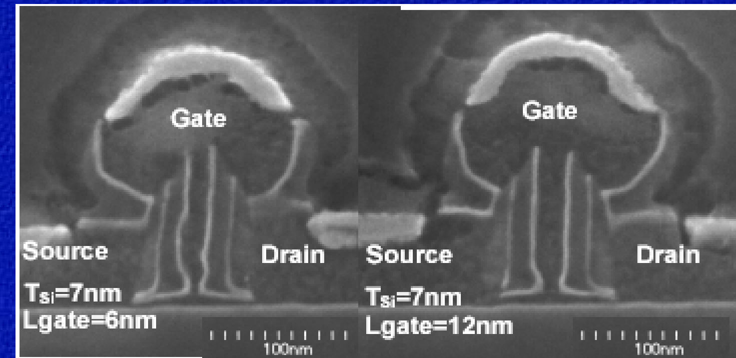
Future Transistors

Non-classical CMOS will take us through next 15 years

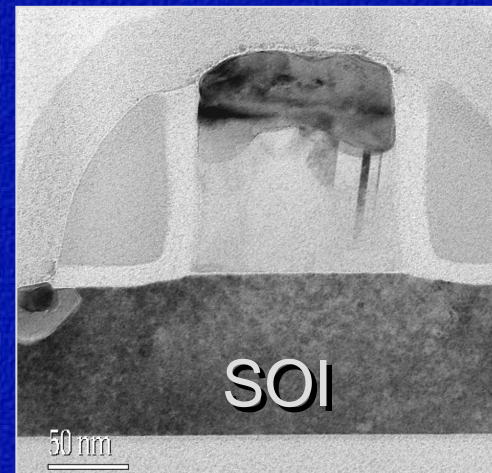
Many Approaches



nMOS MOSFET
pMOS FINFET



Sub 10 nm Beyond CMOS
Already Demonstrated

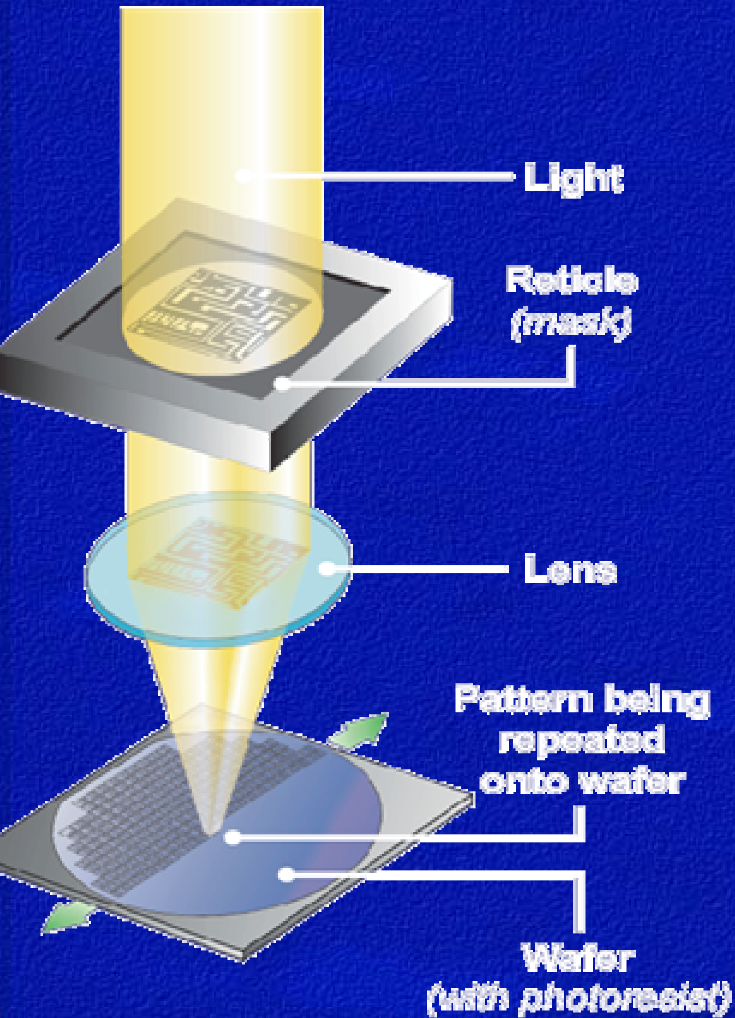


Transistor on thin SOI

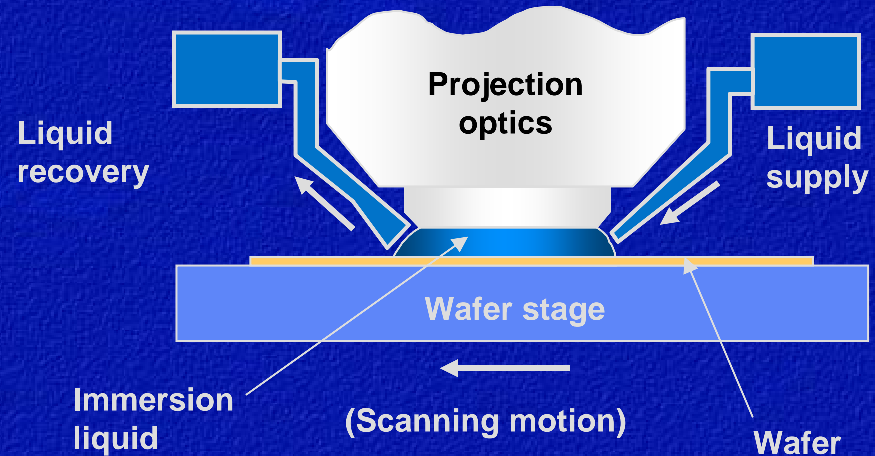
Source: Bruce Doris (IBM)

Future Patterning

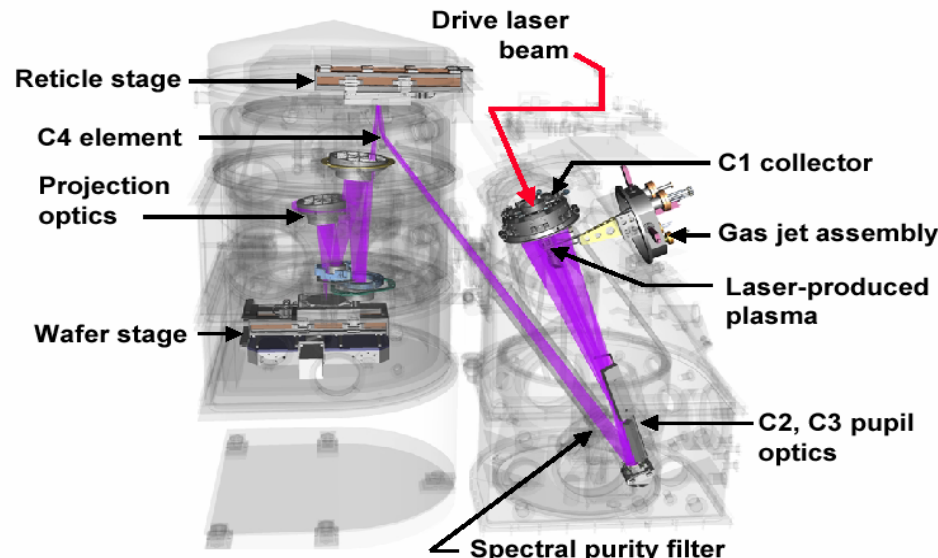
Traditional



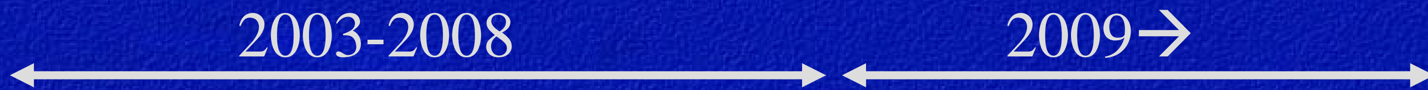
Immersion



EUV



Future Connectivity



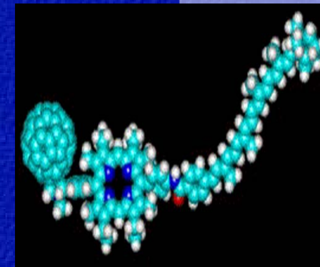
k_{eff} ~ 3.1-3.6	k_{eff} ~ 2.7-3.0	k_{eff} ~ 2.3-2.6

Cu Low k & Reliability

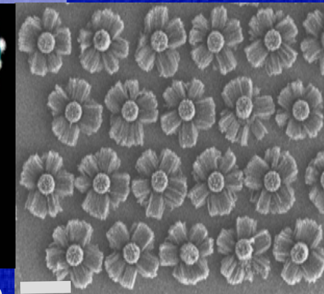
Projects

Projects

3D



Optically active Molecules

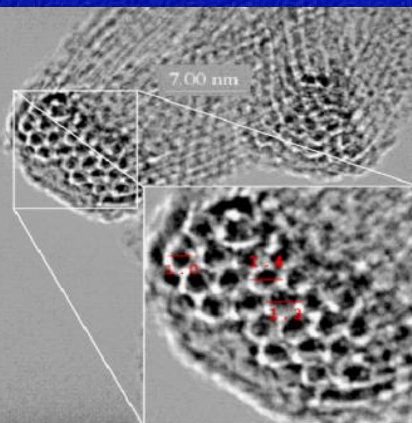


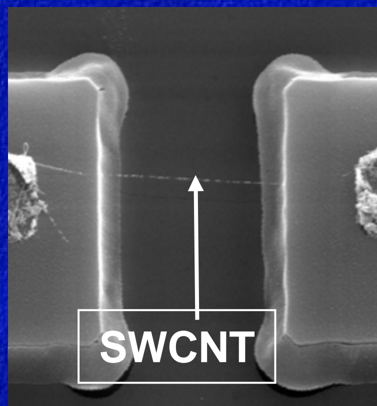
Nanotubes

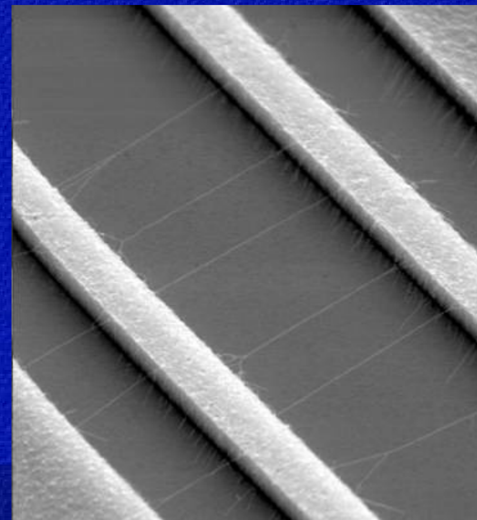
Future Connectivity

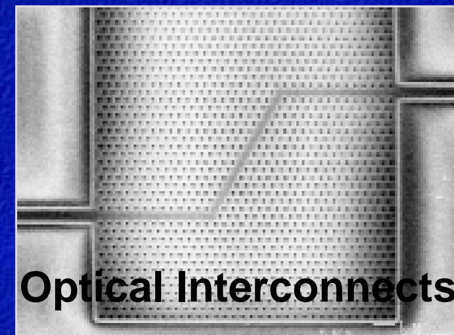
Determine;
Roadmap
Timelines
Critical Needs

Next Generation Interconnect





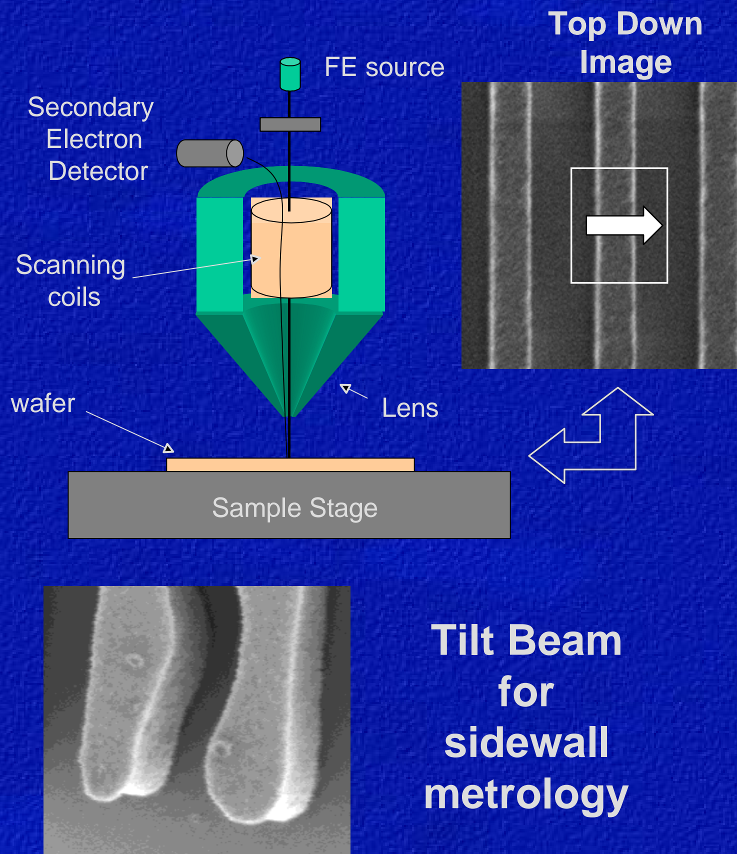


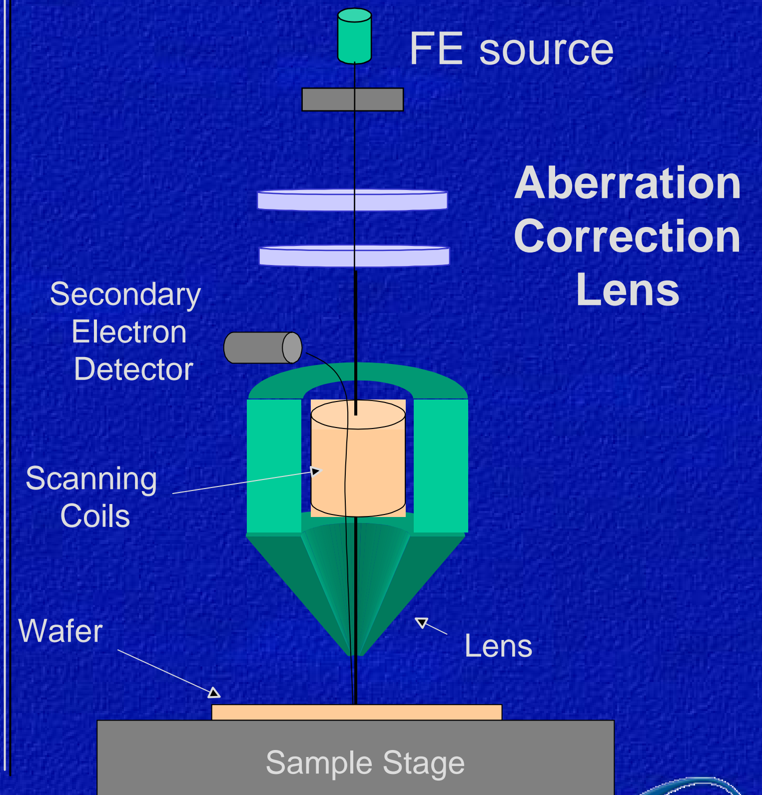


Future Metrology

CD-SEM of the Future?

Migration of TEM LENS Technology to SEM





Future Manufacturing

Active ISMI Project
Future projects

On-line Specs & Tool Maintenance Manuals

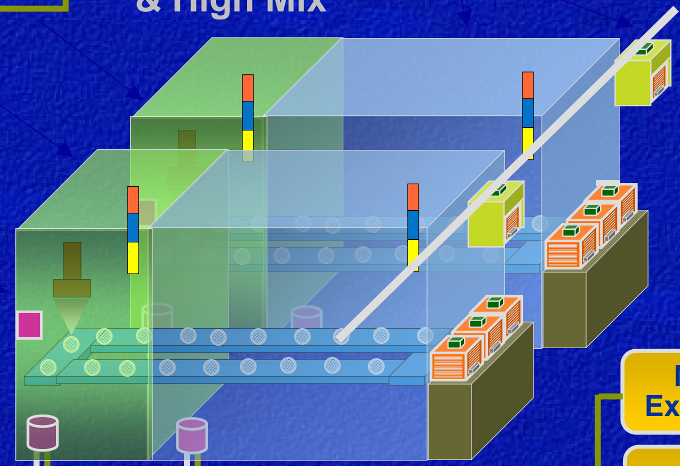
Faster Cycle time Fabs for Hot Lots & High Mix

Predictive Maintenance

Wafer Level Tracking and Recipe/Parameter Changes

Large Scale Process Control Systems

Efficient Spares Management



100% Direct Transport AMHS for Fast Cycle Time

Manufacturing Execution Systems

Equipment Control Systems

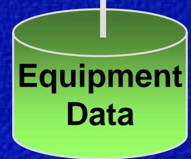
Factory Scheduler And Material Control

SECS Control Line

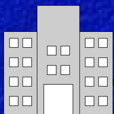
Rapid Process Matching

Equipment Engineering Capabilities (EEC)

R2R | FDC | SPC | Recipes
Yield | PCS | e-Diag. | EPT



Equipment Data Acquisition (EDA) for Rich Standardized Data



Partner, Customer Or Supplier

Pervasive Remote Diagnostics

Today
10 chambers
10 variables per chamber
3 Hz rate each
300 values per sec

EDA Goal
10 chambers
50 variables per chamber
10 Hz rate each
10,000 values per sec

The New Economy for Microelectronics

- Slower growth of industry foreseen, compared to last 30 years
- Escalating R&D, capital, and manufacturing costs
  - A new factory at 90nm technology on 300mm wafers has a capital cost of $2-3B
  - Rising technology R&D product cycle costs
- Staggering technology challenges
  - 193 immersion/EUV, high/low-k, masks, 3D interconnect, 300mm/450mm
- Changing business models in the industry
  - Foundries, fabless and fab-lite
  - New alliances and partnerships

Collaboration at All Levels

- Device manufacturers
  - Crolles cluster: Freescale, Philips, STMicro, TSMC
  - IBM cluster: AMD, IBM, Infineon, Samsung
- Equipment and materials suppliers and device manufacturers
  - SEMATECH, Selete, individual companies
- Universities
  - SRC/MARCO Focus Centers
  - SEMATECH AMRC programs
- Governments
  - Texas Advanced Materials Center
  - Albany Nanotech
  - IMEC
- Suppliers

Innovation and Manufacturability

Two ways to sustain Moore's Law

Moore's Law

$\frac{\text{cost (\$)}}{\text{Function}}$ (Transistors/bits)

$\frac{\text{cost (\$)}}{\text{area (cm}^2)}$

$\frac{\text{transistors}}{\text{area (cm}^2)}$

$\frac{\text{cost (\$)}}{\text{wafer}}$

$\frac{\text{area (cm}^2)}{\text{wafer}}$

Reduce Opperating Cost ($)

Increase Good Wafer Output

$\frac{\text{Wafers}}{\text{Tool set}}$

$\frac{\text{cost (\$)}}{\text{Tool set}}$

OEE

COO

Wafer Size Conversion

Productivity Challenges

Design Lithography Metrology
Front-End Process Interconnect

Technology Challenges

SEMATECH
Worldwide collaboration

PHILIPS

Panasonic

Infineon technologies

SPANSION™

tsmc

intel

HEWLETT PACKARD

IBM

AMD

freescale semiconductor

Texas Instruments

SEMATECH: Focus on Innovation and Manufacturability

- SEMATECH is the catalyst for accelerating the commercialization of technology innovations into manufacturing solutions
    - *Accelerated commercialization of university research (**AMRC**)*
    - *Advanced technology innovations (**SEMATECH**)*
    - *Manufacturing productivity (**ISMI**)*
    - *World-class R&D processing & prototyping (**ATDF**)*
- Benefits of collaboration
    - Save money
    - Reduce risk
    - Accelerate development
    - Increase productivity

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Accelerating the next technology revolution

FOSTERING INNOVATION

Advanced Gate Stack for 45nm Node
Fundamental Materials Understanding

97	98	99	00	01	02	03	04	05	06	07

- Began high-k program with Ta_2O_5, TiO_2, etc
- FEP-RC identified HfO2
- Hf based oxide
- Metal/high-k stack
- Implementation strategy

Electrical test methods

Metal electrode materials

Aggressive targets for HP 45nm node → EOT ~0.6nm, μ~65% · 0.8nm, 85% · 0.8nm, 90%

SEMATECH FEP/Advanced Gate Stack Program

SRC/FEP-RC | **SRC/FEP-TC**

AMRC

Suppliers

Working with more than 40 universities, suppliers, and consortia

Advanced Materials Research Center

Accelerating commercialization of university research

State of Texas

SEMATECH

Select Semiconductor Programs

Advanced Materials Research Center (AMRC)

Select programs in:
Semiconductors, Nanotechnology

Texas Universities

Attributes

- Accelerate commercialization from universities to corporate products
- Provide technology pipeline
  - Fundamental understanding
  - High-quality students, technical skills

Structure/Scope

- Participating facilities include:
  - SEMATECH/ATDF
  - Microelectronics Research Center
  - Texas Materials Institute
  - Center for Nano & Molecular Science and Technology
- Focus on future transistors, interconnects, patterning, metrology; emerging nanotechnology applications

Accelerating the next technology revolution.

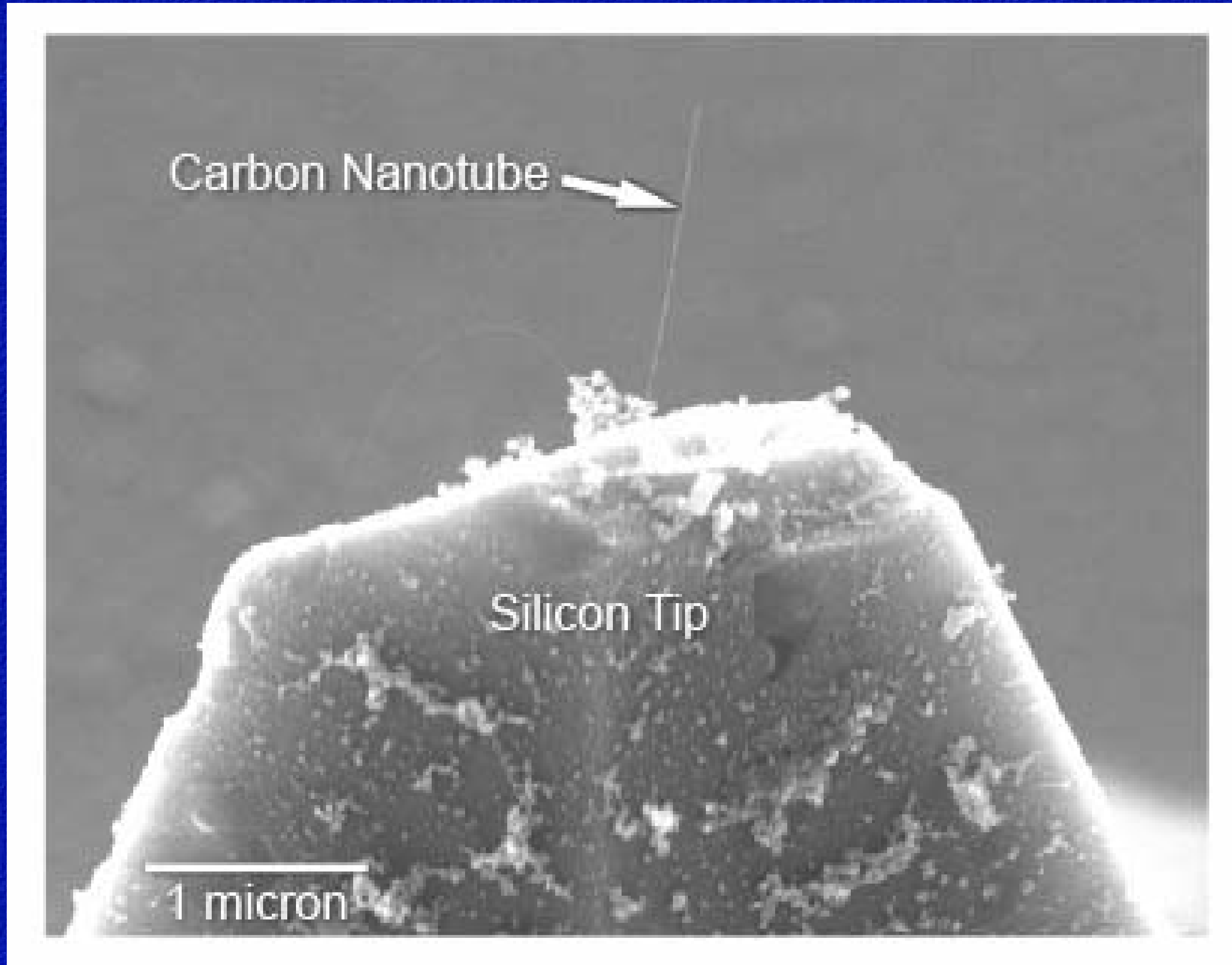
2004 AMRC University Programs

Topic		Details	UT Lead	Title
Materials and Structure for Future Transistors (FEP)	Advanced CMOS Materials & Processes	Gate Stack Materials	Lee	PVD High -K Dielectrics: Reliability Issues
			Kwong	Materials and Structures frng and Characterization of Key Issues Related to High-K Gate Dielectrics and Metal Gate Elecrodes
			Register	Modeling of Gate Stack Materials
		Channel Materials	Banerjee	Channel materials
		Ultra-Shallow Junctions	Hwang	Ultra Shallow Junctions
	Beyond CMOS Novel Transistors	New Transistors on Strained Silicon + SOI	Singh / Banerjee	Novel Transistors: Multi-gate SOI MOSFETS, FinFETs, and Vertical MOSFETS
			Register	Transport Models for Strained Si and FinFETs
		NanoTechnology	Dodabalapur	Advanced Organic/Silicon Devices for chemical and Biosensing
			Ekerdt	Quantum Dot Floating Gate Flash Memories
Marerials and Structure for Future Connectivity (Interconnect)	Advanced Cu & Low-K Interconnects	Barrier Materials / Low-k	Ekerdt / White	Ultra Thin Diffusion Barrier and Pore Sealing Techniques for 45 nm and Beyond
	Future Connectivity	Nano-Conductors / Low-k	Ho	Nanoconductors for Future Interconnects
		3-D Technology	Neikirk	Measurement, Electrical Characterization, and Design of Advanced Interconnects
		Optical Interconnect	R. Chen	Optical Interconnects
			Deppe	Optical Interconnects
		Optical Detectors for Interconnect	Campbell	Optical Interconnects
			Holmes	Optical Interconnects
Patterning of Materials and Structures (Litho)	Optical Extension	Immersions Lithography Studies	Willson / Bonnecaze / Shi	Immersion Lithography - Fluids and Resists
	Nanotechnology Patterning	Functional Resist	Willson / Ekerdt / Shi	Functional Resissts
		Common Resist for 193nm, eBeam, & Imprint Template	Willson / Ekerdt / Shi	Common Electron Beam Resists
		Field Assisted Lithography	Willson / Sreenivasan	Field Assisted Lithography
Metrology and Characterization of Materials and Structures (Metrology)	Future Transistors	Advanced CMOS	Downer	Spectroscopic Methods for Profiling High-K Dielectric Films and Nanometer-Scale SOI Structures
			Shih	Dopant Profiling with STM
			Yacaman	Transition Electron Microscopy Studies
		Beyond CMOS	Campion	Strain Measurement by Raman Spectroscopy
	Patterning	Patterning & Standards	Korgel	Nanowires and Nanodots for Metrology Standards
	Defects		De Lozzane	STM Studies for Metrology

AMRC Metrology Programs
Innovative approaches

- Spectroscopic Methods for Profiling High-K Dielectric Films and Nanometer-Scale SOI Structures
- Dopant Profiling with STM
- Transmission Electron Microscopy Studies
- Strain Measurement by Raman Spectroscopy
- Nanowires and Nanodots for Metrology Standards
- STM Studies for Metrology
  - Conductivity of nanowires

XIDEX Carbon Nanotube Tip for SPM
Accelerating commercialization



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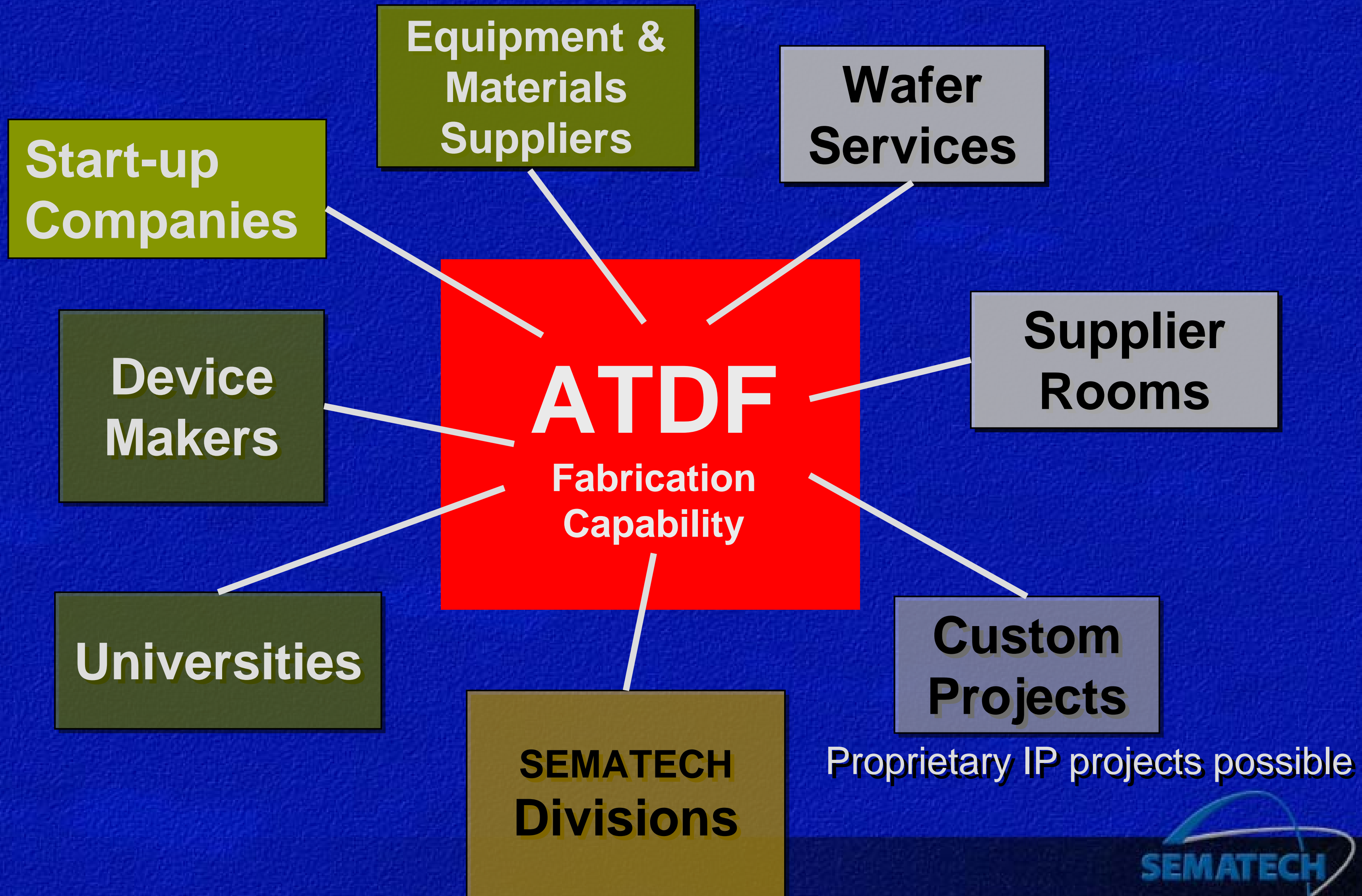
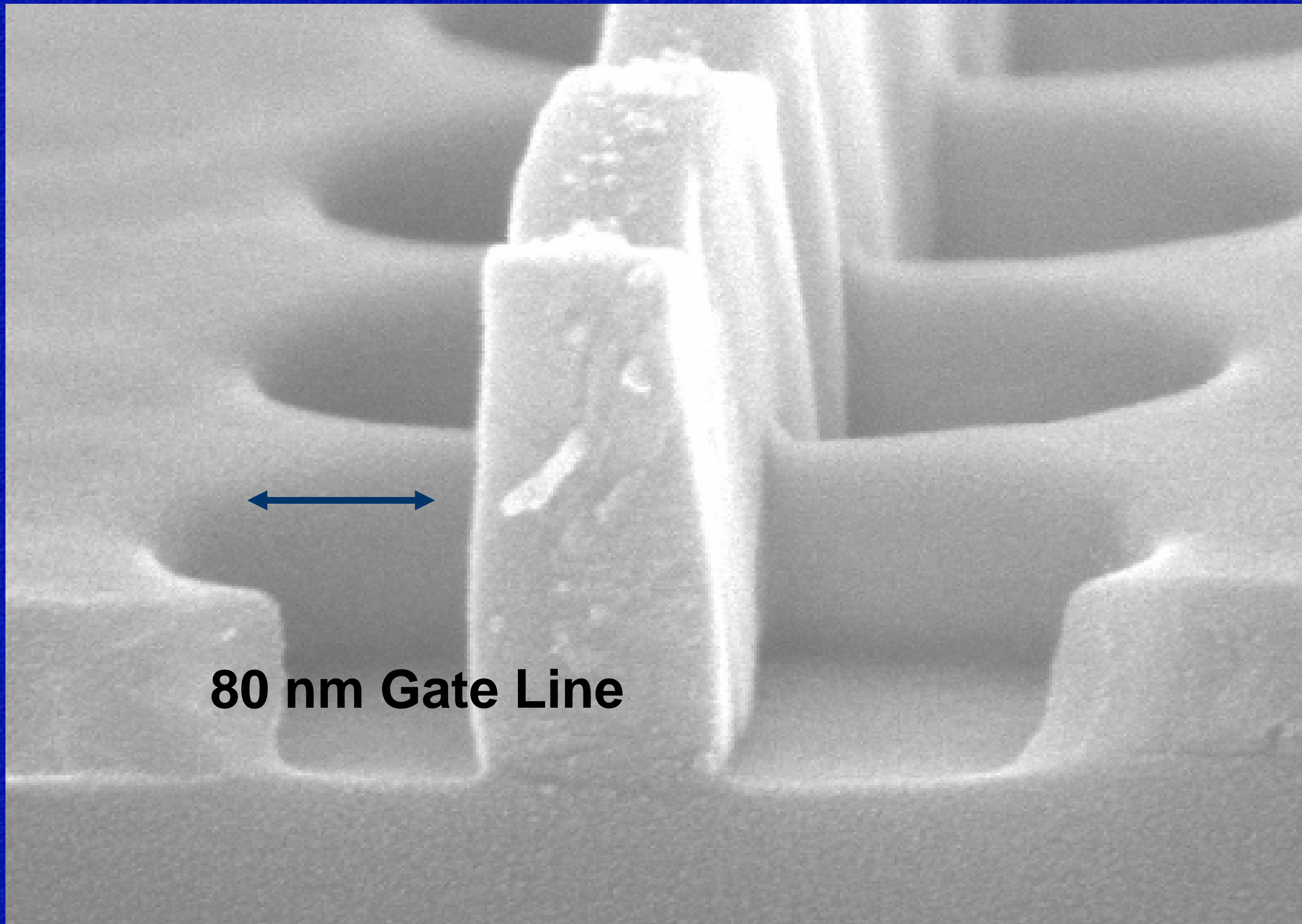
Advanced Technology Development Facility (ATDF): *R&D processing and prototyping*



Non-classical CMOS MuGFET



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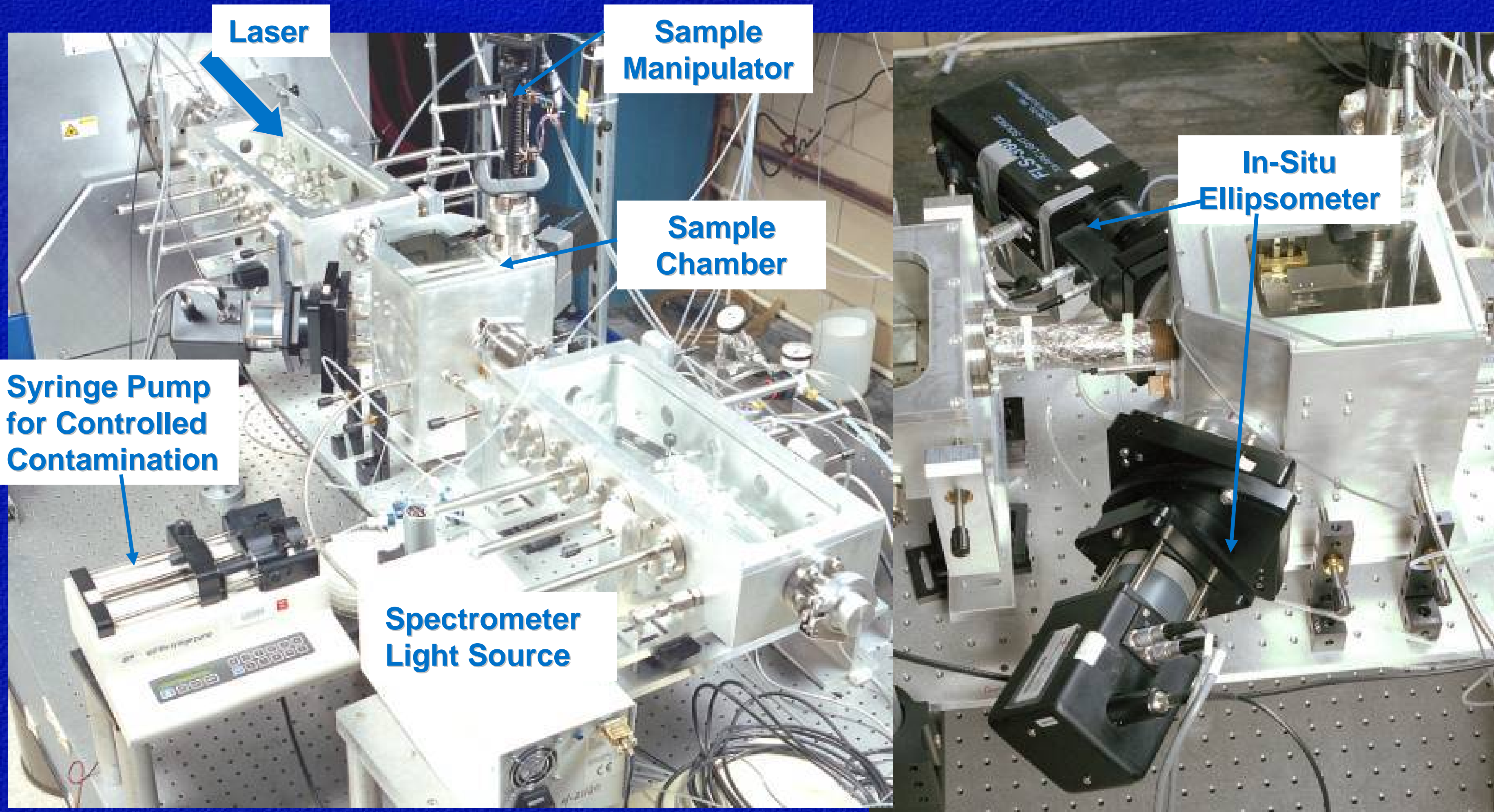
ASSURING MANUFACTURABILITY

Immersion Coatings Test Chamber



Immersion Technology Center (iTC)

Focus on high-NA applications, future extensibility

- Austin-based iTC will support the development of commercial immersion materials for high-NA applications to meet production requirements
  - Centerpiece is 1.3NA 193nm microstepper (Exitech/Tropel)
  - Design study, and option for manufacture and 2006 delivery of ~1.5NA lens
    - Fluid development required
  - Interference lithography tool to provide complementary platform for high-index fluid development
- Additional objective to understand extensibility of immersion lithography

Accelerating the next technology revolution.

SEMATECH EUV Program at Albany
Accelerate EUV infrastructure development

- 5-year strategic alliance
- EUV Mask Blank Development Center will speed the development of commercial EUV masks
- EUV Resist Test Center will support the development of commercial EUV photoresists to meet production requirements

EUV Mask Blank Development
Collaborative model

Commercial Mask Infrastructure

Products

Research Partners

Consortia

VNL

Universities

Contracts

IP, Data

ML Deposition

Defect Analysis

Metrology

Cleaning

Material Development

SEMATECH North EUV Mask Blank Development Center

Technology transfer

Researchers

Commercial Supplier Partners

Researchers

Data

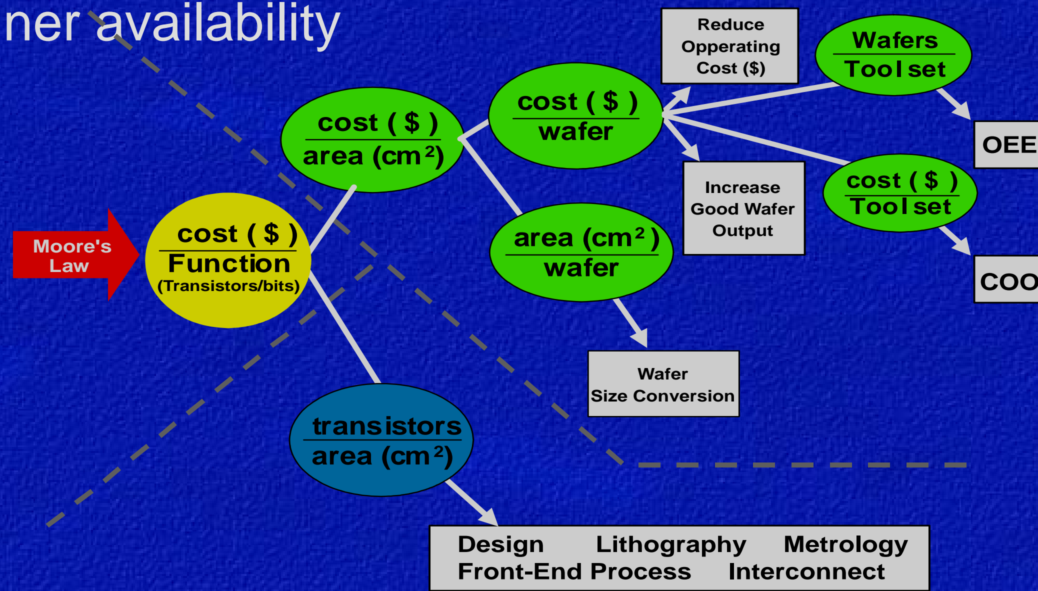
Products

SEMATECH Members

Manufacturing Initiative (ISMI)

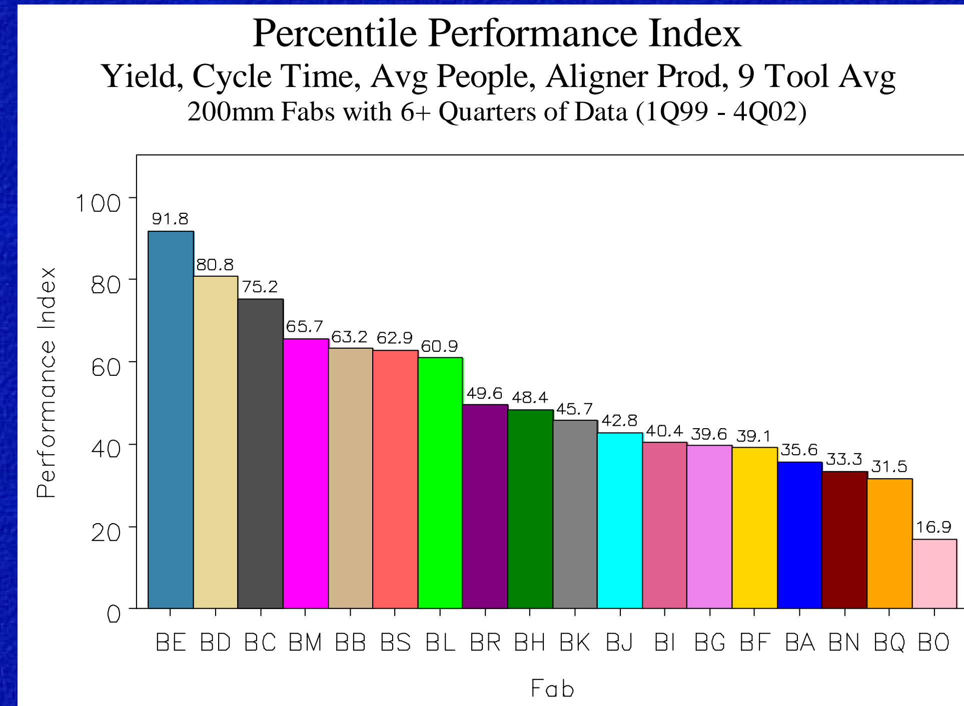
Improving manufacturing effectiveness and productivity

- Fab benchmarking – today's installed base
  Cost reductions
    Resist reduction $1.4M-1.6M/year savings
- Tool improvements (EPITs)
    ~8% improvement in scanner availability
- Factories of the future
  - e-Manufacturing
  - Next wafer size
- Yield enhancement
- Metrology
- ESH



Sharing Manufacturing Excellence
through councils and benchmarking

- Manufacturing Methods Councils
  - 20% productivity improvement in Members' wafer fabs over last two years
- Water optimization and reduction
  - Savings of over 42M gallons per year
- Energy reduction
  - Savings of over $3M per year



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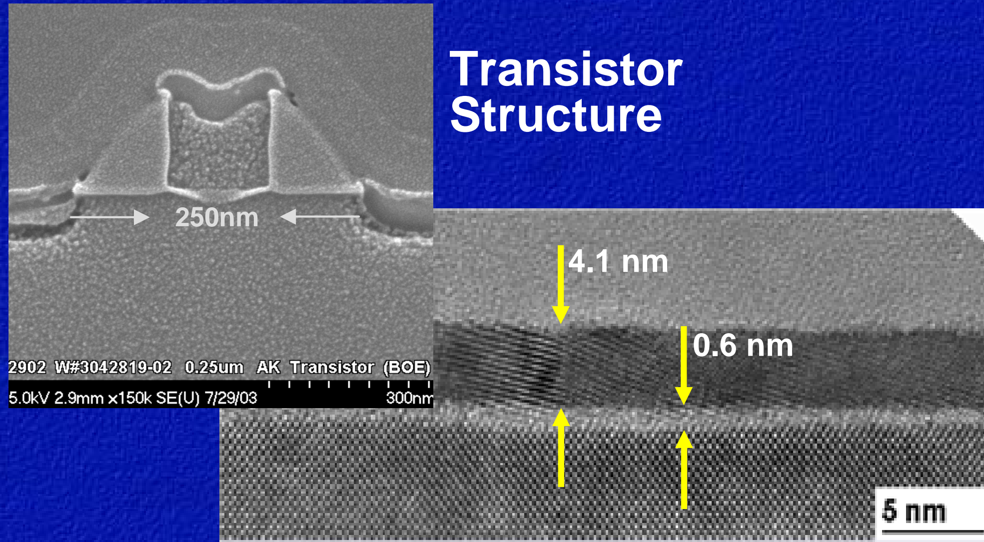
ISMI Strategic Directions
Improving productivity and yields

- Short cycle time
- "Monitor-free" manufacturing
- Plug & play equipment
- Continuous scaling
- Next wafer size transition
- Green fab
- Fully automated fab (hardware, software)
- People productivity
- Zero defects, 100% yield

Semiconductor is the Platform for Emerging Technologies



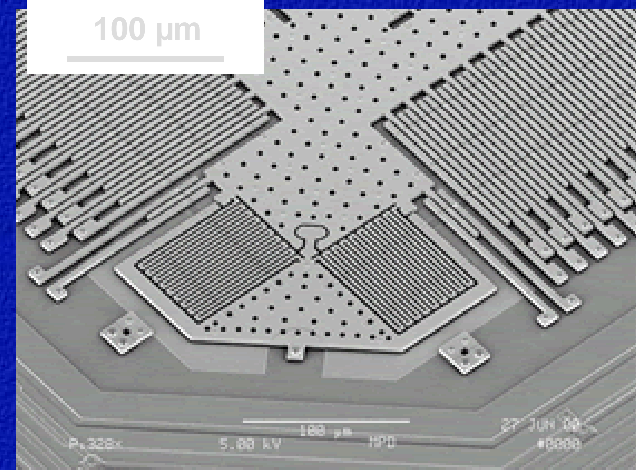
Transistor Structure

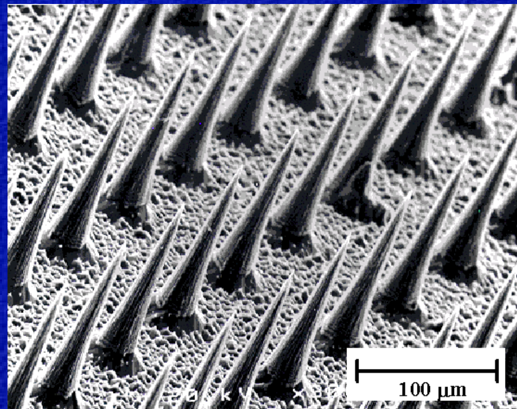
4.1 nm

0.6 nm

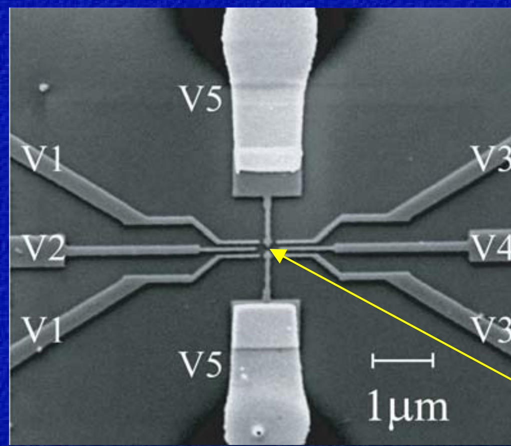
The dots are at the atomic level

MEMS
Airbag Sensor

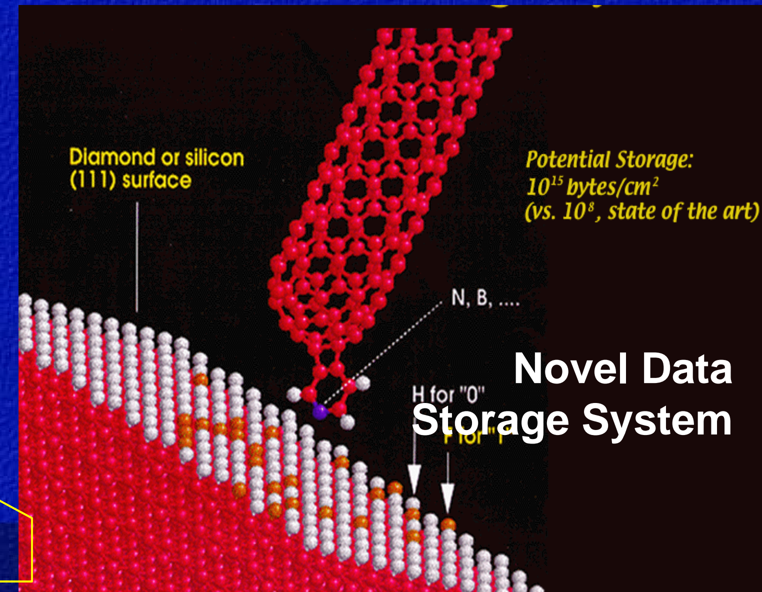




Micro-machined needles for "painless" injections



Quantum Dot Transistor



Novel Data Storage System

Collaboration is the Key at SEMATECH

- Global Collaboration
  - SEMATECH & Selete
    - 300mm, masks, resists
  - SEMATECH & SEMI
    - Industry Executive Forum
  - SEMATECH & IMEC
    - High-k, 157nm → 193i lithography, EUV
  - SEMATECH & Semiconductor Research Corporation
    - FEP Transition Center, FORCe, ERC
  - SEMATECH & Albany Nanotech
  - SEMATECH & the Texas Technology Initiative

Catalyst for Commercialization

Innovation → *Acceleration* → Manufacturability

University Research

Technology Development

Productivity

R&D Processing & Prototyping