Frontiers in Defect Detection

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Agenda

- Introduction
- Yield Enhancement & ITRS
- Metrology
- Latest Equipment Developments
  - Defect Inspection Tools
  - Gi-SAXS
  - Vacuum Ultra-Violet (VUV)
  - Makyoh Metrology Tool
  - Zero-Defect Resizing of Large Crystalline Silicon Wafers with TLS
  - 450 mm Developments
  - Virtual Metrology (VM)
- Summary and Outlook

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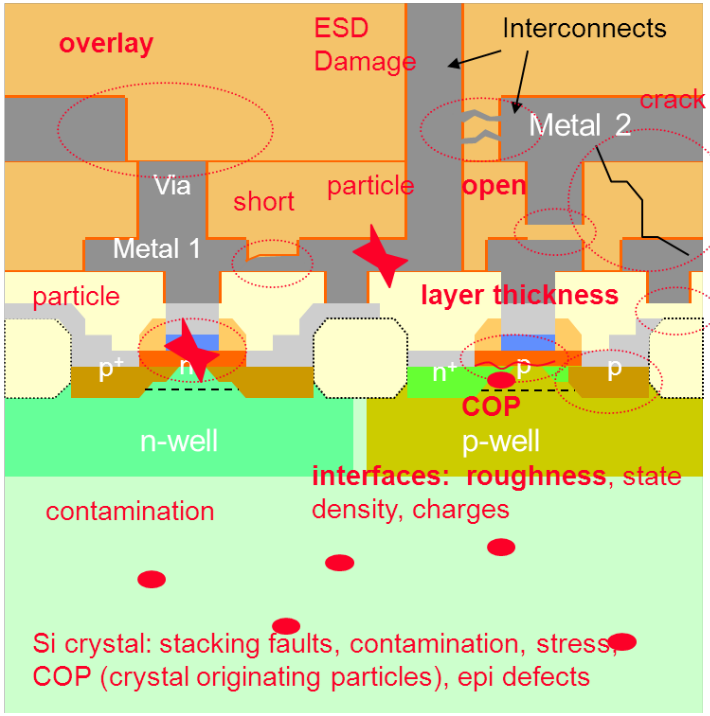
Introduction

Overall objective: to increase manufacturing yields

- Strong increase in processing complexity requires growing efforts in tackling of the challenges in defect detection and yield control
- Defect detection is more than “looking for particles”!
- All defects leading to lower yield must be identified and controlled.



Examples of yield distracting defects possible during microelectronics production processes (source: ITRS YE chapter)

Metrology is defined by the *International Bureau of Weights and Measures* (BIPM) as "the science of measurement, embracing both experimental and theoretical determinations at any level of uncertainty in any field of science and technology."[4] The *ontology* and international vocabulary of metrology (VIM) is maintained by the Joint Committee for Guides in Metrology (JCGM), a group made up of eight international organisations - BIPM, IEC, IFCC, ISO , IUPAC , IUPAP, OIML and ILAC.[5]

Metrology is a very broad field and may be divided into three basic activities subfields, though there is considerable overlap between the various fields:[6][7]

Definiting of internationally accepted unit of measurement.

Realisating these units of measurement in practice

Application of chains of tracability linking measurements made in practice to reference standards.

Metrology also has three basic subfields, all of which make use of the three basic activities, though in varying proportions:[6]

Scientific or fundemental metrology

Applied, technical or industrial metrology

Legal metrology

Agenda

Introduction

Yield Enhancement & ITRS

Metrology

Latest Equipment Developments

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Summary and Outlook

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Yield Enhancement & ITRS

- Defect detection is one major scope of activities.
- Focus of respective activities was changed and extended with time:

Defect detection for leading edge technologies

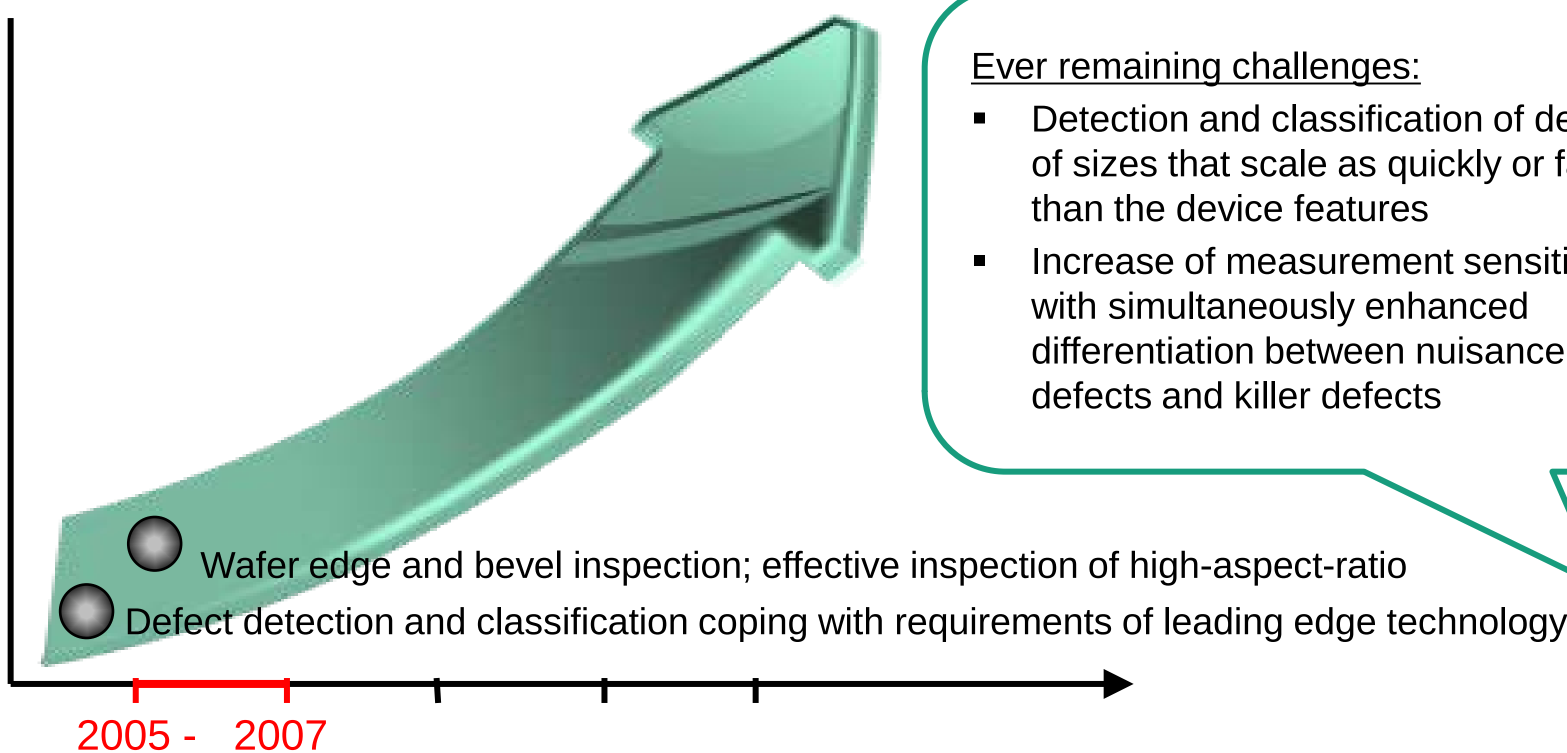
Defect detection for broad applications
("More Moore" (MM) and "More than Moore" (MtM) technologies, power electronics, mechatronics, MEMS applications, …)

- Ever remaining challenges for defect inspection:
  - Satisfaction of demands arising from shrinking of device dimensions and corresponding critical defect dimensions
  - Keeping in-line inspection costs low!

    → Need for high sensitivity, high throughput and low CoO tools.

Yield Enhancement & ITRS

Overview of focus change and extension of defect detection activities within ITRS Yield Enhancement with time

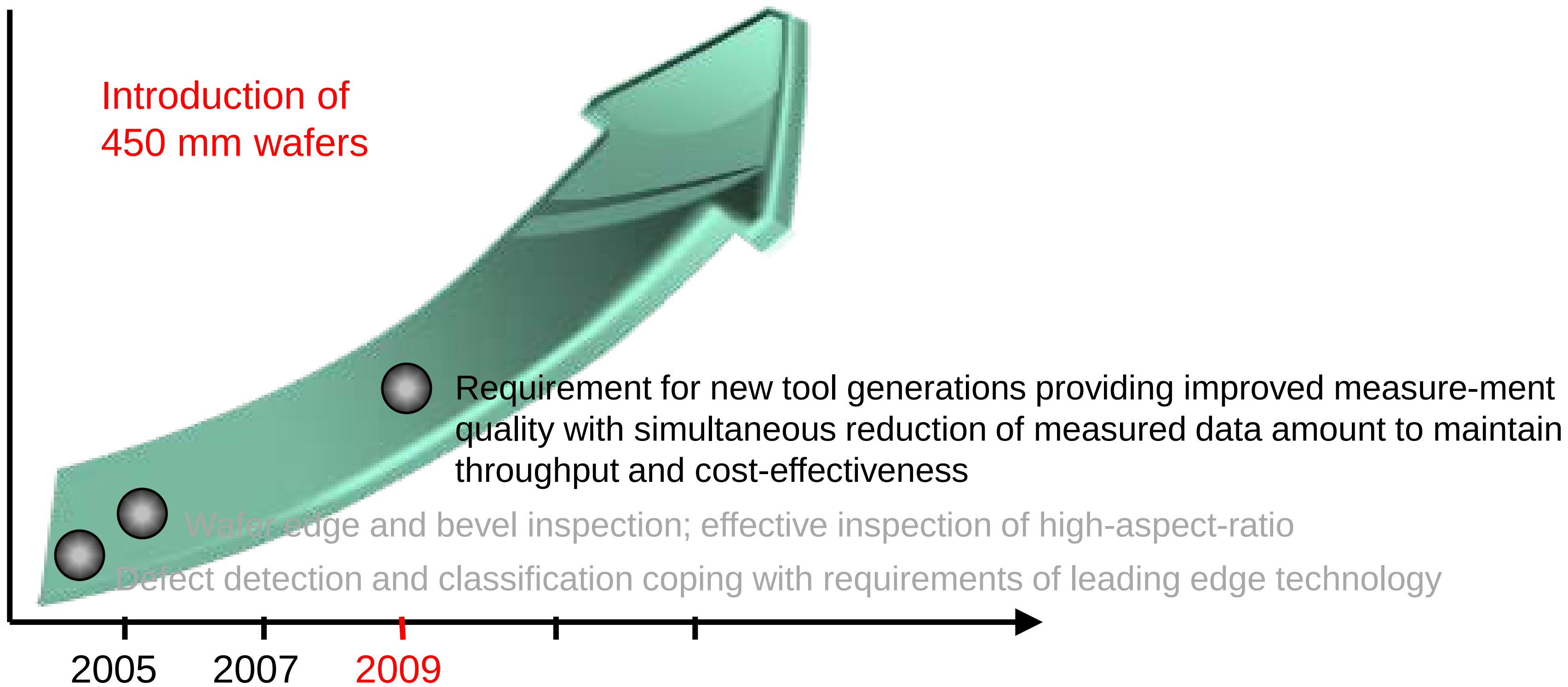


Ever remaining challenges:

- Detection and classification of defects of sizes that scale as quickly or faster than the device features
- Increase of measurement sensitivity with simultaneously enhanced differentiation between nuisance defects and killer defects

Yield Enhancement & ITRS

Overview of focus change and extension of defect detection activities within ITRS Yield Enhancement with time



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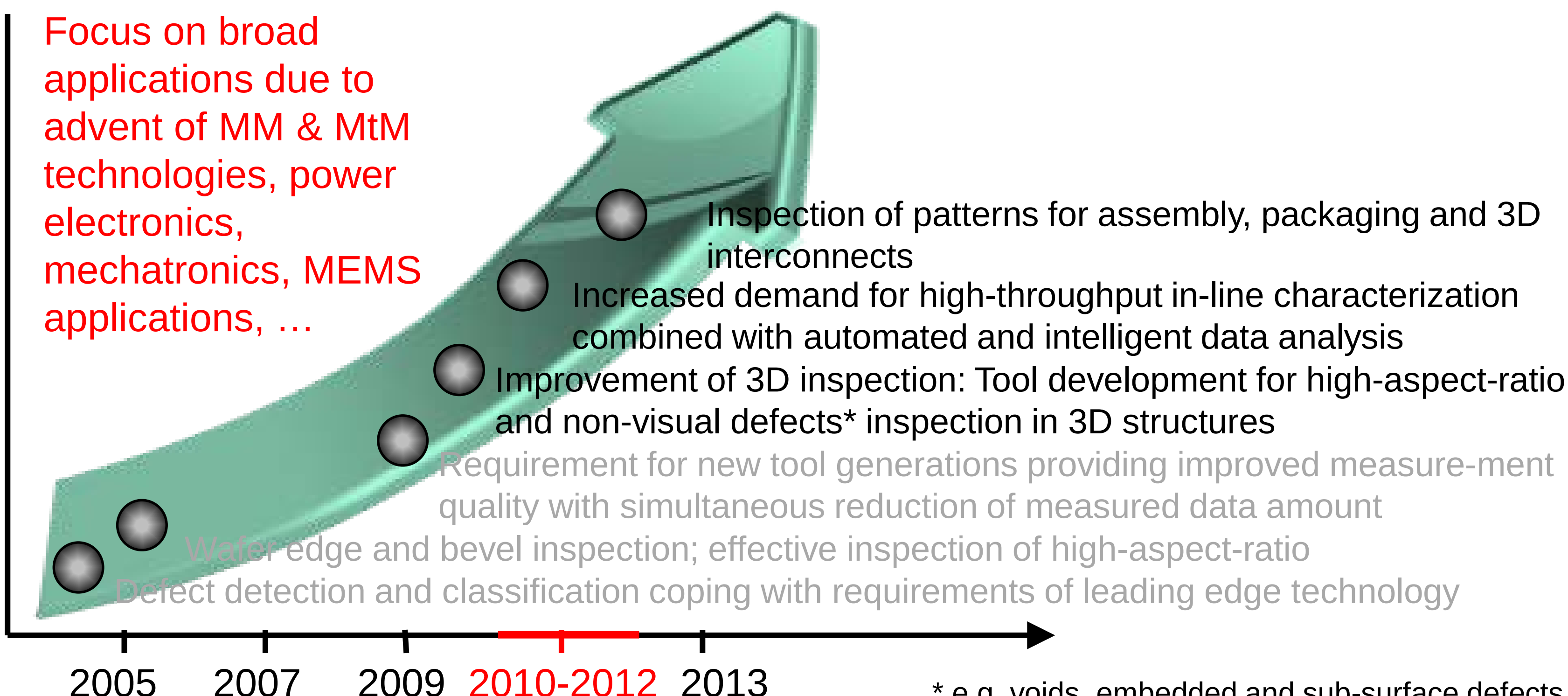
Yield Enhancement & ITRS

Overview of focus change and extension of defect detection activities within ITRS Yield Enhancement with time



* e.g. voids, embedded and sub-surface defects

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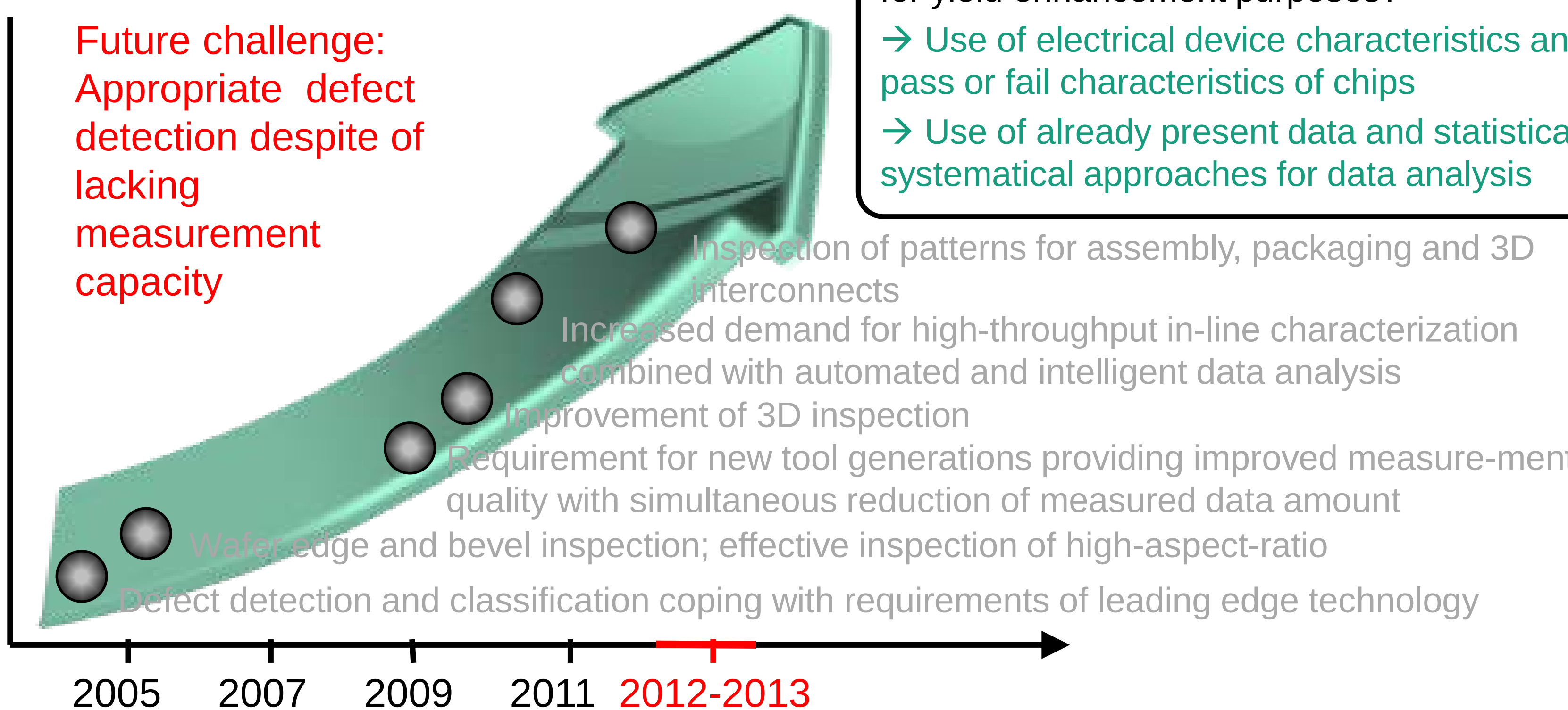
Yield Enhancement & ITRS

Overview of focus change and extension of defect detection activities within ITRS Yield Enhancement with time

How to supplement common defect detection for yield enhancement purposes?

→ Use of electrical device characteristics and pass or fail characteristics of chips

→ Use of already present data and statistical/ systematical approaches for data analysis



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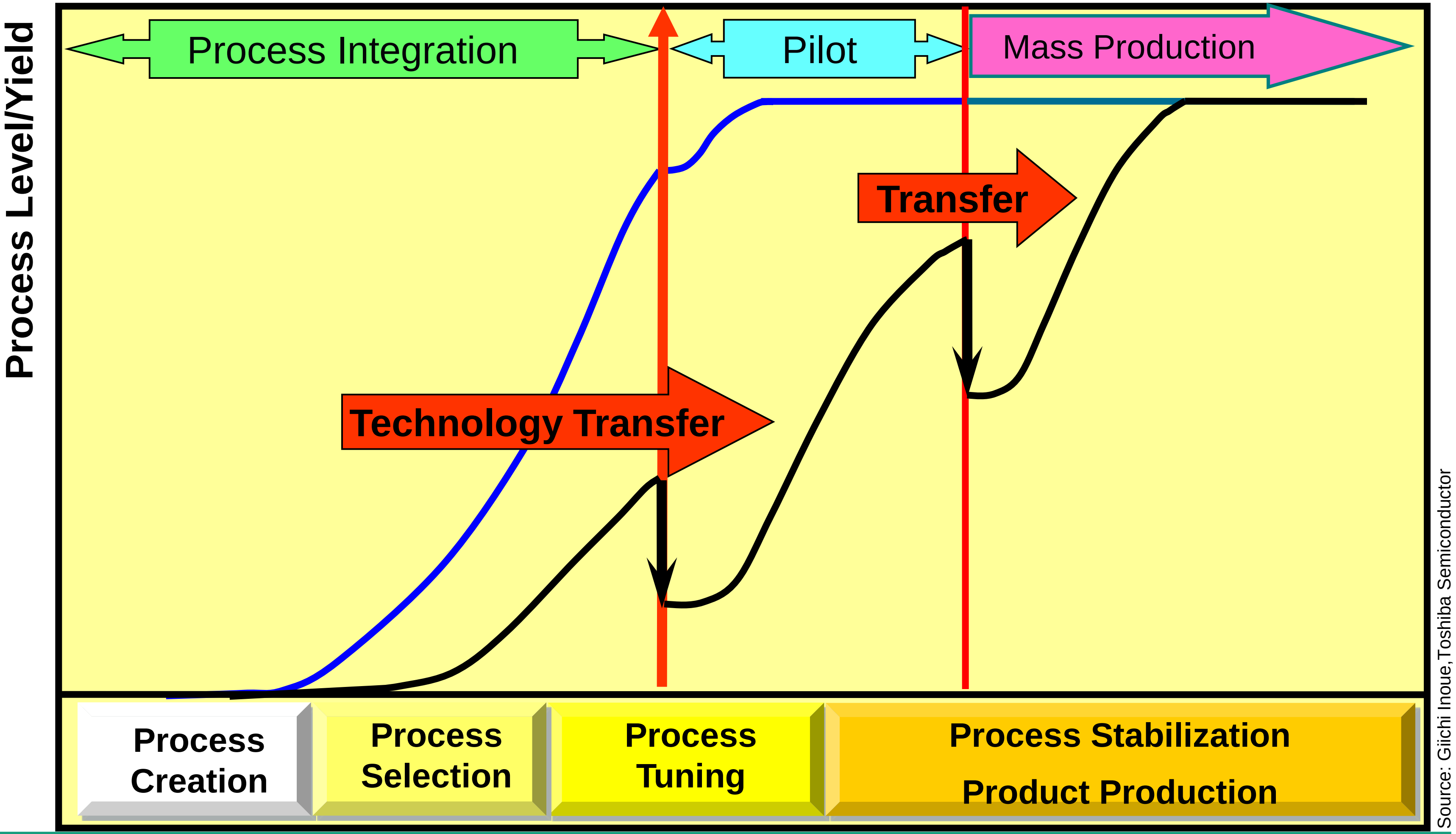
Metrology in Semiconductor Manufacturing

Production Ramp Curve



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Contributions by Fraunhofer IISB

Network in Metrology

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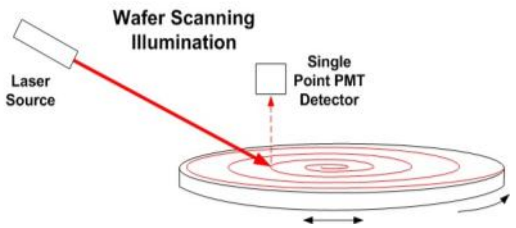
Latest Equipment Developments

Innovative Meso Defect Inspection (SEA-Project)

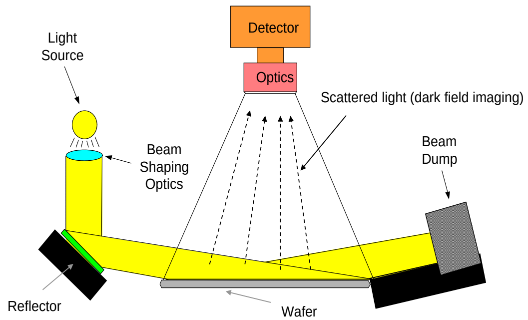
Short description:

- Implementation of new very high throughput and high sensitivity approach for wafer inspection
- Assessment for 3D-Integration (TSV), patterned and un-patterned wafer inspection

Todays Standard Technology:



New Inspection Approach:



Advances

- Combines bright field illumination, dark field illumination with **full wafer illumination without movement of the wafer**
- Bright or dark field images of the full 300mm wafer are captured in one shot at high sensitivity of 1-10µm
- Use of full-wafer imaging permits for a first time to **rapidly inspect** every processed wafer at 100% of the surface
- SW algorithms to extract the defects of interests reliably and to automatically identify defect signatures are being optimized during the project

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Latest Equipment Developments

Defect Inspection Tools

State of the Art in defect inspection:

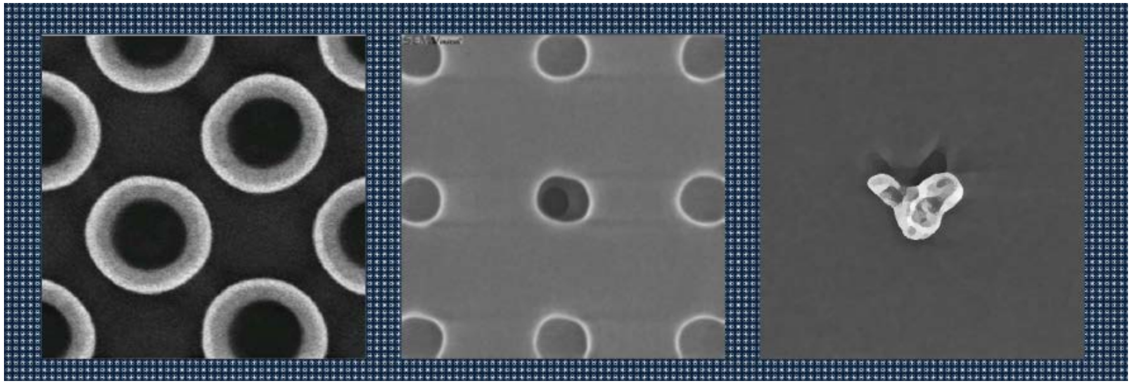
- SEM (pixel resolution < 3nm)
- Patterned and unpatterned wafers
- Root cause analysis:
  - Difficult due to variety of defect types
  - Material information required
- Slow SEM measurements
  - → throughput limited
  - → especially for upcoming 450 mm wafer processing

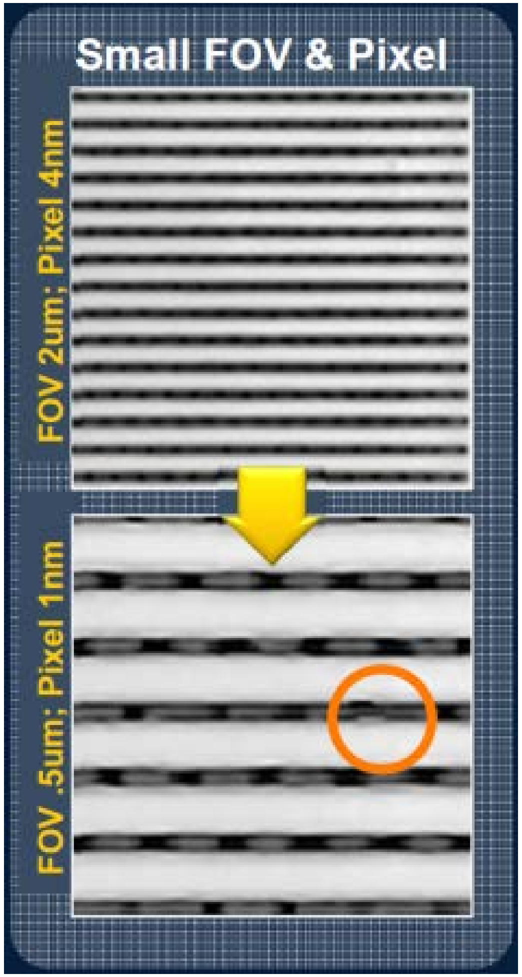
Source: Applied Materials

Latest Equipment Developments
Defect Inspection Tools

New developments in defect inspection:

- Increased pixel resolution (< 1nm) enables detection of smaller defects
- Integration of material analysis detectors (e.g. EDX, WDX) for improved defect review
- Utilization of multi-column e-beam SEM systems for improved throughput





Source: Applied Materials

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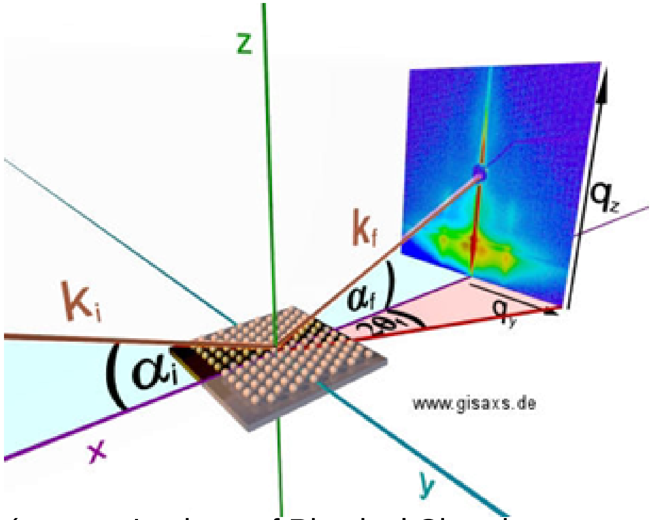
Latest Equipment Developments

Grazing-incidence small-angle x-ray scattering (GI-SAXS)

Inspection of surface structures in thin layers

- Novel functional layers increase demand for advanced layer characterization techniques (e.g. pore size distribution in low-k materials)
- GI-SAXS enables detection and characterization of surface structures in thin layers ➔ improved defect inspection capabilities
- Full layer characterization through combination with XRR/XRD techniques:
  - Film thickness
  - Film density
  - Crystallographic properties



(source: Institute of Physical Chemistry – University of Hamburg)

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Latest Equipment Developments

Vacuum Ultra-Violet (VUV)

Characterization of ultra thin layers at VUV wavelengths

- Key dielectric materials applied in semiconductor manufacturing have unique absorption properties at VUV wavelengths (120 nm to 200 nm)
- VUV measurement applications
  - Thickness measurement at ultra thin (<10 nm) layers, e.g. SiO_2/Si_3N_4 (ONO), HfO_2
  - Determination of material composition, e.g. SiON, high-k layers
  - Fast, non-destructive inline characterization

VUV reflectometer for 200 mm/300 mm wafers

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Latest Equipment Developments
Vacuum Ultra-Violet (VUV)

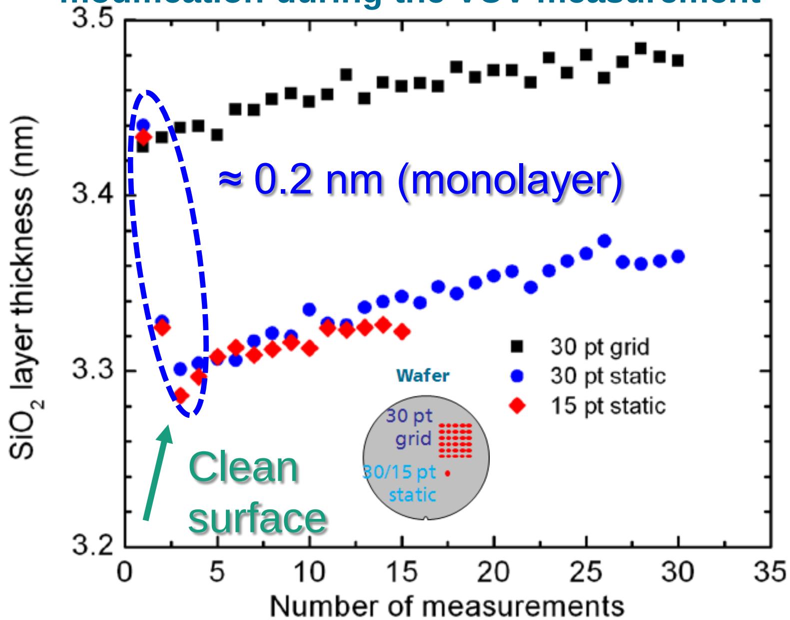
Investigation of *in situ* contamination layer removal by VUV/VIS exposure

- Efficiency and control of the contamination removal
- Influence of the VUV exposure on the measurement result

Results

- Repeated measurements clean monolayer from surface
- Selection of measurement point reflecting clean surface depends on type of material
- Layer modification visible as small increase of thickness (1 to 4 pm/pt); reduction by minimization of measurement time

Surface contamination removal and layer modification during the VUV measurement



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Latest Equipment Developments
Vacuum Ultra-Violet (VUV)

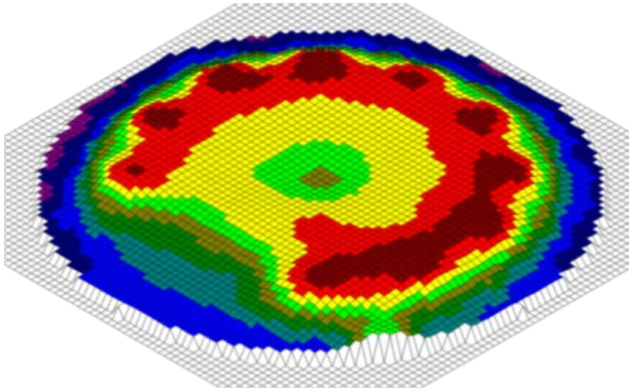
Application example – analysis of SiON thin films

- Analysis of the measurement point after contamination removal

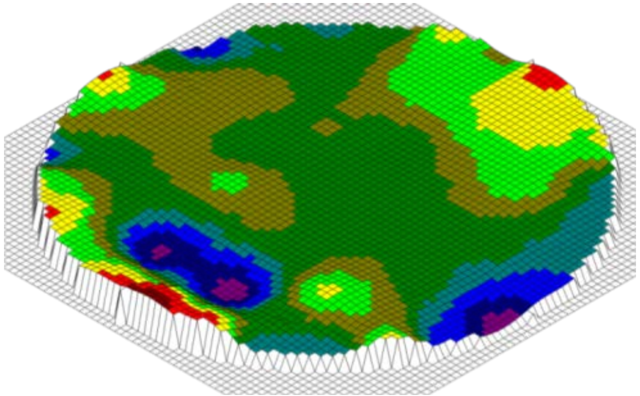
Method	N_2 concentration (%)	SiON layer thickness (nm)
VUV	9.9 ± 0.35	1.6 ± 0.01
XPS	9.4 ± 0.30	1.9 ± 0.02

- The results show a good correlation to the XPS measurement for nitrogen concentration
- The layer thickness measured by VUV is ≈ 0.3 nm thinner the XPS results which may indicate the present contamination layer measured within the XPS results

Nitrogen concentration map of a 2 nm SiON film with 9 % nitrogen



Film thickness map of a 2 nm SiON film with 9 % nitrogen



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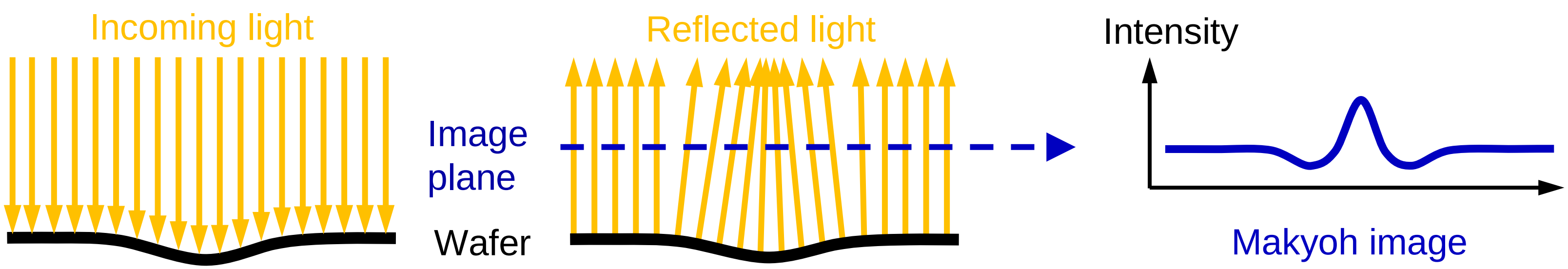
Latest Equipment Developments

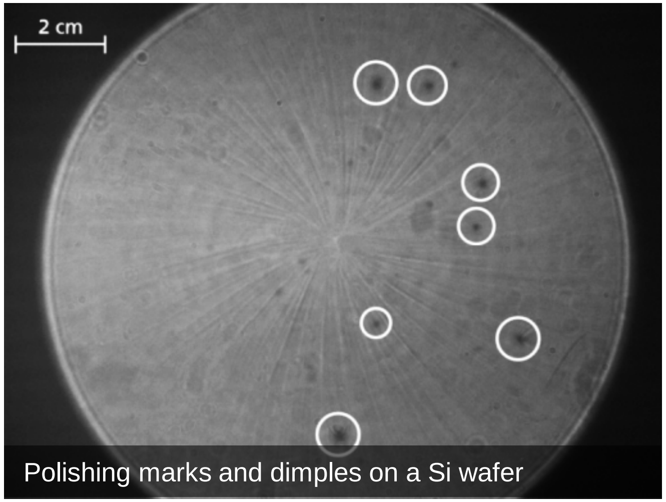
Makyoh Metrology Tool

Makyoh (magic-mirror) principle:



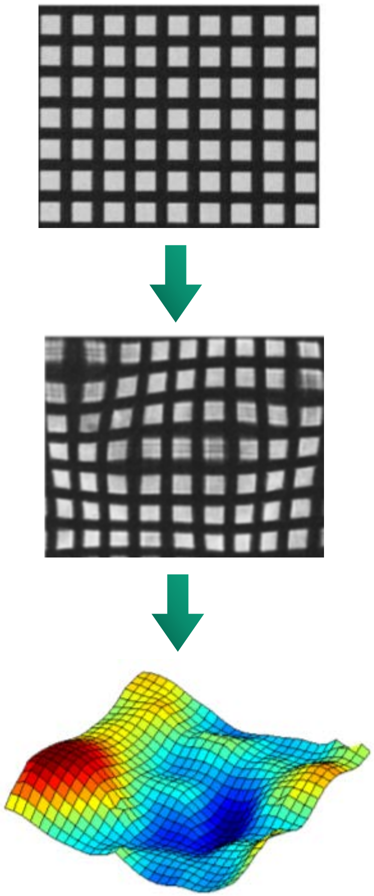
- The intensity distribution of initially collimated light that was reflected from the wafer surface carries (qualitative) information about the wafer topography

  → real-time defect detection



Polishing marks and dimples on a Si wafer

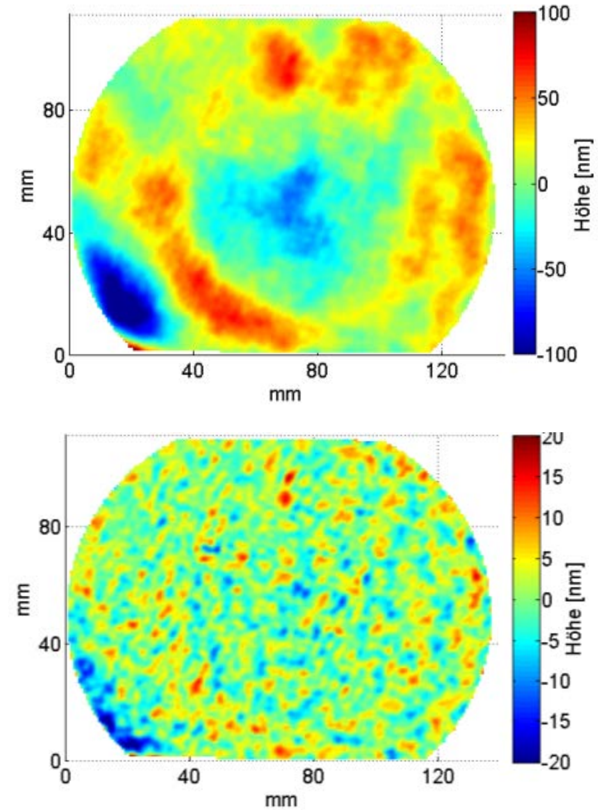
Latest Equipment Developments
Makyoh Metrology Tool



Quantitative Makyoh

Structured illumination is used to quantify the measurement

- Projection of patterns e.g. gratings (binary intensity coding) or continuous (color) patterns (multi-level intensity coding or multi-wavelength coding)
- Detect pattern distortion
- Calculate surface slopes
- Retrieve height topography by 2D-integration



Flatness (top) and Nanotopography (bottom) of a polished Si wafer

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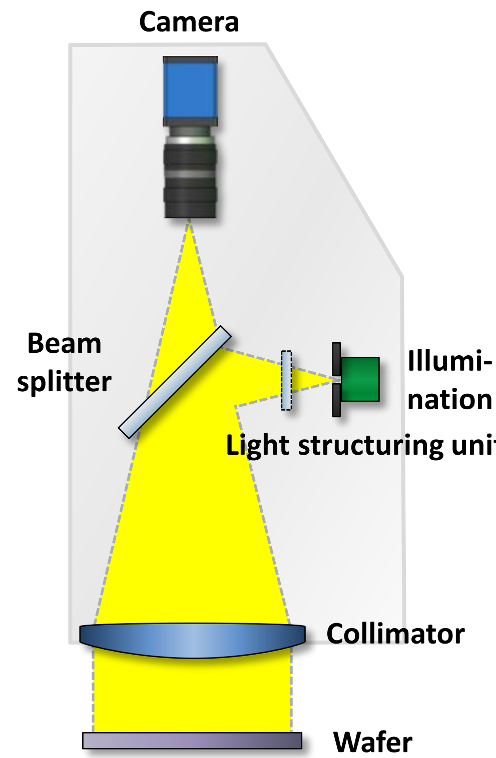
Latest Equipment Developments

Makyoh Metrology Tool

- Current specifications of prototype
  - Measuring area: ⌀ 135 mm (→R&D for ⌀ 300 mm)
  - Vertical resolution: < 20 nm
  - Lateral resolution: 100 µm
- Benefits
  - Large measuring area, no scanning
    → high throughput
  - Fast defect detection
  - Robust to external vibrations due to slope measurement

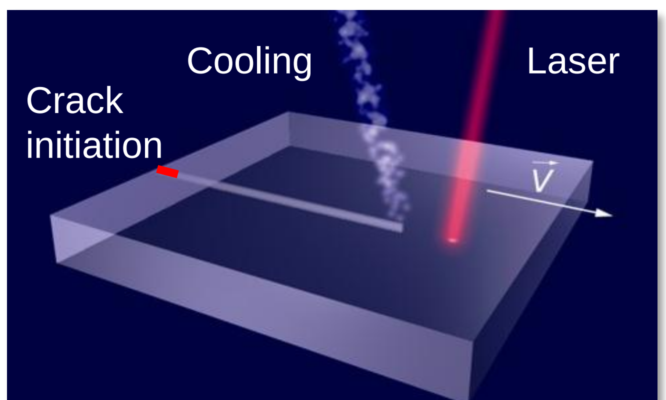


Schematic setup

Latest Equipment Developments
Zero-Defect Resizing of Large Crystalline Silicon Wafers with TLS

Thermal Laser Separation (TLS)

- Principle of TLS: Crack guiding with thermally induced mechanical stress
  - **1. Step – Crack initiation:** With diamond tip or ablation laser
    ➔ Predetermined cleaving point
  - **2. Step – Cleaving:** Laser-based heating, subsequent water cooling
    ➔ High tensile stress inside the overlap zone between heating and cooling results in a complete cleaving of the substrate



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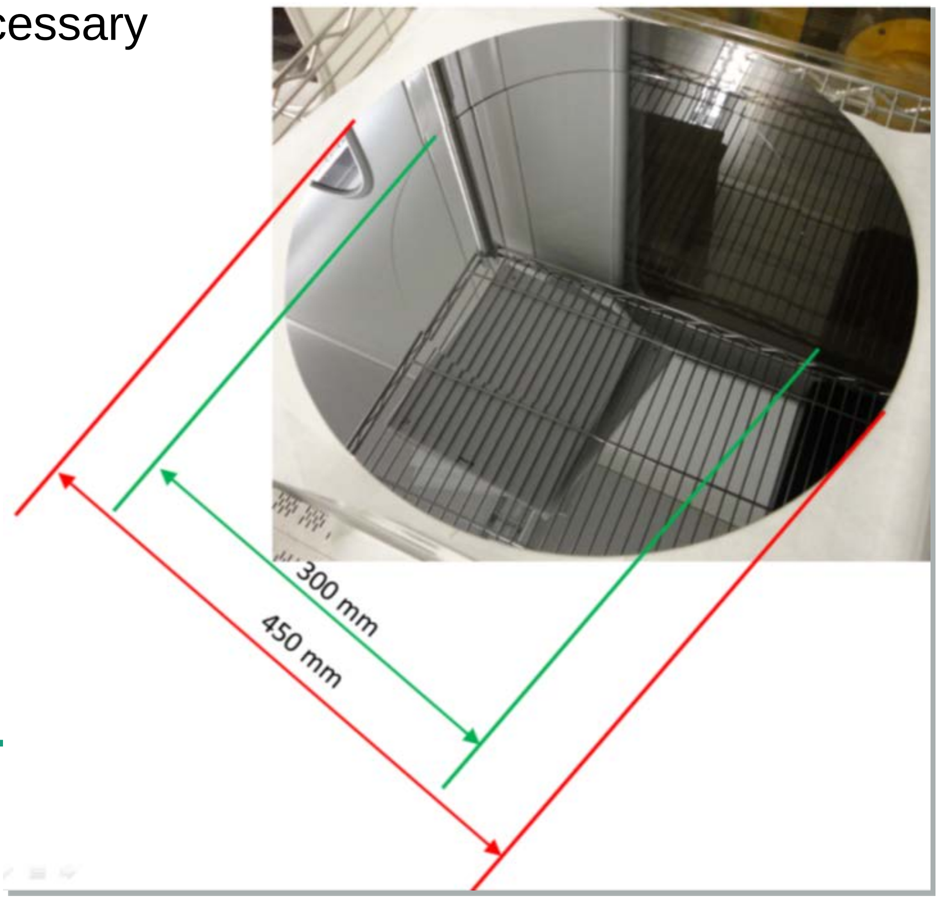
Latest Equipment Developments

Zero-Defect Resizing of Large Crystalline Silicon Wafers with TLS

TLS for resizing large crystalline Si wafers

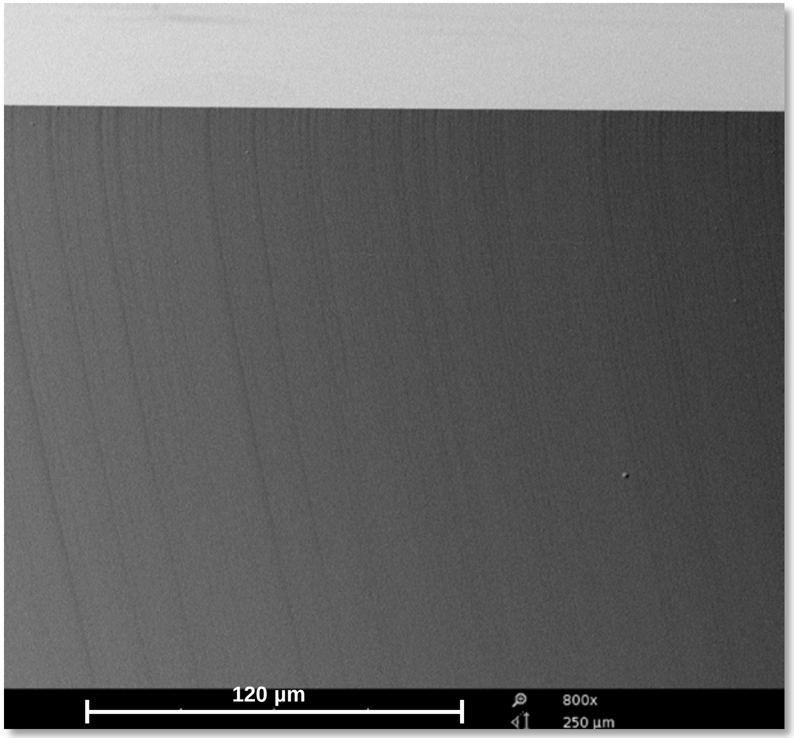
- Cleaving process is **not bound by lattice planes**
- Mounting on tape and frame is not necessary
- Single crystalline (100) Si wafers
- 200 W cw fiber coupled **fiber laser**
- **NIR** wavelength
- 7-9 ml/min water flow rate for cooling



Latest Equipment Developments
Zero-Defect Resizing of Large Crystalline Silicon Wafers with TLS

Results of resizing large Si wafers with TLS

- **High edge quality**
  - Zero chipping
  - Smooth side walls
  - No residual mechanical stress
  - ➔ High bending strength
- **Short process time**
  - Feed rate 20-40mm/s
  - 3-5min/wafer (300mm → 200mm)
  - ➔ High throughput
- **TLS** is a promising technique for **zero-defect resizing**



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450 mm Activities – Equipment as well as Metrology Equipment

- Requirements for 450 mm and possible benefits for smaller diameters include:
  - Improved equipment performance
  - Lower defect generation
  - Significantly better control
  - Advanced sensors
  - Faster handling and processing
  - Higher equipment reliability
  - Significantly better data processing

Impact of 450 mm Wafer Diameter on Equipment and Metrology Tools

Diameter	300 mm	450 mm
Thickness	775 µm	925 µm
Area	706 cm²	1589 cm²

Impacted Areas	Focus Items
Processes	Process uniformity, contamination, thermal effects/ uniformity, (cleaning, polishing, deposition, etch, anneal, ..)
Lithography	Increase of area by 2.25 times requires high performance – high speed litho
Handling	Deformation (→stress), transport issues, wafer translation (large distances, acceleration and settling times increase, vertical drift along the wafer)
Metrology	**Stages and handling, mapping capabilities, increase of area by 2.25 times requires high performance – high speed metrology (inspection), dimensional change due to thermal expansion coefficient, …**
Data Management	Amount of data, data quality, …

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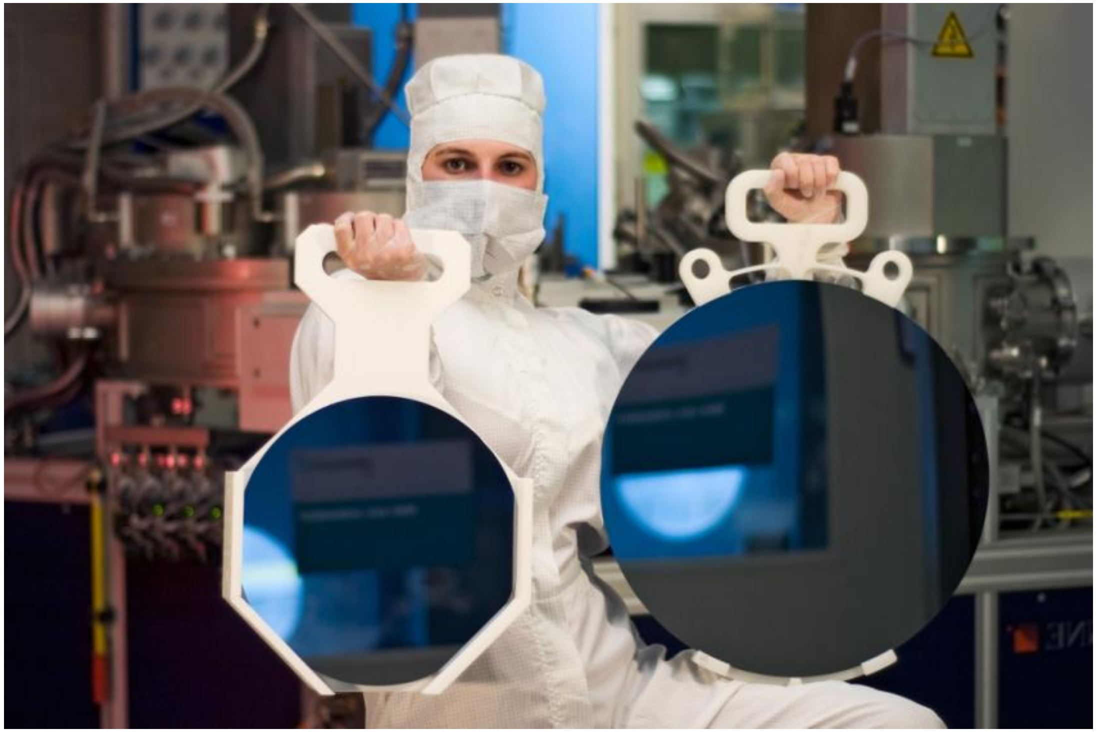
450 mm Activities - Material

- Wafer Manufacturing
- Important Wafer Parameters
- Required Metrology



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IMPORTANT WAFER PARAMETERS/CHARACTERISTICS

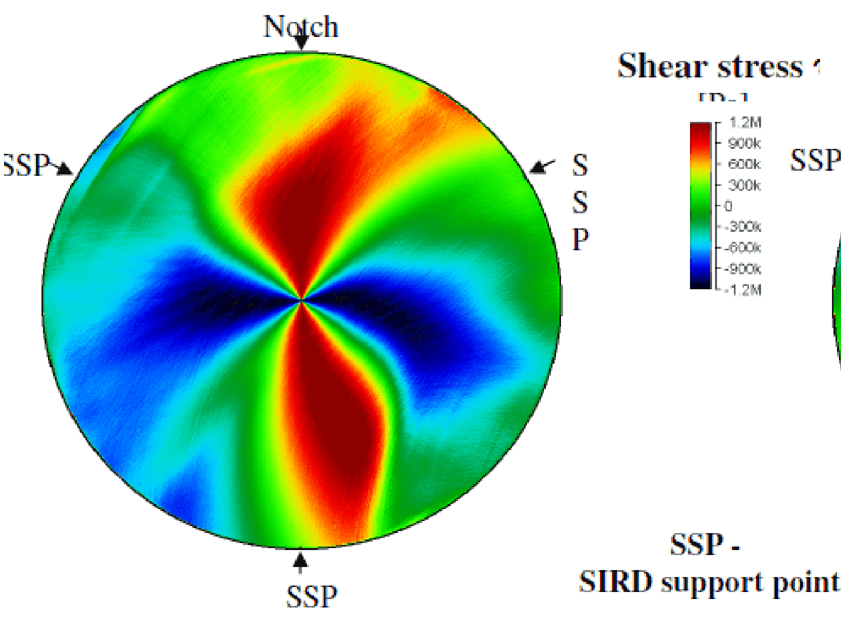
- Specified wafer parameters are:
  - Resistivity
  - Oxygen concentration
  - Bulk defects (dislocations, COP, swirl,…)
  - Surface defects (LLS, particles, PID,…)
  - Metal contamination (bulk, surface)
  - Local flatness
  - Global Flatness, Nanotopography
  - Edge profile
  - Roughness
  - Backside conditions

All parameters have to be verified by adequate metrology!

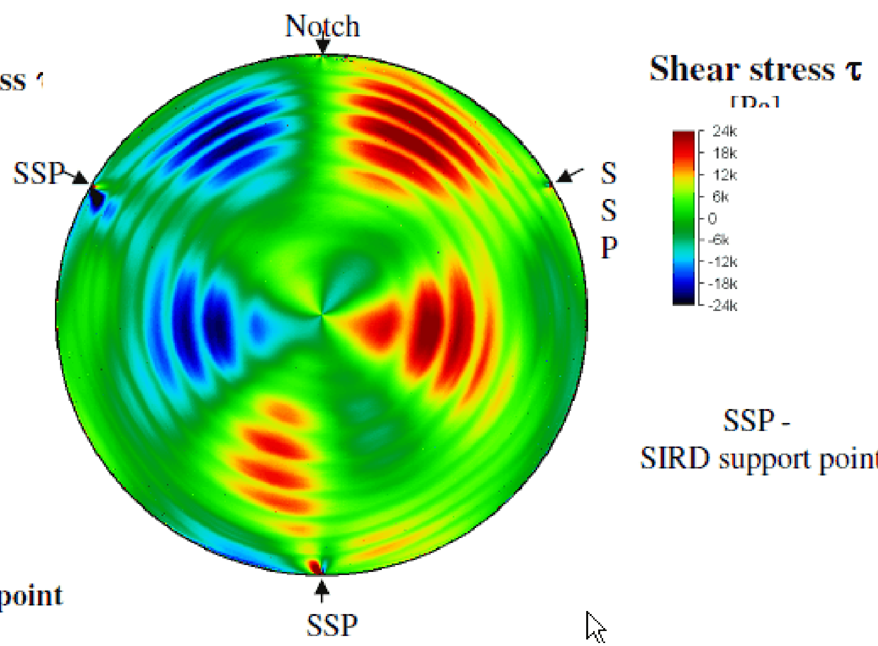
Courtesy of Siltronic

Example: Bulk wafer metrology

Grinded wafer



Polished wafer



Stress measurements

SIRD: Scanning Infra Red Depolarization

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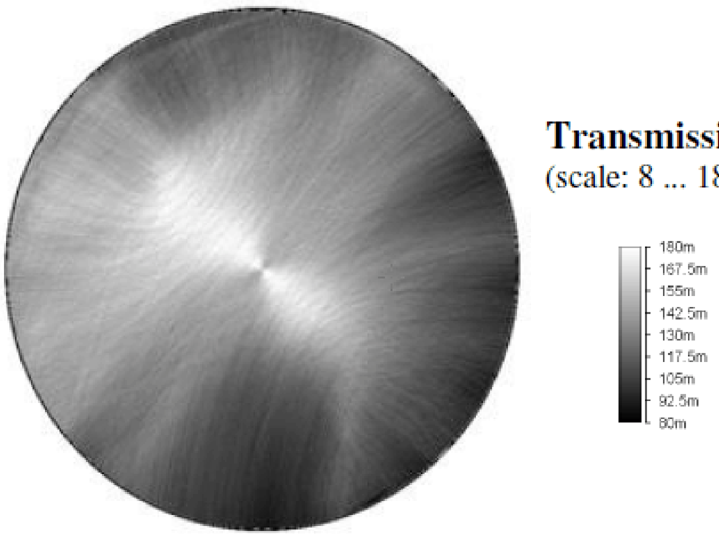
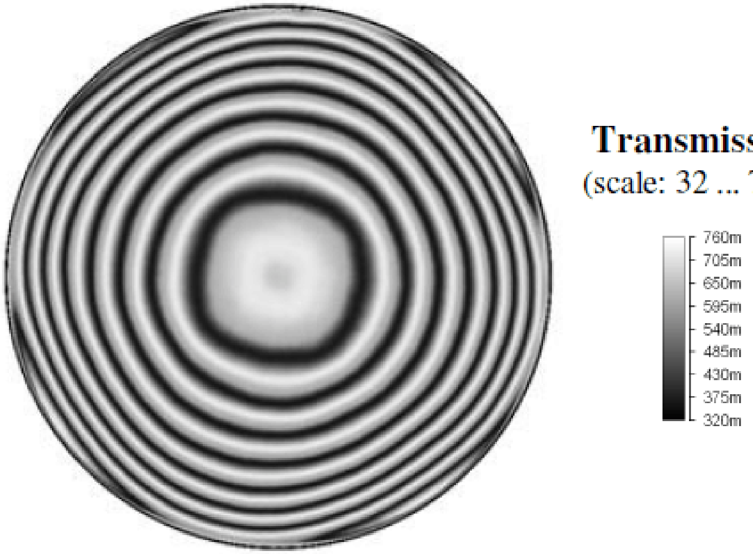
Example: Bulk wafer metrology

Grinded wafer



Transmission
(scale: 8 ... 18%)

Polished wafer



Transmission
(scale: 32 ... 76%)

Interferometer Measurement:

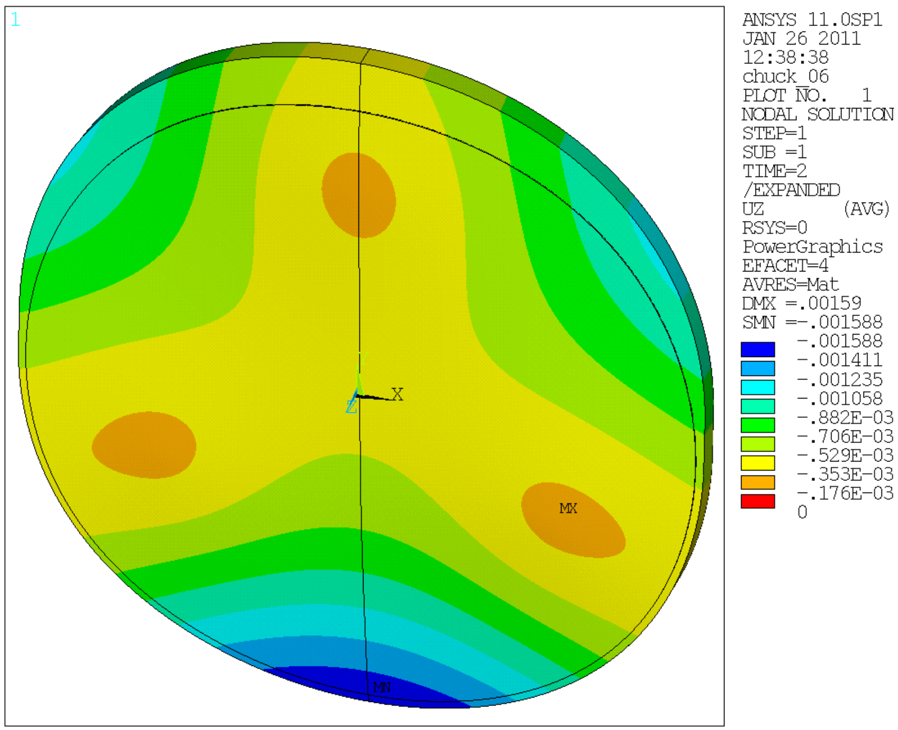
Total Thickness Variation: 1.4 µm

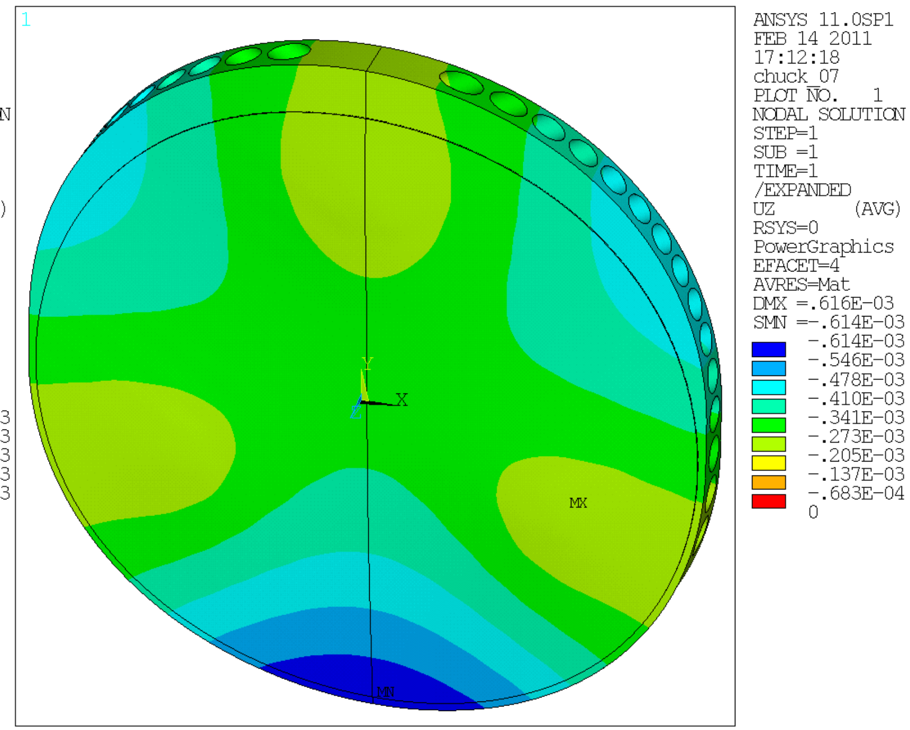
ULE: Two chuck design options

support at 3 points (Bessel's radius)

Massive chuck: 19 mm max. thickness (by mass constraint)

Light-weight chuck: 32 mm max. thickness
bore holes unsymmetric (below centerplane)





massive: OPD=1250 nm light-weight: OPD=397 nm

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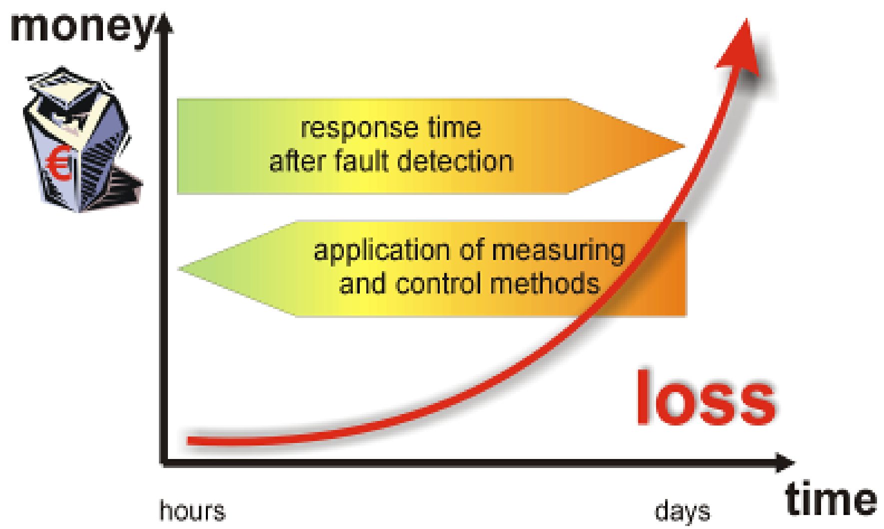
Metrolgy as Basis for Advanced Process Control (APC)

Objective:

Draw metrology nearer towards the process,

to reduce the time between process, measurement and corrective actions



Offline Metrology	Metrology tool apart from process tool	Long time between process and measurement
Inline Metrology	Metrology tool attached to process tool	Measurement immediately before/after processing
In situ Metrology	Metrology tool integrated in process chamber	Measurement during processing
Virtual Metrology	Wafer parameters derived from tool parameters (process state, additional sensors) by using physical models or from upstream metrology	"Measurement" during processing

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Latest Developments in Manufacturing Science

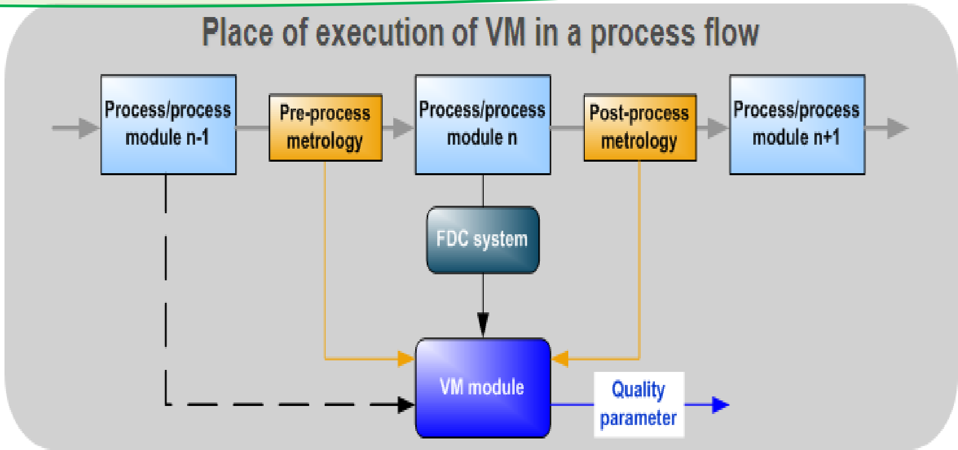
Virtual Metrology (VM)

VM definition

- Technology of prediction of post process metrology variables (either measurable or non-measurable) using process and wafer state information that could include upstream metrology and/or sensor data.

VM benefits

- Support or replacement of stand-alone and in-line metrology operations
- Support of FDC, run-to-run control, and PdM
- Improved equipment control for VM running on equipment level
- Improved understanding of unit processes



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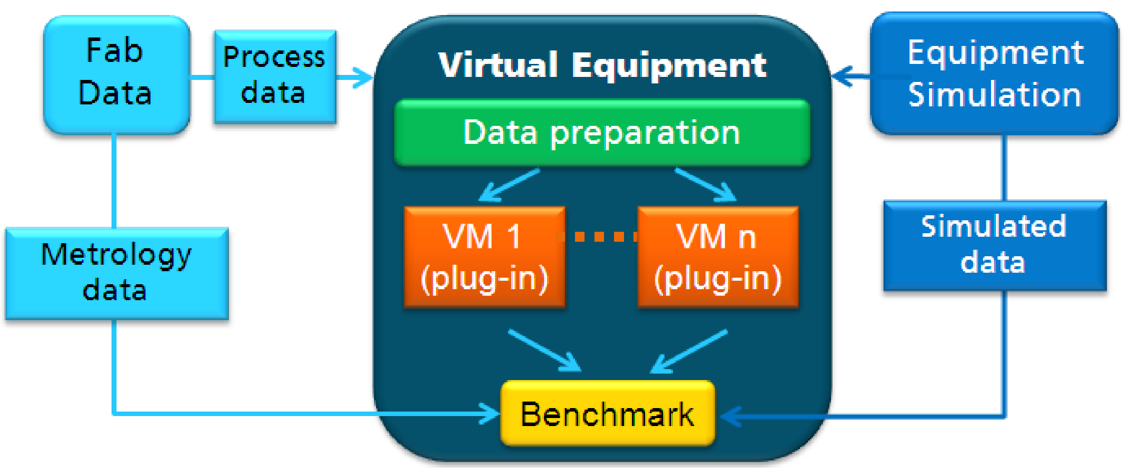
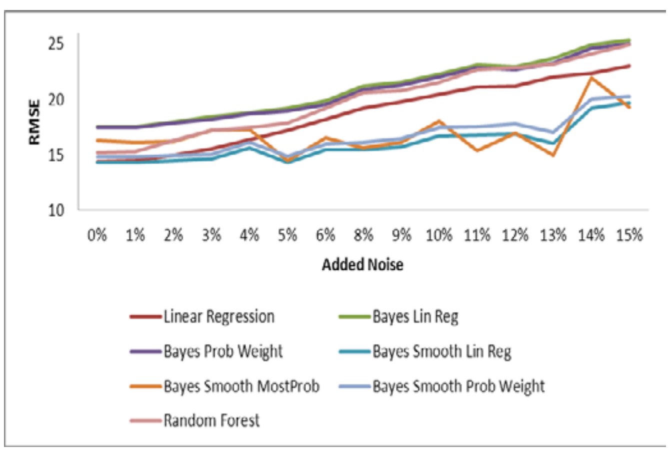
Latest Developments in Manufacturing Science
Virtual Metrology (VM)

Virtual Equipment test bench for development and test of VM models

- Utilization of history fab data
- Simulation of relevant equipment and process behaviour
- Application of noise, typical faults, and process drifts



Comparison of prediction error for different VM models

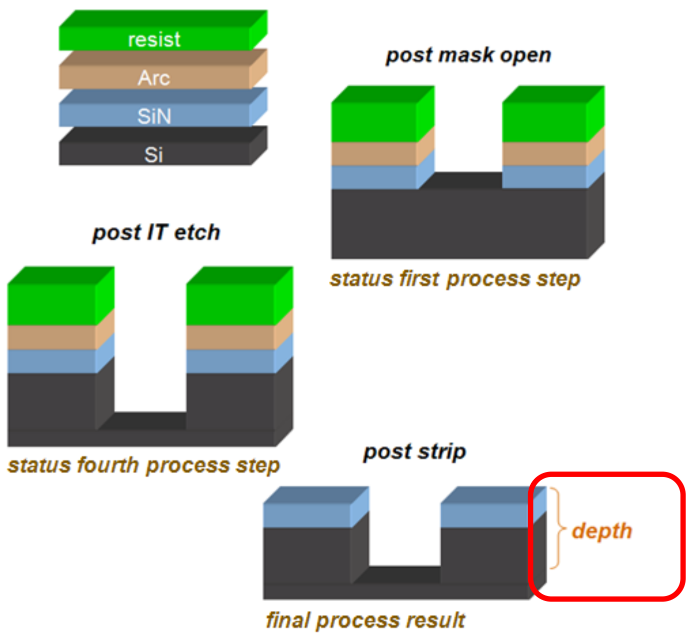


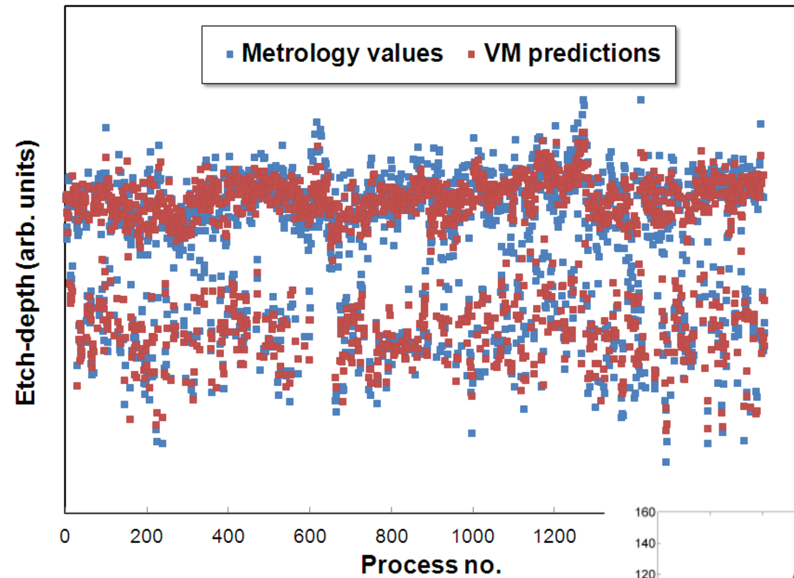
Latest Developments in Manufacturing Science

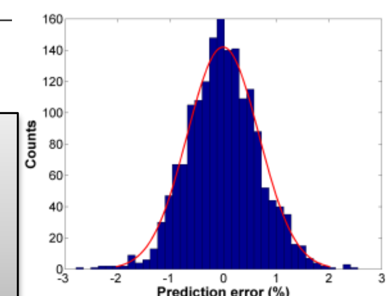
Virtual Metrology (VM)

Prediction of etch-depth in a trench etch process

- Objective: Establish wafer-fine run-to-run control in deposition, etch, CMP module







- Precise predictions of etch-depth in a trench etch process by VM
- Consideration of multiple products, etch chambers and recipes

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*)Source: ISMI

*)Source: ISMI

Summary and Outlook

- Metrology is a non-productive step: ideally ZERO metrology
- BUT reality:
  - Increasing number of non-product wafers during
    - Process development
    - Pilot production
    - Transfer into high-volume manufacturing
  - New developments needed
  - Advanced strategies needed
  - Advances required by
    - Technology nodes
    - Wafer diameters
    - Quality improvements

Acknowledgment

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