Advanced Metrology for Understanding Charge Transport Phenomena in Charge Trap Flash Memory

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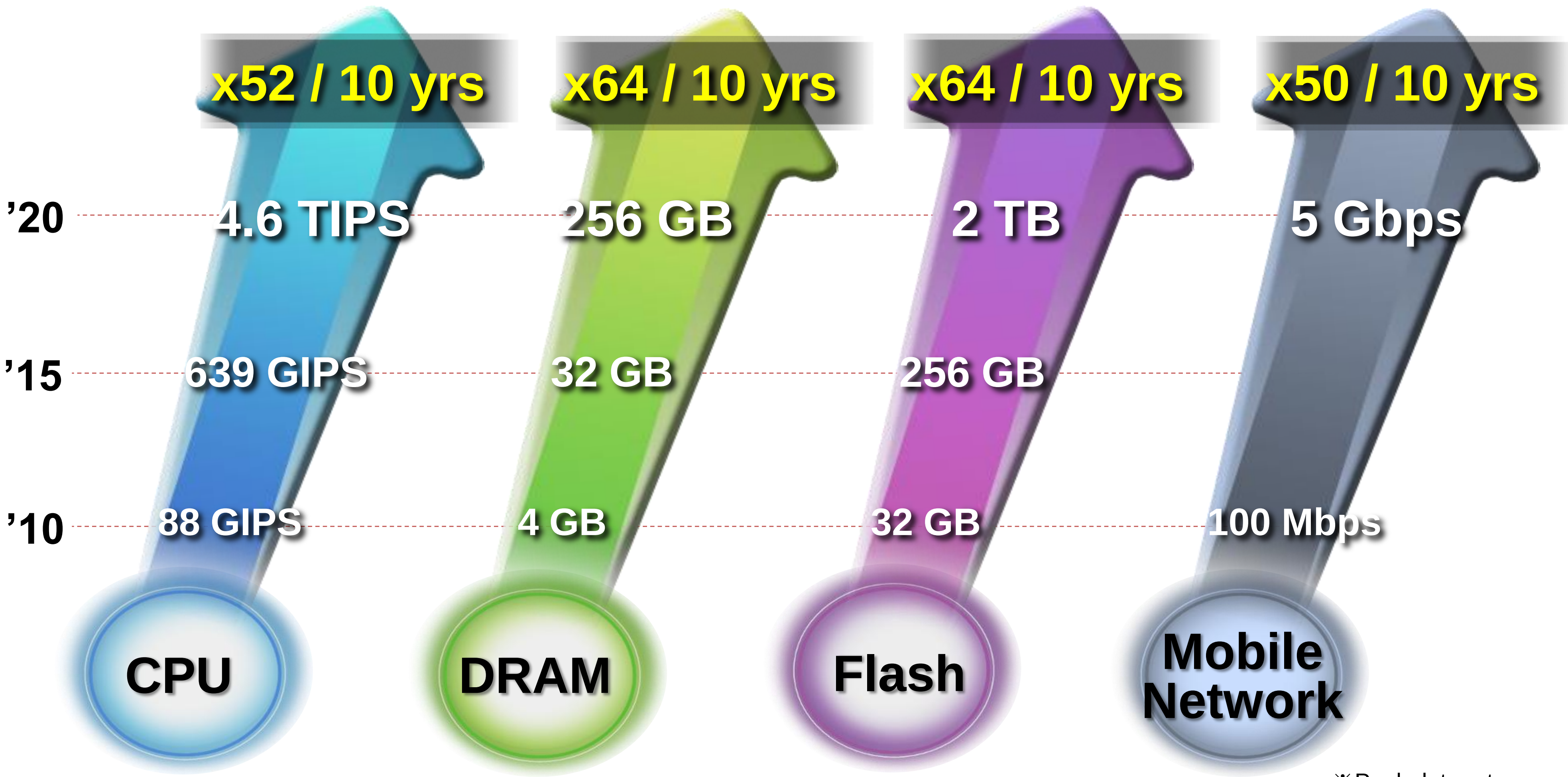
Outline

- Si technology trend & issues for semiconductor analysis
- Nanometrology for understanding charge transport phenomena of CTF memory
  - Analysis of charge trap distribution & charge injection
  - Measurements of band structure & defect states
  - Analysis of charge loss
- New metrology for the study of charge transport phenomena
  - *In-situ* probing inside TEM
- Conclusion

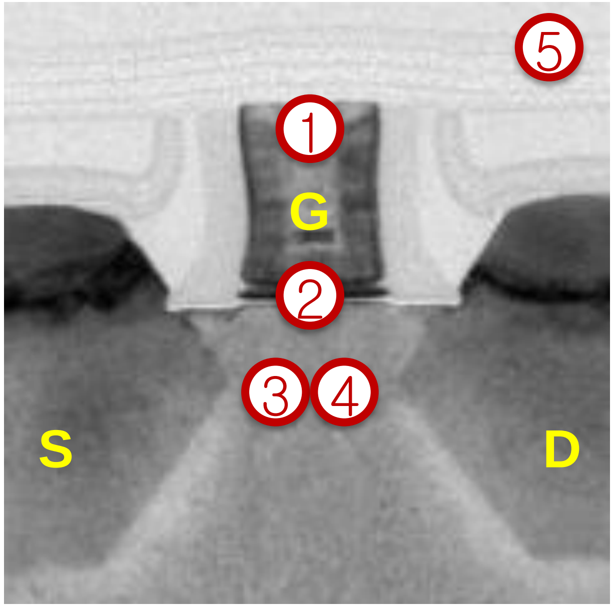
System performance forecast in 2020

Performances increase 50 to 64 times



※Peak data rate

Key issues for semiconductor analysis



Key Issues	Present → 2020	Analytical Evolution
① Critical Dimension	32 → 14nm (2D → 3D)	In Line Resolution ↑, 3D
② Equivalent Oxide Thickness (EOT)	12.6 → 5.3 Å	High Resolution, Bonding Structure, 3D
③ Junction Profile (# of Dopants)	$6x10^5$ → $6x10^4$	3D, Sensitivity, Spatial Resolution
④ Strain	~1% → ~?	Nondestructive, Spatial Resolution
⑤ Contamination (Defect size)	23 → 5nm	Spatial Resolution, Sensitivity

Key issues for semiconductor analysis

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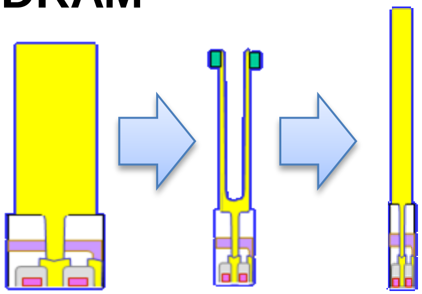
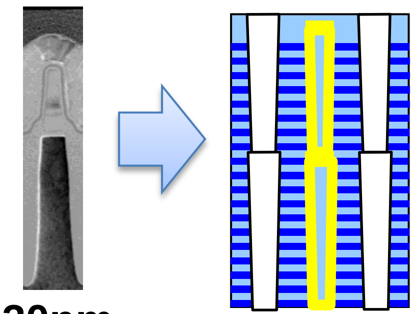
⑥ DRAM



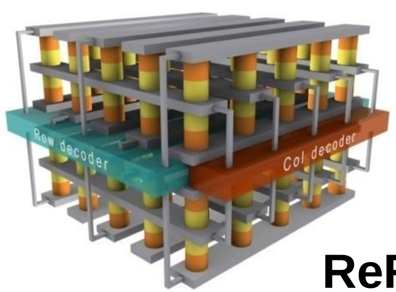
High-k & Simple structure

⑦ Flash



30nm

⑧



ReRAM

Key Issues	Present → 2020	Analytical Evolution
⑥ DRAM - Capacitor (Aspect ratio)	25 → ≥ 80	In Line Structure Monitoring, Composition of Dielectric Material
⑦ Flash - Cell structure (# of stack)	Single → ≥ 128	Nondestructive, In line Structure Monitoring, Grain Structure
⑧ Mechanism for new materials & devices	N/A → ReRAM, PRAM STT-MRAM *etc.*	*In situ* observation

Key Issues	Challenges
① Critical Dimension	In line SEM with BSE, Electron tomography(3D)
② Equivalent Oxide Thickness (EOT)	High Resolution EELS, Atomic scale 3D imaging
③ Junction Profile (# of Dopants)	SPM-based dopant profile, Atom probe tomography
④ Strain	Off line : NBD, In line : TERS
⑤ Contamination (Defect size)	EDS with microcalorimeter
⑥ DRAM - Capacitor (Aspect ratio)	In line 3D analysis of morphology (SEM/Optical method?)
⑦ Flash - Cell structure (# of stack)	In line 3D, EBSD
⑧ Mechanism for new materials & devices	*in situ* SPM/TEM, Low voltage, high resolution TEM/STEM

* **BSE** : Backscattered secondary electron, **NBD:** Nano beam diffraction **, TERS:** Tip-enhanced Raman spectroscopy**, EBSD:** Electron backscatter diffraction

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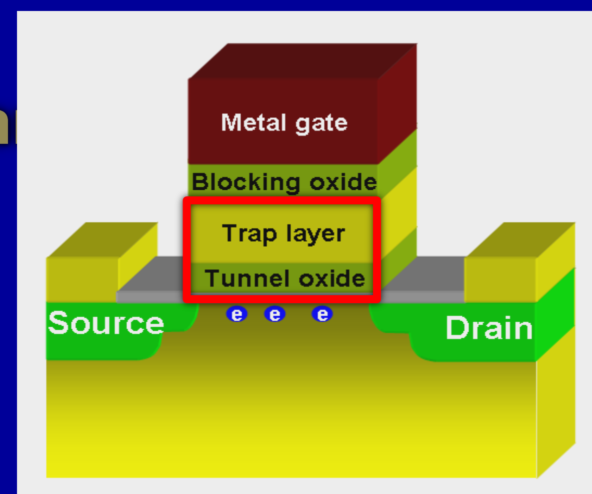
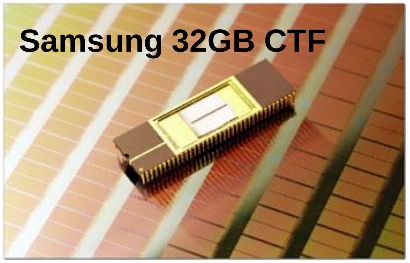
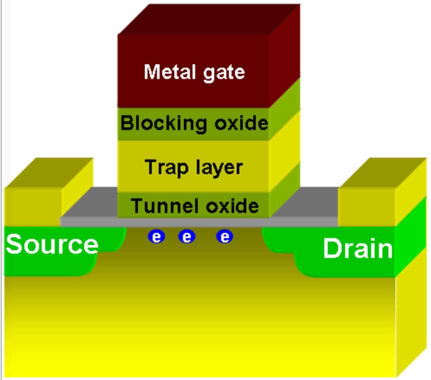


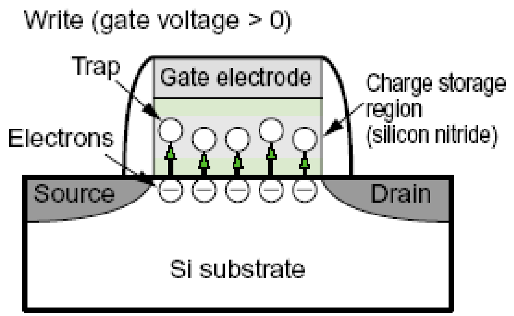
What is a CTF memory?

- **Advantages of CTF memory:** better scaling capability, higher logic compatibility, and lower programming voltage
- **TANOS device has difficulties in controlling the trap density & trap distribution**
  → Si-NC based CTF structure

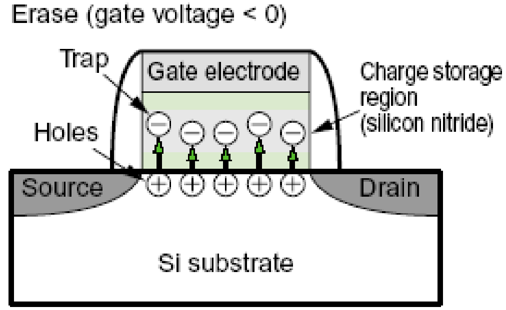




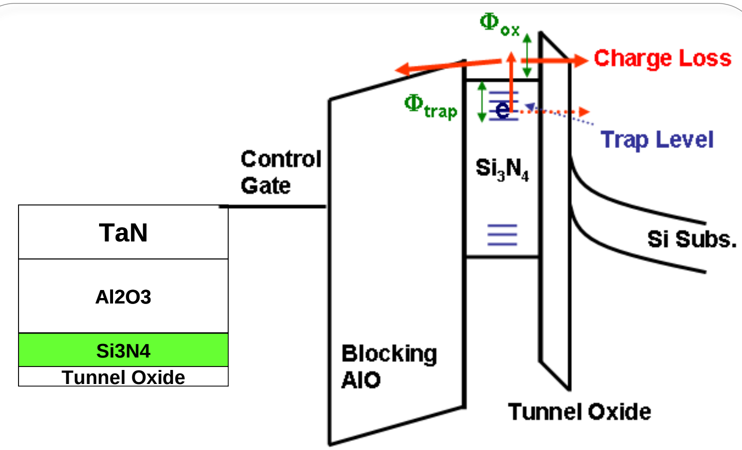
❑ Program



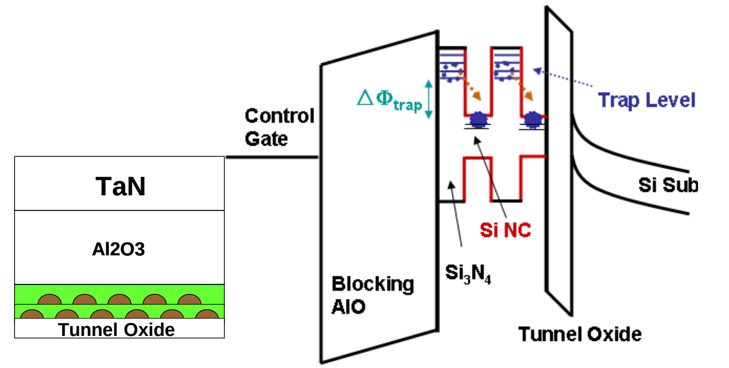
❑ Erase



● TANOS (TaN-Al_2O_3-Nitride-Oxide-Silicon)



TaN/Al_2O_3/SIN_x/SiO_2/Si sub

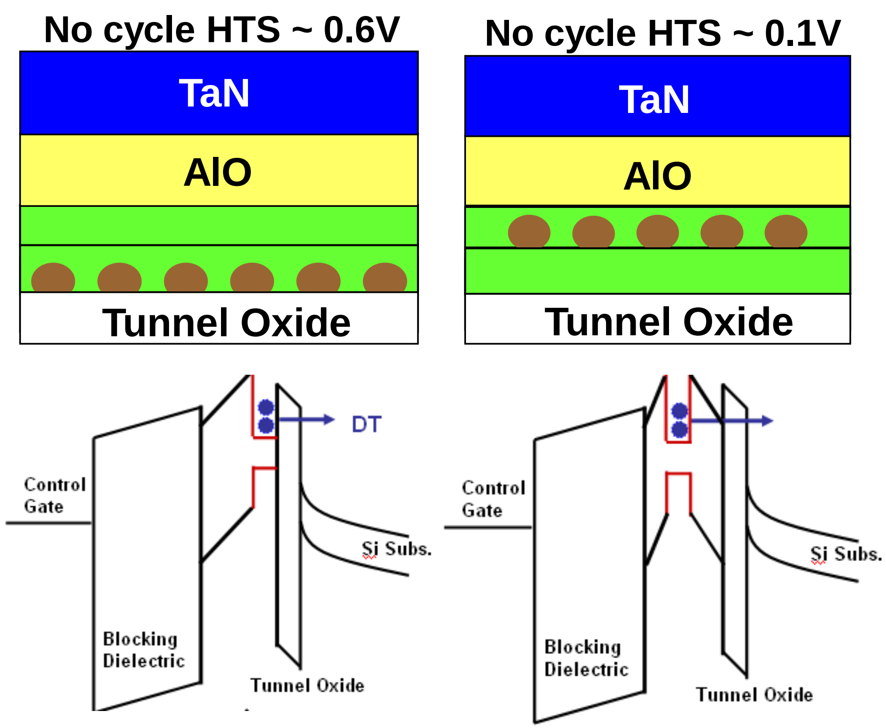


TaN/Al_2O_3/SiNC in SIN_x/SiO_2/Si sub

Key issues for Si-NC distribution

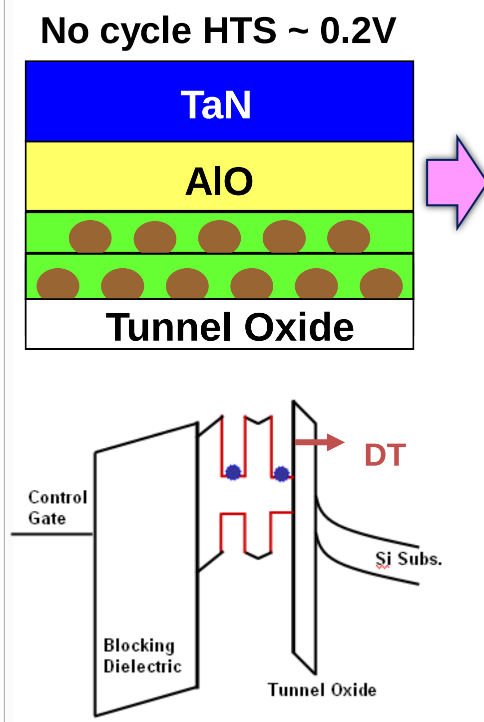
- **Single layer of Si-NCs embedded in SiNx has problems**
  - increase of C/L & degradaion of ERS property
  - → double layer of Si-NCs is available to obtain high density of charge trapping and good charge retention

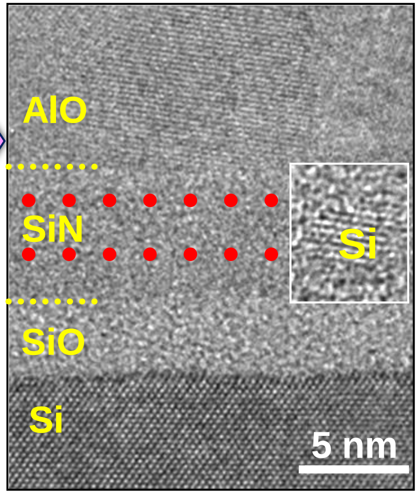
【Single layer of Si-NC】



" increase of C/L" **"degradation of ERS property"**

【Double layer of Si-NC】





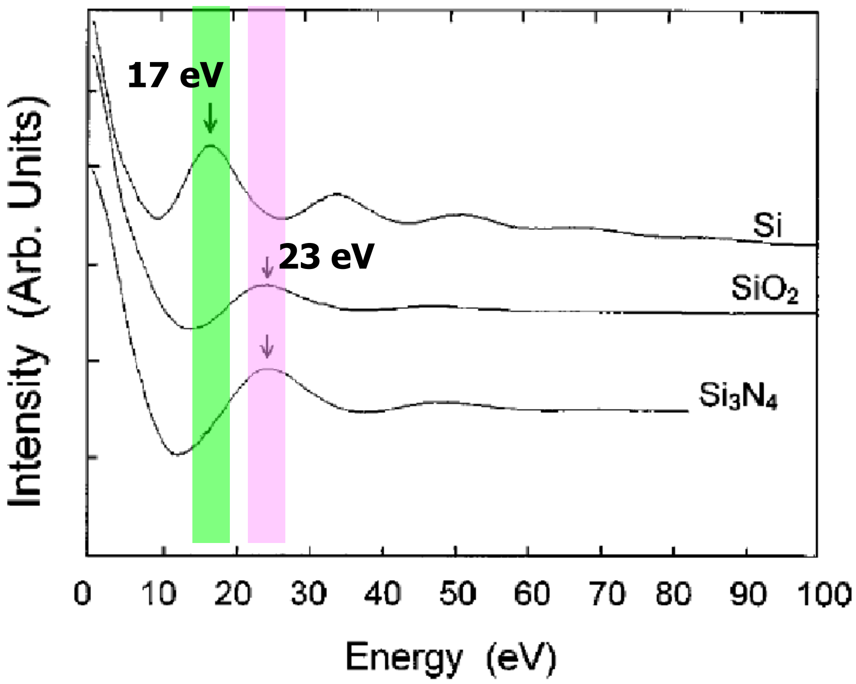
cross-sectional TEM image

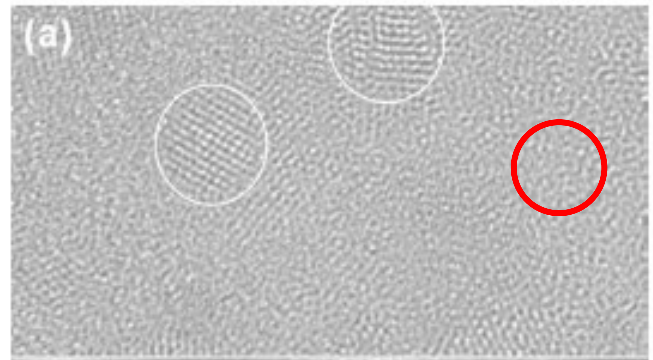
C/L: Charge Loss, ERS: Erase, DT: Direct Tunneling, HTS: Hot Temperature Storage

① Analysis of charge trap distribution

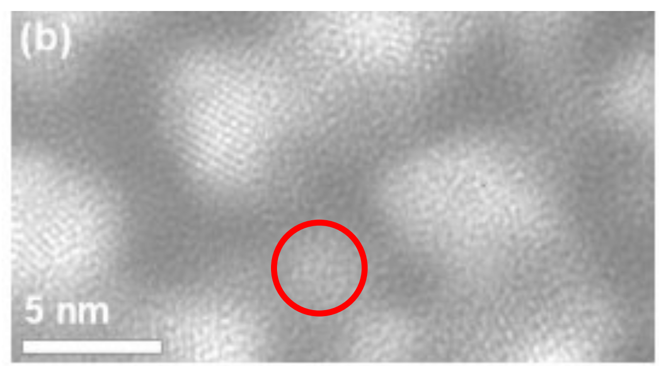
- **HR-TEM image of Si-NCs in SiN_x →** obtainable only when Si-NCs are crystalline and tilted to a strong Bragg condition
- **To see Si-NCs in SiO_x or SiN_x, energy-filtered image at 17 eV** (plasmon loss for Si) **is very useful**

【 Plasmon loss energy-filtered image】





HR-TEM image (Si NC/SiOx):
only a strong Bragg condition

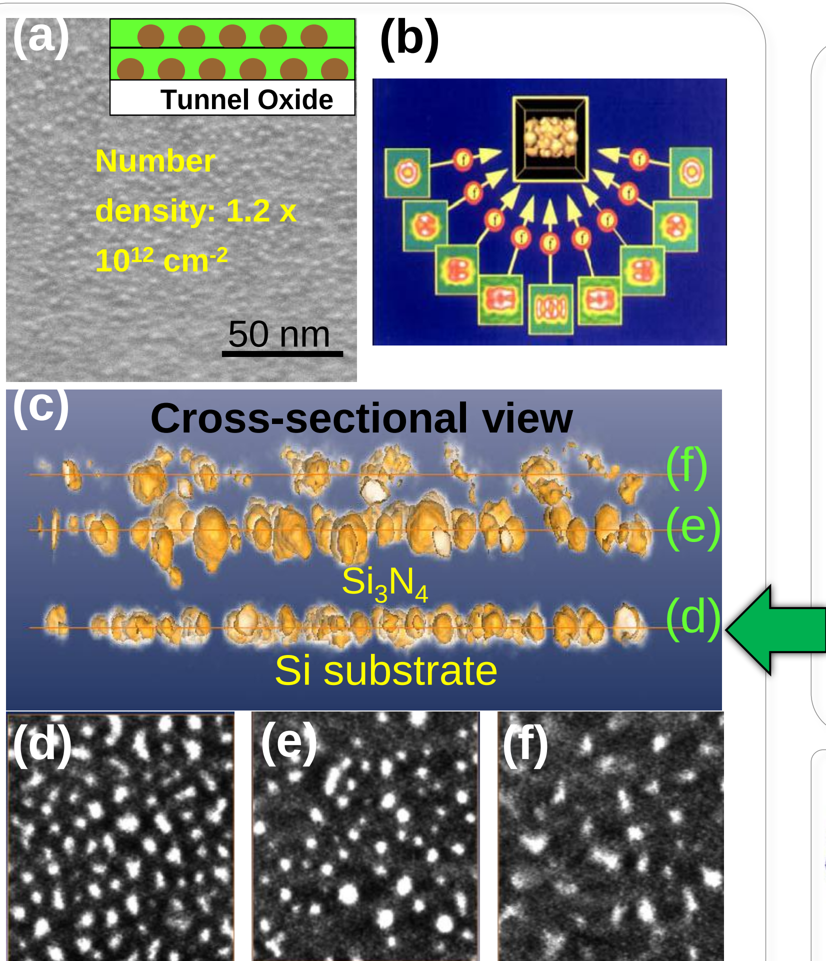


Plasmon energy-filtered image (Si NC/SiOx)

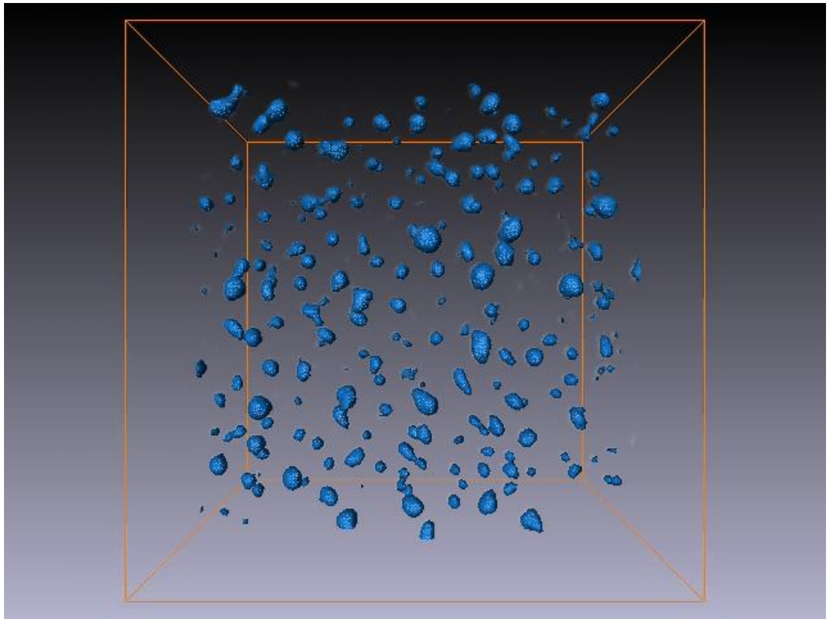
Courtesy: APL 89 (2006) A. Yurtsever *et al.*

① Analysis of charge trap distribution

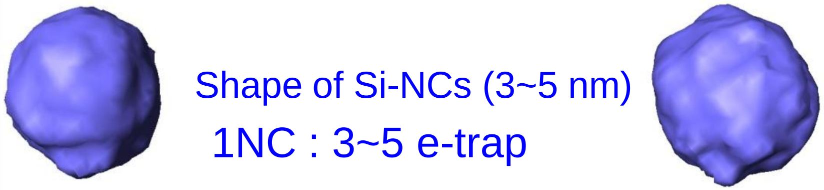
- **Plasmon tomography can measure the morphology & 3D distribution of Si-NCs**
  - Si-NC number density: layer A is higher than layer B
  - additional Si-NC layer C was formed
  - size of Si-NCs is about 3~5 nm, but the Si-NCs in layer C exhibit irregular shape



Plane view



Electron tomography



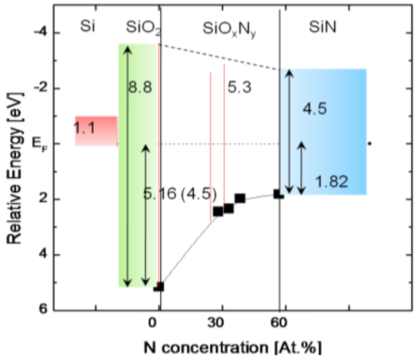
Key issues for SiO_2/SiN_x interface

Dilemma between P/E speed & charge loss

- **Imperfect P/E speed**

  - **Slow carrier recombination velocity:**

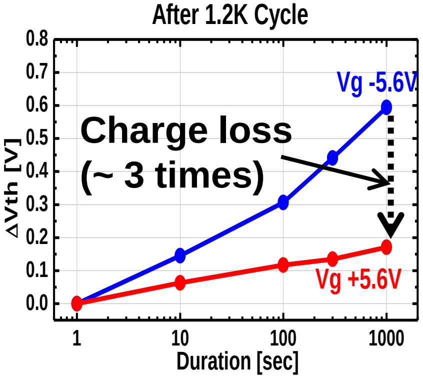
    - **increase of electron & hole trap** in the SiN_x/SiO_2 interface by the defective structure
    - **thick T_{ox} (SiO_2) layer** → use of SiON layer for the increase of hole tunneling



- **Charge loss through tunnel oxide (T_{ox}) in the same E-field**

  - **Lower tunnel barrier:**

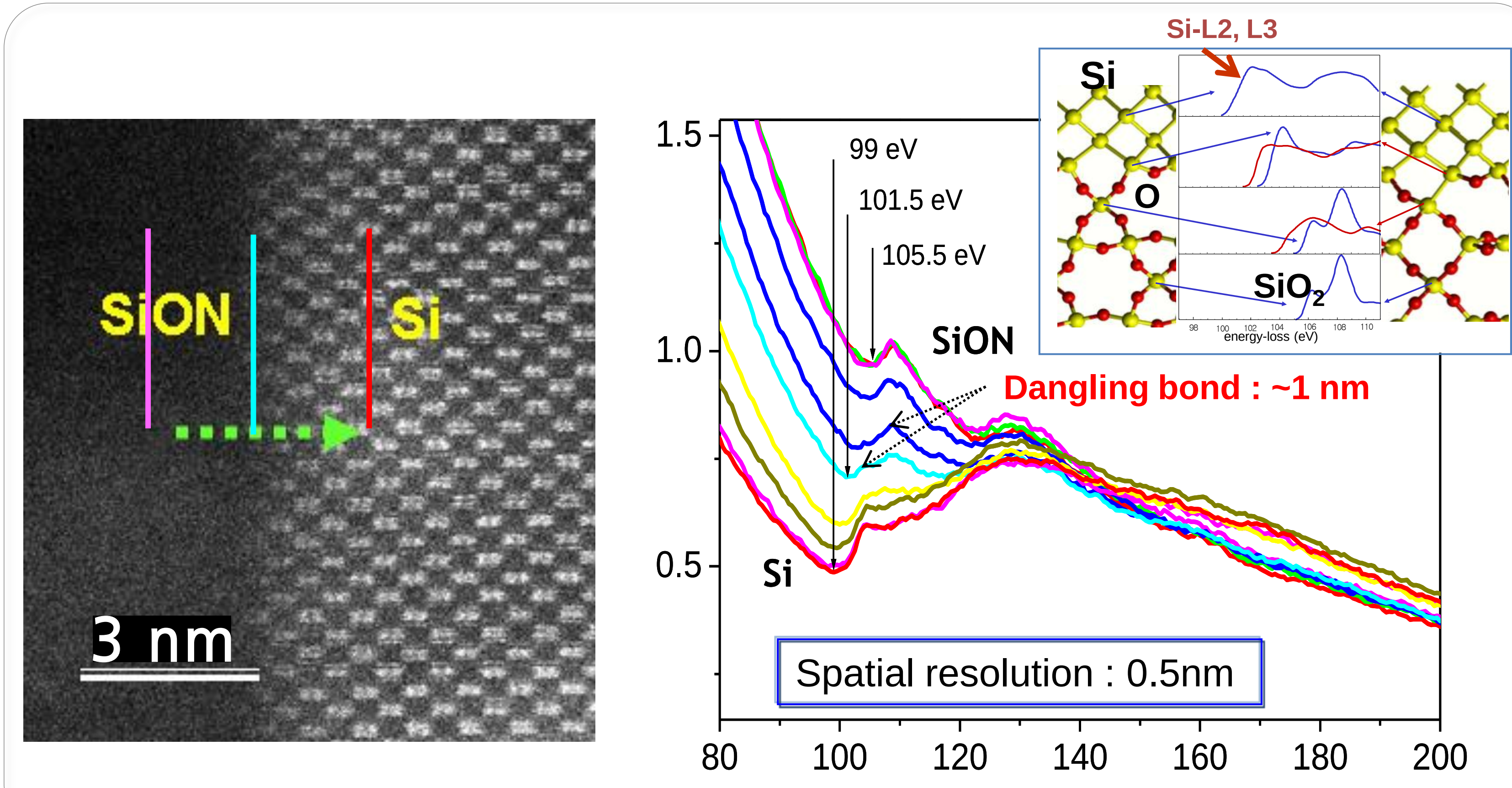
    - **barrier height change** due to the compositional changes in the SiNx layer
    - **thin T_{ox} (SiO_2) layer**



② Analysis of interface trap & charge injection

- **Interface structure: aberration-corrected STEM/EELS with 0.5 nm probe**

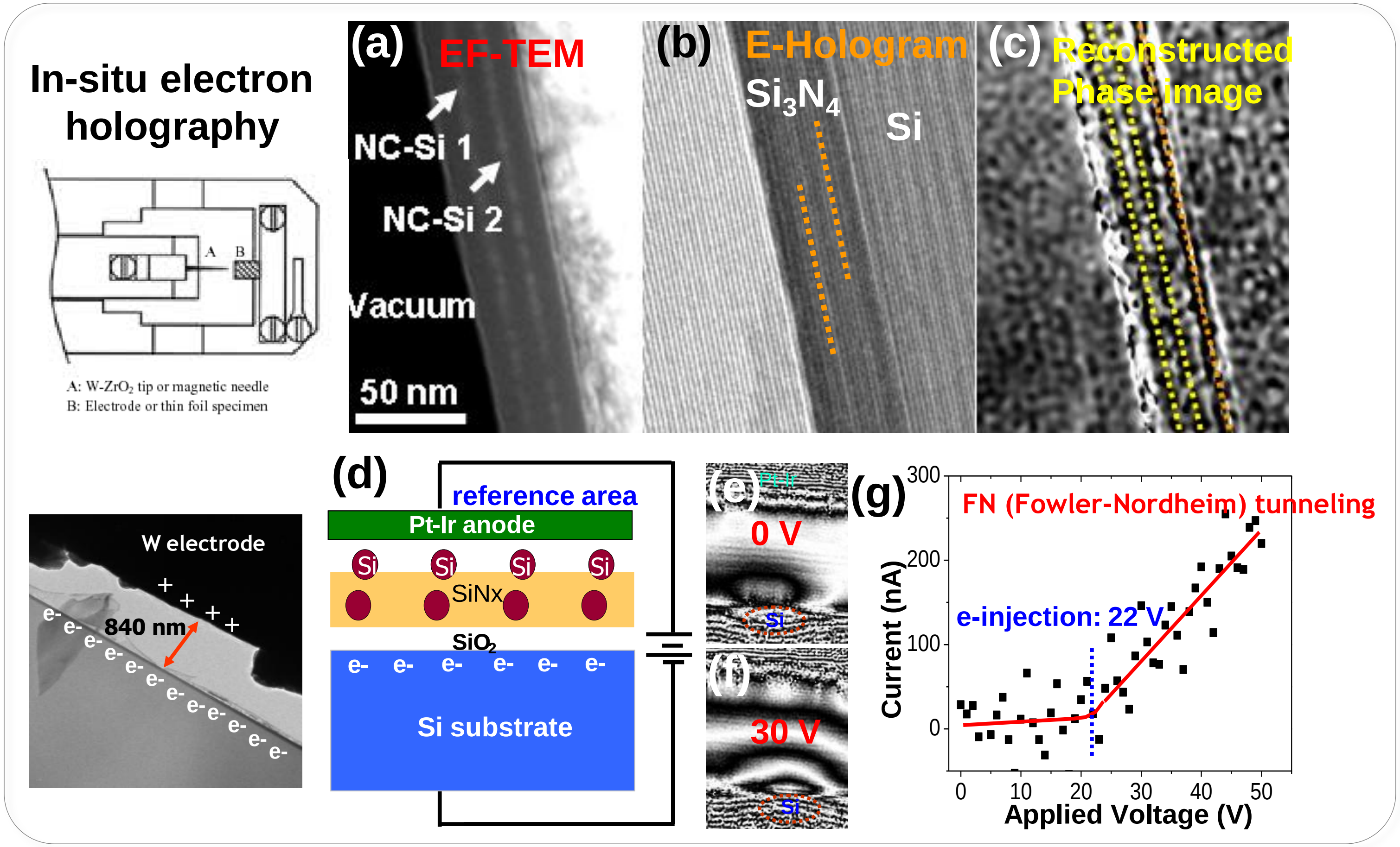
  - Si/SiON interface with suboxide bonding (dangling bonding): ~1 nm



Atomic-scale interface (Si/SiON) structure analysis

② Analysis of interface trap & charge injection

- ***In-situ*** **electron holography enables to confirm the charge trap in Si/SiNx interface & charge injection from Si-NCs**
  - black contrast at three regions (c): trap in the double Si-NC layers and the Si/SiNx (SiO_2) interface
  - electron injection starts from ~ 22 V
  - FN tunneling across the tunneling oxide layer



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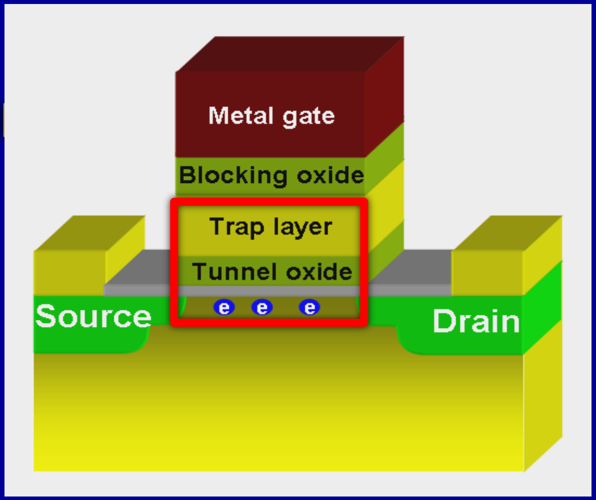
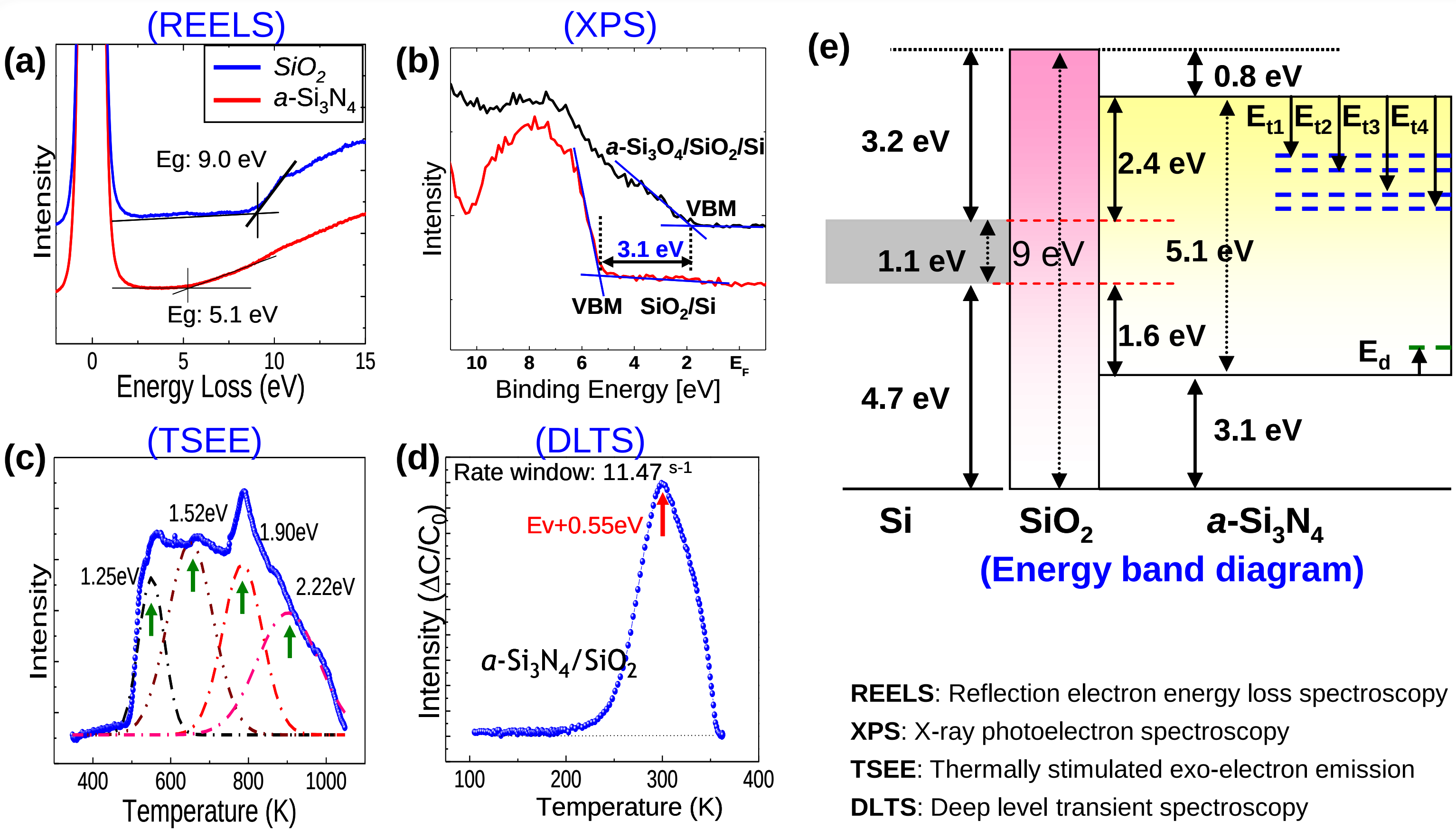


③ Measurements of band structure & defect states

- **Band-gap engineering of *a*-Si_3N_4 and SiO_2 films: measurements of band-gap, band offset, and defect state are necessary**

  - bandgap: REELS, valence band offset: XPS/UPS, defect states: TSEE & DLTS



E_{t1}=1.25 eV, E_{t2}=1.52 eV, E_{t3}=1.90 eV, E_{t4}=2.22 eV

E_d=0.55 eV

REELS: Reflection electron energy loss spectroscopy

XPS: X-ray photoelectron spectroscopy

TSEE: Thermally stimulated exo-electron emission

DLTS: Deep level transient spectroscopy

④ Measurements of bandgap: AES-REELS & STEM EELS

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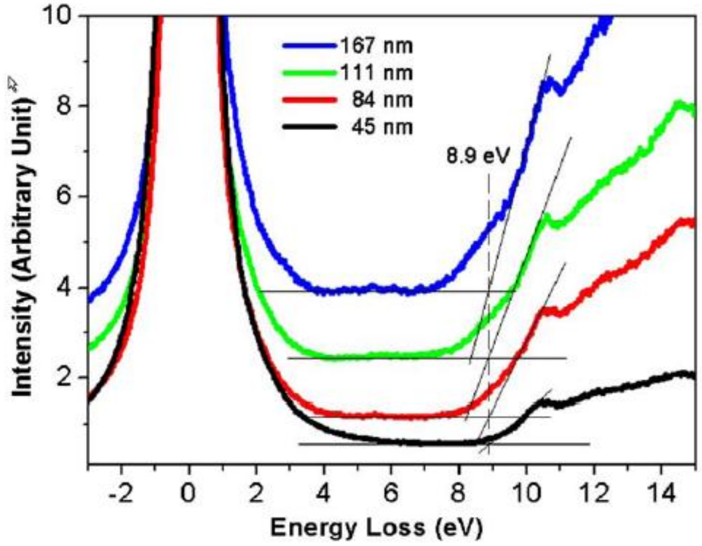
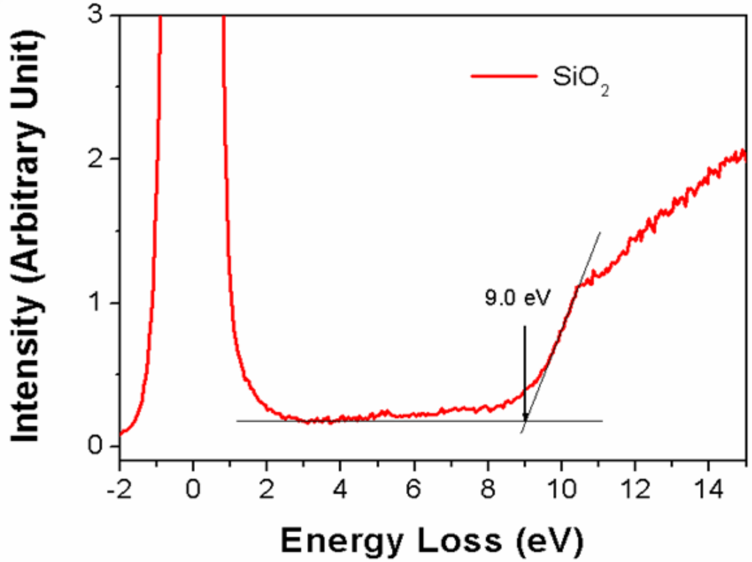
- **Monochromated STEM-EELS**
  - Energy resolution of monochromated EELS (Titan + Monochromator + Tridiem 865 ER): 0.15 eV
- **Comparison AES-EELS and STEM-EELS**
  - **AES-REELS** → larger scan area & higher energy resolution than STEM-EELS, surface charging effect (weak point)
  - **STEM-EELS** → difficulty in reading the onset depending on the sample thickness, and Cerenkov loss effect for insulator



STEM-EELS at various thickness: 300 keV for a SiO_2 thin film



AES-REELS: 1 keV for a SiO_2 thin film

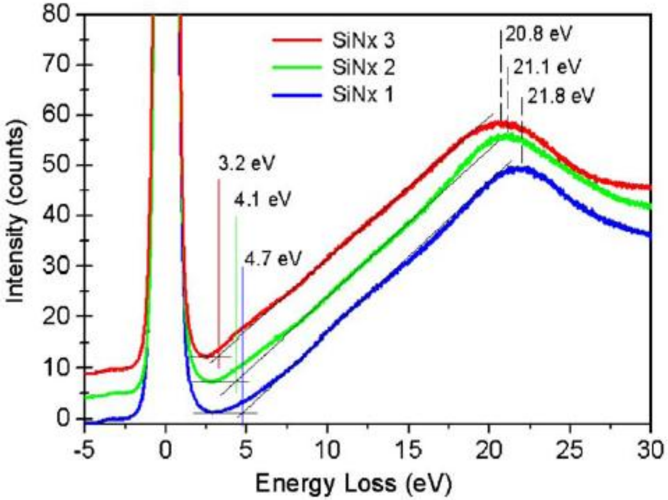
JC Park & G-S Park, *Ultramicroscopy* 109 (2009)

④ Measurements of bandgap: SiN_x layer

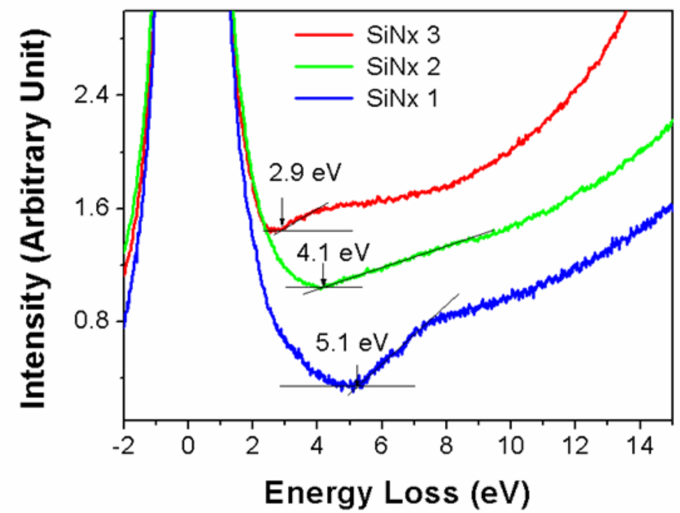
- **Bandgap of *a*-SiNx layers depending on the compositions**
  - as the nitrogen content increases, the bandgap energy of SiNx layer also increases
  - small difference in the bandgap values between two metrology methods

	N	Si	N/Si
SiNx1	59.1	40.9	1.46 ± 0.07
SiNx2	54.5	45.5	1.20 ± 0.06
SiNx3	47.9	52.1	0.92 ± 0.05

Compositions of SiNx estimated by RBS



AES-REELS



STEM-EELS

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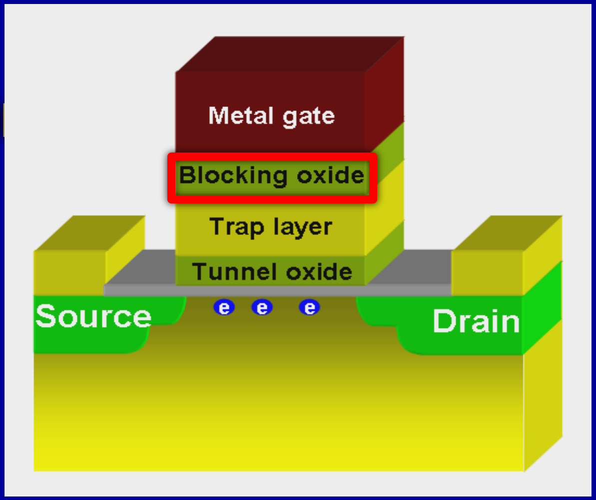

Key issues for blocking oxide (Box) layer

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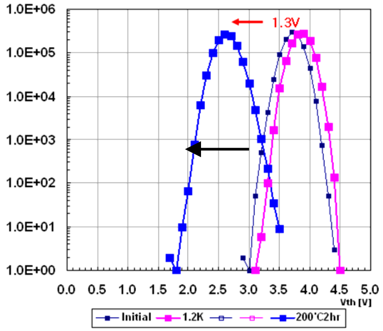
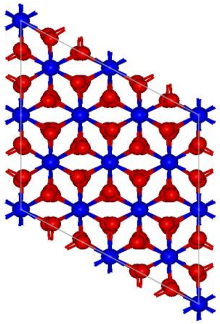
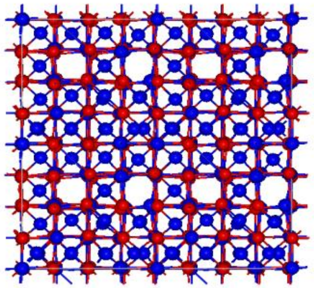
Retention/endurance: back tunneling & charge loss

- **Lower barrier height between CTL and Box layer**
  - interface diffusion (Al, Si), Al_2O_3 structure (Eg)



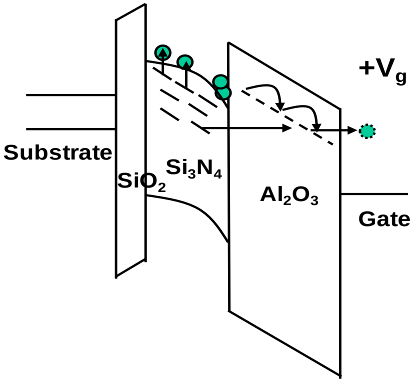
α-Al_2O_3





γ-Al_2O_3

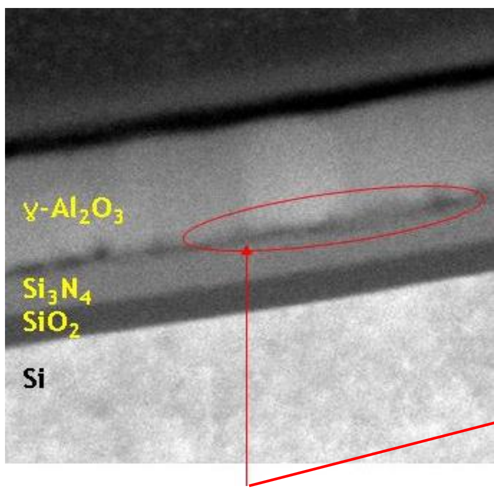
- **Trap in Box layer**
  - density of dangling bond
  - trap energy level



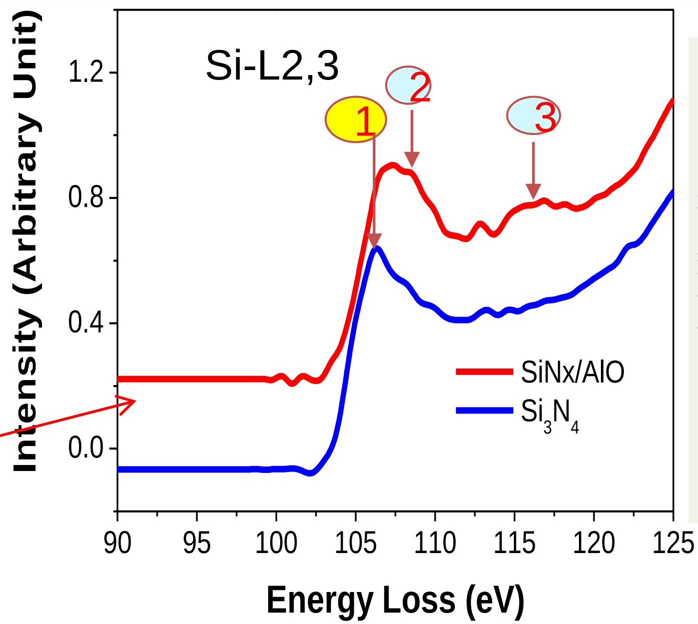
CTL: Chrage Trap Layer

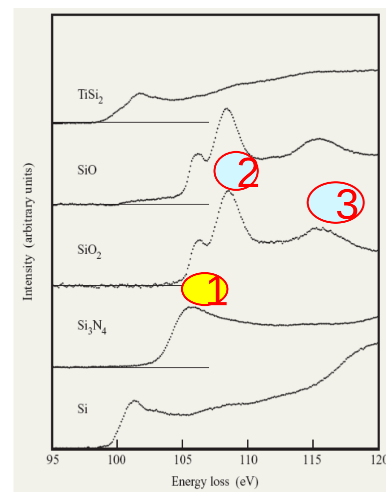
⑤ Analysis of charge loss: SiNx/AlO interface

- **STEM-EELS in the the SiNx/AlO(ALD) interface**
  - oxidation of SiNx generates silicon oxynitride (SiON) layer in the interface
  - SiON layer induces back tunneling by the conduction band offset of Box (AlO) layer
  - clean interface (SiNx/AlO) structure is required to reduce the retention & endurance problems



Formation of new layer in the SiN/AlO interface





⑤ Analysis of charge loss: AlO layer

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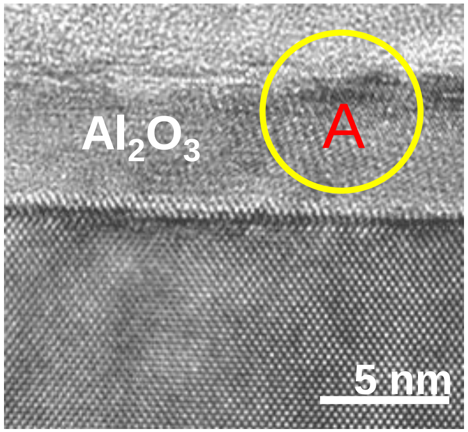
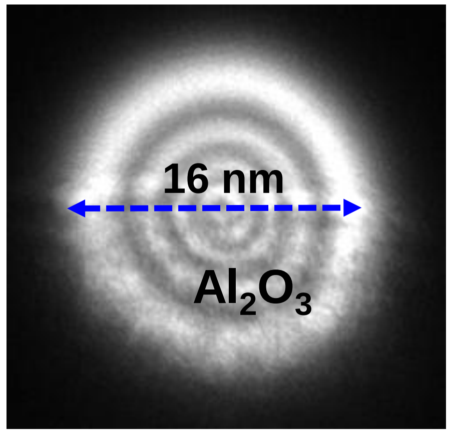
- **Crystal structure of thin Al_2O_3 (Box) layer**
  - wide-bandgap alumina (AlO) is desirable as the Box: α-Al_2O_3 -> 8.8 eV , γ-Al_2O_3-> 6.6~7.0 eV
  - NED/EELS results: γ-Al_2O_3 phase

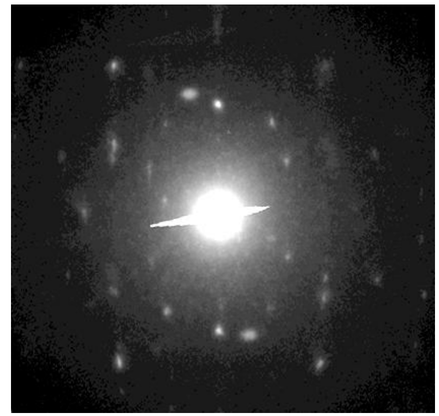
(a) HR-TEM image



(b) Electron probe image

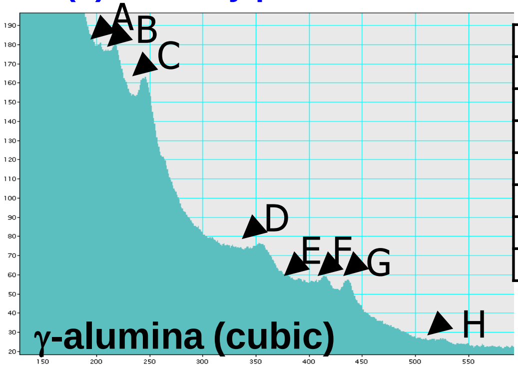


(c) NED



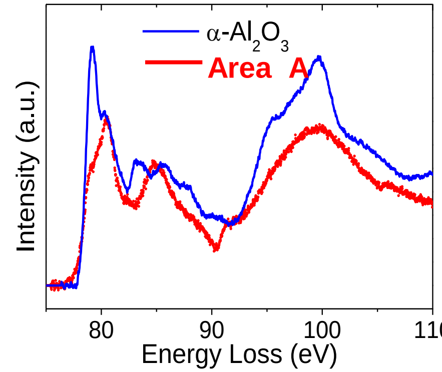
NED: Nano-area Electron Diffraction

(d) Intensity profile of NED shown in (c)



A	2.380 Å
B	2.229 Å
C	1.983 Å
D	1.359 Å
E	1.241 Å
F	1.168 Å
G	1.112 Å
H	0.921 Å

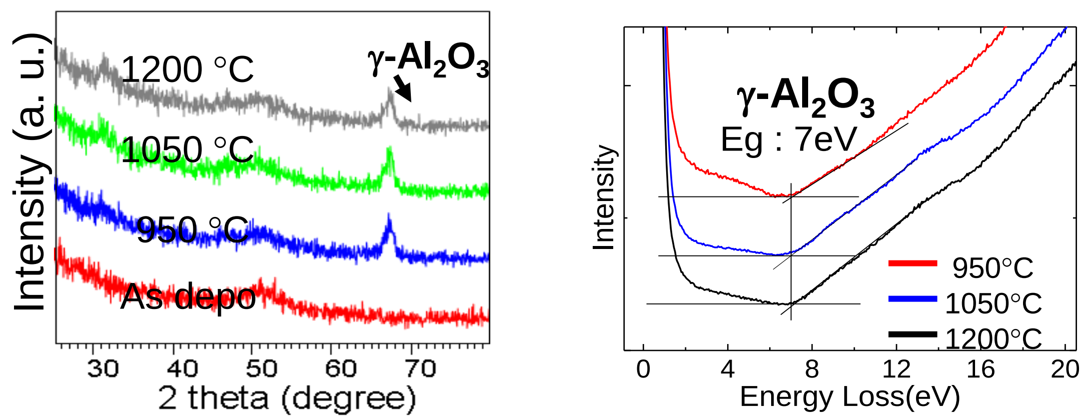
(e) Core-EELS spectra in A



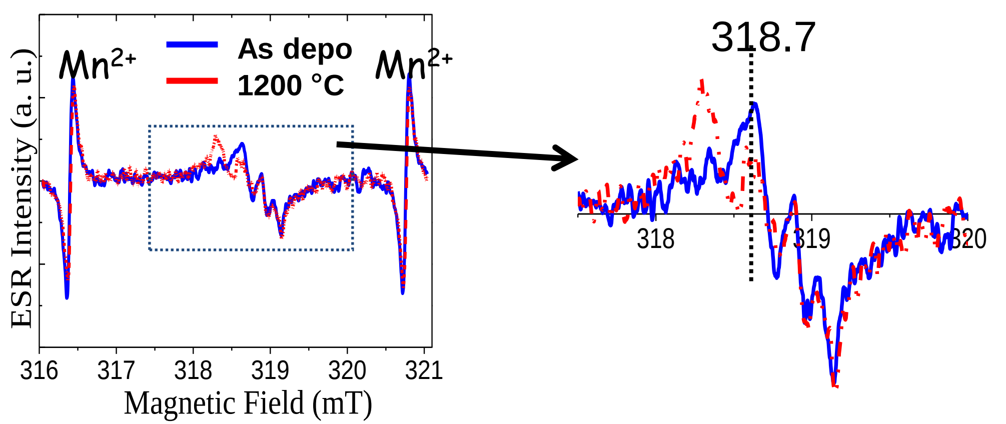
⑤ Analysis of charge loss: AlO layer

- **Eg and defect density of thin Al_2O_3 (Box) layer**
  - E*g* of γ-Al_2O_3: 7.0 eV
  - Dangling bond density of γ-Al_2O_3 measured at 15 K → as-depo:1200 °C = 100:72.8 (27.2% ↓)

(a) XRD for the ALD grown-Al_2O_3 films **(b) REELS: bandgap**



(c) ESR (Electron spin resonance)



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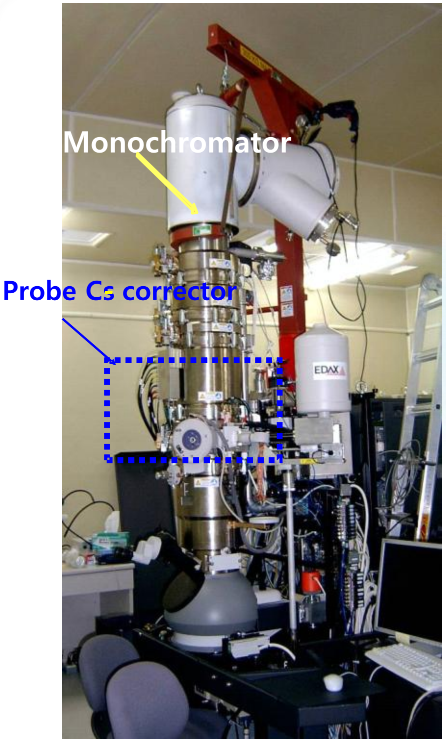
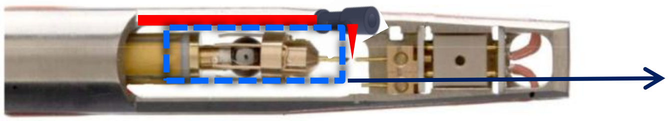
In-situ probing inside TEM

- **SAIT TEM/TEM (Titan 300 kV, FEI)**

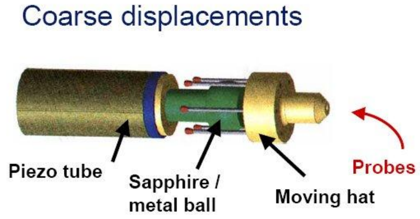
  - monochromated EELS: 0.15 eV, Cs-corrected STEM image: 0.8 Å
  - Piezo motor : fine displacement of probe → 0.2 nm
  - Bias modulation (<140 V)
  - High power, tunable laser irradiation (~150 mW, λ : 400~800 nm)

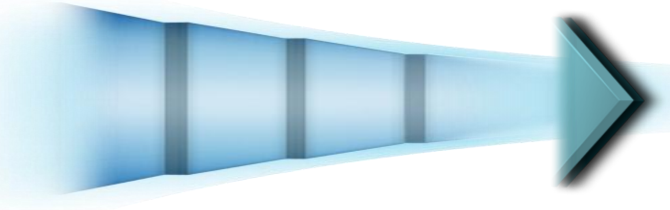


SAIT TEM

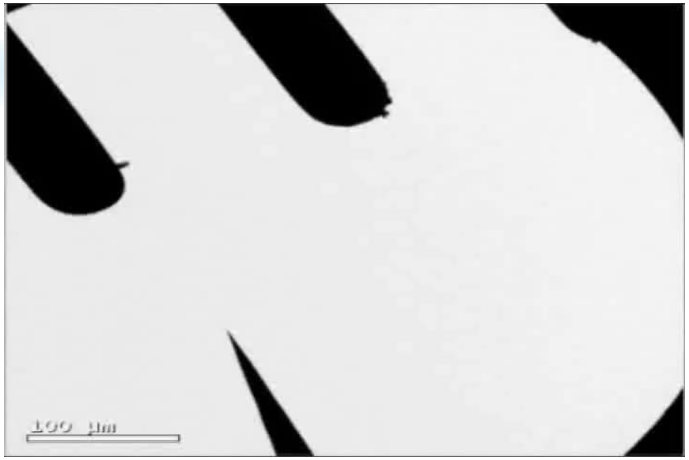


In-situ holder: Piezo motor, bias modulation





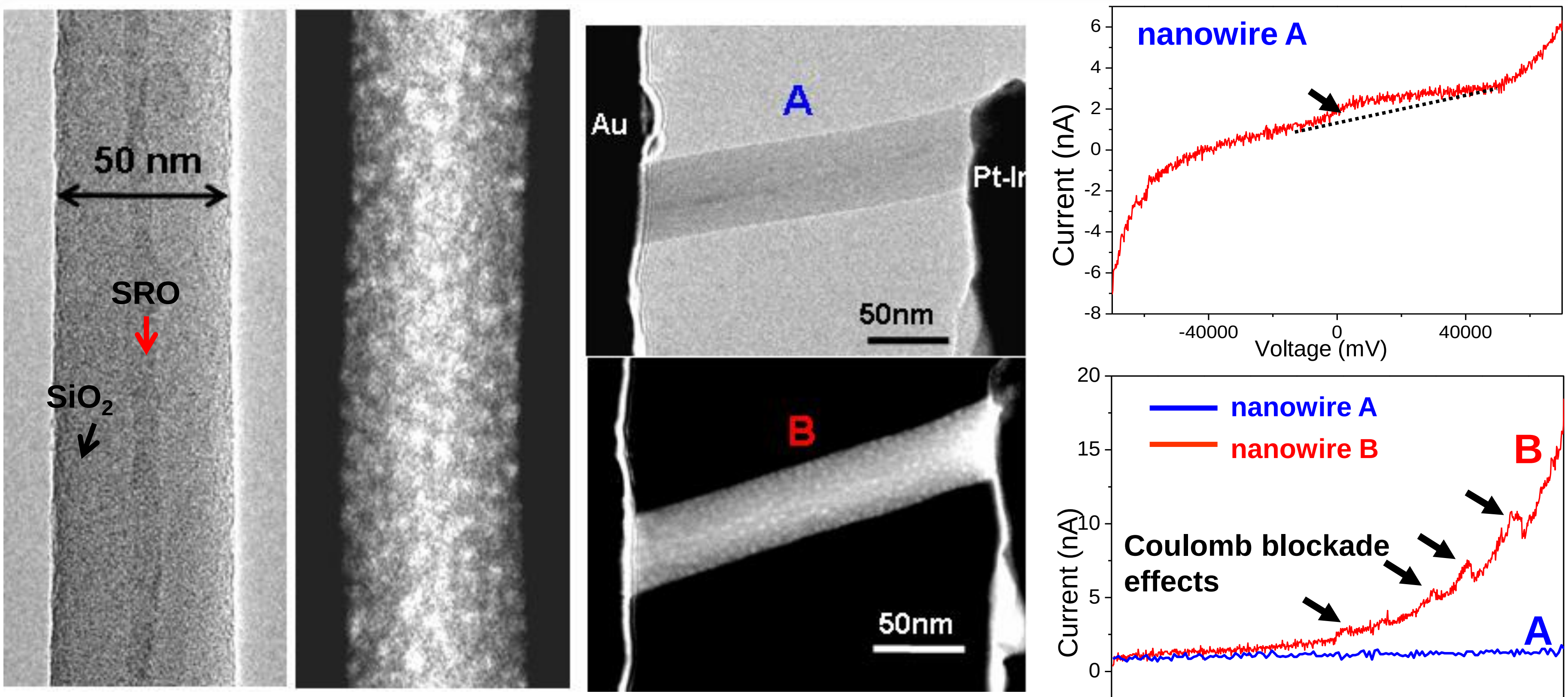
Laser system
(λ : 400~800nm, ~180mW)



Approach of probe

In-situ probing inside TEM: core-shell NW (Ex. 1)

- **Electron transport properties of the core-shell (SRO/SiO_2) nanowire**
  - before Si nanodot formation: broad bump in current → electron accumulation in the NW
  - after Si nanodot formation (e-beam irradiation at 25 A/cm^2 for 5 min) : staircase-like behavior → Coulomb blockade effects



Original SRO/SiO_2 nanowire (A)

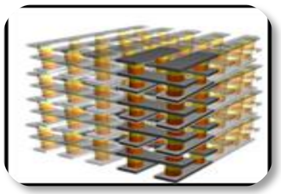
SRO/SiO_2 nanowire after Si Nandot formation (B)

G-S Park *et al.*, Nano Letters 9 (2009)

Mechanism for New Devices

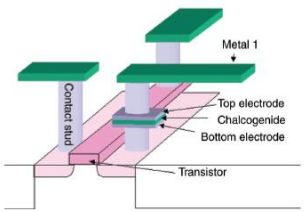
- *In situ* / atomic scale analysis is essential to understand switching mechanism of new devices

ReRAM



- Understanding of **oxygen vacancy path** of Ta_2O_{5-x} in real time, different from existing memory mechanism

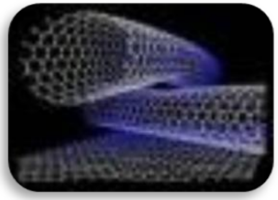
PRAM



- Finding of **the phase change mechanism** between amorphous and crystalline GST

Graphene

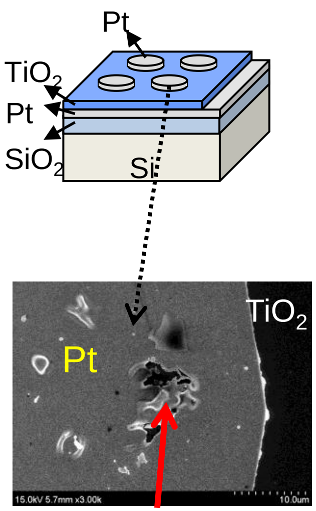
⋮



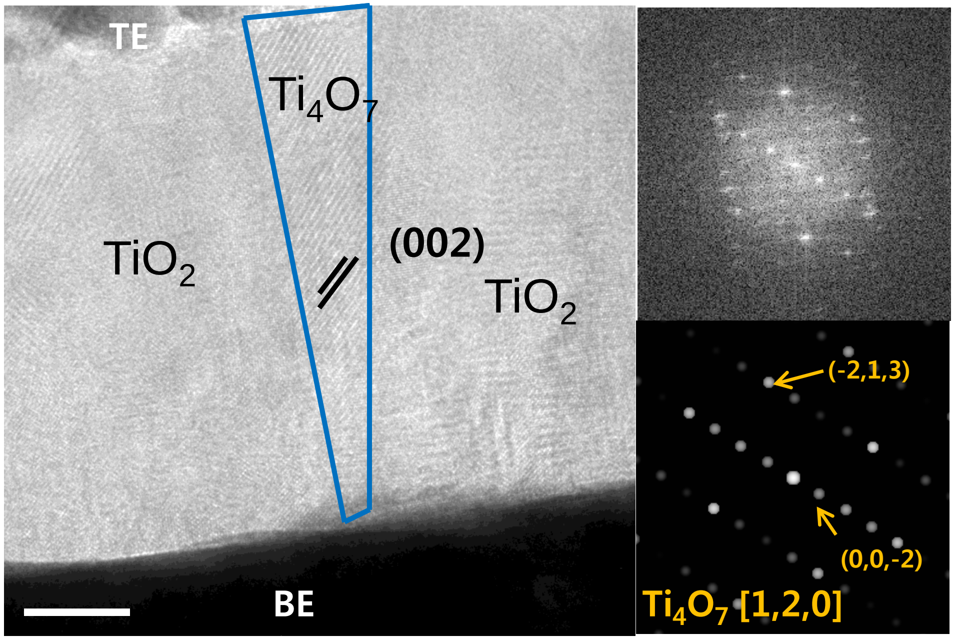
- Need for understanding of **surface oxidation-reduction mechanism** in atomic level

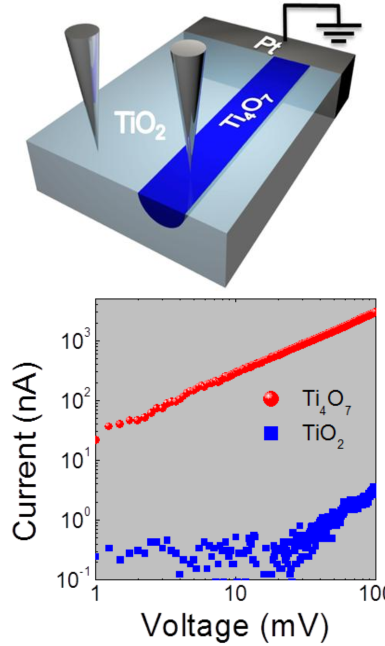
In-situ probing inside TEM: nanofilaments(Ex. 2)

- **Direct measurements of *I-V* scan on nanofilaments**
  - HRTEM, SAED pattern, and FFT diffractogram confirm the Magne´li structure of a grain
  - Conductivity ratio (Ti_4O_7/TIO_2) : ~1,000
  - Resistive switching mechanism in TiO_2 thin film can be directly confirmed



Blown-off region after forming process





Ti_4O_7 (**red circles**)
Anatase TiO_2 (**blue squares)**

Identification of Ti_4O_7 (magneli) structure

D-H Kwon & G-S Park, *Nature Nanotech. 5 (2010),148.*

Outline

- Si technology trend & issues for semiconductor analysis
- Nanometrology for understanding charge transport phenomena of CTF memory
  - Analysis of charge trap distribution & charge injection
  - Measurements of band structure & defect states
  - Analysis of charge loss
- New metrology for the study of charge transport phenomena
  - *In-situ* probing inside TEM
- **Conclusion**

Conclusion

SAMSUNG

Developments of advanced analytical techniques for unveiling the nature of charge transport phenomena are essential to accomplish high performance nonvolatile CTF memories.

We introduced potential analytical approaches for examining the charge trapping, charge injection, and charge loss phenomena in Si nanocrystal-based CTF memory.

Charge trap distribution and charge injection behaviors in the Si NC-based memory can be analyzed, with plasmon tomography, aberration-corrected STEM/EELS, and *in situ* electron holography.

Recently developed REELS, monochromated STEM-EELS, TSEE, DLTS, and ESR methods allow the measurements of the bandgap, defect states, and defect density for the Tox layer, CTL, and Box layer with higher accuracy.