NC STATE UNIVERSITY

Source/Drain Junctions and Contacts for 45 nm CMOS and Beyond

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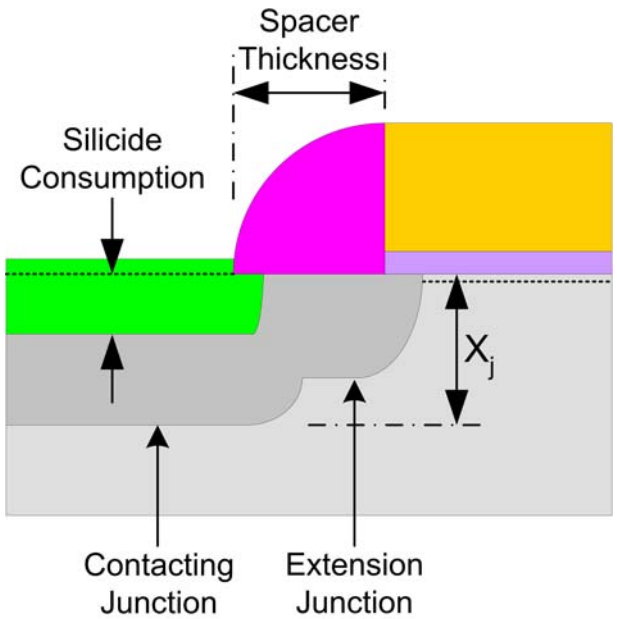
2005 International Conference on Characterization and Metrology for ULSI Technology

Outline

- Series Resistance Challenges
- SiGe Source/Drain Technology
- Local Strain for Enhanced Mobility
- Ultra-thin SOI & FINFET

Extension Structure

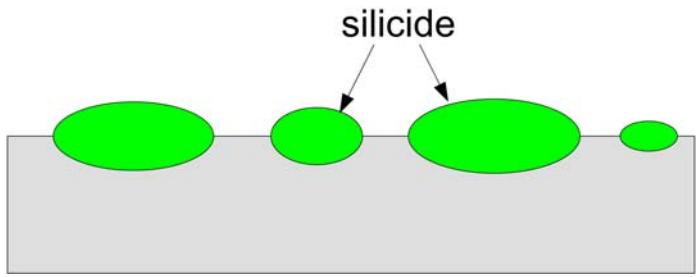


Junction &

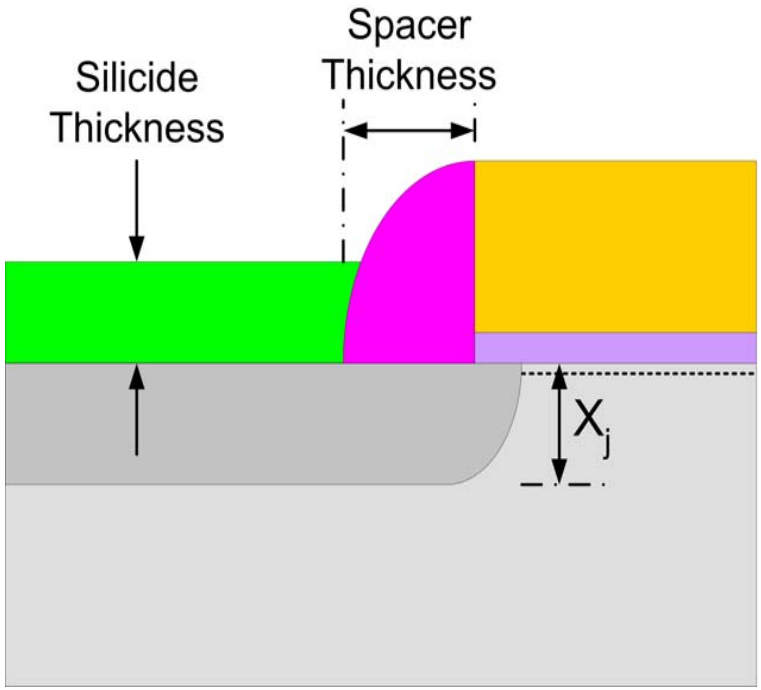
Silicide Scaling

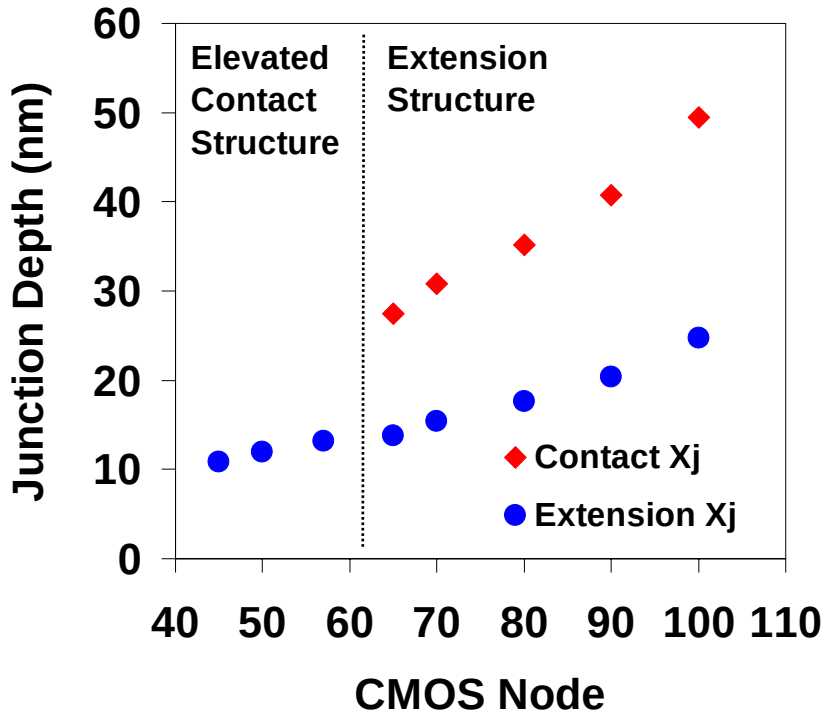
Silicide scaling cannot continue forever:

1) Leaky Junctions
2) Agglomeration



Elevated Contact Structure

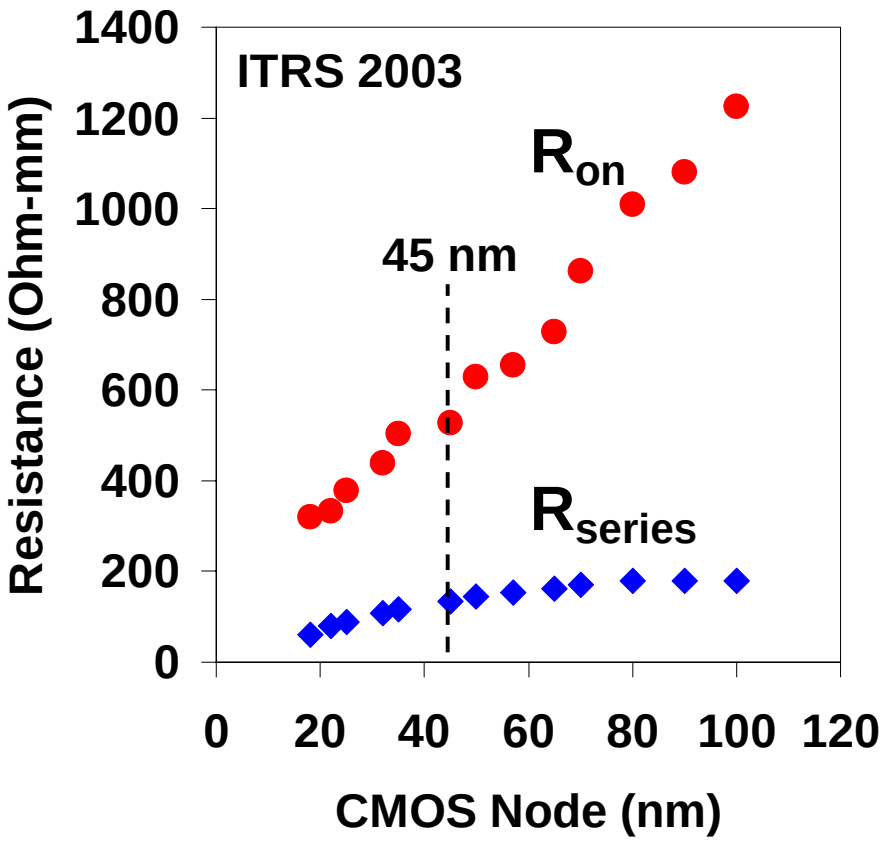




Silicide is formed after selective deposition of a sacrificial Si layer (Si or SiGe)

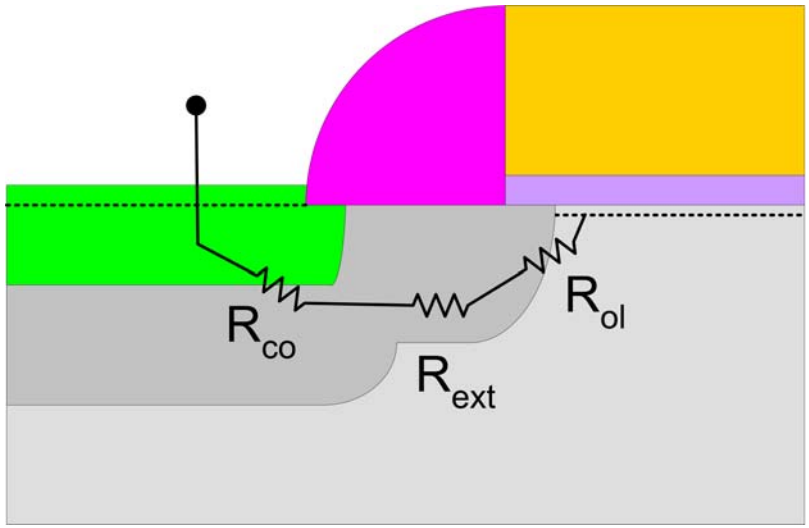
Parasitic Source/Drain Resistance

The Primary Source/Drain Challenge

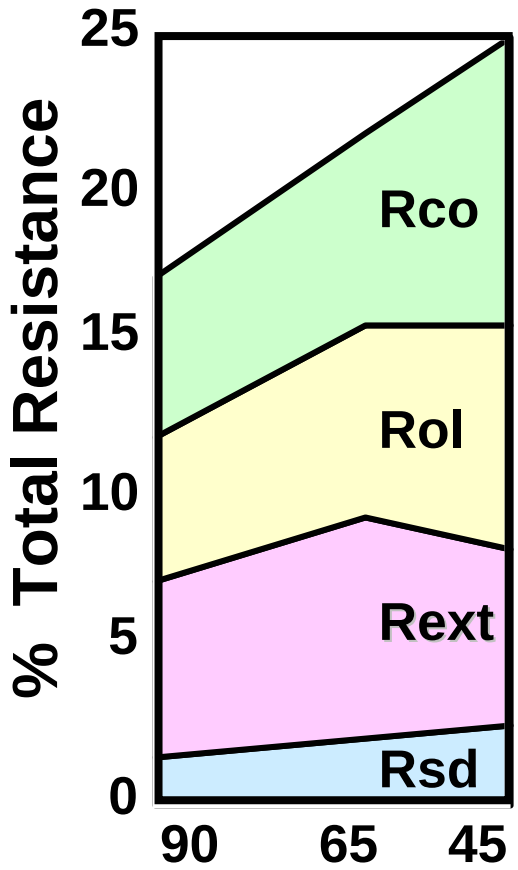


- **Channel Resistance**
  - *$R_{on} = V_{DD}/I_{DSAT}$*
- **Series Resistance**
  - *26% of the channel resistance at 45 nm*

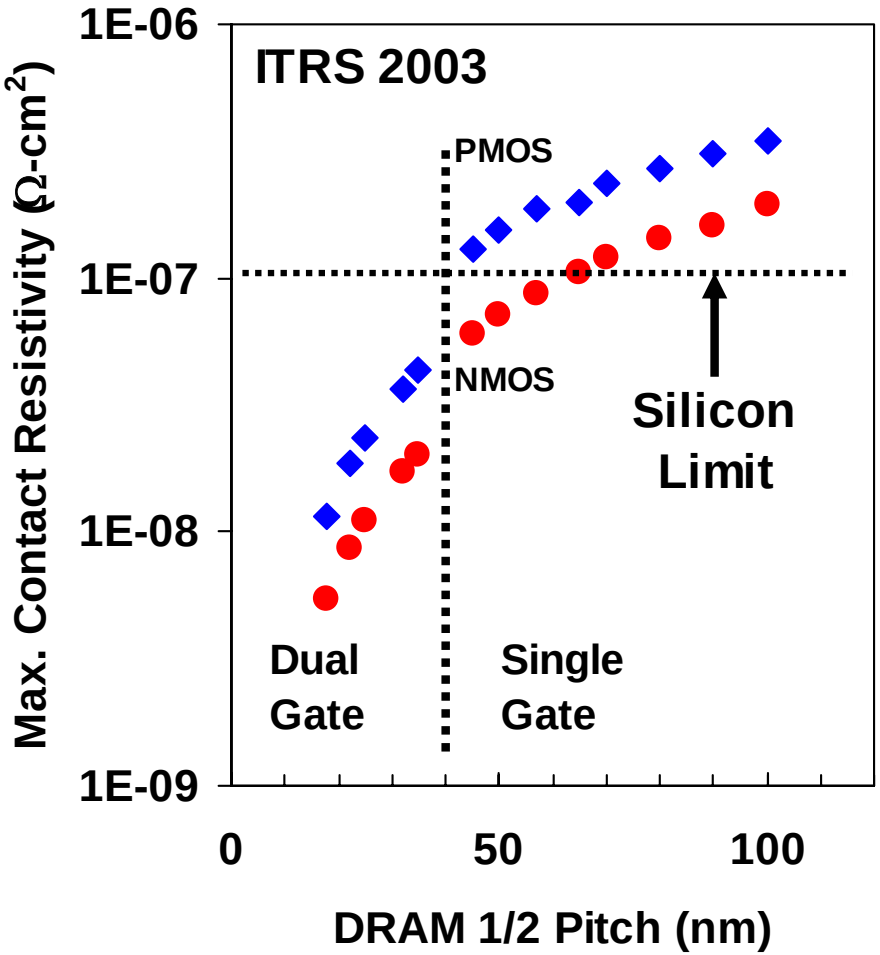
Series Resistance Components



- **Overlap Resistance:**
  - *Abrupt Junctions*
- **Extension Resistance**
  - *Ultra-Shallow Junctions*
  - *High Dopant activation*
- **Contact Resistance**
  - *Small Barrier Height*
  - *High Dopant Activation*



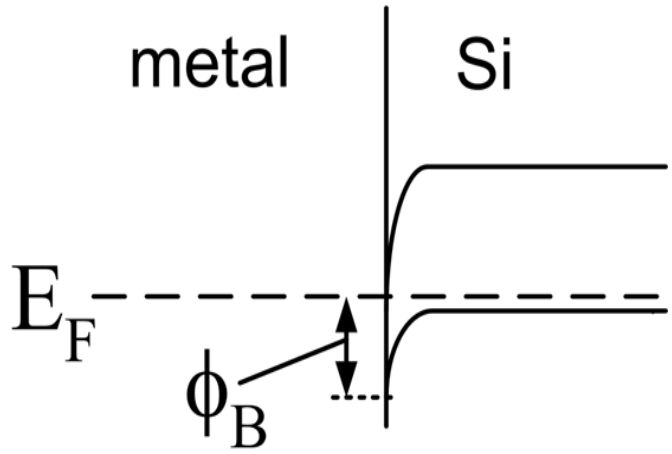
Maximum Allowable Contact Resistivity



- **Calculated assuming**
  - *series resistance is entirely due to contact resistance*
- **For dual gate devices**
  - $W_c = W/2$

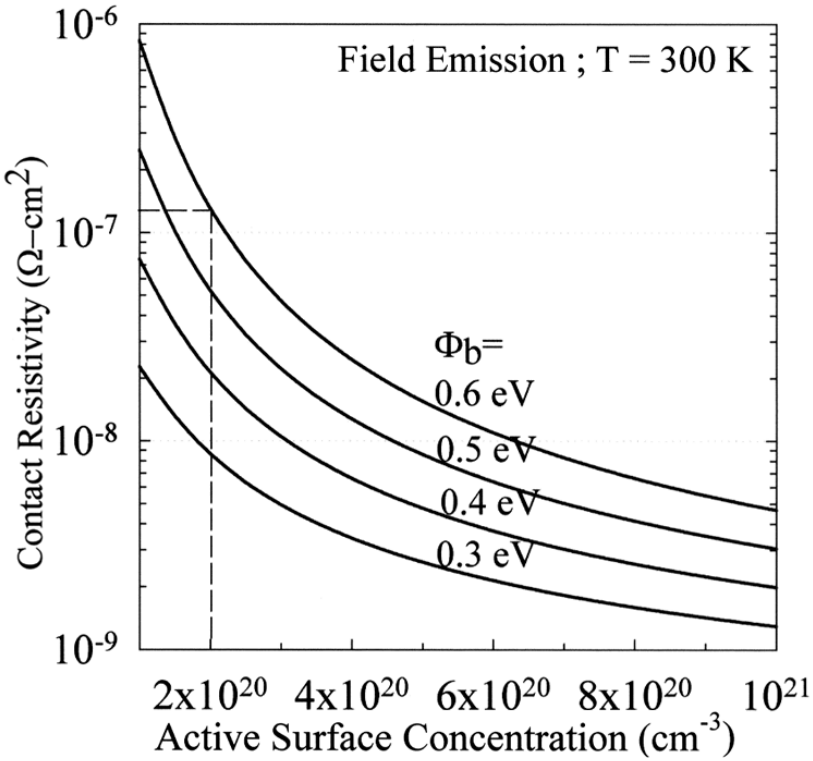
Contact Resistivity

$$\rho_c \propto \exp\left[\frac{4\pi\sqrt{\varepsilon m^*}}{h}\frac{\phi_B}{\sqrt{N_D}}\right]$$



- **Exponential Function of**
  - ***Doping Density, N_D***
  - ***Barrier Height, ϕ_B***
- **Fermi level pinning**
  - ***Barrier Height ~ Independent of Metal Work Function***

Contact Resistivity



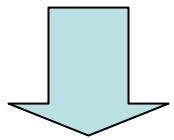
- **Barrier Height on Si**
  - *$\phi_B \sim \frac{1}{2} E_g \sim 0.6$ eV*
- **Maximum Doping**
  - *Boron ~ 2 x 10^{20} cm^{-3}*

Best Contact Resistivity ~ 10^{-7} Ω-cm²

We need 10^{-8} or better!

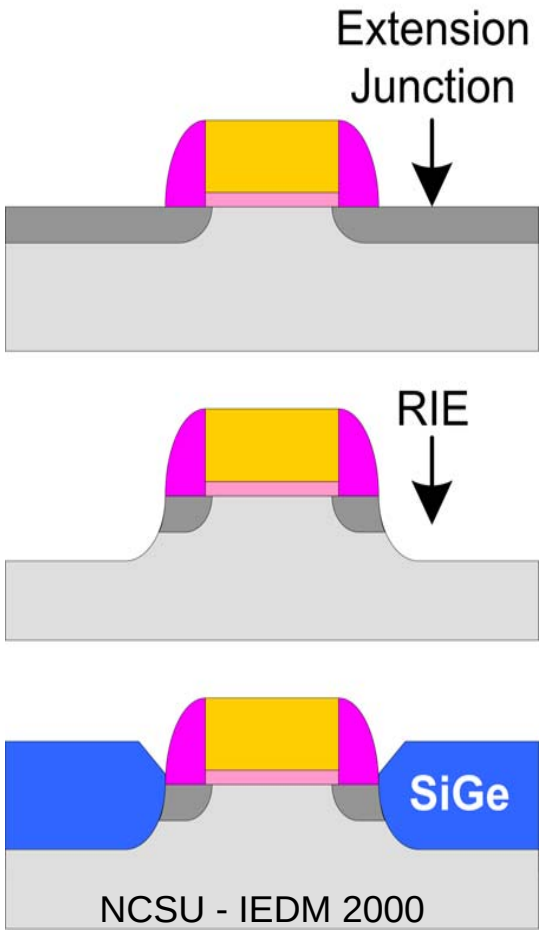
Solutions to Contact Resistance Challenge

- **Dual Metal Contacts**
  - *Two self-aligned metal contacts with Fermi levels near conduction and valence bands*
  - *Requires passivation of metal induced surface states to suppress Fermi level pinning*
- **Single Metal - Different Semiconductor**
  - *Smaller Bandgap – Smaller Barrier Height*
  - *Enhanced dopant activation*

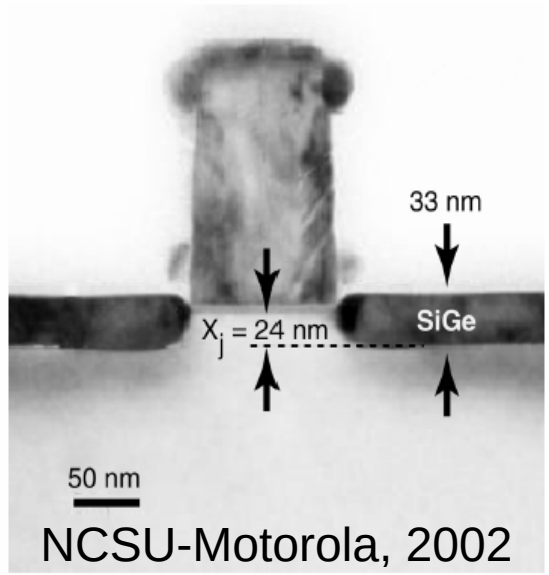


Silicon-Germanium Alloys

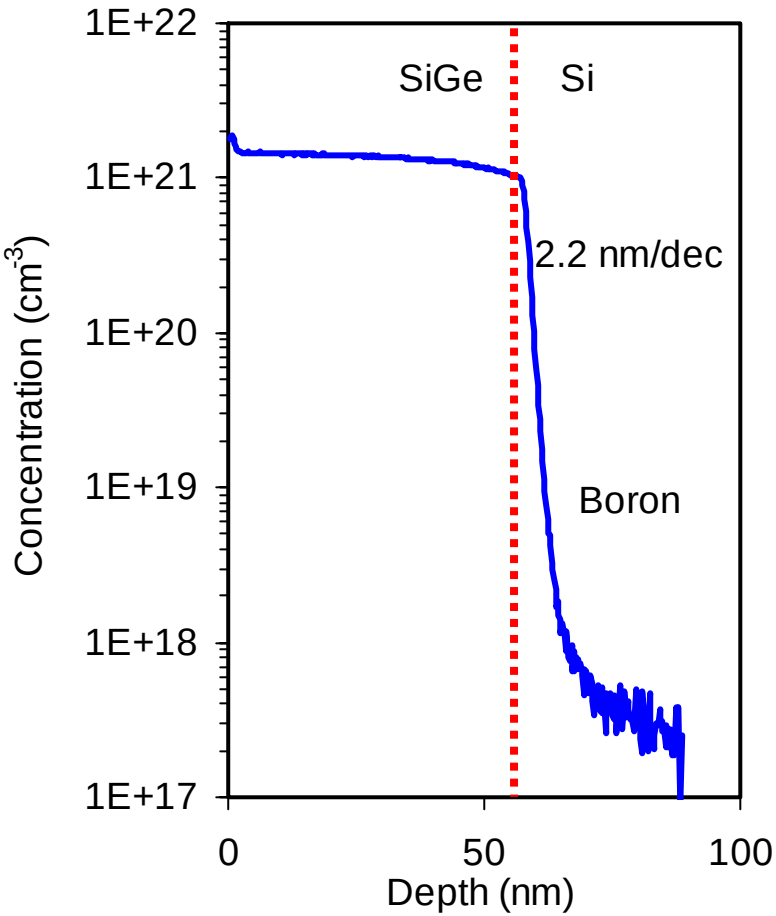
SiGe Source/Drain Technology



- **Form extension junction**
- **Form sidewall spacer**
- **Recess Source/Drain by RIE**
- **Deposit In-Situ doped SiGe**

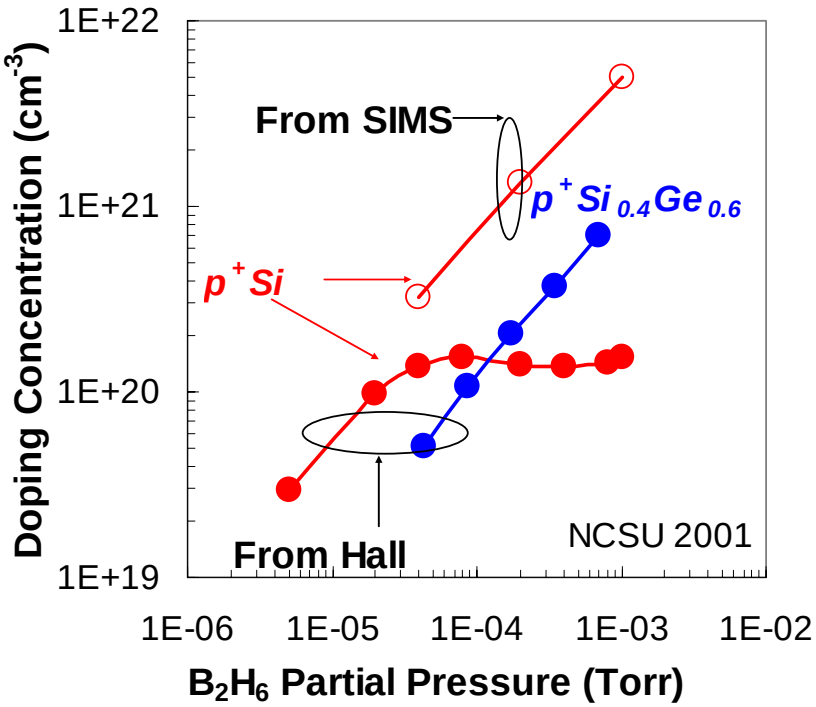


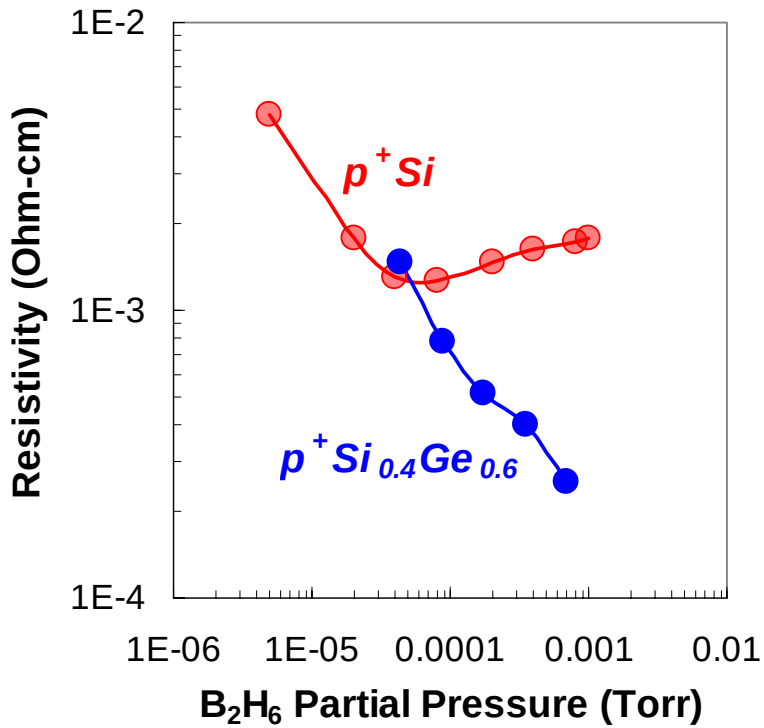
In-Situ Doped SiGe



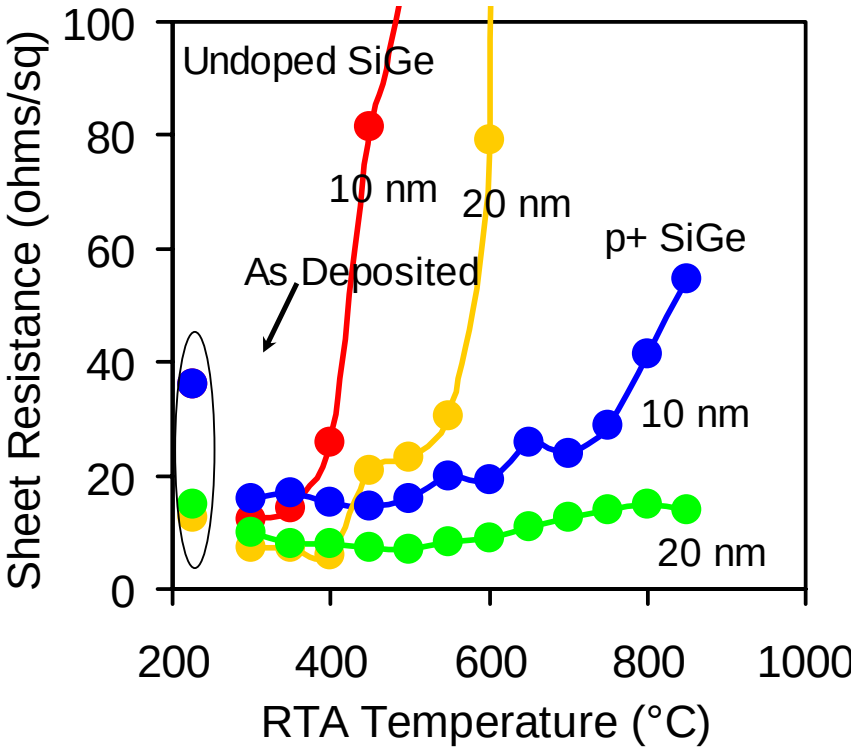
- **T = 500ºC Process**
  - *Dopant activation during growth*
  - *No activation anneal*
    - *No diffusion*
    - *Abrupt Junctions*
- **Very High Boron Activation**
  - *SiGeB alloy!*
  - *Small boron atoms play a similar role to carbon in SiGeC*
  - *Strain Compensation*
    - *Higher dopant activation*
    - *Larger bandgap*

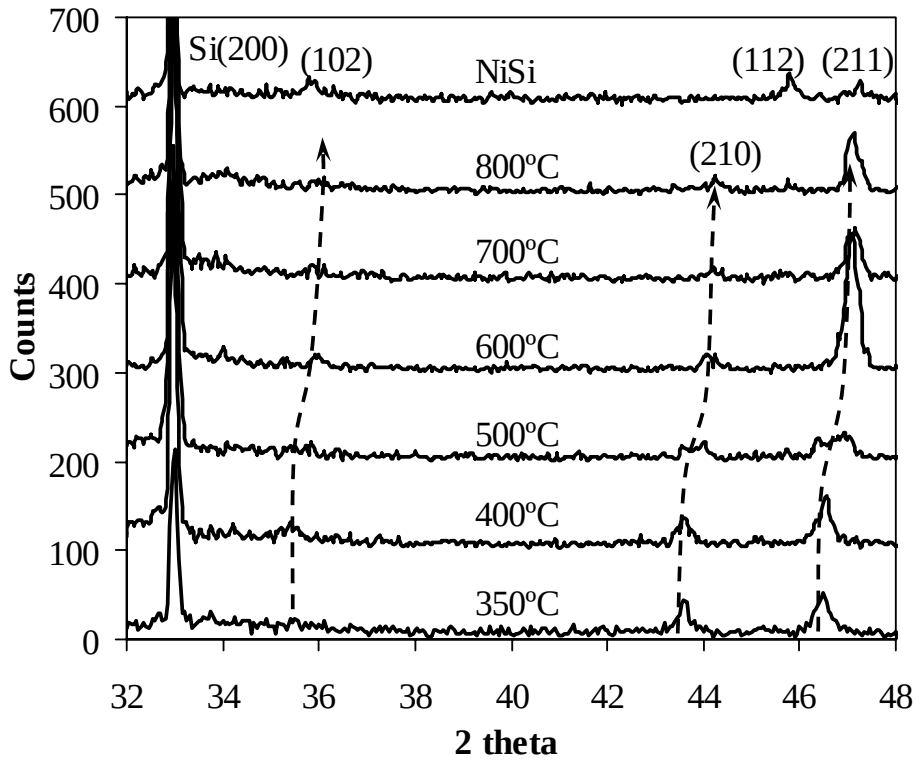
Boron Activation in SiGe





Nickel Germanosilicide Contacts to SiGe

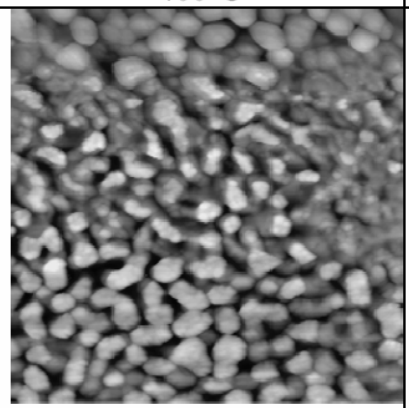
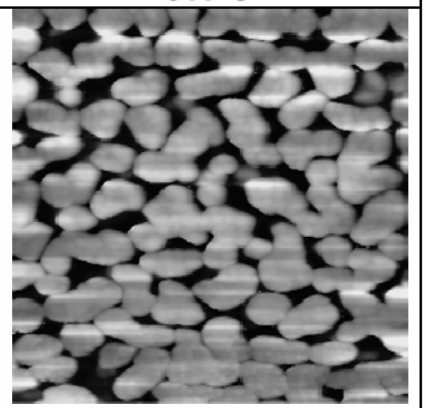
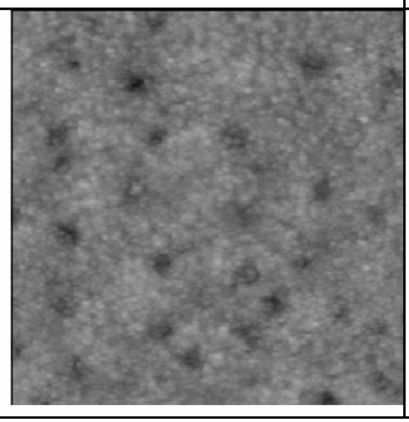
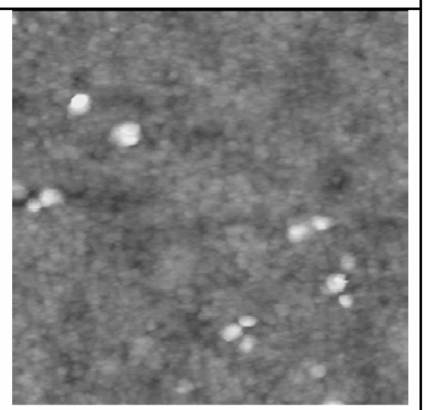




- **Above 400ºC, Ge atoms**
  - *Leave the germanosilicide grains and segregate at the grain boundaries*
- **Reason:**
  - *A large difference in the silicide and germanosilicide heat of formation*

NiSiGe/SiGe Interface Roughness

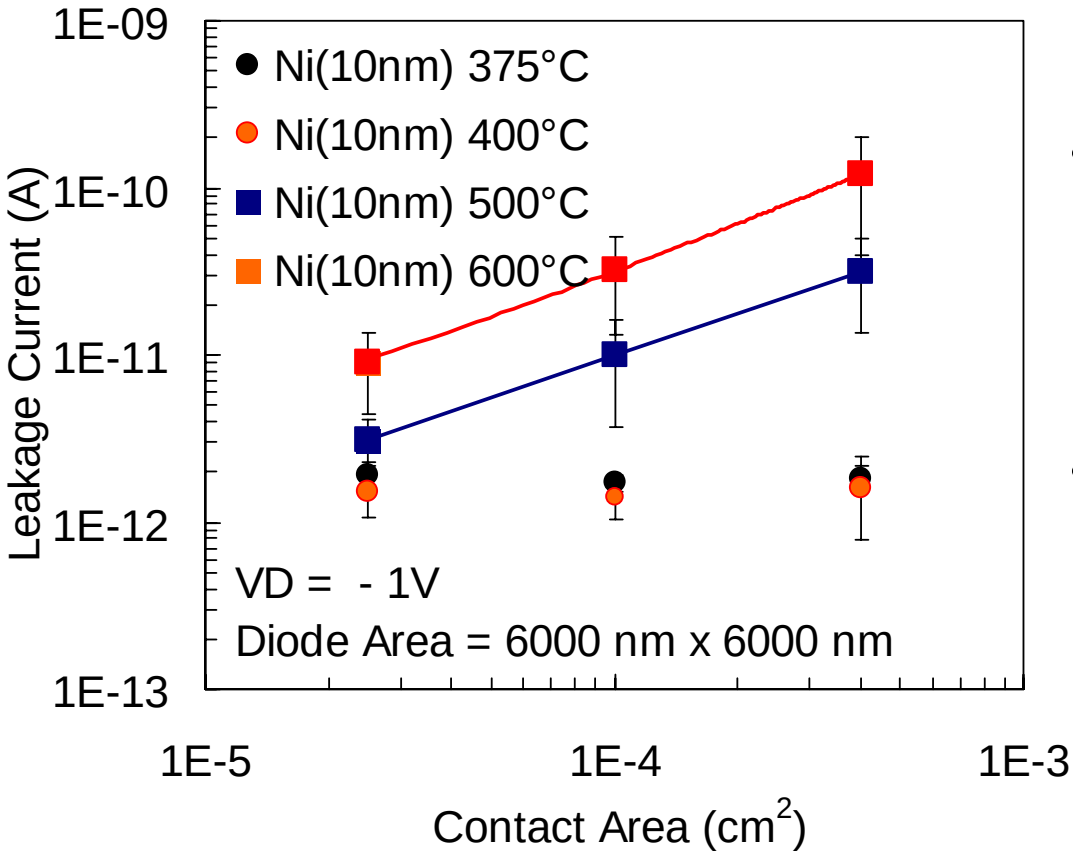
(*Atomic Force Microscopy*)

20nm Ni	400°C	500°C
On undoped $Si_{1-x}Ge_x$		
On heavily boron doped $Si_{1-x}Ge_x$		

AFM surface scans obtained after selective etching of NiSiGe in HF

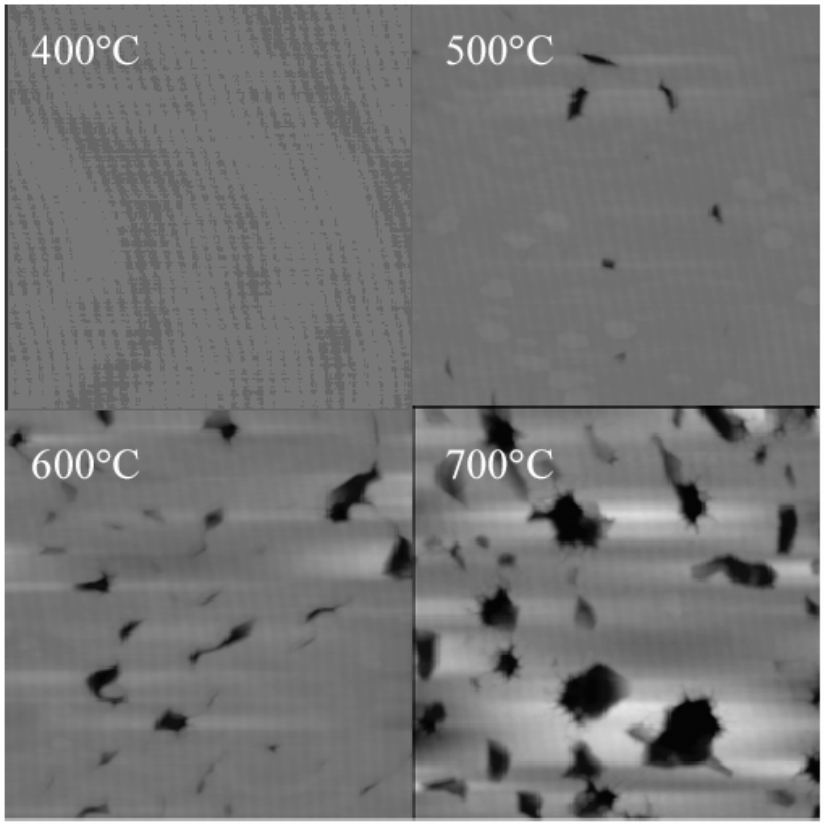
Junction Leakage

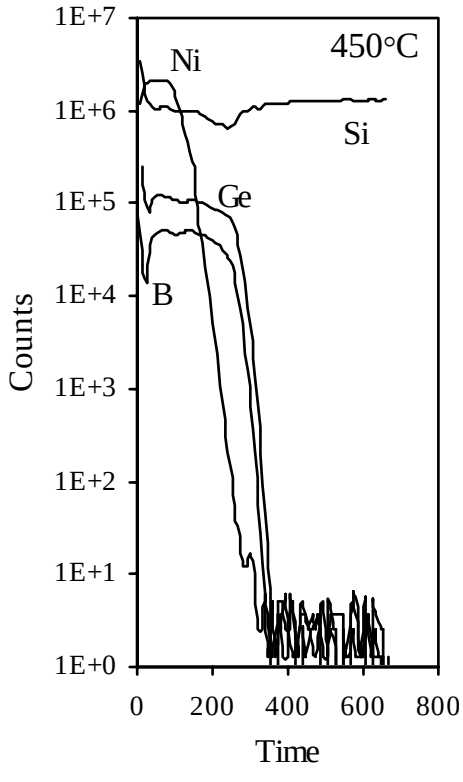
(*Same Active – Different Contact Area*)

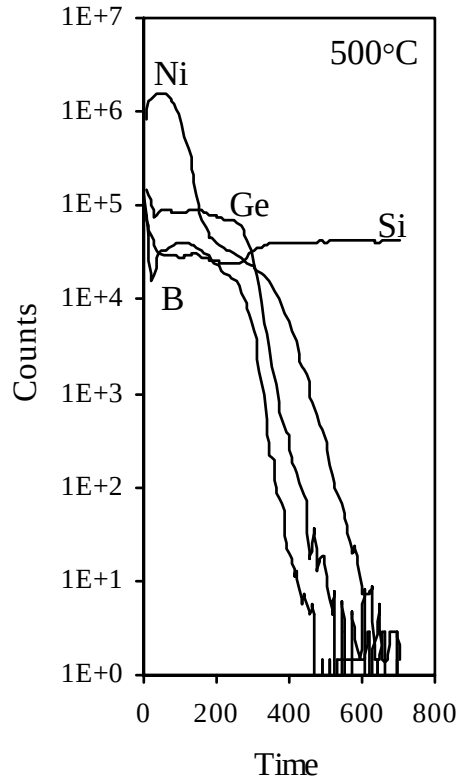


- **Junction leakage is independent of contact area at 375 and 400°C**
  - ***No Silicide induced leakage!***
- **Junction leakage increases with contact area at 500 & 600°C**

Si-SiGe Interface After Selective Etching of Germanosilicide and SiGe

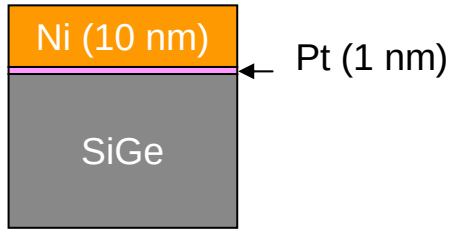


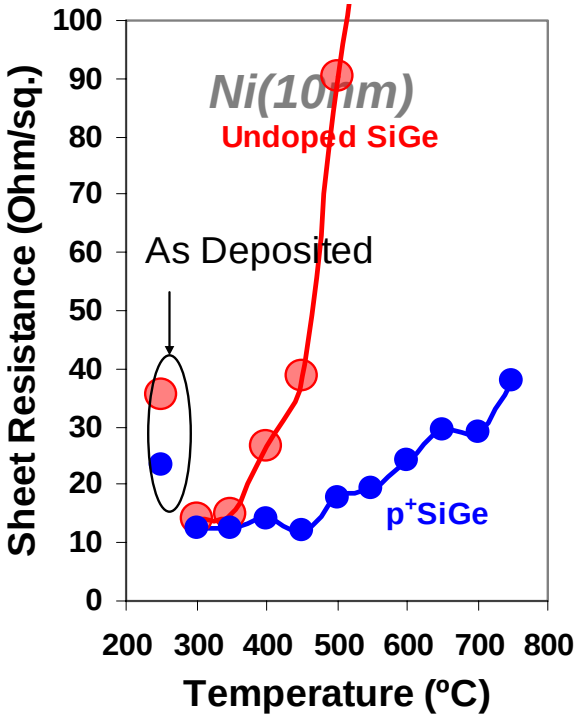


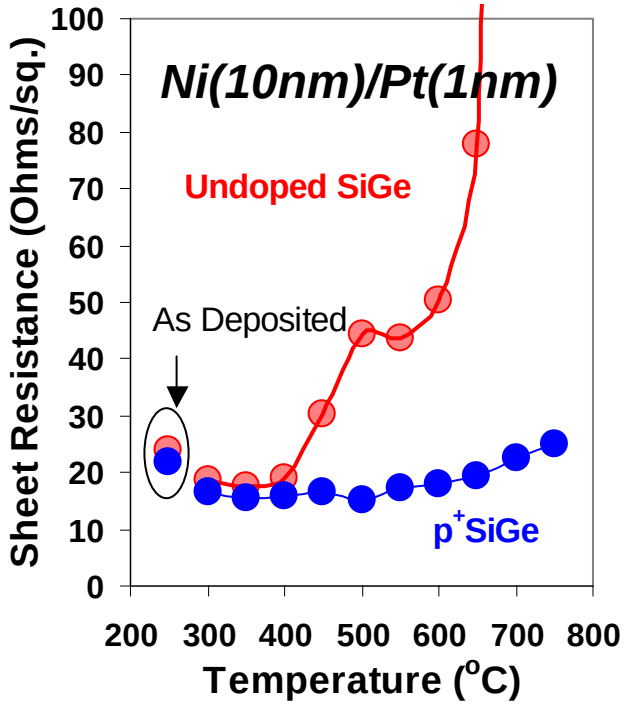


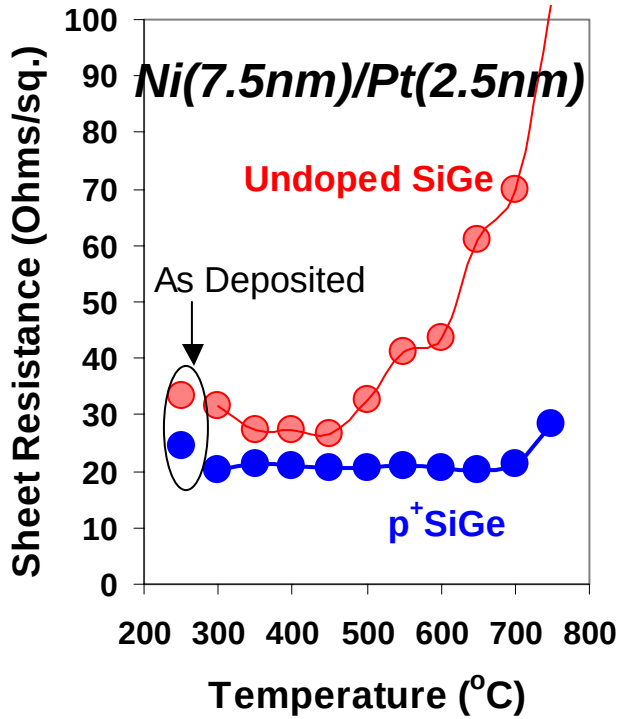
With the loss of Ge from the germanosilicide grains, Ni diffusion into the underlying SiGe results in NiSi spikes that extend deep into the substrate

Ni/Pt Germanosilicide



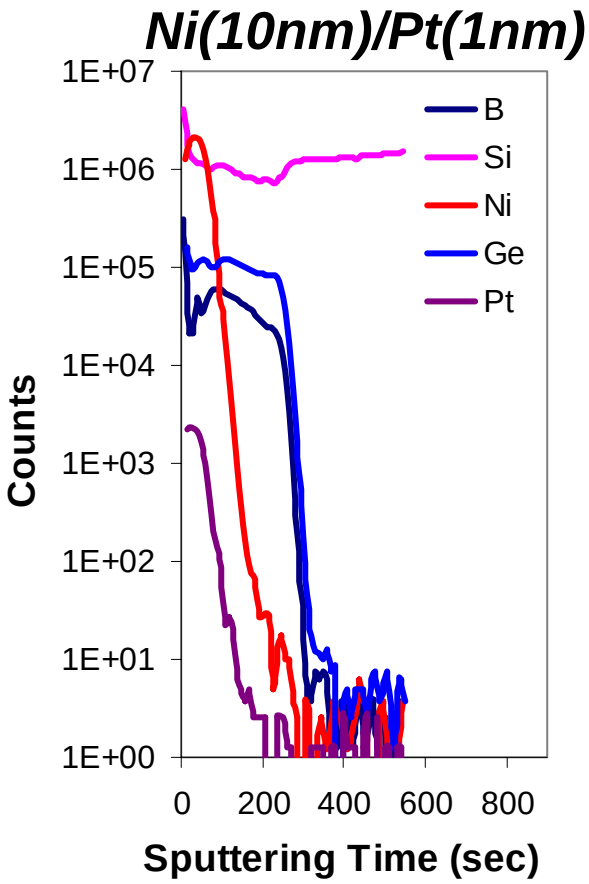


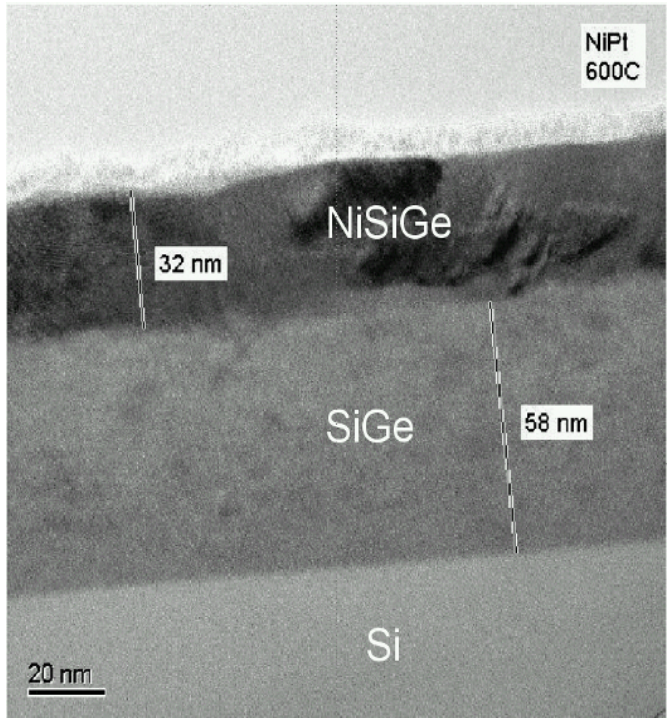




Sheet resistance thermal stability greatly improved
On p⁺ SiGe - sheet resistance of Ni(7.5nm)/Pt(2.5nm) is stable up to 700ºC

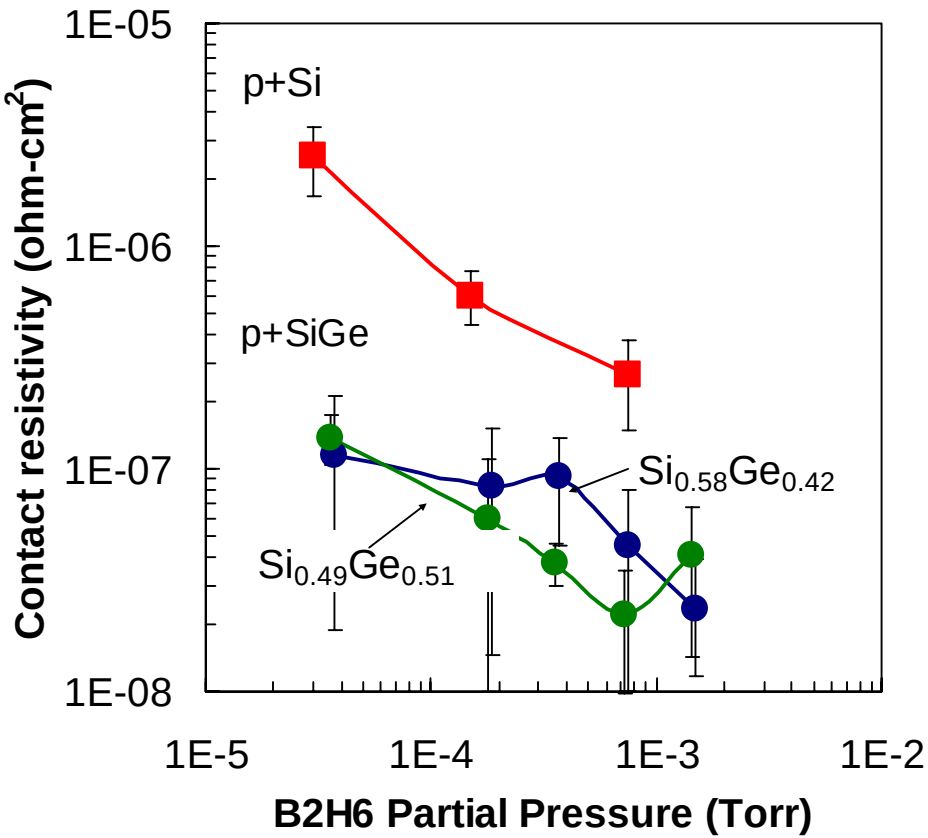
Ni/Pt Germanosilicide Interface





RMS Interface Roughness ~ 1 nm

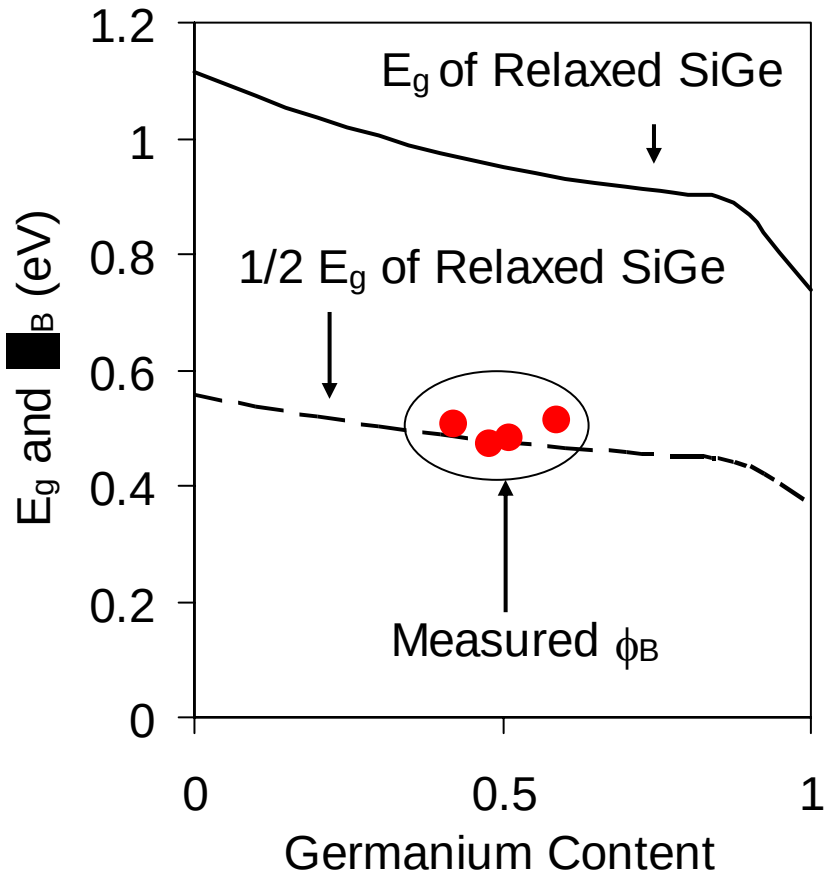
Contact Resistivity – NiSiGe



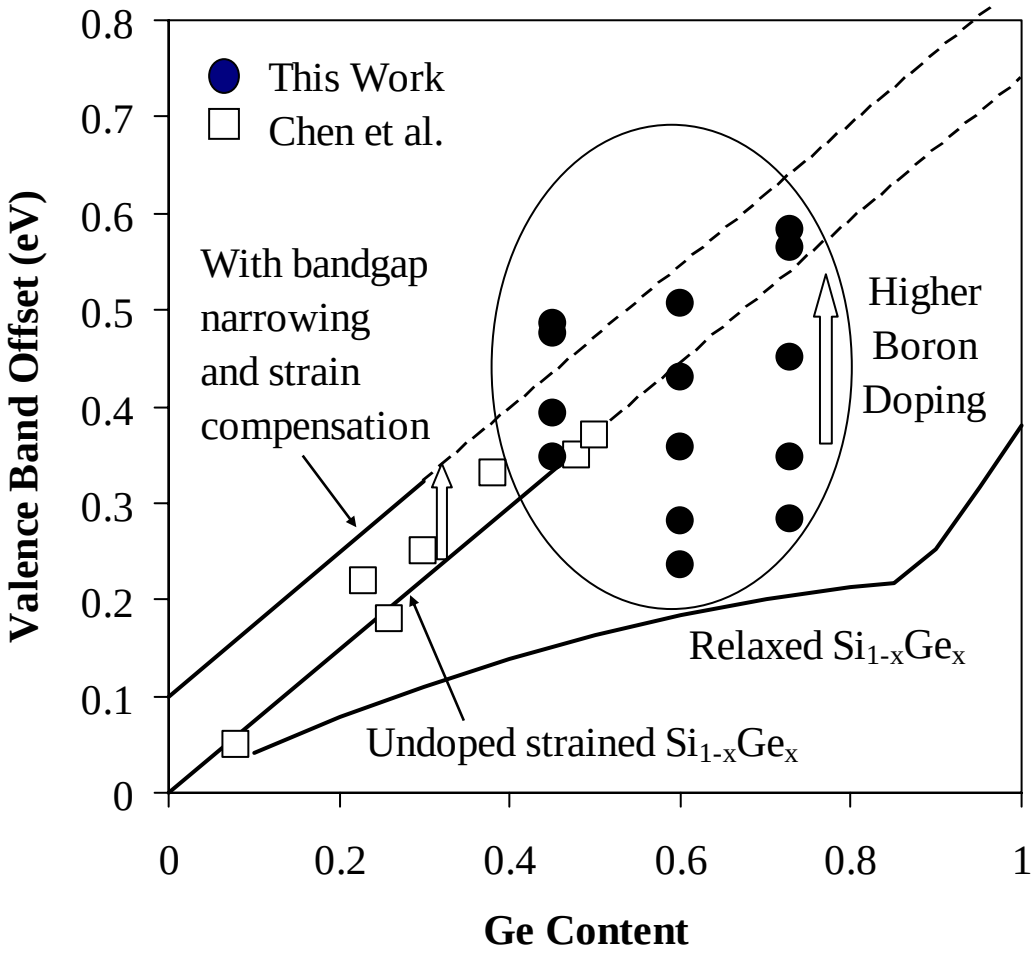
- **Contact Resistivity decreases with**
  - ***Doping Density***
  - ***Ge concentration***
- **An order of magnitude improvement is possible by using SiGe**
  - ***ρ_c = 10^{-8} ohm-cm^2 is possible***

Barrier Height

- **Fabrication:**
  - *Self aligned NiSiGe Contacts formed on Lightly doped SiGe*
- **Measurements:**
  - *Ge content by XRD*
  - *Barrier height from reverse bias I-V measurements*
- **Barrier Height (~ 0.5 eV)**
  - *Fermi level fixed relative to E_c?*
  - *ϕ_B ~ ½ Eg ?*
- **Bandgap**
  - *No bandgap narrowing*
  - *No boron strain compensation*



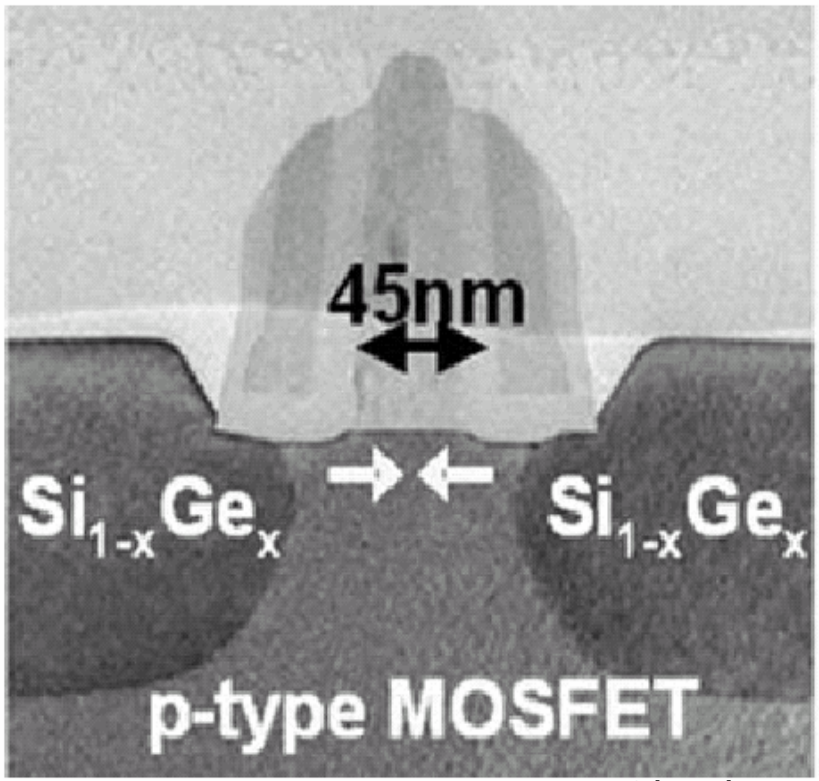
Si – SiGe Valence Band Offset
SiGe Bandgap = Si Bandgap - ΔE_v

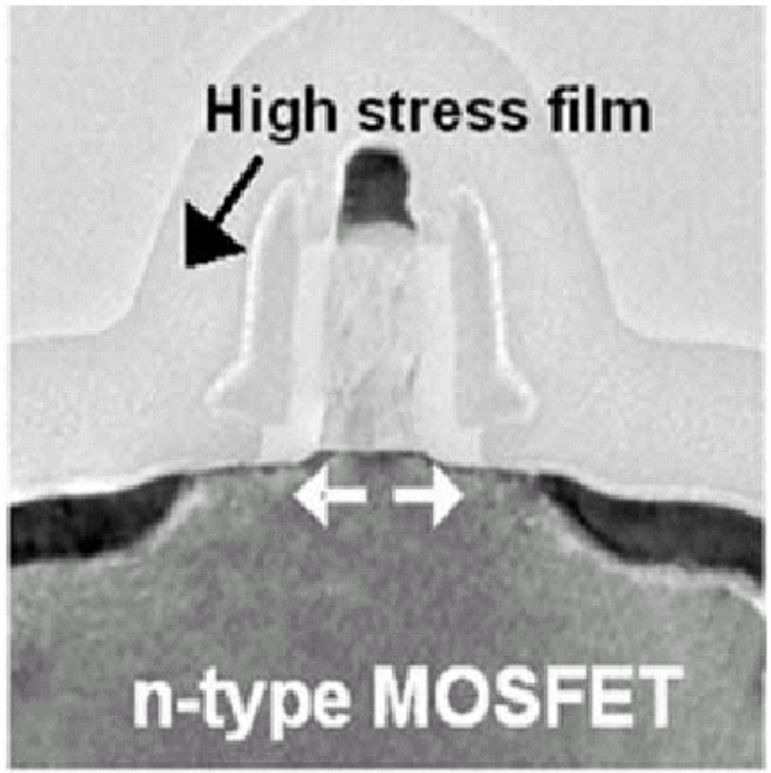


- **Heavy boron doping has a significant impact on SiGe bandgap**
- **Bandgaps equivalent to that of undoped strained SiGe can be obtained in thicker, p+ SiGe layers**
- **Both barrier height and high boron activation contribute to low contact resistivity**

Enhanced PMOS Mobility by Local Strain - Source/Drain Engineering

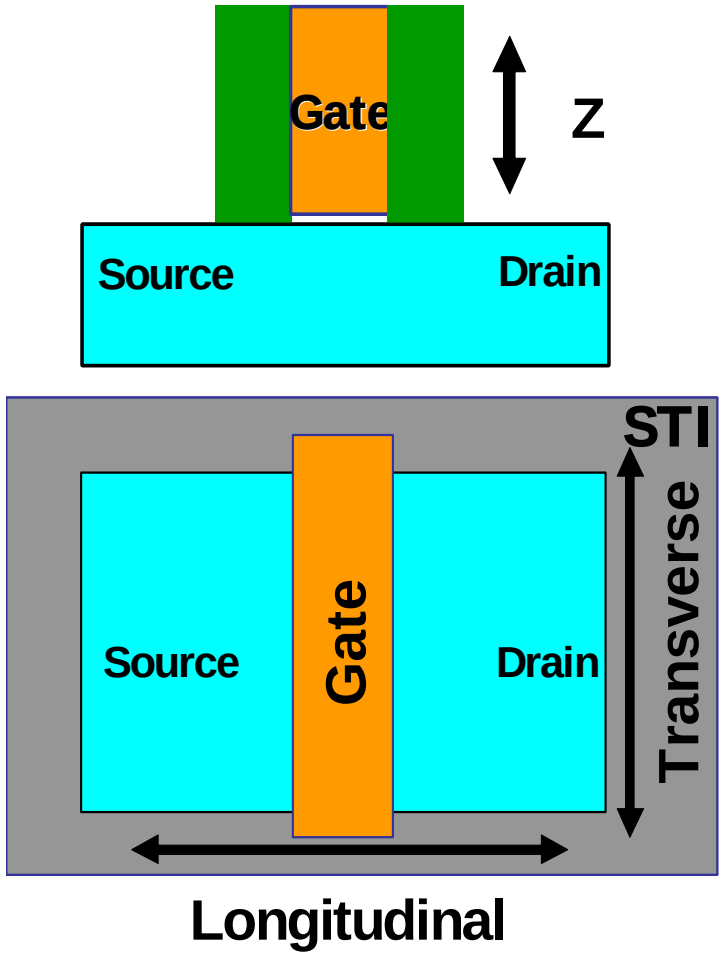
Local Strain – Enhanced Mobility
INTEL's 90 nm CMOS





T. Ghani et al., IEDM 2003
S. Thompson, EDL 2004

Desired Types of Uniaxial Stress

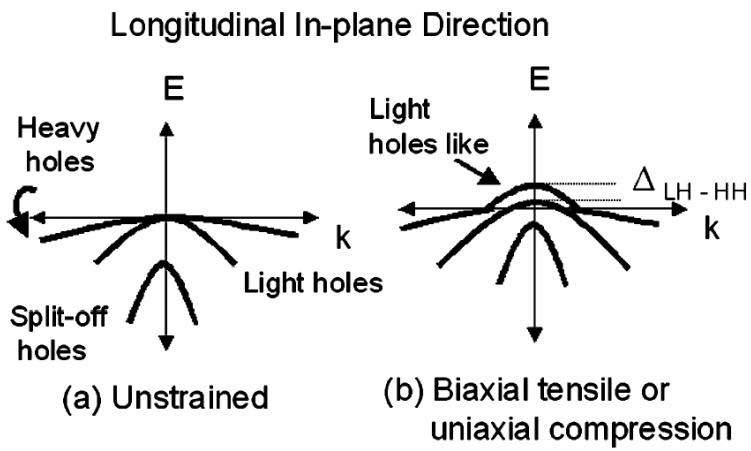


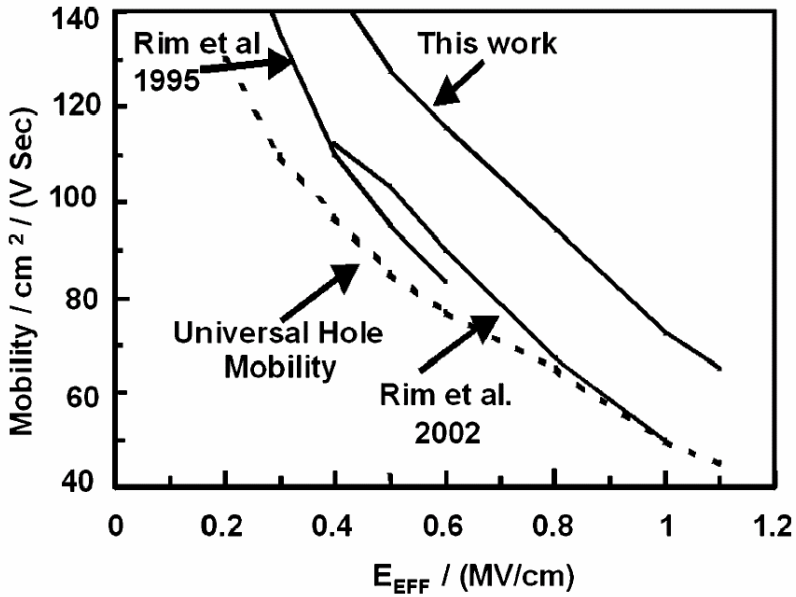
Desired Stress:

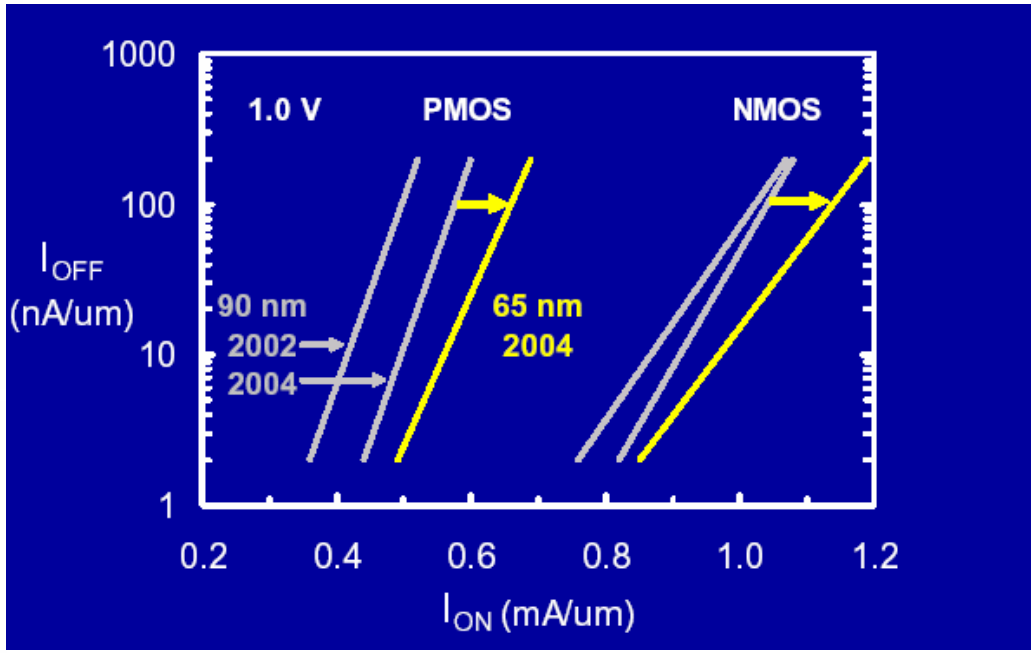
	Tran.	Long.	Z
pFET	T	C	T
nFET	T	T	C

T: Tensile stress
C: Compressive stress

PMOS Mobility





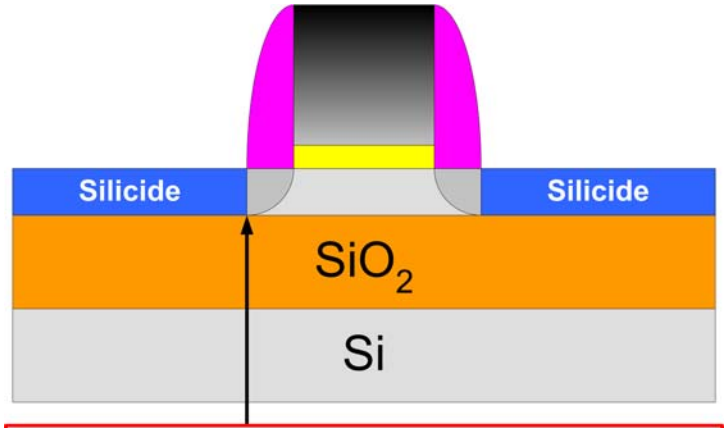


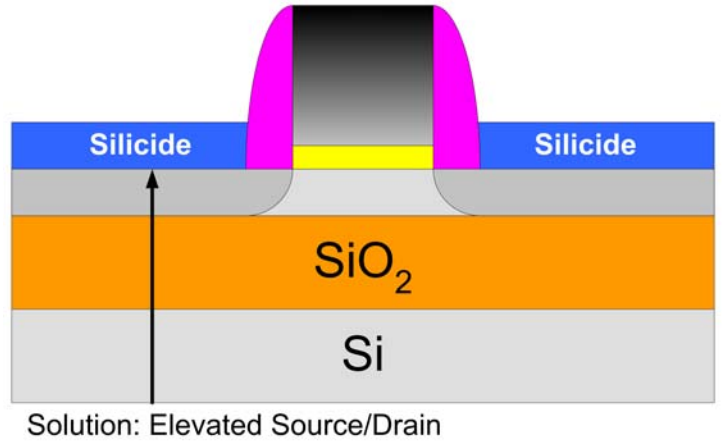
INTEL - August 2004

65 nm transistors exhibit 10-15% increase in drive current with enhanced strain

Fully-Depleted MOSFET Structures

Ultra-thin SOI MOSFET

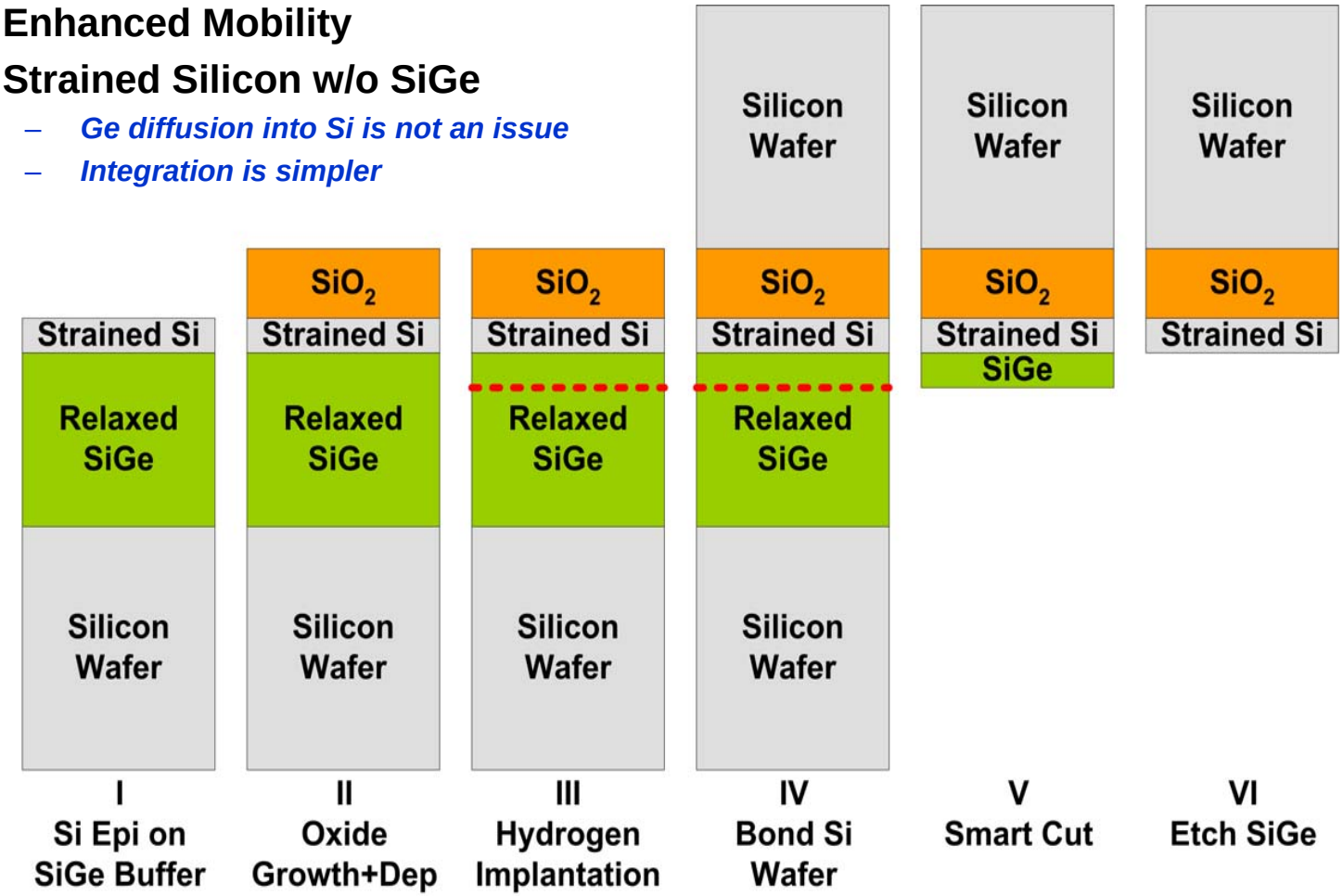




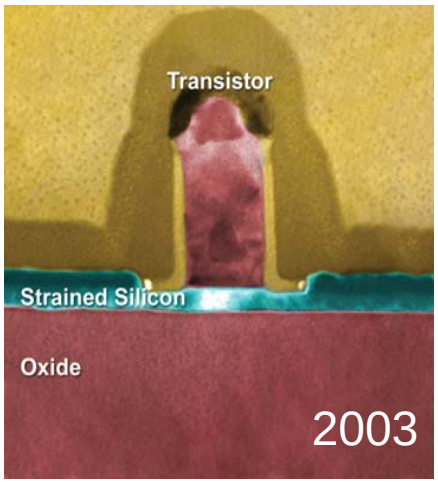
- **Advantages**
  - *Extension of existing architecture*
  - *Si thickness can be used to control the short-channel effects*
  - *Low Junction Capacitance*
  - *Steeper subthreshold slope*
- **New Source/Drain Challenges:**
  - *Silicide fully consumes the ultra-thin Si layer*
  - *Large contact resistance*
  - *High leakage*
- **Elavated source/drain is required**
  - *Epitaxy on ultra-thin silicon*
  - *Thermal Instability is a concern*

Strained Silicon Directly on Insulator

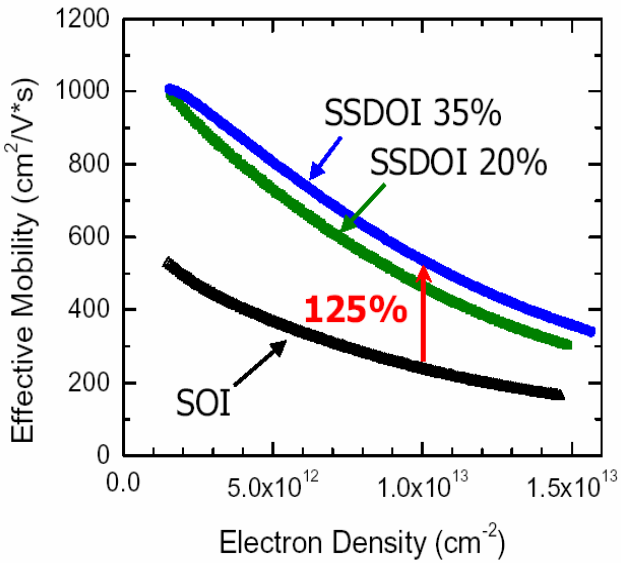
- Similar to Ultra-thin SOI
- Enhanced Mobility
- Strained Silicon w/o SiGe
  - *Ge diffusion into Si is not an issue*
  - *Integration is simpler*



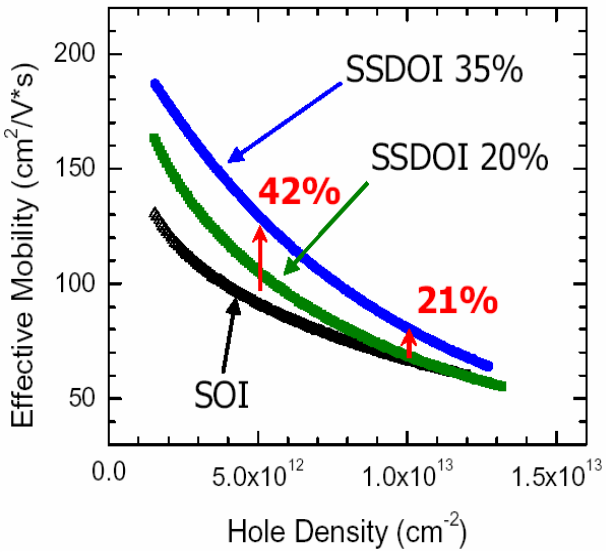
SSDOI Mobility– IBM



(a)

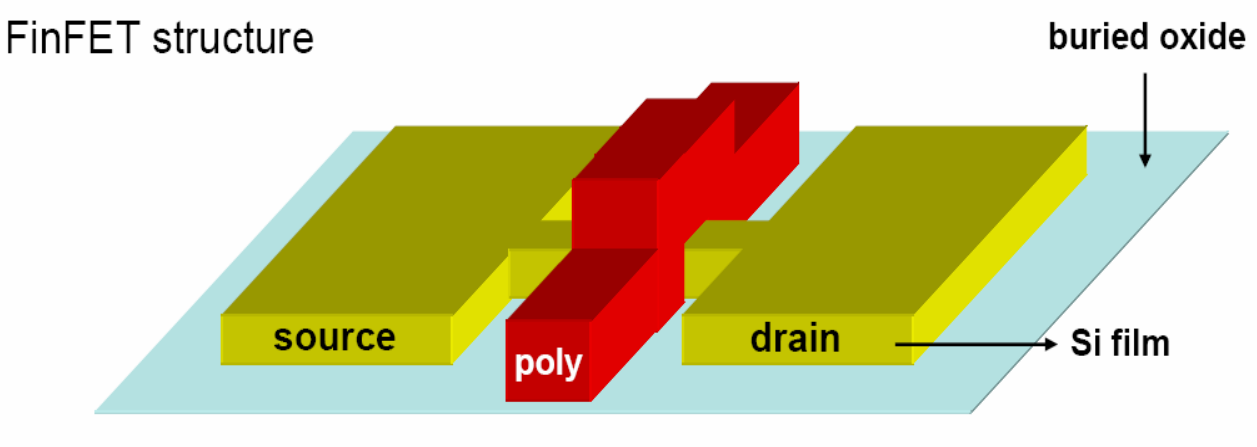


(b)



(c)

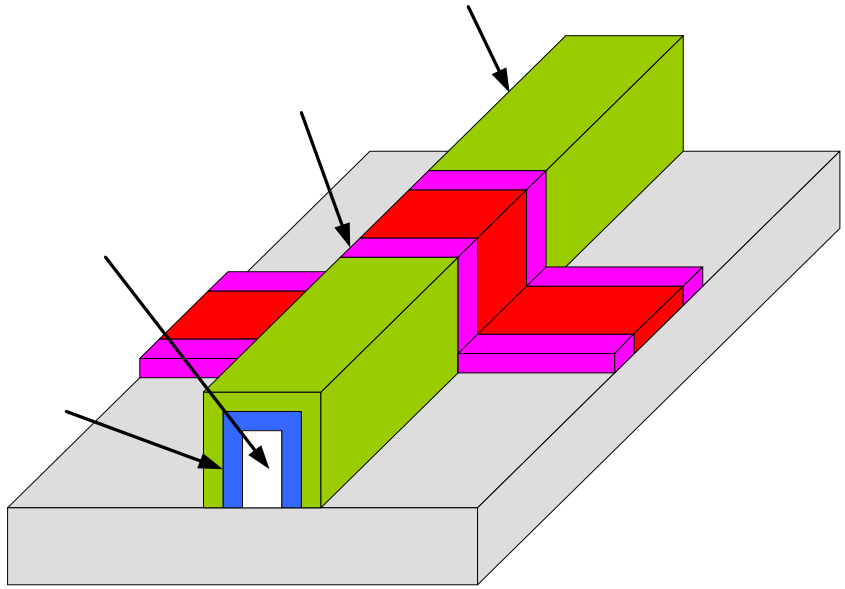
FINFET



- **Promising future!**
- **3-D Silicon on Insulator Technology**
- **Fully-Depleted, Double Gate MOSFET**

FINFET Source/Drain Engineering

- **Extension Resistance:**
  - *Narrow fin - large resistance under the spacer*
  - *Similar to ultra-thin SOI*
- **Contact Resistance**
  - *Silicide should not be allowed to consume the fin*
  - *The fin should be expanded in all three directions*
  - *Novel contacting solutions will still be necessary for low contact resistance*
    - *SiGe epi instead of Si*
    - *Dual metal contacts*



FINFETs with Raised Source/Drain

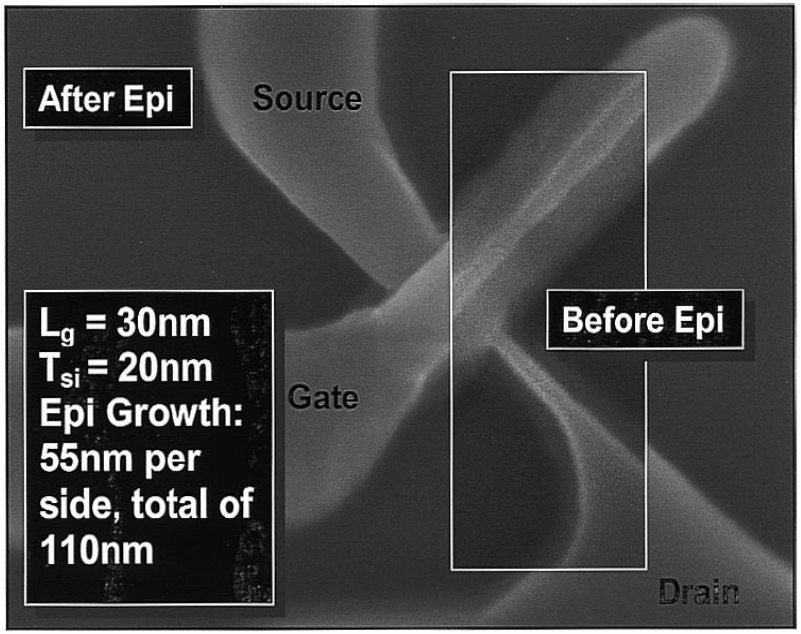
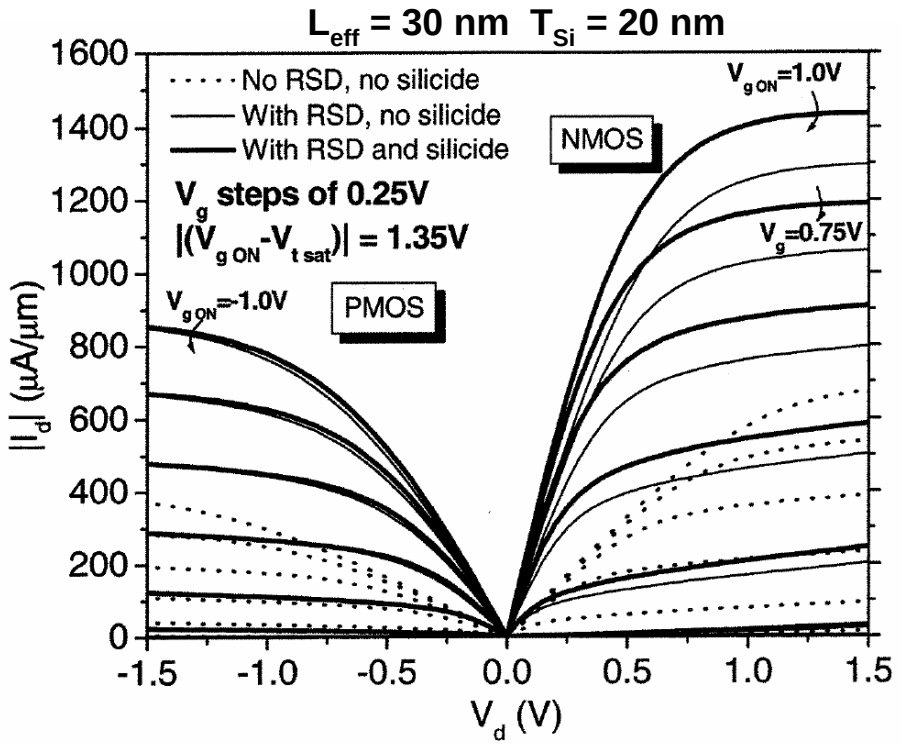


Fig. 7. Top down SEM micrograph, of ⟨100⟩ FinFET before and after selective Si epitaxy. Device measurements: $T_{si} = 20$ nm, $L_{poly} = 30$ nm, 55 nm of silicon was grown selectively on each side of the fin.



Without Raised Source/Drain the series resistance is too large!

Kedzierski et al., IBM, IEEE-TED, 2003

Summary

- **Parasitic series resistance is a grand challenge for future CMOS generations**
  - ***Contact and Overlap Resistances are the key contributors***
- **Silicon-Germanium Source/Drain Technology can provide:**
  - ***Local Strain for Enhanced Mobility***
  - ***High boron activation and small barrier height for low-contact resistivity***
  - ***Low-temperature processing for compatibility with high-k dielectrics and metal gate electrodes***
  - ***Abrupt Junctions for small overlap resistance***
  - ***Elevated source/drain for fully depleted MOSFETs with ultra-thin Si channels***