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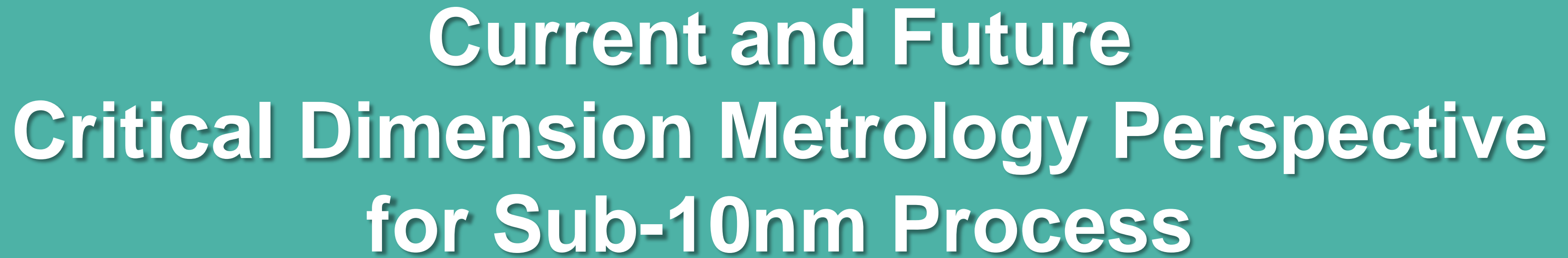

Current and Future Critical Dimension Metrology Perspective for Sub-10nm Process

Mar/23/2017

Mari Nozoe
Business Strategy Planning Division
Electronic Device Systems Business Group

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Technology Trend of Advanced Devices

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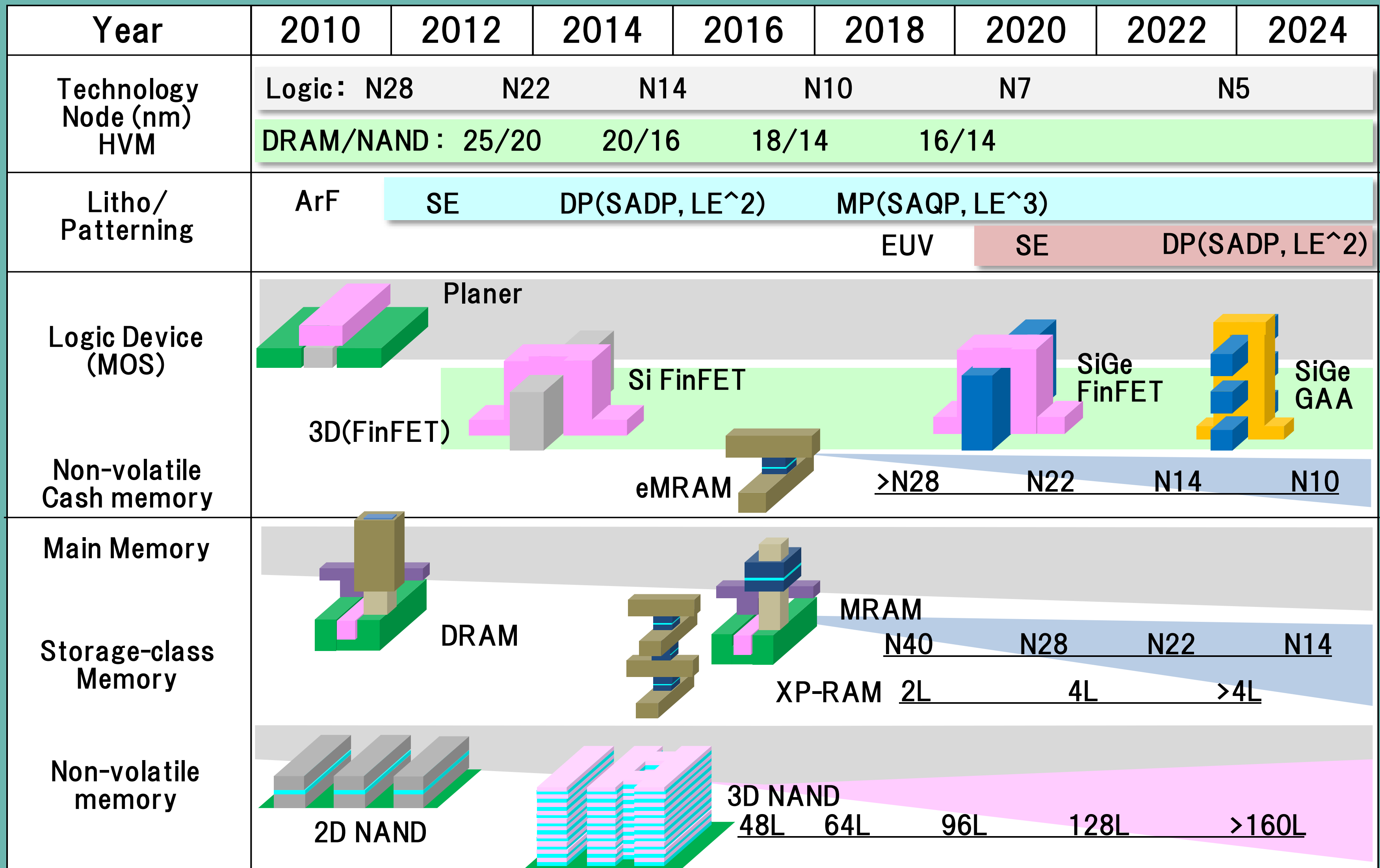

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FCMN 2017 Mari Nozoe

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Evolution in Structure, Process and Material

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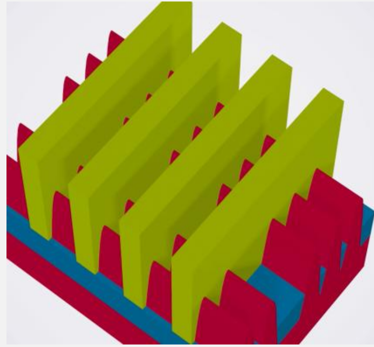
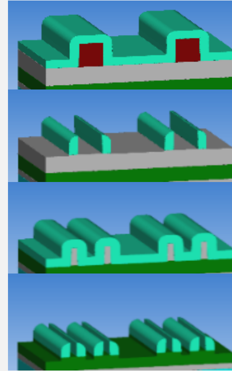
FinFET



Multi-Patterning



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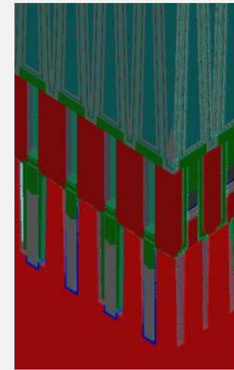
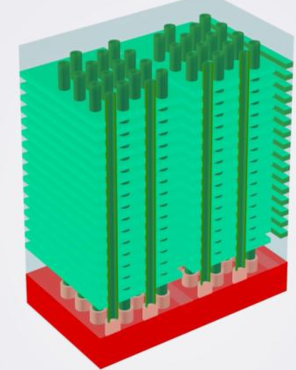
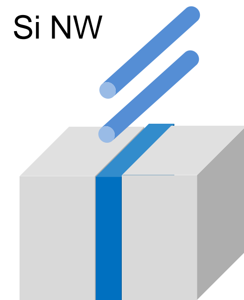


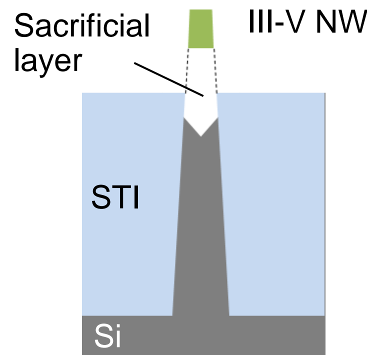
3D-NAND



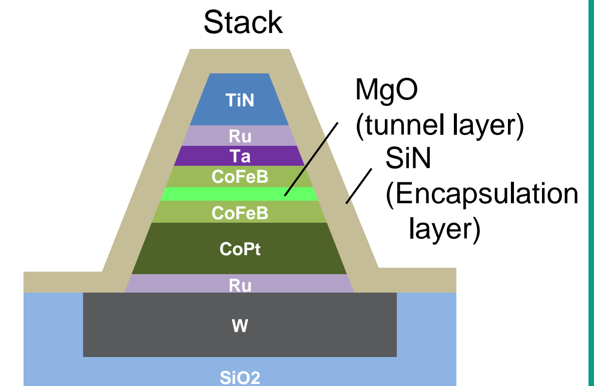
Nano-wire, GAA



High-Mobility NW



MRAM



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Evolution in Structure, Process and Material

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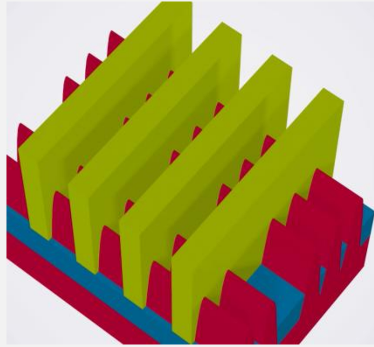
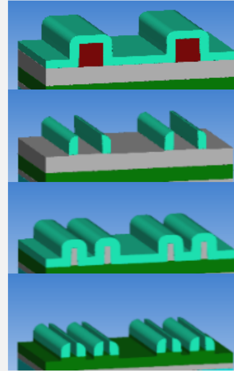
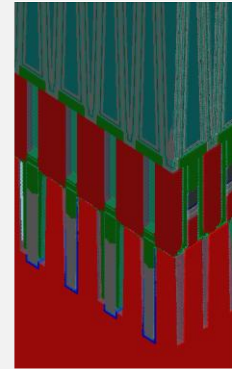
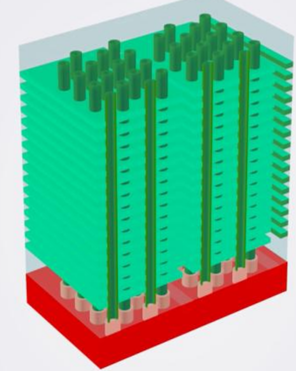
FinFET	Multi-Patterning	DRAM	3D-NAND
			

- CD Metrology
  → EPE Metrology
- LER, LWR
  PSD analysis
- HAR feature
  Bottom , profile
  measurement
- Pattern Fidelity
  Analysis
- Overlay
  (in die, layer to layer)
- Precision
  < 0.1nm
- Massive
  Measurement

PSD: Power Spectrum Density

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CD Metrology Overview

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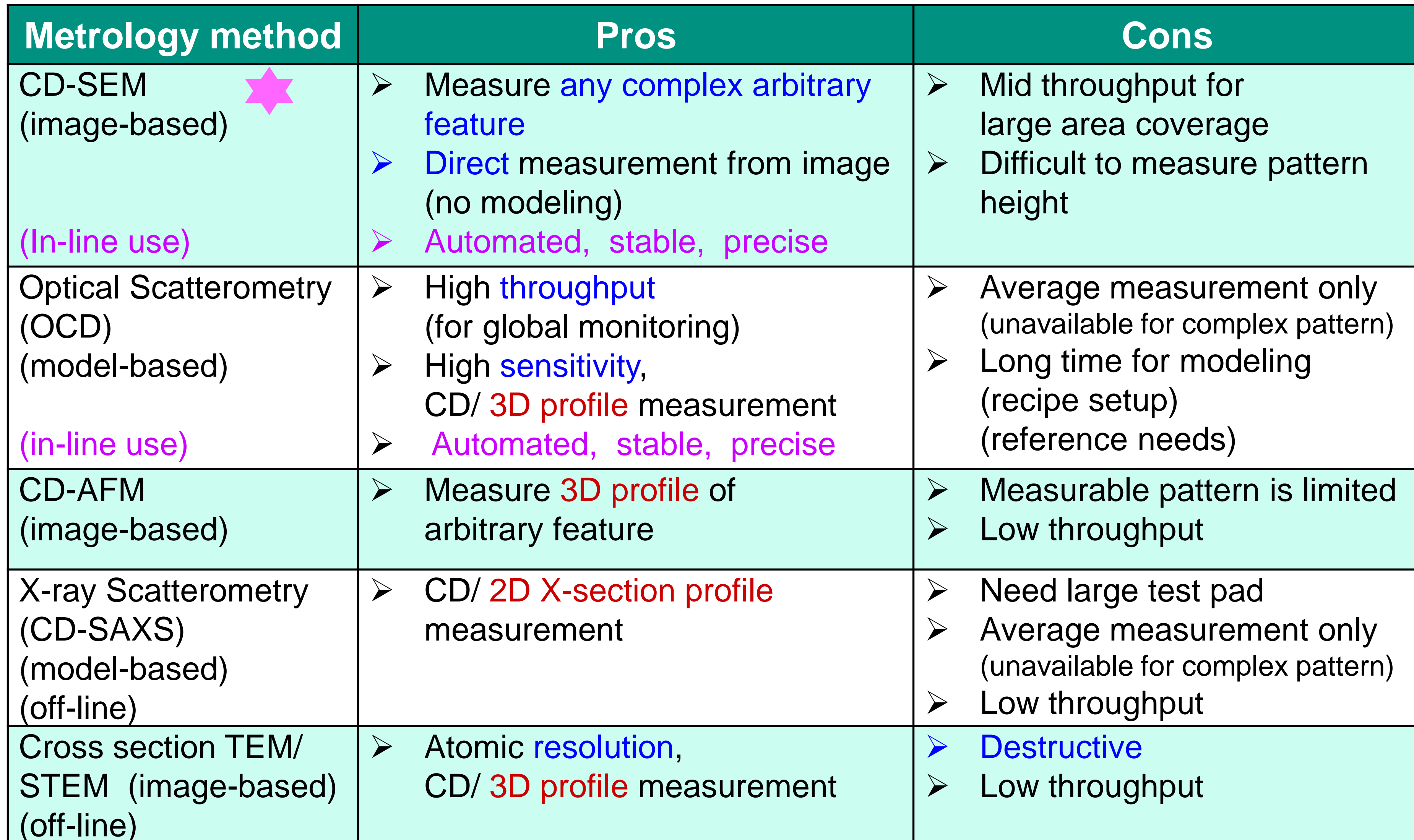

Metrology method	Pros	Cons
CD-SEM (image-based) (In-line use)	➢ Measure any complex arbitrary feature ➢ Direct measurement from image (no modeling) ➢ Automated, stable, precise	➢ Mid throughput for large area coverage ➢ Difficult to measure pattern height
Optical Scatterometry (OCD) (model-based) (in-line use)	➢ High throughput (for global monitoring) ➢ High sensitivity, CD/ 3D profile measurement ➢ Automated, stable, precise	➢ Average measurement only (unavailable for complex pattern) ➢ Long time for modeling (recipe setup) (reference needs)
CD-AFM (image-based)	➢ Measure 3D profile of arbitrary feature	➢ Measurable pattern is limited ➢ Low throughput
X-ray Scatterometry (CD-SAXS) (model-based) (off-line)	➢ CD/ 2D X-section profile measurement	➢ Need large test pad ➢ Average measurement only (unavailable for complex pattern) ➢ Low throughput
Cross section TEM/ STEM (image-based) (off-line)	➢ Atomic resolution, CD/ 3D profile measurement	➢ Destructive ➢ Low throughput

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EPE Metrology
&
Pattern Fidelity Analysis

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CD metrology → EPE Metrology

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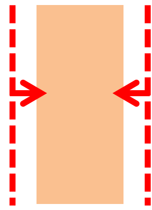
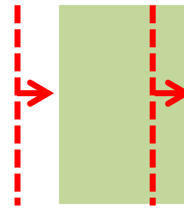
Edge Placement Error $\sigma^2_{EPE} = \sigma^2_{CD} + \sigma^2_{OVL} + \sigma^2_{LCDU}$

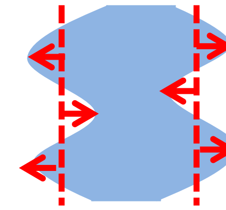
CD, Space, Pitch



OVL

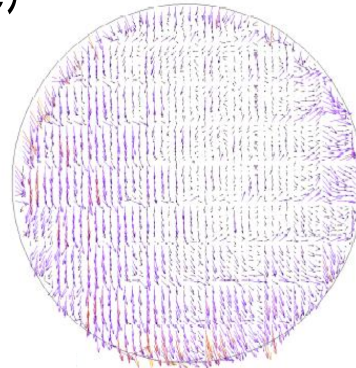


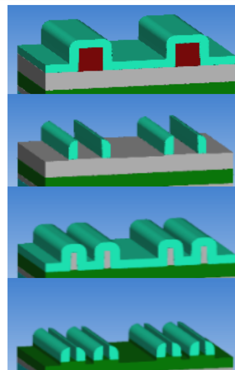
LCDU, Pattern Fidelity

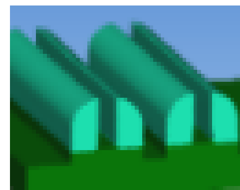


global (average)

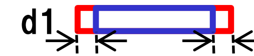
local





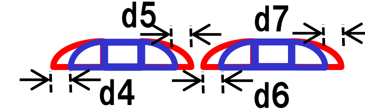


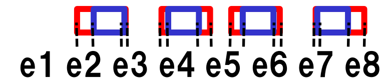
1st litho



1st side wall

2nd side wall





MNC 2016, Y. Momonoi, H. Fukuda

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Pattern Fidelity Analysis

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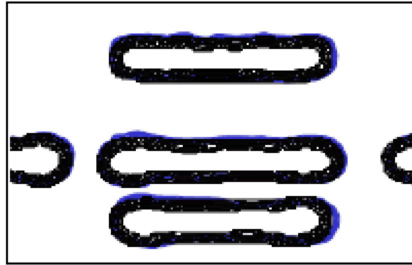
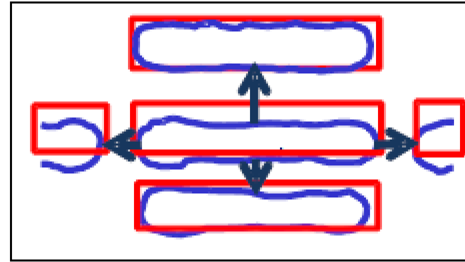
Measurement of Every Pattern in FOV

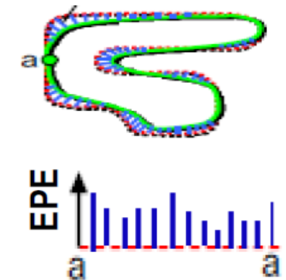
Extract contour from SEM image



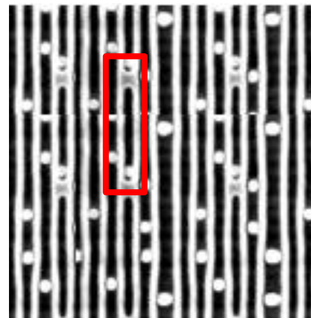
Design matching

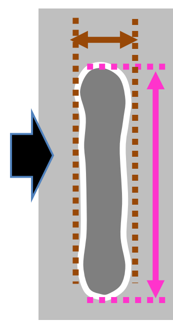


Edge Place Analysis

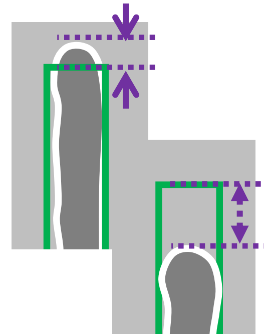


Measurement Value

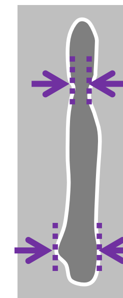




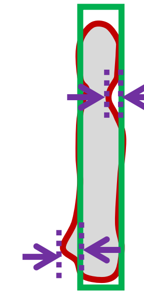
Size(X,Y)



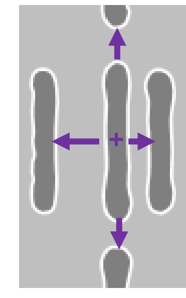
Push out/
Pull back



Max CD/
Min CD



Protrusion/
Necking



Tip-to-tip/
Side-to-side

2016 March, Hitachi Review Vol 65

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Pattern Fidelity Analysis

Logic/ SRAM Metal-1
(Target Design) MA/MB

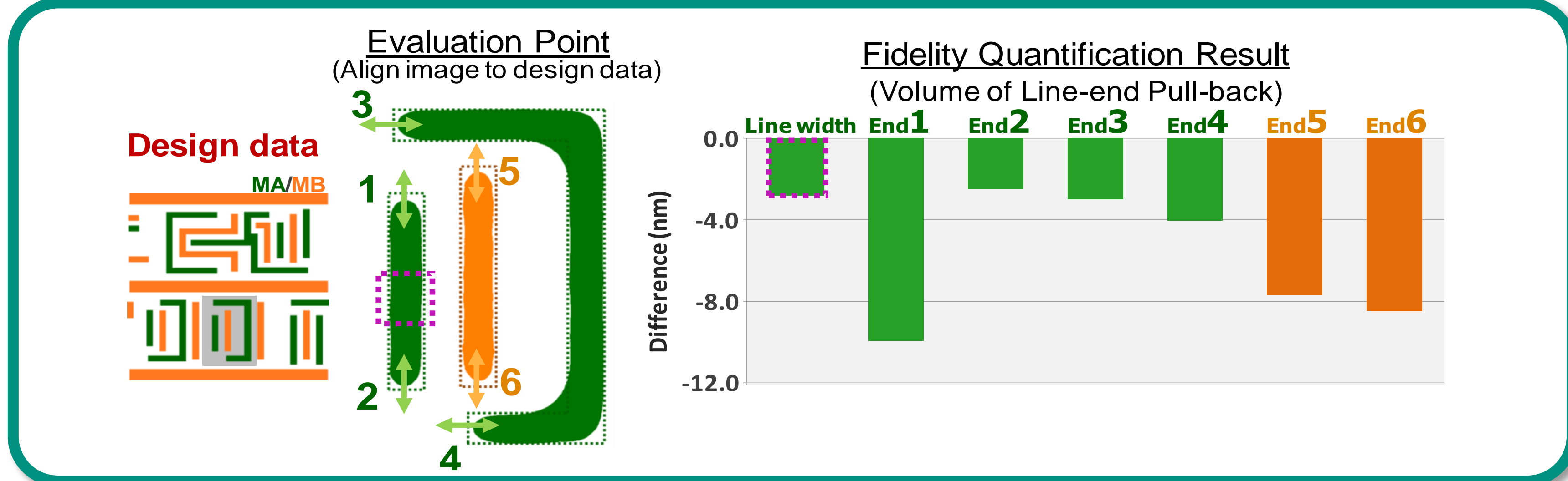
Patterns after Final Etching
(Pattern Contour) MA/MB

Lower Layer Pattern

Push-out Case

Line-end Pull-back:
Risk for Missing Connection

Line-end Push-out:
Risk for Leak-current



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EPE Analysis of Metal 1 Block

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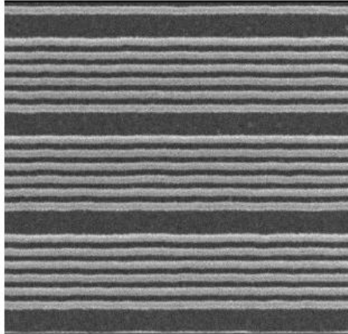
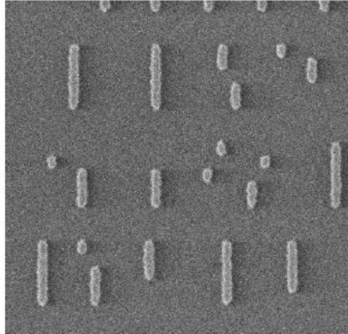
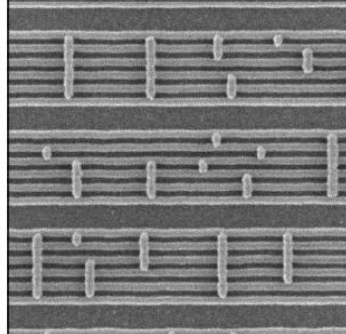
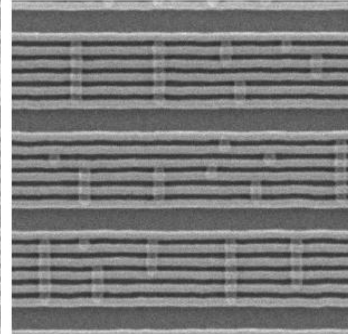
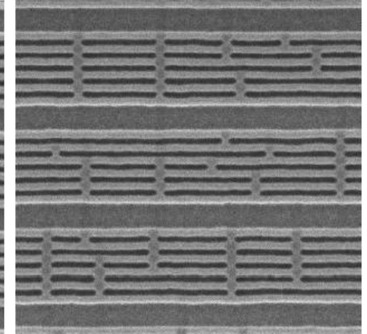
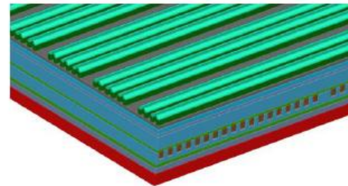
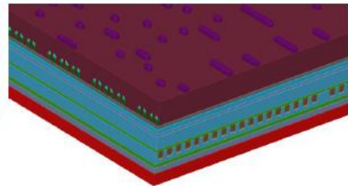
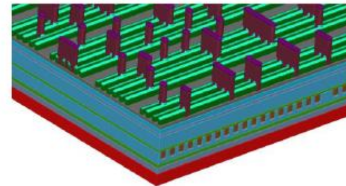
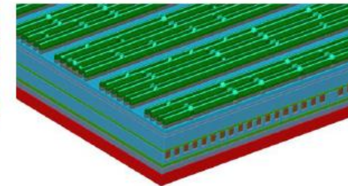
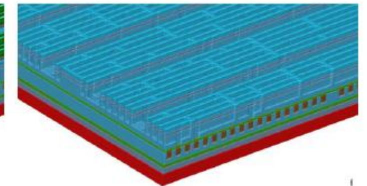
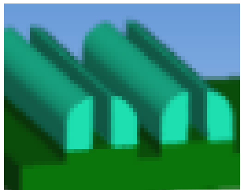
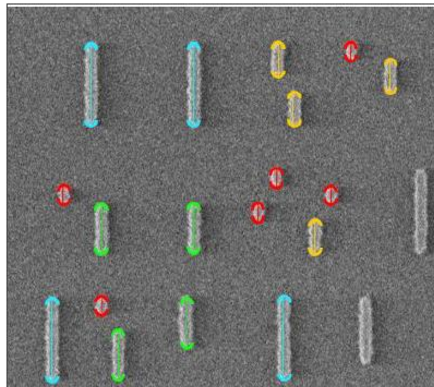
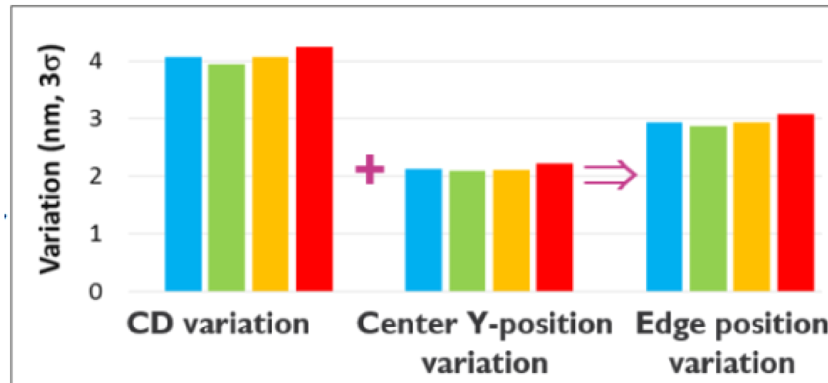
Especially important for multi-patterning (spacers and block)

P32 spacers on TiN | Block litho on SoC | SoC etch | TiN etch | Low-k etch

L1 L2 L3 L4

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2016.Nov, Greg McIntyre
Patterning and Lithography update

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Line/Space CD Variation Analysis of Metal 1 Trench

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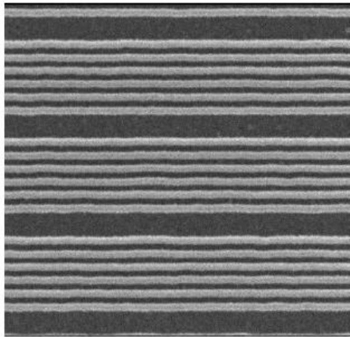
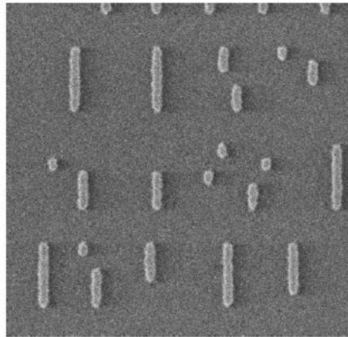
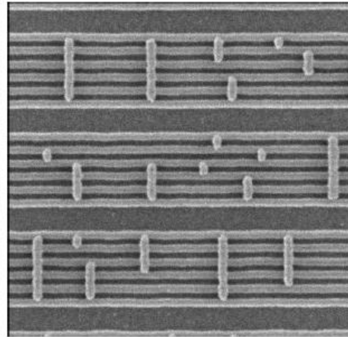
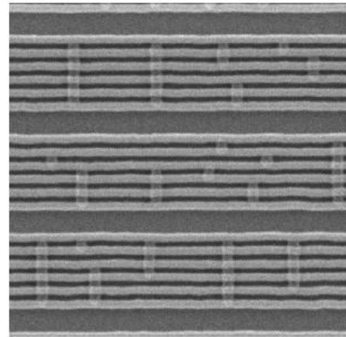
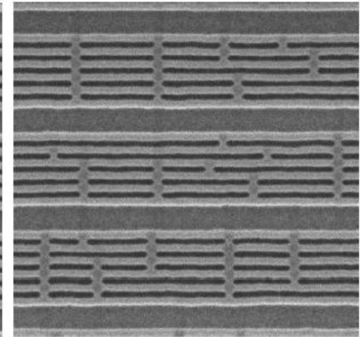
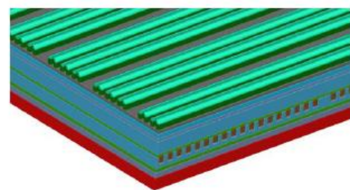
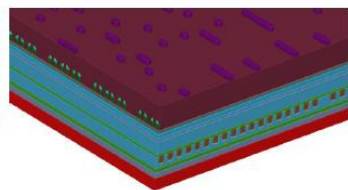
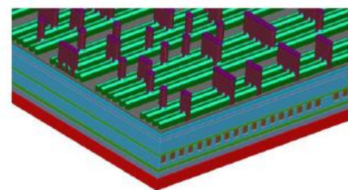
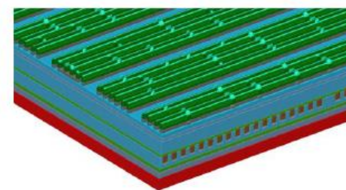
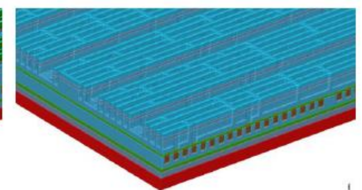
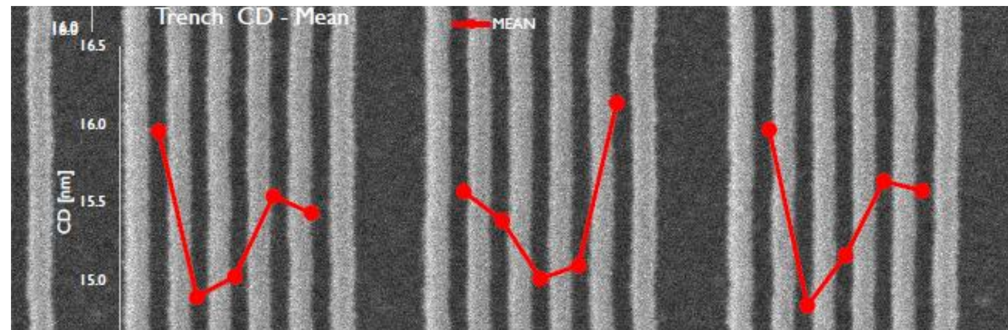
Pitch walking measurement require to identify each line and space

P32 spacers on TiN	Block litho on SoC	SoC etch	TiN etch	Low-k etch
				
				



2016.Nov, Greg McIntyre
Patterning and Lithography update

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Overlay Metrology

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Overlay Requirement

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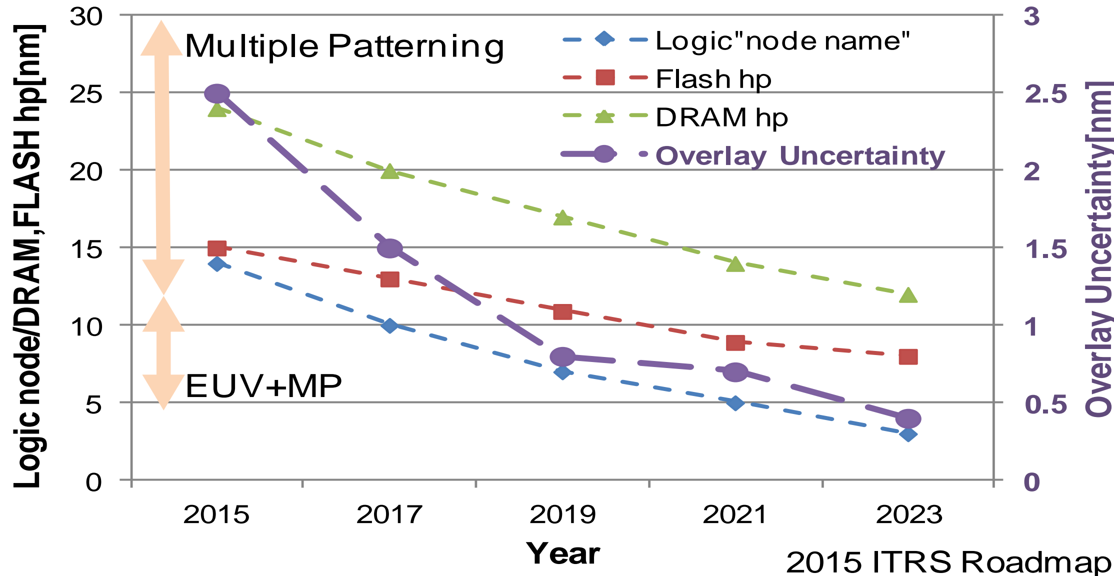
In-die device feature, control <1nm, layer-to layer



2015 ITRS Roadmap

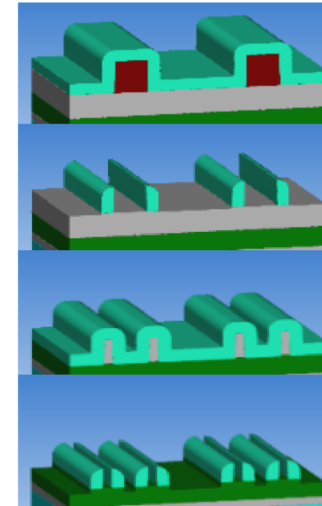
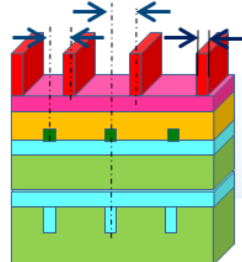
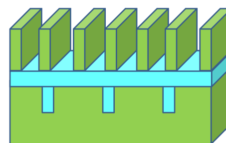


Photo resist patterning
- Optical overlay measurement
- SEM based Overlay measurement



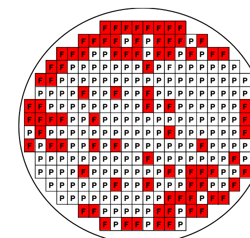
Etching
- Optical overlay measurement
- SEM based Overlay measurement

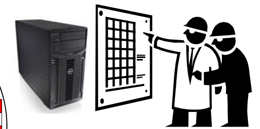
2016SPIE[9778-47]



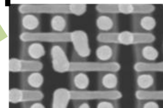
Scanner

Prove Test+ Root Cause Analysis





Decap



SPIE 2017, Kazuhisa Hasumi
SEM based overlay measurement between Via patterns and buried M1 patterns using high voltage SEM

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High-precision, layer-to-layer overlay

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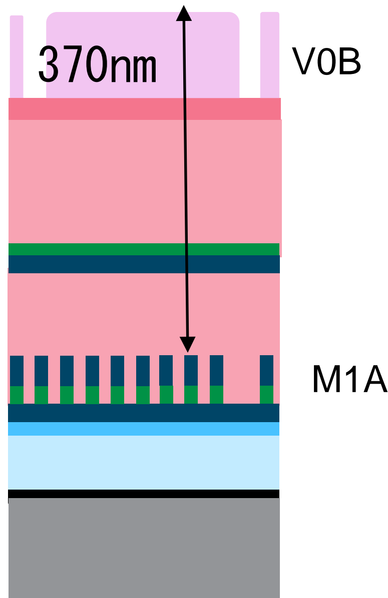
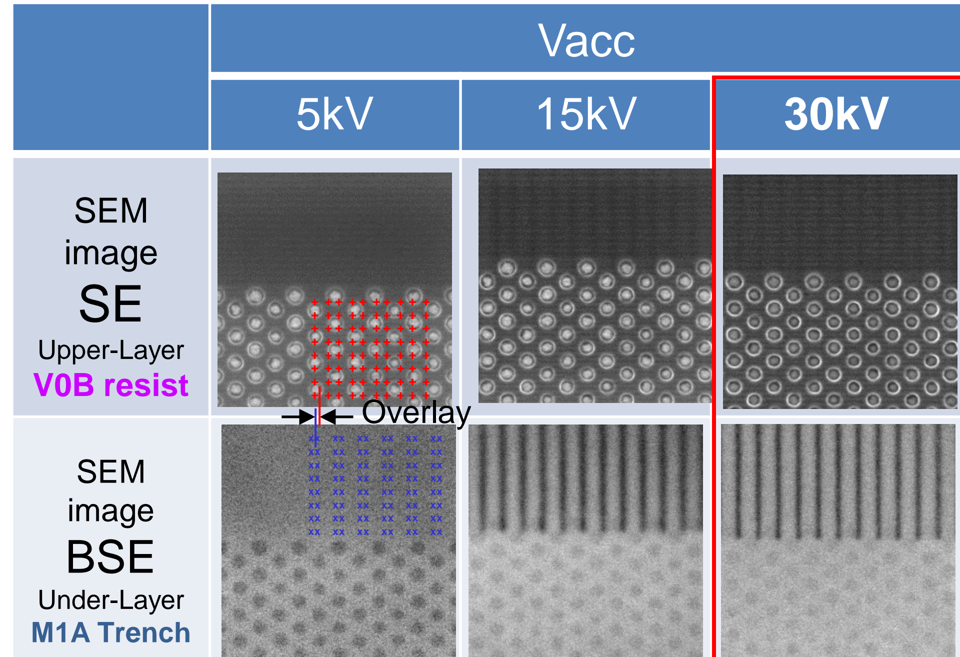
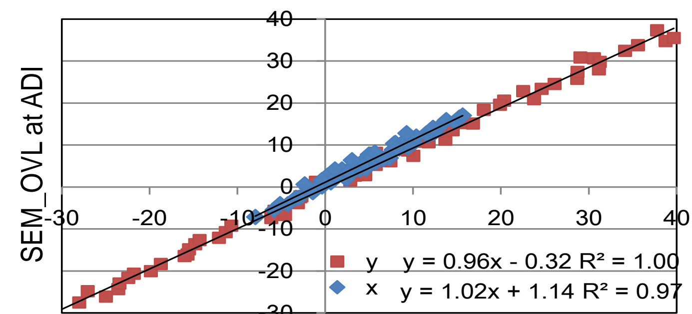




With high voltage SEM (HV_SEM),

1) Actual device pattern, layer-to-layer overlay is available
2) Under layer (um order depth) becomes visible
3) SEM_OVL results at ADI show good correlation to OPT_OVL



Optical Overlay Result (μDBO) at ADI

SPIE 2017, Kazuhisa Hasumi
SEM based overlay measurement between Via patterns and buried M1 patterns using high voltage SEM

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LER / LWR Metrology

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LER/ LWR and PSD analysis

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PSD analysis: effective tool to reveal patterning process problems

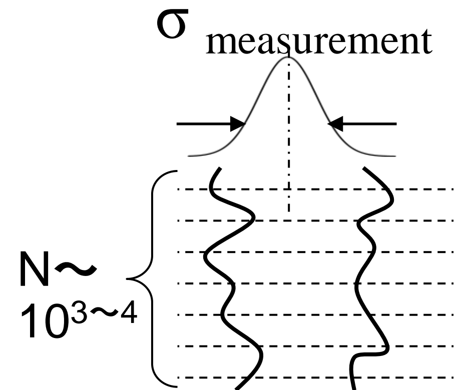
- Various source in roughness, each having different spatial period range, need different index
  - side-wall film thickness (white)
  - resist stochastic (1/f)
  - wiggling in etching (long period)

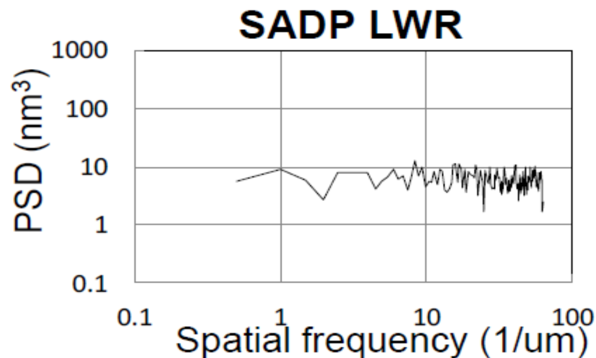
Precision in CD measurement

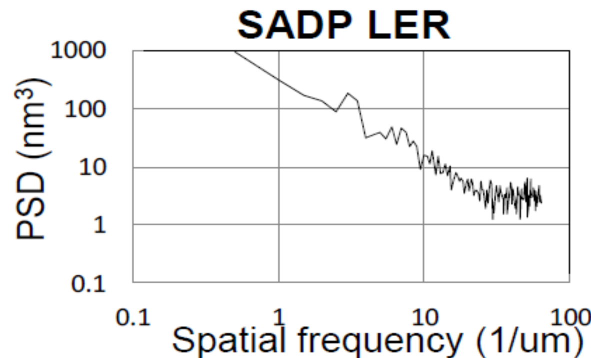
$$\sigma^2_{CD} = \frac{LER^2_{real} + \sigma^2_{measurement}}{N}$$

LER measurement

$$observed\ LER^2 = LER^2_{real} + \sigma^2_{measurement}$$







MNC 2016, Y. Momonoi, H. Fukuda

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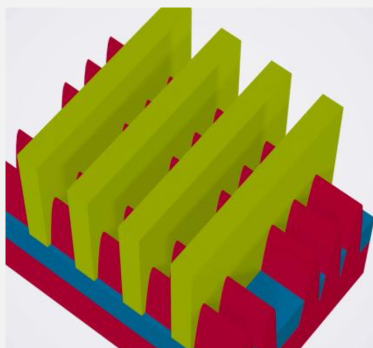
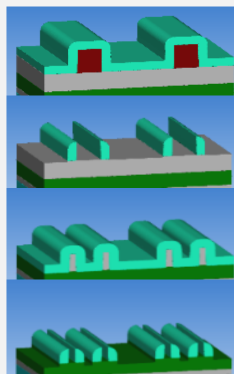
HAR Pattern Measurement

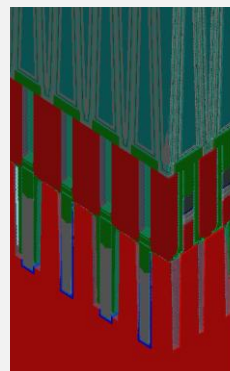
FinFET



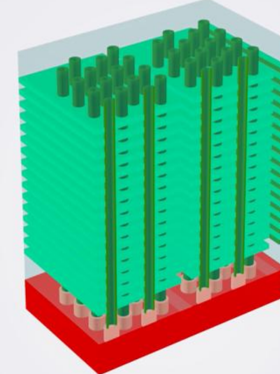
Multi-Patterning



DRAM



3D-NAND



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Bottom CD Measurement of HAR pattern

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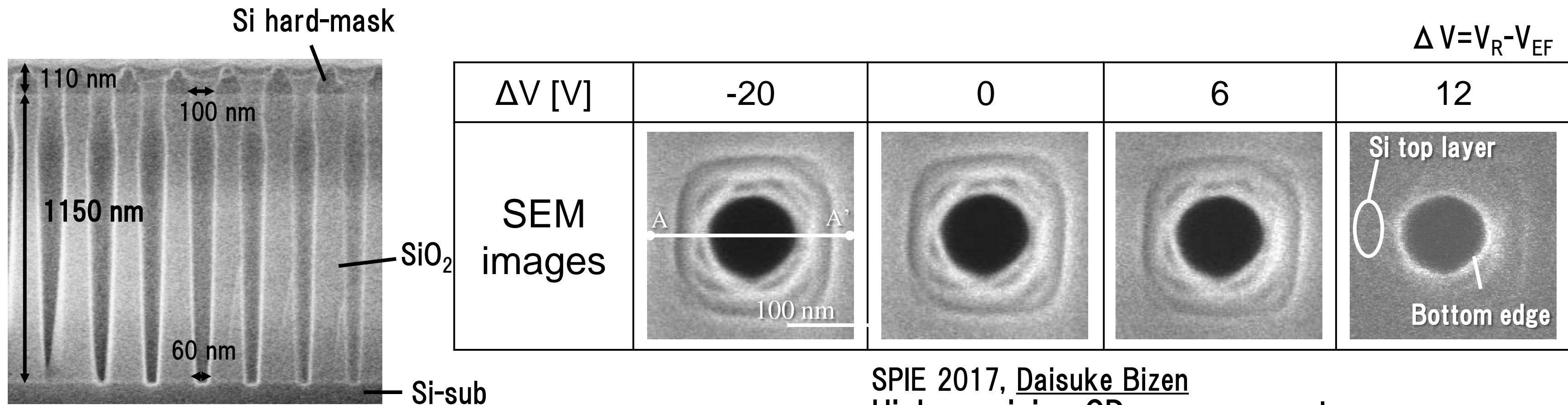
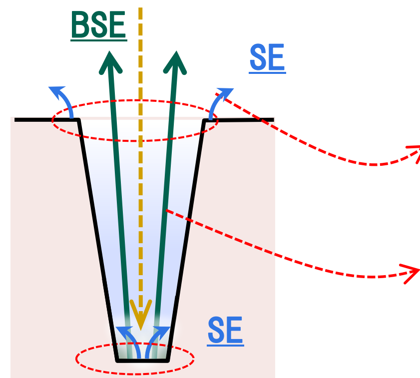
■ Low voltage, with energy filtering

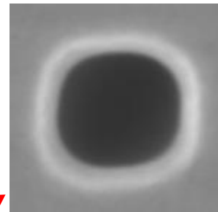


ΔV [V]	-20	0	6	12
SEM images				

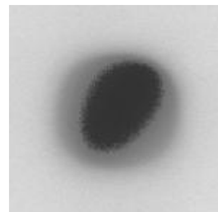
SPIE 2017, Daisuke Bizen
High-precision CD measurement using energy-filtering SEM techniques

■ High voltage, detect BSE signal

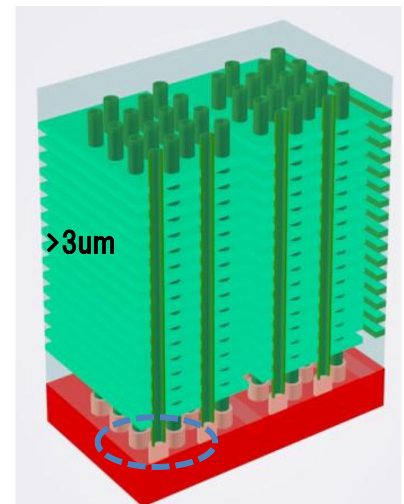




In the SE image, the shape of the surface is clearly visible, but the bottom is not visible.



BSE is increased by a high-acceleration electron beam, and the contour of the bottom becomes clearer. (The slope is also visible)



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Bottom CD Measurement of HAR pattern

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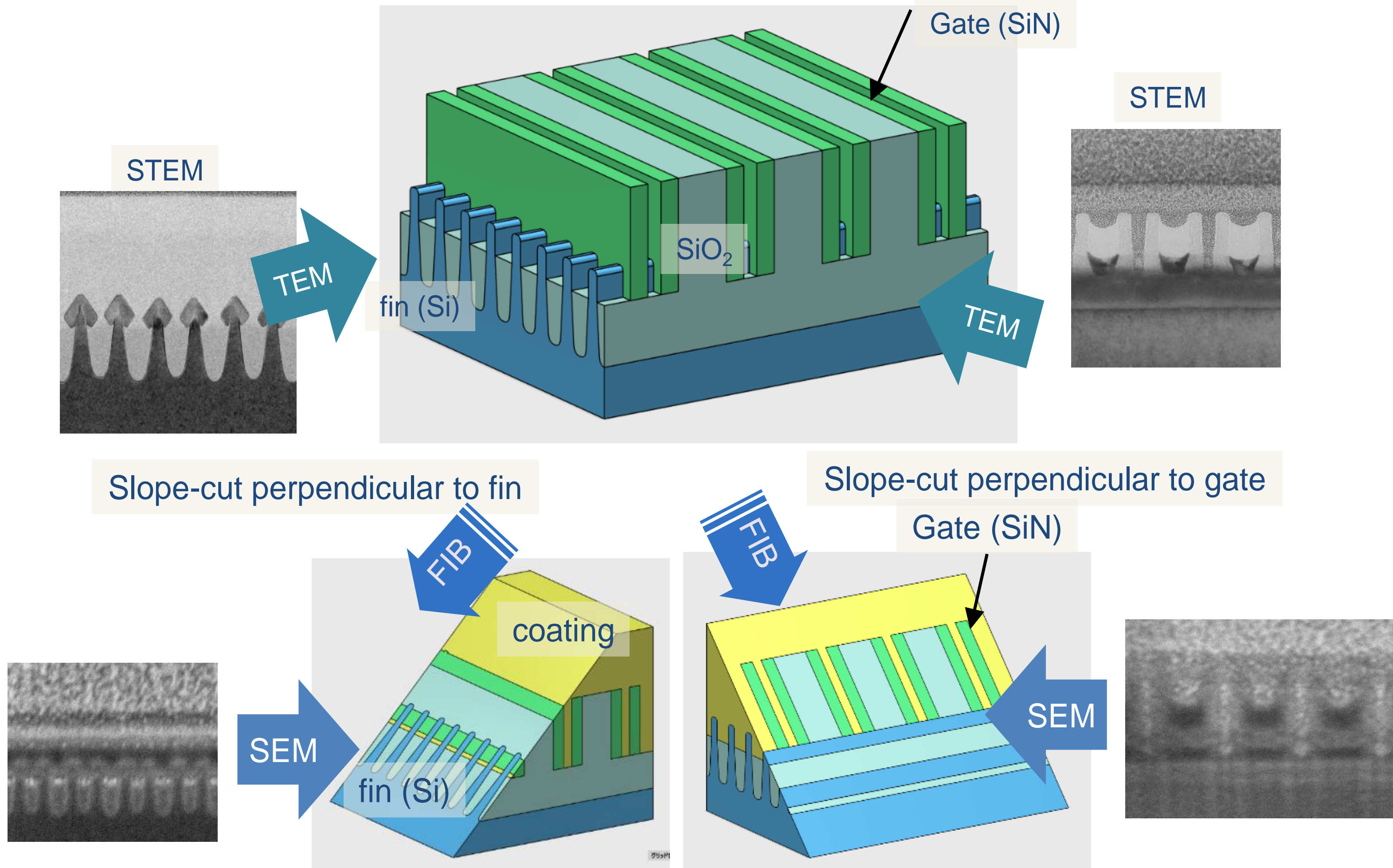
Another approach: FIB + SEM/STEM



K Takamasu, Y Iwaki; Satoru Takahashi; Hiroki Kawada; M Ikota; G F Lorusso; N Horiguchi "3D-profile measurement of advanced semiconductor features by reference metrology" SPIE 2016

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Bottom CD Measurement of HAR pattern

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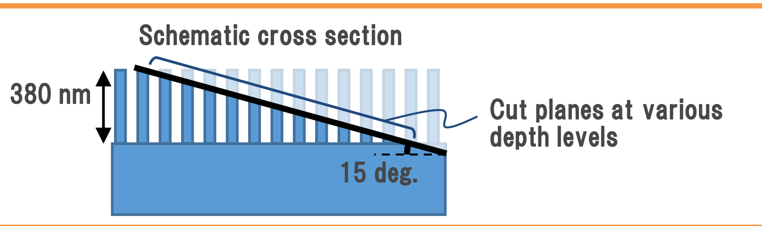
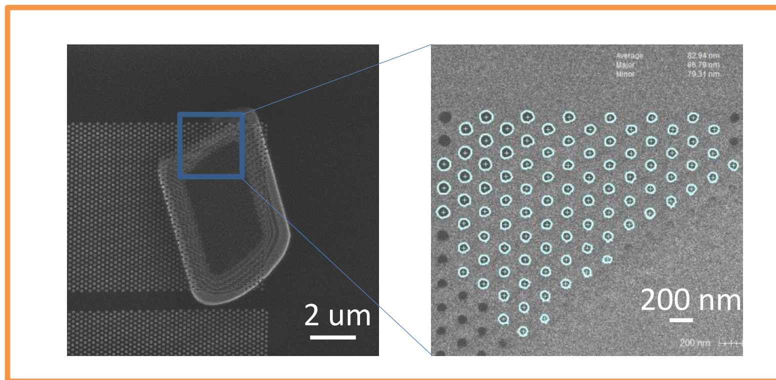
New approach: Oblique FIB + Top-down CD-SEM

Tilted FIB on 3D-NAND hole array

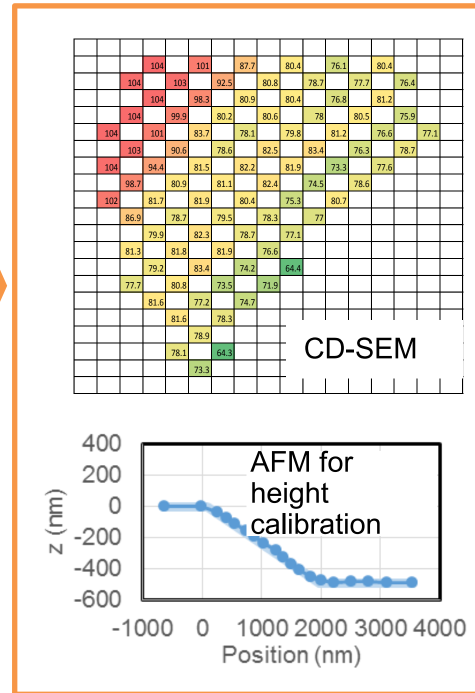


+

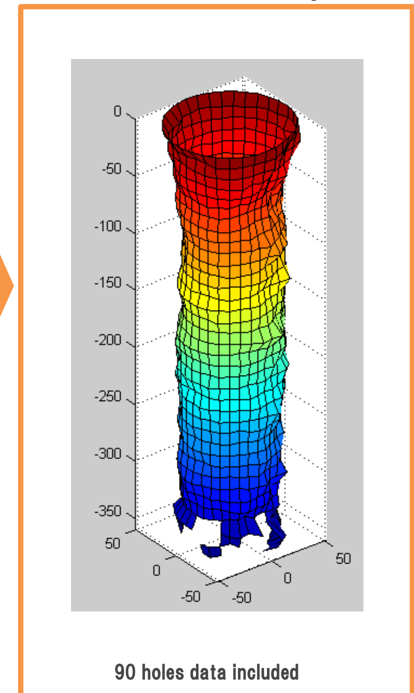
Top-down CD-SEM measurement



Raw results



Reconstructed 3D prof.



90 holes data included

- CD-SEM and FIB enable full 3D reconstruction

SPIE 2017, Gian Lorusso
Enabling CD SEM Metrology for 5nm Technology Node and Beyond

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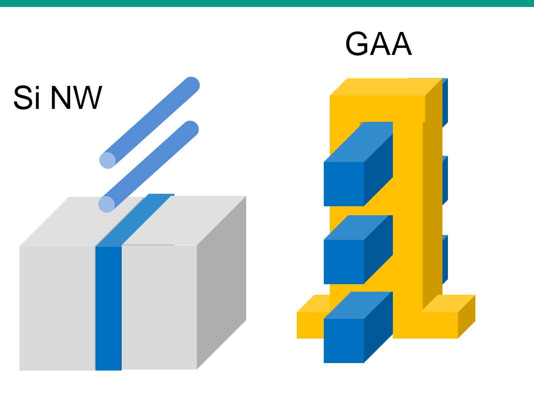
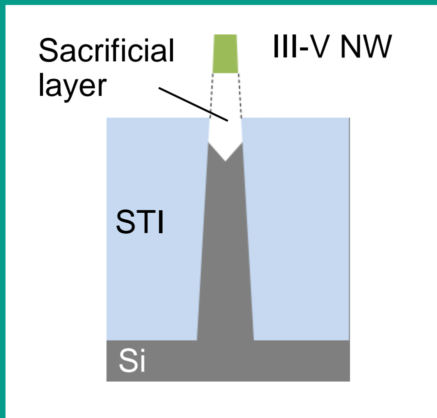
Metrology for Next Generation Device

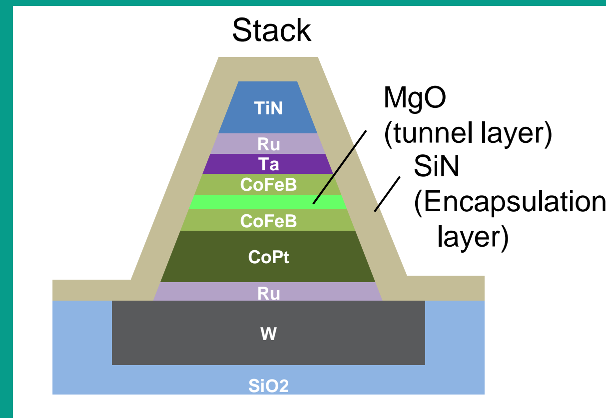
Nano-wire, GAA



High-Mobility NW



MRAM



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Nanowire metrology

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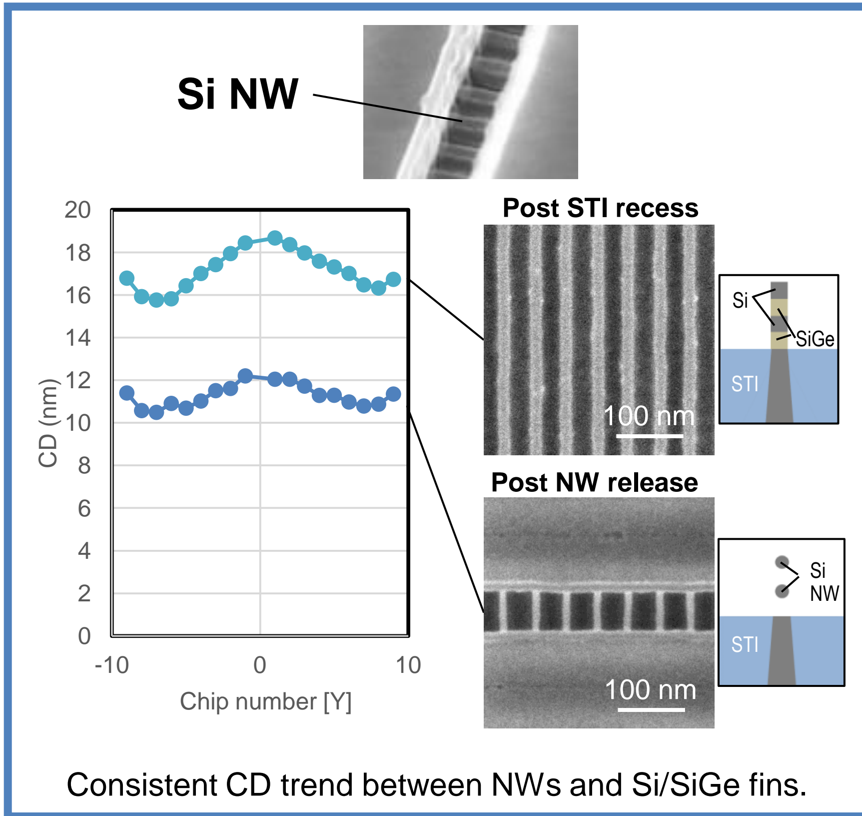
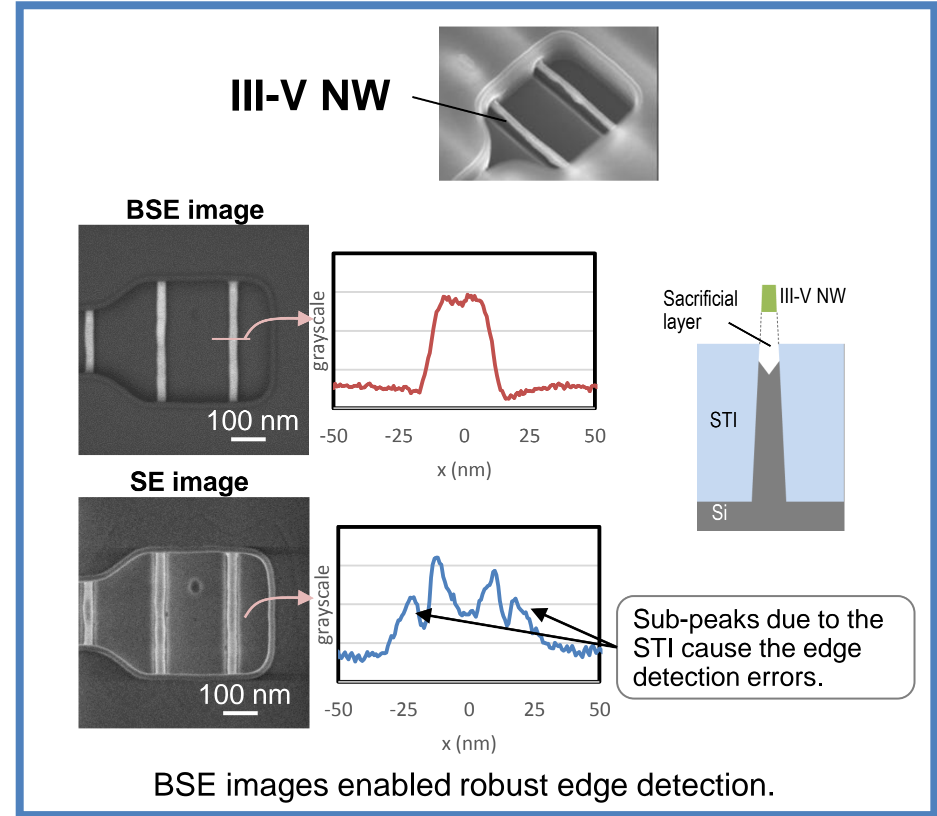
CD measurement of Si and III－V lateral nanowires is feasible



Consistent CD trend between NWs and Si/SiGe fins.



BSE images enabled robust edge detection.

SPIE 2017, Gian Lorusso
Enabling CD SEM Metrology for 5nm Technology Node and Beyond

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Emerging Memory metrology

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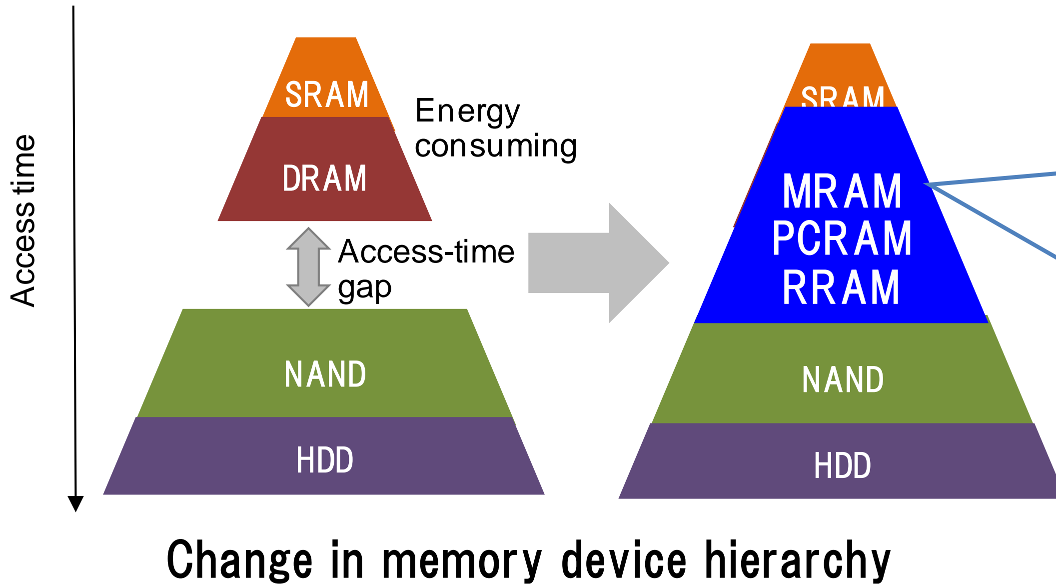
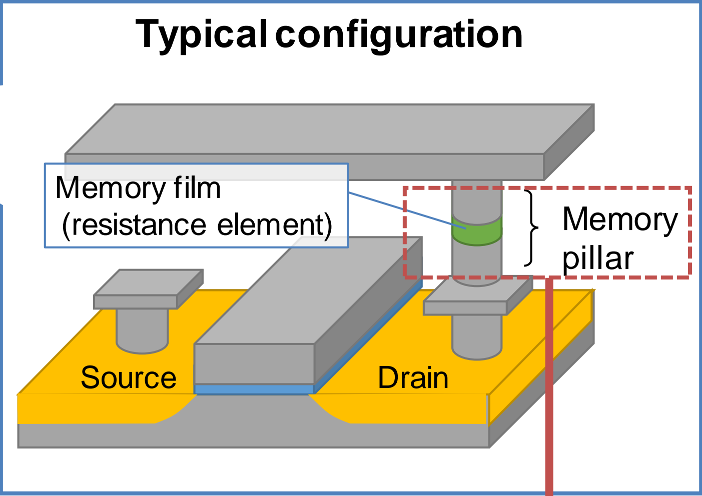
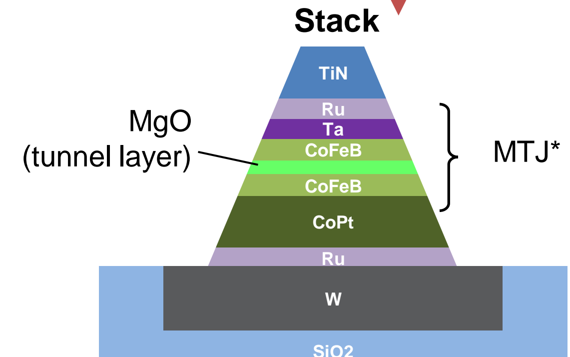
Studying STT-MRAM CD measurement

High / low resistance difference is used as a memory bit "0/1".



Change in memory device hierarchy





*MTJ : Magnetic Tunnel Junction

STT-MRAM memory cell

SPIE 2017, Takeyoshi Ohashi
Variability study with CD-SEM metrology for STTMRAM

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Emerging Memory metrology

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Metrology for size-independent resistance variability qualification

Etching

Encapsulation

SiN

Δ CD/2

Etching bias

16-19 nm

Δ CD/2

SiN thickness

4-9 nm

Electrically effective area

Damage width

MgO

Physical area

Edge bias

Measured area

Constant CD offset : D (fitting parameter)

Effective area : A_e

Measured area : A_m

Measured perimeter : C

Subtracted area : $D(C-\pi D)$

$$A_e = A_m - D(C - \pi D)$$

Under-estimated **Best fit** **Over-estimated**

Conductance

Estimated effective area

Effective area   Effective area   Effective area

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SPIE 2017, Takeyoshi Ohashi
Variability study with CD-SEM metrology for STTMRAM

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Metrology for HVM

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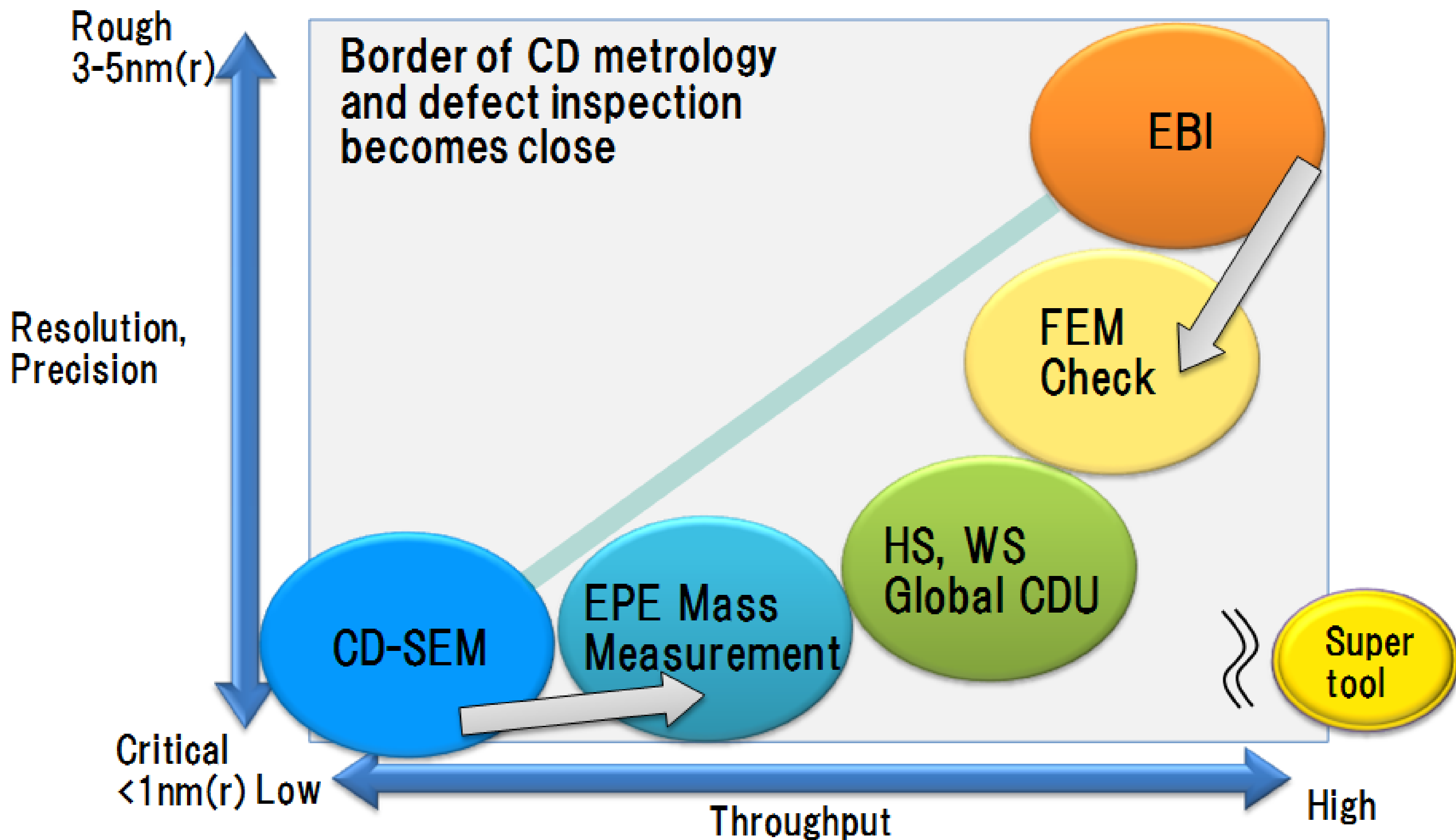
Requirement for HVM metrology tool

1nm resolution, <0.1nm precision, >10K point /Hr



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Requirement for HVM metrology tool

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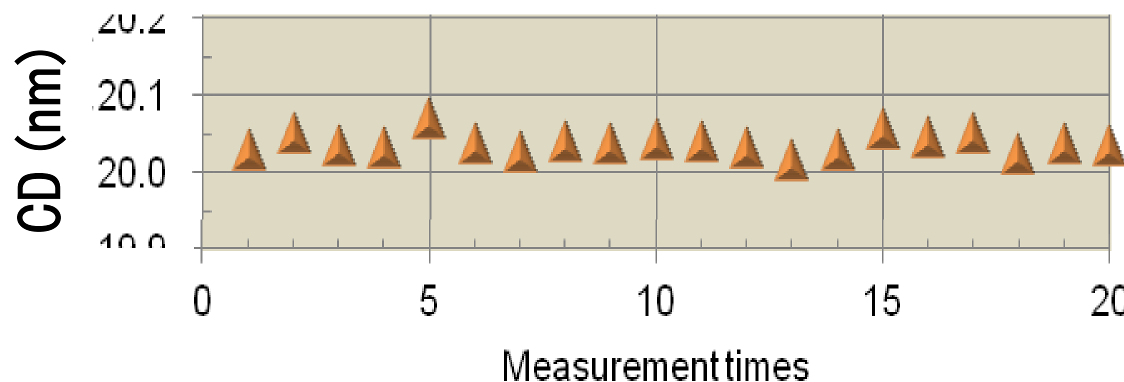
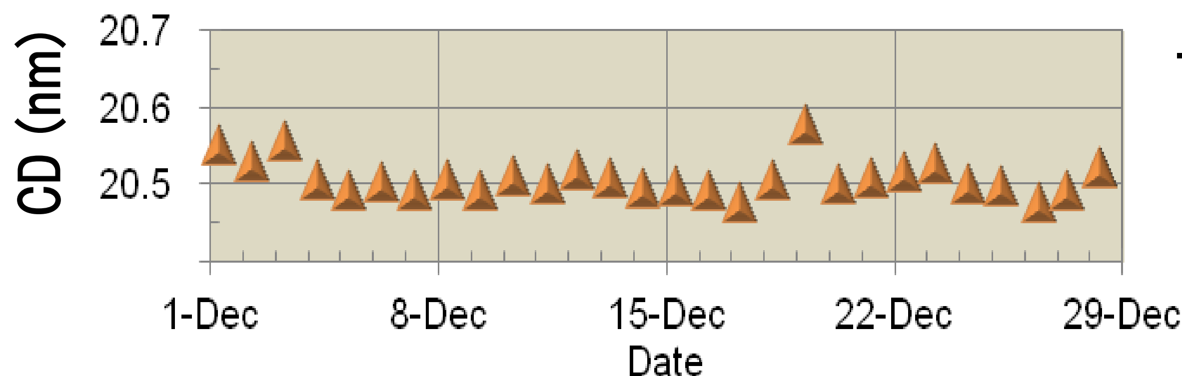
$$TMU^2 = \sigma^2_{short-term} + \sigma^2_{long-term} + \sigma^2_{matching} + \sigma^2_{other}$$

Stability, matching is required

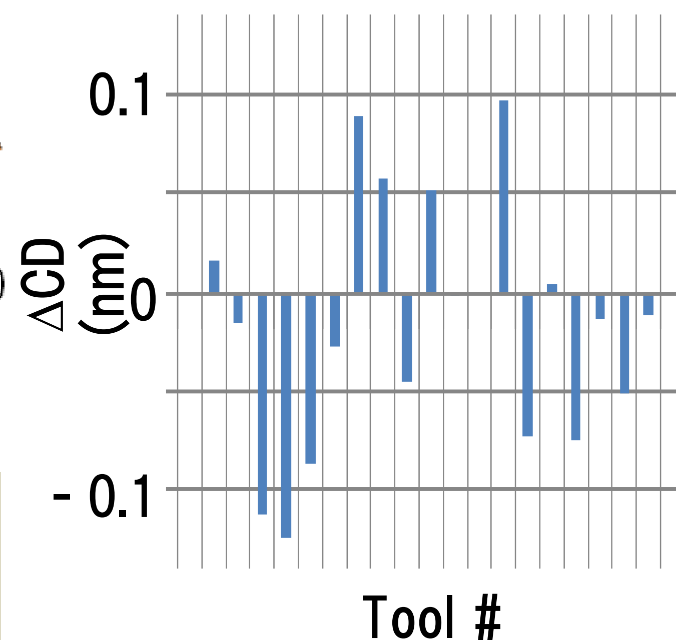
- Short-term ~ 0.04 nm



- Long-term ~ 0.06 nm



- Matching < 0.1 nm



K. Ueda, et al., SPIE 8681-82 (2013)
(Data of previous model)

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Gap
&
Potentials of Hybrid Tool

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Gap from the requirement

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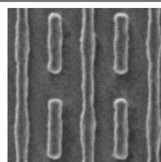

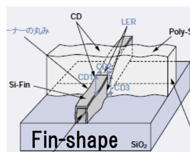

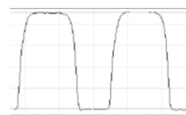

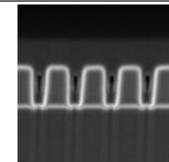

Requirement	CD-SEM	OCD	CD-AFM	CD-SAXS	SEM/STEM
Sensitivity (sub-1nm)			Probe effect at lateral direction		

Where to measure

	CD-SEM	OCD	CD-AFM	CD-SAXS	SEM/STEM
Measure any pattern	In-die, Complex pattern	grating	In-die, Complex pattern	grating	In-die, Complex pattern

What to measure

		CD-SEM	OCD	CD-AFM	CD-SAXS	SEM/STEM
EPE	CD					
	LER/LWR					
	OVL	High Voltage	DBO			
3D	Profile	Top view				
	HAR bottom	High Voltage				

In-line useage

	CD-SEM	OCD	CD-AFM	CD-SAXS	SEM/STEM
Throughput					
Recipe setup		modeling		modeling	Preparation
Non-destructive					

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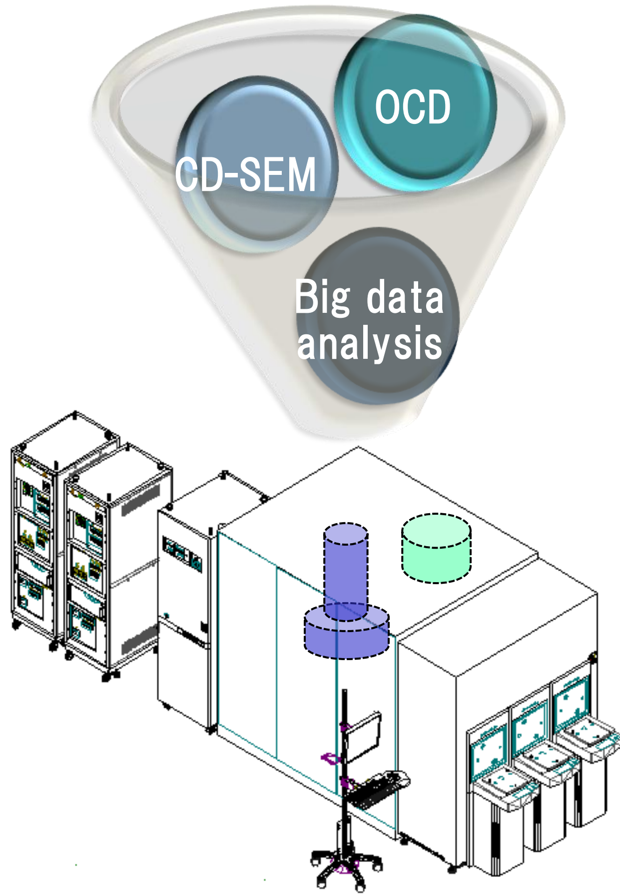
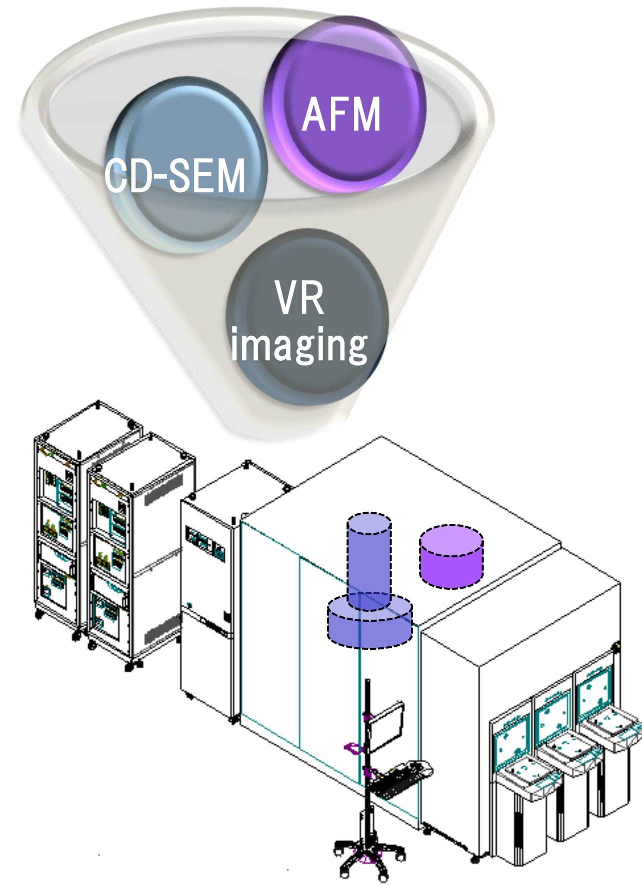
Potential of Hybrid Tool





- Smart sampling for precise measurement
- Smart recipe for OCD measurement
- Fusion map of height and EPE

- Precise 3D measurement for any complex pattern

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Further ideas of Hybrid Tool

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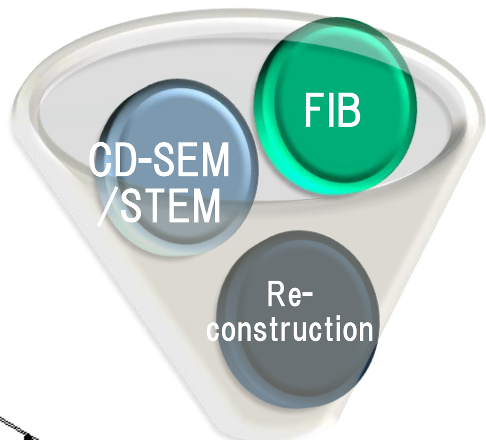
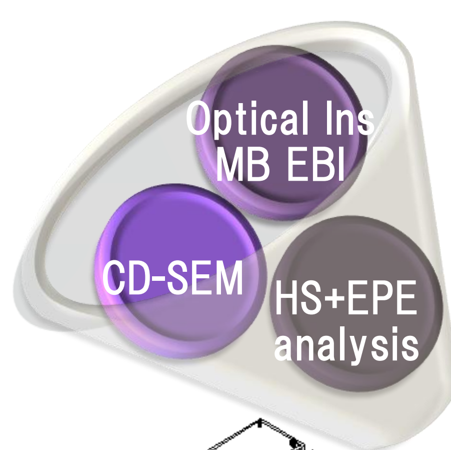
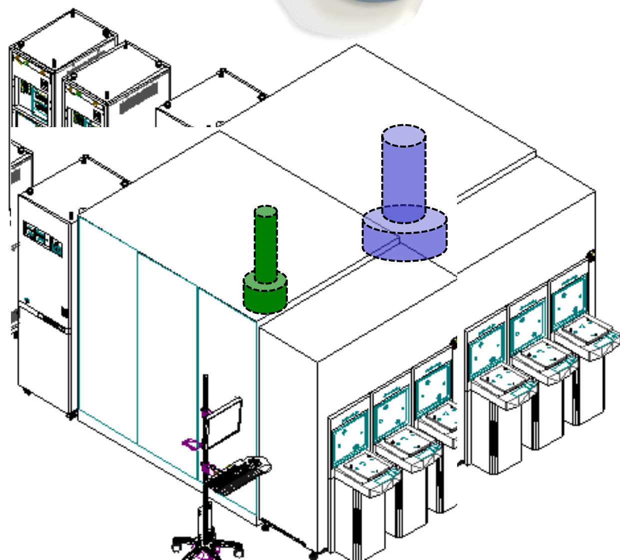
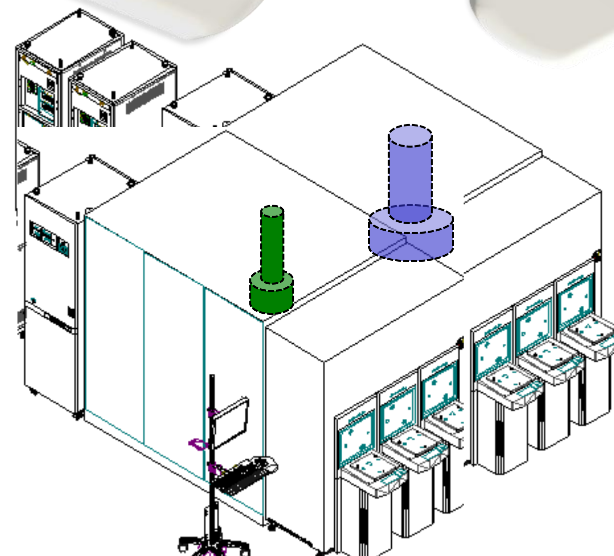




or





- Wafer level 3D measurement
  (precise, availability for complex pattern)

- Other combination ?

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Summary

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- Evolution in structure, process and material brings new requirement to CD-metrology, such as EPE metrology (including pattern fidelity check, overlay, LER/ LWR analysis), HAR pattern measurement (including bottom/underlayer measurement, 3D-profile).
- In-line CD-SEM had changed its HW/ SW to suit every use application.
- Though metrology technologies improve, there are many challenges to reach the requirements.
- Collaboration needed

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Acknowledgment

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We would like to thank Gian Lorusso, Greg McIntyre, Daisuke Bizen, Takeyoshi Ohashi and all the people in imec and Hitachi team to provide the data and discussion.

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Abbreviation

ADI	After development inspection
AFM	Atomic force microscopy
BSE	Back scattered electron
CD	Critical dimension
CDU	Critical dimension uniformity
DBO	Diffraction based overlay
EB	Electron beam
EBI	Electron beam inspection
EF	Energy filter
EPE	Edge placement error
EUV	Extreme ultra violet
FEM	Focus exposure matrix
FET	Field effect transistor
FIB	Focused ion beam
GAA	Gate all around
HAR	High aspect ratio
HS	Hot spot
HVM	High volume manufacturing
LCDU	Local CDU
LELE	Litho etch litho etch
LER	Line edge roughness
LWR	Line width roughness
MB	Multi beam
MP	Multi patterning
MRAM	Magnetoresistive random access memory
OCD	Optical CD measurement
OVL	overlay
PFC	Pattern fidelity check
PSD	Power spectrum density
SAQP	Self aligned quadruple patterning
SAXS	Small angle X-ray spectroscopy
SE	Secondary electron
SEM	Scanning electron microscope
STEM	Scanning transmission electron microscope

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Current and Future Critical Dimension Metrology Perspective for Sub-10nm Process

Mar/23/2017
Mari Nozoe
Business Strategy Planning Division
Electronic Device Systems Business Group