NOTICE OF FUNDING OPPORTUNITY (NOFO)

National Advanced Packaging Manufacturing Program (NAPMP) Materials & Substrates

Executive Summary

Federal Agency Name: National Institute of Standards and Technology (NIST), United States Department of Commerce (DOC)

Funding Opportunity Title: FY2024 CHIPS R&D National Advanced Packaging Manufacturing Program (NAPMP) Materials & Substrates

Announcement Type: Initial

Funding Opportunity Number: 2024-NIST-CHIPS-NAPMP-01

Assistance Listing Number(s): 11.042 – CHIPS R&D

Funding Opportunity Description: This NOFO seeks applications for research and development activities that will establish and accelerate domestic capacity for advanced packaging substrates and substrate materials. Through this NOFO, the NAPMP program seeks to achieve the following objectives:

(1) Accelerate domestic R&D and innovation in advanced packaging materials and substrates;
(2) Translate domestic materials and substrate innovation into U.S. manufacturing, such that these technologies are available to U.S. manufacturers and customers, including to significantly benefit U.S. economic and national security;
(3) Support the establishment of a robust, sustainable, domestic capacity for advanced packaging materials and substrate R&D, prototyping, commercialization, and manufacturing; and
(4) Promote a skilled and diverse pipeline of workers for a sustainable domestic advanced packaging industry.

NAPMP plans to release subsequent NOFOs relevant to other research areas and for an Advanced Packaging Piloting Facility (APPF), where successful development efforts will be transitioned and validated for scaled transition to U.S. manufacturing. The APPF is expected to be a key facility for technology transfer to high-volume manufacturing.

Dates: Relevant dates in the application process are listed in Table 1 and described in the text that follows.

Table 1. Materials & Substrates NOFO Key Dates	
Webinar Information Session	March 1, 2024
Proposers Day	March 12, 2024
Concept Papers Due	April 12, 2024
Invited Full Applications Due	July 3, 2024

The Department of Commerce may amend this NOFO at any time. It may also close the funding opportunity with at least 60 days' notice. Changes will be communicated via https://www.grants.gov and https://www.chips.gov.

Webinar Information Session: The National Institute of Standards and Technology (NIST) CHIPS Research and Development Office (CHIPS R&D) will host an informational webinar on March 1, 2024, to provide general information regarding this NOFO, offer general guidance on preparing applications, and answer questions. Proprietary technical discussions about specific project ideas will not be permitted during the webinar, and CHIPS R&D staff will not critique or provide feedback on specific project ideas while they are being developed by an applicant, brought forth during the webinar, or at any time before the deadline for all applications. However, questions about the funding opportunity, eligibility requirements, evaluation and award criteria, selection process, and the general characteristics of a competitive application will be addressed at the webinar and by e-mail to research@chips.gov with "2024-NIST-CHIPS-NAPMP-01 Questions" in the subject line. There is no cost to attend the webinar, but participants must register in advance. Participation in the webinar is not required and will not be considered in the review and selection process.

Proposers Day and Teaming Meetings: In addition to the informational webinar described above, CHIPS R&D plans to host a proposers day March 12, 2024, to promote awareness of the funding opportunity and provide a forum for organizations to identify prospective partners. Information about the event can be found on the CHIPS for America events website.

Concept Papers: The submission of a concept paper is required for submission of a full application. Applicants must send an email to research@chips.gov with "2024-NIST-CHIPS-NAPMP-01 Concept Papers" in the subject line to request instructions for submitting Concept Papers. Applicants are strongly advised not to wait until the last minute to request submission instructions. The CHIPS R&D Program will respond by email with instructions for securely submitting a Concept Paper. Concept Papers must be received no later than 11:59 p.m. Eastern Daylight Time, April 12, 2024. Concept papers received after this deadline will not be reviewed or considered.

Full Applications: Full applications will be accepted only from those applicants invited after concept paper evaluation. Full applications must be received at Grants.gov no later than 11:59 p.m. Eastern Time, July 3, 2024. Applications received after this deadline will not be reviewed or considered. Applicants should be aware, and factor in their application submission planning, that the Grants.gov system closes periodically for routine maintenance. Applicants should visit Grants.gov for information on any scheduled closures.

Full Application Submission Address: Full applications must be submitted using Grants.gov. Paper applications will not be accepted.

Anticipated Amounts: In FY24, CHIPS R&D anticipates making available approximately $300,000,000 for funding of multiple awards in amounts up to approximately $100,000,000 over up to 5 years per award, not including voluntary co-investment, though additional funding may be provided to applicants who address more than one technical area.

Funding Instrument: Awards in this program will be made as cooperative agreements or other transactions, as appropriate for the selected project. See Section 2.1 of this document for additional information regarding the type of award agreement.

Eligibility: Eligible applicants include domestic for-profit organizations; non-profit organizations; accredited institutions of higher education including community and technical colleges; and state, local, territorial, and Indian tribal governments.

Eligible applicants may only submit one concept paper under this NOFO. Entities may not be included as subrecipients on more than two concept papers.

Applicants and recipients are required to have an active registration in SAM.gov and are encouraged to begin the process of registering as early as possible.

Co-investment (cost share) Requirements: Co-investment (cost share) is not required in this program. CHIPS R&D will, however, give preference to applications that demonstrate committed co-investment in their Project Narrative and Budget Narrative and Justification. See Sections 4.6.1.6 and 4.6.1.8 of this NOFO for additional information.

Public Website, and Frequently Asked Questions (FAQs): CHIPS R&D has a public website with a "Frequently Asked Questions" page and other information pertaining to this Funding Opportunity.

Agency Points of Contact (POC): Section 7 identifies Agency Points of Contact. Applicants must submit all questions in writing to the appropriate agency point of contact with "2024-NIST-CHIPS-NAPMP-01" in the subject line. All inquiries regarding this NOFO must be submitted to the email addresses in that section.

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1 PROGRAM DESCRIPTION

The statutory authority for the National Advanced Packaging Manufacturing Program (NAPMP) Materials & Substrates NOFO is 15 U.S.C. §4656(d) and 15 U.S.C. §4659, as amended,[1] and 15 U.S.C. §272(b)(4).

1.1 NAPMP PROGRAM OVERVIEW

The CHIPS and Science Act appropriated $50 billion to the Department of Commerce's CHIPS for America program both to support semiconductor research and development (R&D) and to expand semiconductor manufacturing capacity in the United States. This includes $39 billion for the Department of Commerce (the Department) to expand domestic semiconductor manufacturing capacity through an incentives program and $11 billion to advance U.S. leadership in semiconductor R&D. These R&D advances will be realized through four programs: the National Semiconductor Technology Center (NSTC), the National Advanced Packaging Manufacturing Program (NAPMP), the CHIPS Metrology Program, and Manufacturing USA institute(s). These investments, across both the R&D and incentives programs, seek to strengthen U.S. competitiveness, support domestic production and innovation, create, across the country, good jobs with working conditions consistent with the Good Jobs Principles published by the Departments of Commerce and Labor, and advance U.S. economic and national security.

1.1.1 CHIPS R&D Mission and Goals

Within CHIPS for America, the mission of the National Institute of Standards and Technology's (NIST) CHIPS Research and Development Office (CHIPS R&D) is to accelerate the development and commercial deployment of foundational semiconductor technologies by establishing, connecting, and providing access to domestic research efforts, tools, resources, workers, and facilities. CHIPS R&D aims to achieve the following goals by 2030:

- ***U.S. Technology Leadership***: The United States improves its capacity to invent, develop, prototype, manufacture, and deploy the foundational semiconductor technologies of the future.
- ***Accelerated Ideas to Market***: The best ideas achieve commercial scale as quickly and cost effectively as possible.
- ***Robust Semiconductor Workforce***: Inventors, designers, researchers, developers, engineers, technicians, and staff sustainably meet evolving domestic government and commercial sector needs.

[1] DOC CHIPS activities were authorized by Title XCIX—Creating Helpful Incentives to Produce Semiconductors for America of the William M. (Mac) Thornberry National Defense Authorization Act for Fiscal Year 2021 (Pub. L. 116-283, often referred to as the CHIPS Act).

1.1.2 NAPMP Objectives

NAPMP seeks to drive U.S. leadership in advanced packaging and provide the technology and skilled workforce needed for packaging manufacturing in the United States. Within a decade, NAPMP-funded activities, coupled with CHIPS manufacturing incentives, will establish a vibrant, self-sustaining, profitable, domestic advanced packaging industry where advanced-node chips manufactured in the United States and abroad can be packaged in appropriate volumes within the United States and innovative designs and architectures are enabled through leading-edge packaging capabilities. In combination with other CHIPS for America education and workforce efforts, NAPMP-funded activities produce the diverse and capable workforce needed for the success of the domestic packaging sector.

As the global microelectronics industry continues to make an expensive and technologically challenging, yet essential, leap from conventional packaging to advanced packaging, the United States has a once-in-a-generation opportunity to establish a competitive advanced packaging sector. To promote the emergence of domestic packaging innovations, NAPMP will invest in four hardware-related development areas:

- Materials and Substrates
- Equipment, Tools, and Processes
- Power Delivery and Thermal Management
- Photonics and Connectors

Additionally, NAPMP will invest in two interrelated areas that address the chiplet and co-design ecosystem and in an Advanced Packaging Piloting Facility (APPF), where successful R&D efforts will be further developed and validated for scaled transition to U.S. manufacturing.

1.1.3 NAPMP Materials and Substrates NOFO Objectives

This NOFO, the first under the NAPMP, seeks applications for activities that will achieve the following objectives:

(1) Accelerate domestic R&D and innovation in advanced packaging materials and substrates;
(2) Transition domestic materials and substrate innovation into U.S. manufacturing, such that these technologies are available to U.S. manufacturers and customers, including to significantly benefit U.S. economic and national security;
(3) Support the establishment of a robust, sustainable, domestic capacity for advanced packaging materials and substrate R&D, prototyping, commercialization, and manufacturing; and
(4) Promote a skilled and diverse pipeline of workers for a sustainable domestic substrate manufacturing sector.

1.2 DEFINITIONS

This section provides definitions for purposes of this NOFO.

- **Basic and Applied Research** – Basic research refers to experimental or theoretical work undertaken primarily to acquire new knowledge of the underlying foundations of phenomena and observable facts. Basic research may include activities with broad or general applications in mind, such as the study of how plant genomes change, but should exclude research directed towards a specific application or requirement, such as the optimization of the genome of a specific crop species. For the purpose of this NOFO, the term "applied research" refers to original investigation undertaken in order to acquire new knowledge. Applied research is, however, directed primarily towards a specific practical aim or objective.[2]
- **Demonstration device** – The Integration of dielets onto the substrate to create a functional and testable device. The design of a demonstration device may include (but is not limited to) embedding of passive and active components in/on the substrate, small testable dielet assemblies on the substrate at pitches relevant to project technical targets, and dielet assemblies on both sides of the substrate.
- **Dielet** – A small block of semiconducting material carrying an integrated circuit with reduced size and potentially limited or focused functionality in comparison to a conventional scale semiconductor die.
- **Milestones** – Actions or events marking a significant change or stage in developments in a project.
- **Phase-specific Target** –Includes both technical and non-technical targets, derived from applicant-specified milestones, to inform go/revise/no-go points for the transition from one project phase to the next. Phase-specific technical targets focus on measurable progress toward Project-Level Technical Targets. Phase-specific non-technical targets focus on measurable progress towards the applicant's Education and Workforce Development plan and Commercial Viability and Domestic Production Plan. CHIPS R&D may identify additional phase-specific targets, including to address other applicant-defined plans.
- **Project** – All activities funded under a single award made under this NOFO, including but not limited to all planning and management, basic and applied research, substrate and demonstration device development and production, commercial viability and domestic production preparation, integrated workforce education and training, and pilot-level substrate production activities.
- **Project-level Technical Target** – Specific technical advances in materials and substrate technologies to be achieved by the end of the project (See Section 1.5).

[2] The definitions of basic and applied research are taken from Office of Management and Budget Circular A-11 (2023).

- **Project-level Non-Technical Target** – Specific non-technical targets in either education and workforce development or commercial viability and domestic production to be achieved by the end of the project (See Section 1.6).
- **Semiconductor** – An integrated electronic device or system, most commonly manufactured using materials such as, but not limited to, silicon, silicon carbide, or III-V compounds, and processes such as, but not limited to, lithography, deposition, and etching. Such devices and systems include but are not limited to analog and digital electronics, power electronics, and photonics, for memory, processing, sensing, actuation, and communications applications.
- **Substrate** – The foundation or supporting base on which or within which the elements of a semiconductor device are fabricated or attached.[3]
- **Substrate material** – The class of materials from which a substrate is made. This NOFO focuses on organic, glass, and semiconductor-based (e.g., silicon-based) classes of materials.
- **Substrate sample** – Samples provided to CHIPS R&D or to an independent evaluator along with relevant documentation, including process assumptions, design manual, process design kit (PDK, compatible with NAPMP-specified formats), reliability criteria, and electrical specifications for purposes of evaluation of progress toward phase-specific technical targets.

1.3 BACKGROUND

Emerging technologies like artificial intelligence, advanced telecommunications, biomedical devices, and autonomous vehicles require leap-ahead advances in microelectronics capabilities. In the past, the semiconductor industry has largely addressed performance needs by increasing the number and density of transistors on a chip, a process known as miniaturization. However, the previous pace of miniaturization, as expressed by Moore's Law, is slowing and cannot alone provide the performance improvements needed for emerging microelectronics technologies. Improving all aspects of system performance to support the breadth of new semiconductor applications will require advanced packaging.

Semiconductor packaging serves two general purposes. One is to protect the chip mechanically, thermally, and environmentally. The other is to enable reliable inter-chip communication and data processing, power delivery, and a stable test and system integration platform. Advanced packaging and related capabilities, such as heterogeneous integration, encompass the need to integrate multi-component-assemblies with large numbers of interconnects to achieve a degree of integration that blurs the line between chip and package. The ability to "scale-down and scale-out" will be critical to advanced

[3] Derived from the JEDEC general dictionary at https://www.jedec.org/standards-documents/dictionary/terms/substrate-semiconductor-device-1-general#

packaging, where "scale-down" refers to shrinking the size of features on the package, and "scale-out" refers to increasing the number of chips assembled on the substrate.

Advanced packaging allows semiconductor manufacturers to make improvements in device performance and function and to shorten time to market through enabling versatile use of components. Additional benefits include a reduced physical footprint, lower power, increased chip reuse, improved security, and potentially decreased costs, allowing for more diverse and customizable manufacturing lots.

Currently, the vast majority of advanced packaging manufacturing capacity resides in Asia.[4] As the CHIPS for America program invests in leading-edge semiconductor design and fabrication, the United States will also need a cost effective and efficient domestic advanced packaging capability to enable semiconductors made in the United States to be packaged in the United States. The United States will need this capability to sustain its global competitiveness and to maintain supply chain security and resilience.

Materials and substrates are foundational to advanced packaging. Moreover, materials and substrates R&D, particularly applied R&D, is critical to expanding the U.S. packaging ecosystem.

1.4 FUNDING OPPORTUNITY DETAILED DESCRIPTION

1.4.1 Project Activities

Project activities are expected to include, but not necessarily be limited to, basic and applied research, substrate and demonstration device development and production, commercial viability and domestic production preparation, integrated education and workforce development and pilot-level substrate production.

CHIPS R&D encourages collaborative proposals under this NOFO. Though not required, CHIPS R&D expects that applicants assembling teams (comprising one or more subrecipients and potentially unfunded collaborators) may be best suited to collectively provide the full range of expertise and capabilities needed to achieve the program objectives, including the proposed project-level targets. All subrecipients must meet the applicant eligibility requirements stated in Section 3.1.

1.4.2 Project Structure

Applications under this NOFO must describe projects that, consistent with the objectives under Section 1.1.3:

[4] North American Advanced Packaging Ecosystem Gap Assessment — Critical Systems, Capability, Capacity Analysis and Recommendations IPC Industry Research Report — November 2021

1. Focus on one or more of the Technical Areas described in Section 1.4.3;
2. Propose achieving specific Project-level Technical Targets and Project-level Non-Technical Targets, as described in Sections 1.5 and 1.6;
3. Define milestones marking measurable progress toward those targets, as described in Section 1.6.3;
4. Provide for supplying substrate samples and demonstration devices to CHIPS R&D and to other entities, as described in Section 1.7 and 1.8;
5. Sub-divide project activities into four phases, with each phase ranging in length from 3 to 18 months, as described in Section 1.8;
6. Are designed to achieve pilot-scale production of new substrates in Phase 4 (see Section 1.8.4); and
7. Are structured around a period of performance (PoP) not to exceed five years.

1.4.3 Technical Areas

This NOFO seeks applications relevant to one or more of the following technical areas: Technical area 1 (TA1), focused on organic materials and substrates (including fan-out); technical area 2 (TA2), focused on glass materials and substrates; and technical area 3 (TA3), focused on semiconductor-based substrates. Applicants may address one or more technical areas in a single proposal. The focus in all technical areas is to achieve the objectives of this NOFO (See Section 1.1.3), including by advancing U.S. leadership in "scale-down and scale-out" (See Section 1.3), driving the development of new substrate industry solutions, and demonstrating manufacturability for future sustainable domestic production. Composite substrates using fan out wafer level packaging, including substrates for flexible and biomedical applications, are in scope for this NOFO. Projects involving traditional boards, silicon or glass interposers, and small area substrates, are not in scope for this NOFO.

1.5 PROJECT-LEVEL TECHNICAL TARGETS

Project-Level Technical Targets set out the specific technical advances to be achieved by the end of the project. These targets comprise two categories: CHIPS R&D-specified Technical Targets and Embedded Substrate Features.

1.5.1 CHIPS R&D-specified Technical Targets

Table 2 establishes a set of ten technical target categories and associated technical targets, selected by CHIPS R&D for their potential to improve the performance, manufacturability, and cost effectiveness of advanced substrates and associated manufacturing processes, among other factors. In some but not all cases, CHIPS R&D-specified Technical Targets differ across TA1, TA2, and TA3.

Applicants must describe, for each of the CHIPS R&D-specified Technical Targets relevant to their selected technical area(s), whether they expect to:

(1) exceed the target;
(2) meet the target;
(3) partially meet the target; or
(4) not need to meet the target.

Applicants may propose additional Project-Level Technical Targets in addition to the CHIPS R&D-specified Technical Targets described in Table 2.

Technical targets for substrate wiring, via pitches, and number of levels on both sides of the substrate are expected to be aggressive and the substrate is expected to be compatible with direct attach at fine pitch of advanced node CMOS, legacy nodes, and non-silicon dielets. In cases where the applicant does not intend to meet or exceed a technical target in Table 2 and/or opts to include additional technical targets, the applicant should carefully explain how their proposed approach nonetheless represents a significant technical advance relative to the global state of the art and will accomplish the CHIPS R&D mission and goals (See Section 1.1.1) and the specific objectives of this NOFO as described in Section 1.1.3.

Table 2: CHIPS R&D-specified Technical Targets

Technical Target Category	CHIPS R&D-specified Technical Targets		
	TA 1 (Organic)	**TA 2 (Glass)**	**TA3 (Semiconductor-Based)**
1. Minimum Line Width, Spacing, and Pitch	1 μm line width, 1 μm line spacing, 2 μm pitch	0.5 μm line width, 0.5 μm line spacing, 1 μm pitch	0.25 μm line width, 0.25 μm line spacing, 0.5 μm pitch
2. Coplanarity at Die Attach (Bonding Area)	Below 0.5 μm over dielet area, where dielet area can vary between 1 mm x 1 mm to 10 mm x 10 mm	Below 0.5 μm over dielet area, where dielet area can vary between 1 mm x 1 mm to 10 mm x 10 mm	Below 0.5 μm over dielet area, where dielet area can vary between 1 mm x 1 mm to 10 mm x 10 mm
3. Interlevel via diameter	1 μm	0.5 μm	0.25 μm
4. Through substrate via diameter	Less than 100 μm	Less than 100 μm	Less than 100 μm
5. Max wire thickness	Equal to wiring pitch	Equal to wiring pitch	Equal to wiring pitch
6. Max number of Layers (hierarchical)	10+10 (side 1 + side 2), or 15 single sided for Fan Out wafer level packaging	10+10 (side 1 + side 2)	15+15 (side 1 + side 2)

7. Effective coefficient of thermal expansion (CTE) of the multilayer stack	6 to 10 parts per million (ppm) -77 °C to 350 °C	6 to 10 parts per million (ppm) -77 °C to 350 °C	6 to 10 parts per million (ppm) -77 °C to 350 °C
8. Max substrate size	500 mm x 500 mm	500 mm x 500 mm or 300 mm diameter	210 mm x 210 mm or 300 mm diameter
9. Max thickness	3 mm	2 mm	1 mm
10. Warpage	Should be consistent with lithographic requirements for specified minimum line width and spacing		
11. Applicant-Defined Target(s)	If consistent with the objectives of this NOFO, the Applicant may propose one or more additional technical targets, such as targets addressing environmental sustainability.		

1.5.2 Embedded Substrate Features

Advanced substrates may include one or more passive or active components embedded in the substrate for enhanced functionality. For all technical areas, applicants are strongly encouraged to consider providing additional embedded substrate features, including active and passive devices, that may advance / enhance U.S. leadership in substrate offerings. Examples include, but are not limited to, the following:

- Advanced voltage regulation structures
- Advanced RF antenna structures
- Advanced substrate thermal solutions (e.g., substrate heat pipes and/or thermal vias)
- Advanced high density decoupling capacitors
- Substrate inductor or resistor structures
- Cross substrate waveguides and/or TLVs (Through Light Vias)
- Substrate trackability / traceability structures or substrate tags
- Substrate radiation shielding structures
- Substrate cavity, curvature, or geometric flexibility provisions, or biomedical applications.

1.6 PROJECT-LEVEL NON-TECHNICAL TARGETS

1.6.1 Education and Workforce Development (EWD) Targets

NAPMP investments under this NOFO are intended to create innovation-driven domestic substrate manufacturing capability, which requires fostering a diverse and capable domestic workforce with access to good jobs, such as those consistent with the Good Jobs Principles. The combination of expertise, facilities, and equipment required to meet the technical targets defined in this NOFO provide exceptional opportunities for tailored EWD programs.

Applicants must provide an EWD plan that leverages capabilities supported through the proposed project to address domestic advanced packaging workforce needs, including educational opportunities arising from engaging students in research. CHIPS R&D encourages applicants to, in providing an EWD plan, describe any efforts to attract and retain a diverse student and trainee population and to demonstrate that the EWD efforts are worker centered, industry-aligned, and promote high-quality jobs.

Examples of relevant activities in an EWD plan may, but are not required, to include paid research internships and fellowships focused on project activities, paid research experiences for undergraduates, and training programs that take advantage of the project's facilities, including in-person and virtual programs, partnerships with employers, labor, and the public workforce system, as well as any other institutions key to the delivery of quality employment and training pathways, such as educational institutions, government agencies, industry organizations, and programs focused on training for underserved communities, as defined by Executive Order 13985, Advancing Racial Equity and Support for Underserved Communities Through the Federal Government (Jan. 20, 2021) and Executive Order 14091, Further Advancing Racial Equity and Support for Underserved Communities Through the Federal Government (Feb. 16, 2023). Applicants must propose SMART (Specific, Measurable, Achievable, Relevant, and Time-Bound) EWD targets, such as the number of students trained or engaged in research and subsequently placed in good jobs in the domestic semiconductor industry, to be achieved under the EWD plan.

Educational and workforce activities not unique to project capabilities, such as developing general curriculum or generic training program design, will not be funded under this NOFO.

1.6.2 Commercial Viability and Domestic Production (CVDP) Targets

Consistent with promoting a robust, sustainable domestic capacity for substrate R&D, prototyping, and production, and in keeping with the provisions of Executive Order 14104 and the CHIPS Act domestic production requirements (15 U.S.C. §4656(g)), CHIPS R&D requires applicants to develop and provide a Commercial Viability and Domestic Production Plan describing activities to be funded as part of the project. The CVDP plan must include a realistic business model for the funded innovations (e.g., manufactured substrates), include a technology transition plan, and describe pathways to benefitting national and economic security, such as through the domestic availability of the technology and successful adoption by commercial or defense partners. Applicants should propose measurable CVDP targets that demonstrate the viability of the proposed business model and of domestic production. Where relevant, CVDP milestones should complement technical milestones.

Strong applications will present evidence of existing or potential demand for the funded innovations; identify existing or potential customers, or categories of customers, at

volumes necessary for commercial viability; provide an initial assessment of marketability in terms of cost and value proposition that can be updated as the project advances; describe existing or potential competitors and competing technologies; and demonstrate the potential to attract private capital, such as venture capital.

CHIPS R&D strongly encourages applicants to identify approaches to maximizing market advantages of the funded innovation, such as by reducing manufacturing costs and improving yields (e.g., optimizing process times and achieving economies of scale through increasing volume). Other approaches could include addressing performance, availability, conformance to technical standards, and environmental sustainability.

For the purposes of 15 USC §4656(g) and the CVDP, "production" includes the manufacture, integration, assembly, testing, and packaging of semiconductor substrates and substrate materials. CHIPS R&D does not require the covered "production" to occur exclusively within the United States. However, applicants that are unable to conduct certain "production" activities in the United States should explain, to the extent practicable at the current level of technology development, why such production may not be possible, considering the following factors:

- The availability or lack of availability of domestic production capabilities, which may consider:
    - Planned or previous efforts made to locate, develop, or contract for the production of the CHIPS R&D-funded technology, or relevant similar technologies, in the United States;
    - Access to resources and other material inputs required for production;
    - The expected additional product development time or cost required to make U.S. production of the CHIPS R&D-funded technology commercially feasible;
- The relative costs of domestic versus foreign production of the CHIPS R&D-funded technology, at relevant production volumes;
- Commercial adoption risks and benefits, such as
    - Risks to the market acceptance and to the value proposition for the CHIPS-funded technology, resulting from U.S. production;
    - Expected commercial, economic, or national security benefits to the United States resulting from distributed production among U.S. and overseas sites;
- Any other factors that important to the success of the CHIPS R&D-funded technology.

1.6.3 Milestones and Phase-Specific Targets

Applicants should propose milestones that represent measurable steps toward achieving the applicant's Project-Level Technical Targets. Applicants should also propose milestones that represent measurable steps toward achieving the applicant's Project-level EWD Targets and CVDP Targets, as described in Sections 1.6.1 and 1.6.2. Applicants may also propose additional non-technical milestones.

Milestones for technical targets, EWD plan, and CVDP targets should be SMART (Specific, Measurable, Achievable, Relevant, and Time-Bound) and suitable for validation by the applicant, CHIPS R&D staff, independent expert technology evaluators, or a combination of these entities, as appropriate.

CVDP milestones should complement the technical milestones. For example, technical milestones should, as appropriate, inform CVDP targets and milestones such as manufacturing time, cost, performance, and projected customer demand. Additional CVDP milestones may include measurable progress in business plan development, customer identification, investor commitments, technology licensing agreements, and enabling manufacturing in the United States.

If an application stands a reasonable chance of being funded, CHIPS R&D may negotiate with the applicant to 1) refine the proposed milestones, and 2) define phase-specific targets derived from the proposed milestones. These phase-specific targets will inform go/revise/no-go points for the transition from one project phase to the next.

1.7 DEMONSTRATION DEVICES

Applicants should describe the design of a demonstration device appropriate to the intended substrate design and suitable for demonstrating the ability to successfully integrate the substrate into a simple, functional, and testable package. The design of the demonstration device may include (but is not limited to) embedding of passive and active components in/on the substrate, small testable dielet assemblies on the substrate at pitches relevant to project technical targets, and dielet assemblies on both sides of the substrate. The design of the device should be suitable for evaluation by an independent evaluator of the substrate's intended functionality, as set out in the application.

1.8 PROJECT PHASES

Applicants must propose a step-by-step technical plan (as defined in Section 4.6.1), for achieving both Project-Level Technical Targets and Project-Level Non-Technical Targets (i.e., EWD and CVDP targets). The technical plan must propose 4 phases of work, with each phase ranging in length from 3 months to 18 months. The project's total proposed period of performance must not exceed five years.

A hypothetical project timeline with the required four phases is shown in Figure 1 below.

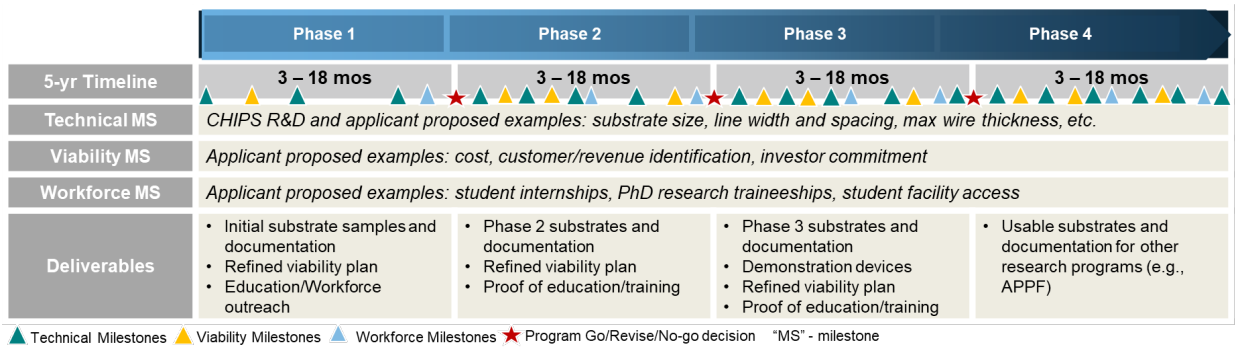

Figure 1: Hypothetical Project Timeline

1.8.1 Phase 1

CHIPS R&D expects activities in Phase 1 to include, as necessary, acquiring any required equipment and staff, demonstrating the capability for prototype-level substrate production, gathering appropriate data to refine CVDP plans, conducting initial education/workforce outreach efforts, and similar activities.

Phase 1 technical milestones should define progress toward achieving prototype-level substrate production. Phase 1 commercial viability and domestic production milestones should include, for example, progress in refining the CVDP plan, including gathering any relevant data.

Award recipients will be expected to deliver to CHIPS R&D or independent evaluators as applicable—

(1) Substrate samples for evaluation, including relevant documentation such as process assumptions, design manuals, process design kits (PDK), reliability criteria, and electrical specifications, each compatible with formats specified by CHIPS R&D during negotiation and with appropriate licensing provisions to protect IP rights;
(2) A refined CVDP plan; and
(3) Evidence of successful EWD outreach efforts.

Phase-specific targets marking go/revise/no-go decision points for transition from Phase 1 to Phase 2 will be finalized at the time of award.

1.8.2 Phase 2

CHIPS R&D expects activities in Phase 2 to include, for example, basic and applied research, innovations in process engineering, development and application of advanced metrology and testing capabilities, refining the CVDP plan based on technical progress, and implementing the EWD plan.

Phase 2 technical milestones should define progress toward achieving Project-level technical targets. Phase 2 CVDP milestones should leverage research and engineering progress to inform refinement and implementation of the CVDP plan and demonstrate progress towards the relevant project-level non-technical targets. Phase 2 EWD milestones should include implementing relevant programs, collecting data for assessing success metrics, and demonstrating progress towards the relevant project-level non-technical targets.

Award recipients will be expected to deliver to CHIPS R&D or to independent expert evaluators as applicable—

(1) Substrate samples for evaluation, including relevant documentation such as process assumptions, design manuals, process design kits (PDK), reliability criteria, and electrical specifications, each compatible with formats specified by CHIPS R&D during negotiation and with appropriate licensing provisions to protect IP rights;
(2) A refined CVDP plan and a detailed description of progress against the plan; and
(3) A refined EWD plan and a detailed description of progress against the plan.

Phase-specific targets marking go/revise/no-go decision points for transition from Phase 2 to Phase 3 will be finalized at the time of award.

1.8.3 Phase 3

CHIPS R&D expects activities in Phase 3 to include, for example, continued work on substrate development, additional basic and applied R&D on substrate integration and integration process engineering, development of device-level metrology and testing capabilities, refining and progressing against the CVDP plan, and continued progress against the EWD plan.

Phase 3 technical milestones should focus on achieving the project-level technical targets. Phase 3 CVDP milestones should leverage research and engineering progress to inform refinement and implementation of the CVDP plan and demonstrate progress towards the relevant project-level non-technical targets. Phase 3 EWD should include implementing relevant programs, collecting data and success metrics, and demonstrating progress towards relevant project-level non-technical targets.

Award recipients will be expected to deliver to CHIPS R&D or to independent evaluators as applicable—

(1) Substrate samples for evaluation, including relevant documentation such as process assumptions, design manuals, process design kits (PDK, compatible with NAPMP-specified formats and with appropriate licensing provisions to protect IP rights), reliability criteria, and electrical specifications;
(2) Demonstration devices in lots sufficient for independent evaluation (approximately 25 per lot);
(3) A refined CVDP plan and evidence of progress against the plan; and

(4) Data-driven evidence of progress against the EWD plan.

Phase-specific targets marking go/revise/no-go decision points for transition from Phase 3 to Phase 4 will be defined at the time of award.

1.8.4 Phase 4

CHIPS R&D expects Phase 4 activities to include—

(1) Scaling up from prototype-level substrate production (i.e., lots in the range of 25 substrate samples) to pilot-level substrate production (i.e., lots in the range of 250 substrate samples);
(2) Reimbursable provision of advanced substrates emerging from work in previous phases for use in other research projects designated by CHIPS R&D;
(3) Refining and implementing the CVDP plan based on initial pilot-level production experience; and
(4) A data-enabled analysis of EWD program progress.

Phase 4 technical milestones should focus on steps toward pilot-level production. Phase 4 CVDP milestones should reflect lessons learned in the process of scaling to pilot level substrate production. Phase 4 EWD should focus on data gathering and analysis of funded EWD programs.

1.8.5 Provision of Substrates for CHIPS R&D-Designated Research Projects

During Phase 4, CHIPS R&D aims to provide substrates developed under this NOFO to research projects in other areas of packaging research that would benefit from access to advanced substrates. Examples of these other research areas include new equipment, tools, and processes; innovation in power delivery and thermal management; novel chiplet and dielet technologies; and wired, radio frequency, and optical connectors. Examples of research projects include those associated with the APPF, the NSTC, Manufacturing USA Institutes, or other Federally funded research programs.

CHIPS R&D will expect recipients to deliver, along with substrate samples for use by other research projects, tools and documentation including process assumptions, design manuals, process design kits (PDK, compatible with NAPMP-specified format), and electrical specifications. CHIPS R&D will work with award recipients to ensure appropriate protections for the recipient's IP rights (see Section 2.8). For Phase 4 budgeting purposes, applicants should plan for a minimum of 100 substrate samples and a maximum of 1,000. NIST will allow award recipients to recover costs for producing these substrates for CHIPS R&D-designated research projects.

Options for providing substrates are direct, reimbursable provision of substrates by the applicant; licensing to other NAPMP-approved U.S.-based entities with capacity for

reimbursable production of substrates at pilot scale; or installing manufacturing capability in an NAPMP-funded facility, such as the planned APPF.

1.9 BROADER IMPACTS

CHIPS R&D is committed to building strong communities that share in the prosperity of the semiconductor industry, as well as ensuring that taxpayer investments maximize benefits for the U.S. economy. CHIPS R&D also strongly supports inclusion, diversity, equity, and access, and firmly believes that the semiconductor industry cannot succeed unless all Americans have an opportunity to participate, including individuals from underserved communities. In its evaluation and selection processes, CHIPS R&D will consider how projects will create broader impacts across the following dimensions:

1.9.1 Commitments to Future Investment

Ensuring U.S. leadership in semiconductor technology and the security and resilience of the domestic semiconductor supply chain will require sustained capital, R&D, and workforce investments. CHIPS R&D encourages applications that can induce larger-scale, private domestic investments into domestic prototyping and manufacturing facilities and equipment that would not have occurred absent an award under this NOFO. CHIPS R&D also encourages applications that demonstrate collaborations across the supply chain to clarify future demand, improve transparency and security, mitigate the risk of future chip shortages or oversupply, and support a more productive, efficient, and self-sustaining semiconductor ecosystem. In selecting applications for award, CHIPS R&D will therefore prioritize applications that include credible commitments, from the applicant or other entities participating in the project, to investing in R&D or semiconductor substrate manufacturing in the United States, as evidenced, for example, by letters of commitment or interest.

1.9.2 Support for other R&D Programs

Strengthening the role of the United States in semiconductor technology requires a robust and collaborative innovation ecosystem. Applicants should help ensure that this innovation ecosystem – which is critical to the semiconductor industry's long-term success – can flourish. CHIPS R&D will favorably consider applications that demonstrate a commitment to participating in the NSTC, the APPF, and if applicable, other semiconductor-related R&D initiatives established by the CHIPS Act[5] or CHIPS and Science Act (P.L. 117-167). These initiatives may include but are not limited to the NIST Manufacturing USA Institute(s) focused on semiconductor manufacturing; NIST Metrology research for microelectronics;

[5] For the purposes of this NOFO, the term "CHIPS Act" refers to Title XCIX of the William M. (Mac) Thornberry National Defense Authorization Act for Fiscal Year 2021, as amended (United States Code Title 15 Chapter 72A).

the NSTC Workforce Center of Excellence; the Department of Defense (DoD) National Network for Microelectronics Research and Development, also known as the Microelectronics Commons; semiconductor education activities at the National Science Foundation (NSF); and other similar initiatives. Further details will become available as these organizations develop their operational plans and membership programs.

Examples of possible activities include the following.

- Applicants could rotate project technical staff to the NSTC or train NSTC technical staff through exchanges.
- Applicants could provide process data to the NSTC to support aggregated large-scale datasets for training and manufacturing process optimization.
- Applicants could provide access to existing R&D facilities either as affiliated partners of the NSTC, the Microelectronics Commons, ongoing NSF programs, or independently.
- Applicants could provide the NSTC, APPF, Manufacturing USA, or Microelectronics Commons with donations of or access to equipment and/or design tools.
- Applicants could increase domestic public and industry access to process design kits to foster IP development, training and education, and improve foundry interoperability.

1.9.3 Creating Inclusive Opportunities

CHIPS for America strives for the inclusion of a broad array of partners, such as educational institutions, small businesses, minority-owned businesses, veteran-owned businesses, and women-owned businesses.[6] CHIPS R&D will favorably consider applications that, for instance:

- Outline robust outreach plans and demonstrate the inclusion of a broad array of partners in the funded activities, such as the above businesses as well as educational institutions (public, private, Historically Black Colleges and Universities (HBCUs), Minority Serving Institutions (MSIs), tribal colleges, etc.);
- Include meaningful leadership opportunities for early career researchers and for emerging research institutions; and
- Provide specific plans for training programs that expand opportunities for participation, including for underserved communities, such as building recruitment partnerships with community-based organizations, investing in pre-apprenticeship programs, investing in supportive services, and/or promoting a safe and respectful workforce culture that prevents harassment.

1.9.4 Environmental Responsibility

CHIPS R&D understands that semiconductor companies can reduce their environmental impact, improve the potential for domestic production, and further their competitive

[6] See Exec. Order No. 14080, 87 Fed. Reg. 52,847 (Aug. 25, 2022).

advantage by helping their customers meet sustainability and environmental goals. CHIPS R&D will favorably consider applications that identify metrics and milestones that demonstrate the capability of funded technologies to improve upon environmental outcomes of current methodologies and minimize the potential for adverse impacts on health, the environment, and the local community, including communities with environmental justice concerns, such as by reducing or eliminating the use of per- and polyfluoroalkyl substances (PFAS). All applicants are further encouraged to incorporate strategies for pollution prevention, energy efficiency, water efficiency, and renewable energy use in their project approach.

The Department expects applicants to design their projects so that they avoid, minimize, and mitigate the potential for significant effects on the human environment. While construction activities are not an eligible use of funds under this NOFO, certain activities may be subject to various Federal, state, and local environmental and permitting requirements, such as under the National Environmental Policy Act (NEPA), National Historic Preservation Act (NHPA), Endangered Species Act, Clean Water Act, Clean Air Act, Resource Conservation and Recovery Act, and related Executive Orders. Applicants must assist the Department with compliance with the above requirements and, where applicable, are responsible for obtaining and complying with Federal, state, and local permits.

CHIPS R&D will review full applications to determine whether they provide sufficient information to support NEPA and NHPA reviews, and may, at its discretion, request the applicant to provide additional information. The Department may request that an applicant prepare draft environmental analyses, which it will review to determine the potential environmental impacts and consultation needs of proposed activities under consideration for CHIPS R&D funds. CHIPS R&D may also request further supplementary written information or may ask questions during pre-selection interviews and/or site visits. CHIPS R&D will not issue an award until any required environmental review under NEPA for that award has been completed.

1.9.5 Community Impact and Support

CHIPS R&D aims to ensure that its semiconductor manufacturing incentives build strong communities that participate in the prosperity of the semiconductor industry, grow the U.S. economy, and support the creation of good jobs, such as those with working conditions consistent with the Good Jobs Principles. CHIPS R&D efforts can complement these goals by further strengthening or expanding regional semiconductor manufacturing and innovation ecosystems, including by facilitating the development of new or existing regional semiconductor industry clusters.[7] CHIPS R&D will favorably consider applications that demonstrate the impact of the project on regional ecosystems, either as a direct consequence of the project or by virtue of the anticipated research results. Project activities

[7] See Executive Order 14080, 87 Fed. Reg. 52847 (Aug. 25, 2022).

do not necessarily need to be completed within a specific geographic area to demonstrate an impact on a regional semiconductor industry cluster.

Applicants or members of project teams seeking to demonstrate community impact and support, including impact on a new or existing regional semiconductor industry cluster, can do so in a variety of ways, as relevant to the objectives and funded activities proposed under this NOFO, including through:

- Letters of commitment or interest from community-based organizations and local officials.
- Letters of commitment or interest from semiconductor and/or supply chain companies with operations or facilities in the selected region or in a relevant regional semiconductor industry cluster.
- Letters of commitment or interest from potential customers and/or other stakeholders.
- Co-investment from third parties and philanthropies.
- Partnerships with State, local, Tribal, and territorial governments and with institutions of higher education in the selected region.
- Partnership with entities focused on innovation, entrepreneurship, access to capital, and technology commercialization in the selected region.
- Partnerships with minority-owned businesses, veteran-owned businesses, women-owned businesses, Minority-serving Institutions (MSIs), including Historically Black Colleges and Universities (HBCUs), Tribal Colleges and Universities (TCUs), Hispanic Serving Institutions (HSIs), Asian American/Pacific Islander Institutions, and organizations that serve underserved communities.
- Alignment with regional, state, or local economic development strategies, such as relevant Comprehensive Economic Development Strategies[8], regional or cluster-based growth efforts, or other complementary Federal investments under programs such as the DOC Build Back Better Regional Challenge (BBBRC)[9], DOC Regional Technology and Innovation Hub (Tech Hubs) program[10], or NSF Regional Innovation Engines program[11], including through strong, concrete commitments to such programs' consortia and participation in consortium/coalition governance.

1.10 PROJECT ASSESSMENTS

CHIPS R&D retains sole discretion to determine whether a recipient has achieved phase-specific targets (including technical, education and workforce development, and commercial viability and domestic production targets). Similarly, CHIPS R&D has the sole

[8] https://www.eda.gov/resources/comprehensive-economic-development-strategy
[9] https://www.eda.gov/funding/programs/american-rescue-plan/build-back-better
[10] https://techhubs.gov
[11] https://new.nsf.gov/funding/initiatives/regional-innovation-engines

discretion regarding whether the applicant has met the requirements for each project-level and phase-specific target.

In making this judgment, CHIPS R&D may, as appropriate to the project phase, consider information provided by the applicant, including an assessment of substrate samples and demonstration devices.[12] Assessment of substrate samples and demonstration devices may be conducted, at CHIPS R&D's sole discretion, by CHIPS R&D or by an independent evaluator designated by CHIPS R&D, with appropriate protections for the applicant's IP rights.

Based on the results of substrate sample and demonstration device assessments, evaluation of overall progress, availability of funding, and continued alignment with CHIPS R&D priorities, CHIPS R&D, at its sole discretion, may decide at the end of each phase to proceed with the next increment of funding, request a revised plan from the applicant (subject to both the constraints of the approved award scope and budget and to CHIPS R&D approval), or terminate funding for the project.

1.11 GOVERNMENT-FURNISHED PROPERTY (GFP) AND GOVERNMENT FURNISHED INFORMATION (GFI)

Availability will be determined for each award. No GFP or GFI is identified to be provided at this time.

2 FEDERAL AWARD INFORMATION

2.1 FUNDING INSTRUMENT

Awards in this program will be made in the form of cooperative agreements or other transaction agreements, as appropriate. Where cooperative agreements are used, the nature of CHIPS R&D's "substantial involvement" will generally include collaboration with the awardee in executing the approved scope of work.

2.2 MULTI-YEAR FUNDING POLICY

When an application for a multi-year award is approved, funding will be provided only for the first phase of the project; additional phases will be funded incrementally. If a project is selected for funding, CHIPS R&D has no obligation to provide any additional funding in connection with that award. Funding for subsequent phases of a project will be contingent

[12] Samples and devices provided for evaluation are expected to be in lots of 25, with 20 from one production batch and 5 from randomly selected production batches.

upon satisfactory performance, continued relevance to the mission, goals, and priorities of the CHIPS Research and Development Office, and the availability of funds.

2.3 FUNDING AVAILABILITY

In FY24, CHIPS R&D anticipates making available approximately $300,000,000 for funding multiple awards. Individual awards will be funded in amounts up to approximately $100,000,000 and over a period of up to 5 years per award, not including voluntary co-investment. CHIPS R&D reserves the right to make an award, multiple awards, or no awards from this funding opportunity, subject to the availability of funds and the merit of applications received.

2.3.1 Eligible Uses of Funds

Eligible uses of funds include basic and applied research, substrate and demonstration device development and production, commercial viability and domestic production preparation, integrated workforce education and training, and pilot-level substrate production. Where consistent with the objectives of this NOFO, applicants may also propose to expend limited funds to protect innovations developed under this NOFO, including to cover fees for patent protection or to enhance research security.

2.4 INDIRECT (F&A) COSTS

CHIPS R&D will reimburse applicants for proposed indirect costs, commonly referred to as Facilities & Administrative (F&A) Costs, in accordance with 2 CFR §200.414. Applicants proposing indirect costs must follow the application requirements set forth in Sections 4.6.1.8 and 4.6.1.9 of this NOFO.

2.5 PUBLIC ACCESS TO CHIPS R&D RESEARCH

NIST is committed to the principle that the results of federally funded research are a valuable national resource and a strategic asset. To the extent feasible and consistent with law, agency mission, resource constraints, and U.S. national, homeland, and economic security, NIST will promote the deposit of scientific data arising from unclassified research and programs, funded wholly or in part by NIST, except for Standard Reference Data, free of charge in publicly accessible databases. Subject to the same conditions and constraints listed above, NIST also intends to make freely available to the public, in publicly accessible repositories, all peer-reviewed scholarly publications arising from unclassified research and programs funded wholly or in part by CHIPS R&D.

All applications for activities that will generate research data (see 2 C.F.R. § 200.315(e)(3)) using funding under this NOFO are required to adhere to a Data Management Plan (DMP) or explain why data sharing and/or preservation are not within the scope of the project (see Section 4.6.1.12).

2.6 FUNDAMENTAL RESEARCH

National Security Decision Directive (NSDD) 189 defines "fundamental research" as follows:

> *'Fundamental research' means basic and applied research in science and engineering, the results of which ordinarily are published and shared broadly within the scientific community, as distinguished from proprietary research and from industrial development, design, production, and product utilization, the results of which ordinarily are restricted for proprietary or national security reasons.*

Funded activities under this NOFO may include efforts categorized as fundamental research. In submitting an application, the applicant acknowledges that research activities considered to be fundamental research may include or produce IP with relevance to U.S. national or economic security and that requires protection against foreign interference and exploitation. As such, the applicant and any subrecipients agree to comply with the research security requirements described in Section 2.7 of this NOFO.

2.6.1 Fundamental Research Declaration

NIST/CHIPS reserves sole discretion to determine which elements of a proposed research project shall be considered fundamental research. However, applicants must indicate in the Project Narrative (see Section 4.6.1.6) whether, in the applicant's understanding, the proposed work includes fundamental research conducted either by the applicant or by subrecipient members of the project team.

2.6.2 On-Campus Research

Wherever feasible, NIST/CHIPS will seek to consider basic or applied research conducted on campus at a university as fundamental research.

2.6.3 Pre-Publication Reviews

Awards under this NOFO that include fundamental research will include appropriate language reaffirming the ability of the applicant and members of the project team to publish and share broadly the results of such fundamental research.

Awards under this NOFO that include research not deemed fundamental will prescribe publication requirements and other restrictions, as appropriate, for such research. This may include requirements for the applicant to submit publications describing work carried

out under this program for an efficient pre-publication review by NIST/CHIPS. The pre-publication review may result in a request for revisions to address national security concerns. The pre-submission review may also include an assessment of and advice to the award recipient regarding whether information disclosed in the publication could negatively impact the patent interests of either the award recipient or the Government.

2.7 RESEARCH SECURITY

It is NIST policy to create a culture of personal and organizational responsibility where the practice and management of research and its products are free from undue influence and interference not essential to the practice of science, such as personal or social allegiances, beliefs, or interests. NIST adheres to the principle that U.S. research leadership benefits from mutually beneficial international collaborations, including welcoming international scientists, and that U.S. national and economic security depends on effective risk management practices for all research organizations to protect against foreign interference and exploitation.

Founded on the NIST core values of perseverance, integrity, inclusivity, and excellence, the NIST Research Security and Safeguarding International Science Team promotes mutually beneficial international engagement using a risk-based methodology to safeguard NIST research programs and intellectual property.

2.7.1 Research Security Definitions

Unless otherwise noted, the definitions for terms used in this section are found in the Appendix to *Guidance for Implementing National Security Memorandum 33 (NSPM-33) on National Security Strategy for United States Government-Supported Research and Development* issued by the National Science and Technology Council (NSTC) in January 2022 (NSTC NSPM-33 Guidance).

2.7.2 Authorities[13]

In recent years, both Congress and the Executive Branch have focused on protecting R&D conducted or funded by Federal agencies from undue foreign influence. On January 14, 2021, National Security Presidential Memorandum-33 (NSPM-33) was issued to "strengthen protections of United States Government-supported R&D against foreign government interference and exploitation." NSPM-33 requires U.S. agencies that fund R&D to require the disclosure of information related to potential conflicts of interest and commitment from participants in the Federal R&D enterprise.

[13] It should be noted that Subtitle D of Title VI of the Research and Development, Competition, and Innovation Act, enacted along with the CHIPS Act, codified at 42 U.S.C. §§ 19231 – 19237 also contains research security requirements most of which are not yet in effect.

With Section 223 of Division A, Title II of the William M. (Mac) Thornberry National Defense Authorization Act (NDAA) for Fiscal Year 2021 (FY21), (Pub. L. No 116–283, codified in 42 U.S.C. §6605), Congress enacted into law certain NSPM-33 disclosure requirements for applicants for Federal R&D funds. Specifically, "covered individuals" (see Section 2.7.4) must disclose the amount, type and source of all current and pending research support, which includes both monetary and non-monetary support, and certify that the disclosure is current, accurate, and complete as part of the application for an R&D award. In addition, covered individuals must agree to update disclosures, as required, before and during the term of the award.

2.7.3 Requirement to Submit a Research Security Plan

Applicants to this NOFO must submit a written plan (see Section 4.6.1.6) identifying a member of applicant's leadership team to serve as the point of contact responsible for coordinating with NIST on research security issues and describing their internal processes or procedures to address cybersecurity, foreign government talent recruitment programs, conflicts of commitment, conflicts of interest, research security training, and research integrity.

2.7.4 Covered Individuals

The term "covered individual" is defined as "an individual (A) who contributes to a substantive, meaningful way to the scientific development or execution of a research and development project proposed to be carried out with a research and development award from a Federal research agency; and (B) is designated as a covered individual by the Federal research agency concerned."[14]

In developing the Project Narrative required under Section 4.6.1.6, the applicant must identify which individuals are covered individuals and provide a brief description (title or one-sentence summary) of the role to be served by each covered individual.

Covered individuals should include the principal investigator, co-investigators, and associate investigators and any individual listed by the applicant as "key personnel" under Sections 4.6.1.6 or as a "Senior/Key Person" in Section 4.6.1.8 of this NOFO or for whom a resume or CV is provided under Section 4.6.1.7. Personnel who participate only through isolated tasks that are incidental to the research (for example, setting up equipment or performing administrative functions), and those individuals who support research by executing discrete tasks as directed are not covered individuals. Consistent with guidance for implementing NSPM-33[15], disclosures from broader classes of individuals (e.g., certain graduate students and undergraduate students) will generally be unnecessary, except

[14] 42 U.S.C. § 6605(d)(1).
[15] https://www.whitehouse.gov/wp-content/uploads/2022/01/010422-NSPM-33-Implementation-Guidance.pdf.

when the activities of such an individual in a specific proposal rise to the level of meeting the definition of a "covered individual" under 42 U.S.C. §6605(d)(1).

2.7.5 Foreign Entities of Concern

Pursuant to 15 U.S.C. §4657, none of the funds awarded under this NOFO may be provided to a foreign entity of concern, as defined in 15 U.S.C. §4651 and implemented by the final rule entitled Preventing the Improper Use of CHIPS Act Funding, 88 FR 65600 (Sept. 25, 2023), codified at 15 C.F.R. 231.104.

2.7.6 Research Security Review and Risk Determination

The NIST Research Security and Safeguarding International Science Team will conduct a research security review and a risk determination of applications likely to be selected for award. In conducting this review, the NIST Research Security and Safeguarding International Science Team will review available information (e.g., the Current and Pending Support Form and Resume or CV) to assess whether the applicant or any covered individuals, including foreign nationals who are not lawful permanent residents or protected persons as defined in 8 U.S.C. §1324b(a)(3), are subject to any undue foreign influence or interference through conflicts of interest or conflicts of commitment. Undue foreign influence or interference may include, but not be limited to, associations or affiliations with foreign strategic competitors or governments of countries that have a history of intellectual property theft, research misconduct, or targeting U.S. technology for unauthorized transfer. Affiliations include any past or present organization (foreign and domestic) with whom the applicant has a formal relationship or obligation (e.g., universities, scholarships, professional societies, foreign talent recruitment programs).[16] The NIST Research Security and Safeguarding International Science Team will examine associations or affiliations during the ten-year period immediately preceding the application.

At the conclusion of the research security review for the application, the NIST Research Security and Safeguarding International Science Team will issue and provide to NIST/CHIPS a risk determination of a low, medium, or high risk of potential foreign interference or exploitation.

NIST will base its risk determination of the project and covered individuals on a totality of information, which may include but is not limited to:

- The ownership structure, subsidiaries, and obligations of the applicant, the project team, and any subrecipients, contractors, and/or unfunded collaborators;
- Conflicts of interest and conflicts of commitment of covered individuals;

[16] NIST IR 8484 at 47.

- Participation of covered individuals in a foreign government-sponsored talent recruitment programs;
- Any military-civil applications of the funded research, as applicable.

2.7.7 Non-Discrimination

Consistent with Section 10637 of the CHIPS and Science Act of 2022 and Executive Orders 13985 and 14031, NIST activities that implement NSPM-33 and 42 U.S.C. §6605 are carried out in a manner that does not inadvertently target, stigmatize, or discriminate against individuals on the basis of race, color, ethnicity, religion, sex (including pregnancy, sexual orientation, or gender identity), national origin, age (40 or older), disability, and genetic information (including family medical history), consistent with title VI of the Civil Rights Act of 1964 (42 U.S.C. 2000d et seq.).

2.7.8 Potential for Mitigation

If the NIST Research Security and Safeguarding International Science Team issues a risk determination that an application is high risk, NIST may, at its sole discretion, provide the applicant an opportunity to mitigate the assessed risk prior to CHIPS R&D making a final funding determination on the application. NIST/CHIPS R&D reserves the right to request specific mitigation actions, including but not limited to requiring additional training for project participants or segmentation of certain tasks of the proposed work, and any follow-up information needed to assess risk or mitigation strategies. CHIPS R&D may determine not to make an award for an application, despite any proposed mitigation terms.

2.7.9 Requirement for Recipients to Update Research Security-Related Information

Pursuant to 42 U.S.C. §6605(a)(1)(C), applicants have an ongoing duty to update the NIST Authorizing Officer of any changes made to the list of covered individuals or to the foreign affiliations and research financial and in-kind support of such individuals or of the applicant and subrecipients. Prior to NIST making an award under this NOFO, applicants must update the NIST Authorizing Officer of any such changes immediately; during a project's period of performance, award recipients must update the NIST Authorizing Officer within five (5) business days of such changes being made or of becoming aware of such changes.

Applicants and subrecipients are expected to reasonably exercise due diligence to ensure that covered individuals involved in the subject award are not subject to foreign interference or exploitation.

2.8 INTELLECTUAL PROPERTY (IP) AND DOMESTIC PRODUCTION

As set forth in 15 U.S.C. §4656(g), the Department of Commerce must develop policies for the domestic production, to the extent possible, of intellectual property resulting from R&D conducted under this NOFO. Further, 15 U.S.C. §4656(g) requires CHIPS R&D to develop domestic control requirements to protect such IP from foreign adversaries. For the purposes of 15 U.S.C. §4656(g), "intellectual property" means any invention that is or may be patentable under U.S. law; and "foreign adversaries" include any "foreign entity of concern" and "foreign country of concern," as those terms are defined in 15 U.S.C. §4651(7)-(8) and 15 C.F.R.§231.102, §231.104.

Consistent with these requirements, applicants must submit a Commercial Viability and Domestic Production (CVDP) Plan, as outlined in Sections 1.6.2 and 4.6.1.6, including milestones to demonstrate progress toward implementing the plan. Applicants must refine and update the CVDP plan during the period of performance, at a minimum before the end of each award phase. Applicants must also submit an Intellectual Property Rights Management Plan, as outlined in Section 4.6.1.6, and will be required to provide regular updates to the IP Rights Management plan to report any new or changed intellectual property or intellectual property governance structures.

For applicants who receive financial assistance through a cooperative agreement, the Standard Patent Rights Clauses described at 37 CFR 401.14 will apply to address inventions (including ownership, licensing, and utilization reporting). Regulations and terms, such as 2 CFR 200.315 and Section C.03 of the Department of Commerce Financial Assistance Standard Terms and Conditions will also apply.

For all financial assistance awards, including both cooperative agreements and other transaction agreements, CHIPS R&D will include special award terms and conditions related to intellectual property and domestic production and control, to meet the requirements of 15 U.S.C. §4656(g). The relevant terms and conditions will include, at a minimum, the following:

1. At least one domestic entity must own or co-own any intellectual property resulting from R&D conducted under this NOFO ("resulting intellectual property") and must have full rights to enforce the applicable intellectual property rights, at least for a period of years to be determined prior to the final award.
2. At the conclusion of the period of years, ownership of the resulting intellectual property may generally be sold, transferred, or assigned to a foreign entity that is not a foreign adversary.
3. In the event a domestic entity sells, transfers, or assigns ownership of the resulting intellectual property, the entity must promptly disclose such transaction to NIST prior to such transaction.

4. Any owner or co-owner of the resulting intellectual property (including successors in interest) may not sell, transfer, or assign ownership of such intellectual property to a foreign adversary.
5. Any owner of the resulting intellectual property may not license such intellectual property to a foreign adversary, subject to specific exceptions:
    a. This restriction is not applicable to any patent(s) or published patent application(s) (i) declared and/or determined to be essential to a technical standard and (ii) under an obligation that the owner of the patent or published patent application license such rights pursuant to the terms of a standards development organization's Intellectual Property Rights policy.
    b. This restriction is not applicable to any license(s) of patent(s) or published patent application(s), including cross-licenses, resulting from settling an actual case or controversy, including patent infringement or validity disputes, whether part of a formal proceeding or not.
    c. In the event an owner or co-owner of the patent(s) resulting from R&D conducted under this NOFO determines that any of the specific exceptions applies and plans to license such patent(s) to a foreign adversary pursuant to the exception(s), the owner or co-owner must promptly disclose for NIST review such action.

CHIPS R&D will also be releasing additional information about these required award terms and conditions, which will be posted on the CHIPS R&D website.

3 ELIGIBILITY INFORMATION

3.1 ELIGIBLE APPLICANTS

Eligible applicants include domestic for-profit organizations; non-profit organizations; accredited institutions of higher education including community and technical colleges; and state, local, territorial, and Indian tribal governments.

Eligible applicants may only submit one concept paper under this NOFO. Entities may not be included as subrecipients on more than two concept papers.

3.1.1 Federally Funded Research and Development Centers

Entities that operate Federally Funded Research and Development Centers (FFRDCs) may participate in awards as subrecipients or contractors, to the extent allowed by law, based on the unique and specific needs of the project. Applicants must identify the FFRDC(s) in the Project Narrative and provide documentation attached to the required letter of

commitment (see Section 4.6.1.11) establishing that FFRDC subrecipients and contractors are able to participate in the proposed work, including:

1. Documentation demonstrating that the proposed work does not compete with the private sector; and
2. Documentation from the FFRDC's sponsoring institution citing the FFRDC's eligibility to participate in competitive Government funding opportunities; the FFRDC's compliance with the sponsor agreement; and confirmation from the sponsoring agency that they can receive Federal funds from NIST.

FFRDCs interested in participating in this NOFO should first contact their sponsoring agency to discuss their eligibility to receive federal funds under this NOFO.

3.1.2 Federal Entities

Federal Entities (e.g., Federal departments and agencies, military services educational institutions, etc.) are eligible to participate in this NOFO as subrecipients or contractors, to the extent allowed by law and subject to applicable direct competition limitations. Federal Entities must clearly demonstrate that the work is not otherwise available from the private sector and provide written documentation citing the specific statutory authority and contractual authority, if relevant, establishing their ability to receive Federal award funds and compete with industry. Applicants must identify the Federal entity in the Project Narrative and provide documentation attached to the required letter of commitment (see Section 4.6.1.11) establishing that Federal entity is able to participate in the proposed work.

3.1.3 Individuals and Unincorporated Sole Proprietors

Individuals and unincorporated sole proprietors are not eligible to receive funding under this NOFO in any form.

3.1.4 Foreign Partners and Foreign Research Activities

Foreign organizations may participate as members of a project team, as subrecipients or contractors, subject to CHIPS R&D approval.

3.1.4.1 Foreign Partner Justification

CHIPS R&D must provide written approval for a foreign organization's participation in a funded project prior to the foreign organization's engaging in any project-related work. The applicant must provide CHIPS R&D with a written justification demonstrating:

1. that the foreign partner's involvement is essential to advancing program objectives, such as by offering access to unique facilities, IP, or expertise that is otherwise not readily available in the United States;

2. the adequacy of any agreements and protocols between the applicant and foreign partner regarding IP protection and data protection;
3. the partnership does not jeopardize the soundness of the project's proposed pathway to domestic production;
4. as applicable, the foreign partner will comply with any necessary nondisclosure agreements, security regulations, export control laws, audit requirements, and other governing statutes, regulations, and policies;
5. the foreign partner is not based in a foreign country of concern as defined at 15 U.S.C. §4651(7) and implemented by the final rule entitled Preventing the Improper Use of CHIPS Act Funding, 88 FR 65600 (Sept. 25, 2023), codified at 15 C.F.R. §231.104; and
6. the foreign partner agrees to be subject to a national security review by CHIPS R&D, which may include a risk assessment of IP leakage, if appropriate.

3.1.4.2 Location of funded activity

While the work funded under this NOFO is to be conducted within the United States, certain tasks outside the United States may be allowed based on the unique and specific capabilities of the foreign partner, their relevance to the project objectives, and the lack of comparable capabilities in the United States. CHIPS R&D's determination regarding the performance of project tasks outside the United States will be based on information provided by the applicant and by other Federal agencies.

CHIPS R&D will only approve work outside of the United States if it is in the best interest of CHIPS R&D and the United States, including the domestic economy generally, U.S. national security, U.S. industry, and U.S. manufacturing competitiveness.

3.1.4.3 Transferring funding to a foreign entity

While applicants may invite eligible foreign partners to join project teams as subrecipients or contractors, any disbursement of funds outside the United States, whether by an awardee, subrecipient, or contractor, must be approved by CHIPS R&D.

In making such a determination, CHIPS R&D will consider whether the disbursement of funds as proposed advances the economic or national security interests of the United States and the justification described in Section 3.1.4.1.

CHIPS R&D will not approve the disbursement of funds to an entity in or under the control of a country of concern under any circumstances.

3.2 CO-INVESTMENT

3.2.1 Provisions.

Non-Federal co-investment (cost share) over the lifetime of the award is strongly encouraged but not required. Non-Federal co-investment is that portion of the project costs not borne by the Federal government. Co-investments may include cash, services, and third-party in-kind contributions, as described at 2 CFR § 200.306. Applicants may propose other types of co-investment provided that the proposed co-investment is allocable and necessary to the success of the project.

3.2.2 Allocation.

The source and detailed rationale of the co-investment, including cash, full- and part-time personnel, and in-kind donations, must be documented in the Research and Related Budget (Total Fed + Total Non-Fed) form and Budget Narrative and Justification submitted with the full application and may be considered as part of the review described in Section 5 of this NOFO. As with the Federal share, any co-investment specifically pledged on a voluntary basis in the proposal's budget will become a binding requirement of any Federal award. Co-investments must be allowable/eligible costs under this program and under the applicable cost principles per Section 3.3. The value of co-investment to be provided by any subrecipients may be determined using Generally Acceptable Accounting Principles (GAAP). For instructions on incorporating co-investment into the Research and Related Budget (Total Fed + Total Non-Fed) form and the Budget Narrative and Justification, see Section 4.6.1.8.

3.3 ALLOWABLE COSTS

Awards in this program will be made in the form of cooperative agreements or other transaction agreements, as appropriate, and at the sole discretion of NIST.
For purposes of submitting an application, costs must be reasonable, allocable, and allowable per the established federal cost principles set forth under 2 CFR Part 200 Subpart E, Cost Principles. Information on cost allowability is available in the Uniform Administrative Requirements, Cost Principles, and Audit Requirements for Federal Awards at 2 C.F.R. Part 200. Adjustments to this requirement may be required at NIST's sole discretion for other transaction agreements.

4 APPLICATION AND SUBMISSION INFORMATION

4.1 OVERVIEW

The application process consists of a mandatory concept paper and a required full application. Full applications will only be accepted from applicants invited after the concept paper stage.

Eligible applicants may only submit one concept paper under this NOFO. No entity may be included as a subrecipient on more than two concept papers.

Applicants should be on alert for any amendments to this NOFO that may adjust submission dates, times, or other submission requirements. Any amendments will be posted to grants.gov. All submissions must be unclassified. The Government will not reimburse applicants for any costs associated with participation in this NOFO process. Likewise, the cost of preparing concept papers and full applications in response to this NOFO is not an allowable charge (direct or indirect) under any Federal award.

4.2 ADDRESS TO REQUEST APPLICATIONS PACKAGE

The application package for full proposals is available at Grants.gov under Funding Opportunity Number 2024-NIST-CHIPS-NAPMP-01.

4.3 PAGE COUNT GUIDANCE

This NOFO identifies strict limitations on page counts for the concept paper and full application. As part of its initial administrative review, CHIPS R&D will redact any pages received in excess of the stated page limits prior to beginning the merit review. The applicant should refer to Tables 3 and 4 to determine which documents and forms are included and excluded in page count limits for concept papers and full applications, respectively.

4.4 SUBMISSION FORMAT

Applicants must send an email to research@chips.gov with "2024-NIST-CHIPS-NAPMP-01 Concept Papers" in the subject line to request instructions for submitting Concept Papers. Applicants are strongly advised not to wait until the last minute to request submission instructions. The CHIPS R&D Program will respond by email with instructions for securely submitting a Concept Paper. Full applications must be submitted using Grants.gov.

Applicants should consult Section 4.5 for concept paper submission and follow guidance on Grants.gov and the information in Section 4.6 for full application submission, including requirements for uploading specific required forms. A concept paper or full application received after the due date and time will NOT be evaluated or considered for an award.

Applicants should carefully follow specific Grants.gov instructions to ensure that all attachments will be accepted by the Grants.gov system. A receipt from Grants.gov indicating an application is received does not provide information about whether attachments have been received. For further information or questions regarding applying electronically for the 2024-NIST-CHIPS-NAPMP-01 NOFO, contact the Grants.gov Help Desk at 800-518-4726.

Document formatting requirements are specified to ensure the readability of the document by reviewers. Neither the concept paper nor application should contain any hyperlink references used solely to circumvent any page restrictions. All information critical for the application must be contained within the specified page limits. See Tables 3 and 4 for the page limits for concept papers (Section 4.5.2) and applications (Section 4.6.3).

4.4.1 Amendments.

Any amendments to this NOFO will be announced through Grants.gov. Applicants may sign up on Grants.gov to receive amendments by e-mail.

4.4.2 Proprietary and Sensitive Business Information

Applicants must clearly identify proprietary information in their Concept Papers and Full Applications. Submissions containing proprietary or sensitive business information must have the cover page and each page containing such information clearly marked with a label such as “Proprietary” or “Sensitive Business Information” and provide an indication as to what specific information is proprietary or sensitive.

Applicants must not submit classified information.

4.5 CONCEPT PAPERS

The required content and form of concept papers submitted pursuant to this NOFO are set forth below.

4.5.1 Required Forms and Documents

The concept paper submission must contain the following.

a. **Cover Sheet -** The cover sheet is a one-page document providing:
   - NOFO Name and Reference Number (FY2024 CHIPS R&D National Advanced Packaging Manufacturing Program (NAPMP) Materials & Substrates, 2024-NIST-CHIPS-NAPMP-01)
   - Concept paper submission date
   - Relevant technical areas
   - Name of the applicant
   - Name of the project director(s)/principal investigator(s)
   - Any major subrecipients
   - Proposal title
   - Point of Contact for the applicant, to include name, address, telephone number, and business e-mail address
   - Total funds requests and total proposed co-investment (if applicable)
   - Any statement regarding confidentiality, including proprietary or sensitive business information, if applicable

The cover sheet does not contribute to the concept paper narrative page limit.

b. **Concept Paper Executive Summary and Quad Chart** - The executive summary is a one-page summary/abstract suitable for dissemination to the public and must not include any classified information or proprietary or sensitive business information. It should be a self-contained document that identifies the name of the applicant, the project director(s)/principal investigator(s), the application title, the objectives of the proposed team, and the intended impacts (i.e., benefits, outcomes) of the proposed project, including both technical and education/workforce goals. The quad chart is in a format selected by the applicant and must contain a problem statement and proposed solution, the concept of the proposed project, technical objectives, and key participants.

   While the executive summary and the quad chart do not contribute to the Concept Paper Narrative page limit, they must not exceed one (1) page each. Any materials provided beyond the one (1) page limit for the executive summary and the one (1) page limit for the quad chart will be redacted and not provided to the reviewers. The executive summary and quad chart must not contain proprietary or confidential information.

c. **Table of Contents** (This does not contribute to the Concept Paper Narrative page limit)

d. **Concept Paper Narrative -** The concept paper narrative is a word-processed document of no more than ten (10) pages and must not include any classified information. Applicants must clearly identify proprietary information in their Concept Paper Narrative. Submissions containing proprietary or sensitive business information must have the cover page and each page containing such

information clearly marked with a label such as "Proprietary" or "Sensitive Business Information" and provide an indication as to what specific information is proprietary or sensitive.

e. The concept paper must contain the following to be considered for initial review:

i. Project Impact Statement
- Provide a clear problem statement and well-defined project outcomes, explaining how both are relevant to the CHIPS R&D mission and goals (See Section 1.1.1) and the objectives of this NOFO, as expressed in Section 1.1.3.
- Describe the project's contribution to economic and national security, as expressed in the evaluation criteria in Section 5.1.1.

ii. Project Plan – Provide an overview of the project plan, including each of the following aspects:
- A description of how the planned project and proposed team contribute to U.S. advanced packaging needs and the objectives of this NAPMP NOFO (See Section 1.1.3).
- An outline of the proposed approach, including intended technical areas (e.g., organic, glass, silicon), and Project-level Technical Targets (see Section 1.5). The applicant should provide a rationale for selecting the Project-level Technical Target(s), why the target(s) represent a significant but achievable technical advance, and the innovativeness of their approach to achieving the target(s).
- An outline of plans for transitioning the proposed technology to commercial deployment.
- A description of how the proposed project will address each of the evaluation criteria and selection factors identified in Section 5.1.
- An outline of the overall education and workforce plan, including the targeted educational or professional levels, support mechanisms (e.g., internships and traineeships).

iii. Project Team – For purposes of this NOFO a project team comprises all funded entities (the applicant and any proposed subrecipients) as well as unfunded collaborators planned for inclusion in a single proposal. The lead institution will be the applicant entity for at the full application stage and must have substrate prototyping capability or describe a plan for achieving that capability within 3 months of receiving an award. The Concept Paper Narrative must address each of the following topics:
- Describe the capabilities of the lead institution, including required substrate prototyping capability. For each of the following, provide a description where applicable or indicate 'no current capability.'
    - Previous experience in developing and producing substrates at prototype scale (i.e., lots of 25) or greater, including substrate types

relevant to the proposed project, types of buildup layers, and relevant dimensions such as pitches, vias, and substrate areas.
    - Previous experience in using substrates, including volumes of such use in parts per month.
    - Types of equipment and materials currently used in developing and manufacturing substrates at prototype scale or above.
    - Manufacturing capability for equipment used in building substrates.
- Describe the planned role for additional team members (subrecipients and unfunded collaborators) and the capabilities each bring that are essential to the planned proposal, including any substrate prototyping capability beyond that of the lead institution. Include in this description the following required capabilities:
    - Materials supplier
    - Component Integrator
    - Equipment provider
    - Research and innovation capability, including innovation capabilities provided by academic research team members
    - Education and workforce development capability
- As an appendix to the concept paper (not included in the page limit), provide a letter of commitment from each planned team member indicating their intention to participate and the capabilities they expect to provide to the proposed project.

iv. **Budget Estimate** – Confirm that the estimated total budget request for the project does not exceed the per award limit under this NOFO of approximately $100,000,000.

4.5.1.1 Letters of Interest

Letters of interest are optional and, where included, should indicate willingness from any third party to support this proposed effort. Letters of Interest should outline the nature and importance of the collaboration or involvement being offered. Letters of interest may also be from non-proposing entities wishing to vouch for the applicant's knowledge, skills, or abilities to conduct the proposed work or to express interest as potential customers for or users of the technologies to be developed under the project plan, including those with commercial, national security, or critical infrastructure interests. Letters of interest do not contribute to the Concept Paper Narrative page limit.

4.5.2 Concept Paper Format and Guidelines

Table 3. Concept Paper Format and Guidelines

E-mail Submissions.	Applicants must send an email to research@chips.gov with "2024-NIST-CHIPS-NAPMP-01 Concept Papers" in the subject line to request instructions for submitting Concept Papers. Applicants are strongly advised not to wait until the last minute to request submission

	instructions. The CHIPS R&D Program will respond by email with instructions for securely submitting a Concept Paper.
Figures, Graphs, Images, and Pictures	Should be of a size that is easily readable or viewable and may be landscape orientation.
Font	Use one of the following fonts: • Arial (not Arial Narrow), Courier New, or Palatino Linotype at a font size of 10 points or larger; • Times New Roman at a font size of 11 points or larger; or • Computer Modern family of fonts at a font size of 11 points or larger.
Line Spacing	Single.
Margins	One (1) inch top, bottom, left, and right.
Page layout	Portrait orientation only except for figures, graphs, images, and pictures.
Page Limit.	Ten (10) pages for concept paper narrative.
Page limit includes	Concept paper including any Figures, Graphs, Images, and Pictures.
Page limit excludes	Cover Sheet; Table of Contents, Executive Summary and Quad Chart; Letters of Interest.
Page numbering	Number all pages sequentially.
Paper size	21.6 cm by 27.9 cm (8 ½ inches by 11 inches) with 2.5 cm (1 inch) margins.
Application language	English.
Typed document	All applications, including forms, must be typed.

4.6 FULL APPLICATIONS

Full applications will only be accepted from applicants invited after the concept paper stage. Submissions from entities other than those specifically invited to submit a full application will not be reviewed or considered in any way.

The required content and form of applications submitted pursuant to this NOFO are set forth below.

4.6.1 Required Forms and Documents

The Full Application must contain the following:

4.6.1.1 SF-424 (R&R), Application for Federal Assistance

The SF-424 (R&R) must be signed by an authorized representative of the applicant organization. For SF-424 (R&R), Items 5, 14, and 19, use the Zip Code + 4 format (##### - ####) when addresses are requested.

The list of certifications and assurances referenced in Item 17 of the SF-424 (R&R) is contained in the Federal Financial Assistance Certifications and Representations (Certs and Reps) as part of the SAM.gov entity registration.

SF-424 (R&R), Item 18. If the SF-LLL, Disclosure of Lobbying Activities form (Section 4.6.1.5 below) is applicable, attach it to field 18.

Instructions for filling in the SF-424 (R&R) can be found on Grants.gov, as well as at the NIST Grants Office SF-424 Research & Related(R&R) Application Package Guidance.

4.6.1.2 Research & Related Budget (Total Fed + Non-Fed)

The budget should reflect anticipated expenses for the full term of the project, considering all potential cost increases, including cost of living adjustments.

The budget should be detailed in these categories:

A. Senior/Key Person;
B. Other Personnel;
C. Equipment Description;
D. Travel;
E. Participant/Trainee Support Costs;
F. Other Direct Costs;
G. Direct Costs (automatically generated);
H. Indirect Costs;
I. Total Direct and Indirect Costs (automatically generated);
J. Fee (not relevant to this competition);
K. Total Costs and Fee (automatically generated);
L. Budget Narrative and Justification document (item (8) below) should be attached to field L.

A separate detailed R&R Budget must be completed for each budget period during the proposed award (e.g., annual basis). To add additional budget periods (e.g., year 2), click "Add Period" embedded at the end of the form. Information regarding the Research & Related Budget (Total Fed + Non-Fed) is available in the R&R Family Section of Grants.gov, as well as at the NIST Grants Management Division SF-424 Research & Related (R&R) Application Package Guidance.

4.6.1.3 CD-511, Certification Regarding Lobbying

Enter "2024-NIST-CHIPS-NAPMP-01" in the Award Number field. Enter the title of the application, or an abbreviation of that title, in the Project Name field.

4.6.1.4 Research and Related Other Project Information

Answer the highlighted questions and use this form to attach the Project Narrative (item 4.6.1.6 4 below), the Indirect Cost Rate Agreement (item 4.6.1.9), the Letters of Commitment and Interest, if applicable, (item 4.6.1.11 below), the Data Management Plan (item 4.6.1.12 below), and the Current and Pending Support Form (item 4.6.1.13 below). Instructions for completing the Research and Related Other Project Information form can be found in the Grants.gov R&R Forms Repository by scrolling down to Research And Related Other Project Information and clicking the Instructions link, as well as in the NIST Grants Management Division SF-424 Research & Related (R&R) Application Package Guidance. Research And Related Other Project Information and clicking the Instructions link, as well as in the NIST Grants Management Division SF-424 Research & Related (R&R) Application Package Guidance.

4.6.1.5 SF-LLL, Disclosure of Lobbying Activities

Complete this form if applicable.

4.6.1.6 Project Narrative

The Project Narrative is a word-processed document of no more than twenty (20) pages (single-spaced between lines), which is responsive to the program description and the evaluation criteria. The Projective Narrative for the full application should contain the following information and required elements:

a. **Cover Sheet.** (This does not contribute to the number of pages.) The cover sheet is a one-page document providing:
   - NOFO Name and Reference Number (FY2024 CHIPS R&D National Advanced Packaging Manufacturing Program (NAPMP) Materials & Substrates, 2024-NIST-CHIPS-NAPMP-01)
   - Concept paper submission date
   - Relevant technical areas
   - Name of the applicant
   - Name of the project director(s)/principal investigator(s)
   - Any major subrecipients and contractors
   - Project title
   - Point of Contact for the applicant, to include name, address, telephone number, and business e-mail address

- Total funds requests and total proposed co-investment (if applicable)
- Any statement regarding confidentiality, including proprietary or sensitive business information, if applicable

b. **Executive Summary.** (This does not contribute to the number of pages.) A concise summary/abstract of the proposed effort. The summary/abstract must contain a summary of the proposed activity suitable for dissemination to the public. It should be a self-contained document that identifies the name of the applicant, the project director(s)/principal investigator(s), the application title, the objectives of the proposed team, a description of the proposed team, methods to be employed, the potential impact of the proposed team (i.e., benefits, outcomes), and major participants (for collaborative team activities). This document must not include any classified information or proprietary or sensitive business information as CHIPS R&D may make it available to the public after awards are issued. A table can be helpful in providing this information. The executive summary shall not exceed two (2) pages.

c. **Table of Contents.** (This does not contribute to the number of pages.)

d. **Project Description**. A description of the proposed project covering each of the items below and sufficient to permit evaluation of the application in accordance with the Evaluation Criteria (see Section 5.3). The Project Description must not include any classified information. Applicants must clearly identify proprietary information in their Project Description. Submissions containing proprietary or sensitive business information must have the cover page and each page containing such information clearly marked with a label such as "Proprietary" or "Sensitive Business Information" and provide an indication as to what specific information is proprietary or sensitive.

   i. **Project Impact Statement**
      - Provide a clear problem statement and well-defined project outcomes, explaining how both are relevant to the CHIPS R&D mission and goals (See Section 1.1.1) and the objectives of this NOFO, as expressed in Section 1.1.3.
      - Describe the project's contribution to economic and national security, as expressed in the evaluation criteria in Section 5.3.
      - Provide, if applicable, evidence of known or expected impacts to the U.S. Department of Defense, other government systems, critical infrastructure, and/or to advancing domestic production.

   ii. **Project Team**
      - For purposes of this NOFO, a team comprises all funded entities (recipient and subrecipients) as well as unfunded collaborators included in the application. The applicant must have substrate prototyping capability or describe a plan for achieving that capability within 3 months of receiving an award.

- Describe the capabilities of the applicant, including required substrate prototyping capability, that make it suitable to lead the proposed project. For each of the following, provide a description where applicable or indicate 'no current capability.'
    - Previous experience in developing and producing substrates at prototype or greater scale (i.e., lots of 25), including substrate types relevant to the proposed project, types of buildup layers, and relevant dimensions such as pitches, vias, and substrate areas.
    - Previous experience in using substrates, including volumes of such use in parts per month.
    - Types of equipment and materials currently used in developing and manufacturing substrates at prototype scale or above.
    - Manufacturing capability for equipment used in building substrates.
- Describe the planned role for additional team members (subrecipients and unfunded collaborators) and the capabilities each bring that are essential to the planned proposal, including any substrate prototyping capability beyond that of the applicant. Include in this description the following required capabilities.
    - Materials supplier
    - Integrator
    - Equipment provider
    - Research and technology capability, including innovation capabilities provided by academic research team members
    - Education and workforce development capability, including a description of relevant partners (e.g., private, public, HBCU, MSI, Tribal colleges, etc.)

iii. **Roles and Responsibilities**

- Provide an organizational chart showing key management positions.
- Describe the roles and responsibilities for each position in the organizational chart.
- Describe the reporting relationships among the positions in the organizational chart.
- Provide the names and roles of all key personnel contributing to the project, including individuals not listed on the organizational part as in key management positions.

iv. **Technical Plan**

- Describe project-level technical targets selected from the categories in Section 1.5 and any additional targets.
- Describe the choice of embedded substrate features (Section 1.5.2), including how this choice may advance or enhance U.S. leadership in substrate offerings and how any chosen embedded substrate features may affect the ability to achieve project-level technical targets.
- Describe the design of the proposed demonstration device for use in Phase 3 and explain how this design is suitable for demonstrating the ability to integrate the substrate into a simple, functional, and testable package.
- Consistent with the overall scientific and technical merit evaluation criterion in Section 5.3, provide an assessment of the current technological state of the art and the projected state of art resulting from this project.
- Describe project Phases 1-4 in terms of measurable steps toward achieving project level goals, noting the feasibility and innovativeness of the required actions and any gaps, constraints, and challenges to address.
- Provide SMART (Specific, Measurable, Achievable, Relevant, and Time-Bound) milestones at approximately quarterly intervals and a corresponding Gantt Chart with timeline covering project Phases 1-4.

v. **Education and Workforce Development Plan**

- Describe the overall education and workforce plan (see Section 1.6.1), including the targeted educational or professional levels, support mechanisms (e.g., internships, Registered Apprenticeships and pre-apprenticeships with direct links to Registered Apprenticeship Programs, and traineeships), and the roles and responsibilities of relevant participating organizations, such as accredited educational institutions, labor organizations, or other workforce training organizations.
- Provide SMART (Specific, Measurable, Achievable, Relevant, and Time-Bound) project-level targets (e.g., number of students graduated and/or hired) and milestones for assessing progress toward targets at approximately semiannual intervals and a corresponding Gantt Chart with timeline covering project Phases 1-4.
- Provide evidence of alignment with U.S. industry needs, such as demonstrated linkages between the skills to be developed in the programs and available jobs or to industry-recognized credentials or certifications. Other evidence may include letters of interest from potential employers and labor organizations.

- Describe any efforts to maximize access to and participation in the semiconductor workforce, including efforts to attract and retain a diverse student and trainee population such as supportive services and outreach to underserved communities.
- Describe any physical or virtual infrastructure that will be made available to support education and workforce training programs.

vi. **Commercial Viability and Domestic Production Plan**

- Provide a Commercial Viability and Domestic Production Plan (See Section 1.6.2), including a timeline with SMART milestones at approximately semiannual intervals demonstrating the viability of the proposed business model (see below) and of the pathway to domestic production (see below), and a corresponding Gantt Chart with timeline covering project Phases 1-4. Where relevant, milestones should complement technical milestones.
- Describe the business model, including an initial assessment of the funded innovation's marketability, considering factors such as cost competitiveness, value proposition, and the impact of competitor products.
- Describe the technology transition plan and pathway to domestic production and, if relevant, the potential for adoption for commercial or defense uses. If relevant, identify any mitigating factors, as described in Section 1.6.2. Identify any relevant approaches to maximizing the market advantages of the funded innovation, such as through improving cost-efficiency, performance, manufacturing yield, and process times.
- Provide an overview of current or expected customer demand at the volumes required for commercial viability, including examples of possible top customers or categories of customers, and plans for engaging with the customer ecosystem as the project advances.

vii. **Broader Impacts Statement**

- Consistent with Section 1.9, provide an overview of the proposed project's broader impacts, such as commitments to future investment, support for other R&D programs, creating inclusive opportunities, climate and environmental responsibility, or community impact and support.
- If relevant, identify impacts on a new or existing regional semiconductor industry cluster.
- If relevant, identify any known or potential collaborations across the supply chain, IP rights or licensing plans, or investments into domestic prototyping and manufacturing facilities that would result from this project.

- If relevant, describe the potential for the funded innovation to attract private capital and induce larger-scale, private domestic investments into domestic prototyping.
- While construction activities are not an allowable cost under this program, costs related to internal modifications of existing buildings may be allowed, at NIST discretion. Where such costs are proposed, a description of whether and how the applicant intends to utilize domestically produced iron, steel, and construction materials as part of their projects, including for non-Federal entities[17] how they plan to meet any applicable legal requirements pursuant to the Build America, Buy America Act.

viii. **Fundamental Research Declaration** (Not to exceed 2 pages. This does not contribute to the Project Narrative page limit.)
- Identify which of the proposed research activities, if any, the applicant believes NIST/CHIPS R&D should consider as fundamental research and the rationale for that determination.
- For any proposed fundamental research, identify the involved project team member. Note that NIST/CHIPS R&D reserves sole discretion to determine which elements of a proposed research project shall be considered fundamental.

ix. **Research Security Plan** (Not to exceed 5 pages. This does not contribute to the Project Narrative Page limit.)
- Provide a written plan describing internal processes or procedures to address foreign talent recruitment programs, conflicts of commitment, conflicts of interest, research security training, and research integrity. Provide a point of contact on research security issues within the project leadership team.
- Cybersecurity should be addressed in the planning, design, and project oversight phases for all awards. Applicants must describe measures taken to ensure that appropriate practices for cybersecurity, such as the NIST Cybersecurity Framework and Cybersecurity and Infrastructure Security Agency (CISA) Cybersecurity Performance Goals (CPGs) are incorporated in the project.[18]

x. **Intellectual Property Rights Management Plan** (Not to exceed 5 pages. This does not contribute to the Project Narrative Page limit.)

[17] Non-Federal entity (NFE) means a State, local government, Indian tribe, Institution of Higher Education (IHE), or nonprofit organization that carries out a Federal award as a recipient or subrecipient (see M-24-02).
[18] The CISA performance goals provide a baseline set of cybersecurity practices that are broadly applicable, with known risk-reduction value. They also allow applicants the ability to measure and improve their cybersecurity maturity, and a combination of recommended practices for IT and OT owners, including a prioritized set of security practices.

- Clearly identify (1) any pre-existing IP (which may include patents, proprietary information, etc.) that will be used in completing the project, (2) IP that may be developed with funding under this NOFO, and (3) the path through which any partners who may join later could access the above IP.
- For all awards regardless of type, describe any desired deviations from standard regulations and terms, such as 2 CFR 200.315 and Section C.03 of the Department of Commerce Financial Assistance Standard Terms.
- Describe how the proposed management and ownership of IP support the Commercial Viability and Domestic Production Plan and any existing or planned protocols to ensure domestic control of CHIPS R&D-funded intellectual property, including to protect such intellectual property from foreign adversaries (see Section 2.8).
- Describe any additional licensing provisions to protect IP rights, as relevant to the provision of documentation such as process assumptions, design manuals, process design kits, as described in Section 1.8.

xi. **Physical Infrastructure** (Not to exceed 2 pages. This does not contribute to the Project Narrative page limit.)
- Describe the physical location(s) of project team members and the associated physical infrastructure capabilities relevant to achieving the project-level targets.
- Describe existing or planned facilities to be used for substrate and demonstration device production, including detailed plans and timelines for creating or modifying facilities within 3 months of the initial award, if applicable.
- Include a description of the existing or planned testing and measurement infrastructure for use in assessing progress toward Phase-Specific and Project-Level Technical Targets.

xii. **Table of Abbreviations and Acronyms**. (Not to exceed 2 pages. This does not contribute to the Project Narrative page limit.) An alphabetical list of all abbreviations, acronyms, and their meanings.

xiii. **Bibliographic List of References**. (Not to exceed 5 pages. This does not contribute to the Project Narrative page limit.) A complete bibliographic listing of all references used within the application.

xiv. **Compliance Matrix.** (Not to exceed 2 pages. This does not contribute to the Project Narrative page limit.) Applicants shall provide a compliance matrix in table format that explains how and where each evaluation criterion is addressed. The table's format is at the discretion of the applicant.

xv. **Table of Funded Participants and Unfunded Collaborators.** (This does not contribute to the Project Narrative page limit.) A table that

identifies all organizations that will participate in and collaborate with the awarded team, known at the time of the application submission. The table should consist of an alphabetically ordered list, by organization, of all team members, funded and unfunded, including any known contractors.

xvi. **Table of Co-investment Components and Contributors.** (Not to exceed 2 pages. This does not contribute to the Project Narrative page limit.) Where voluntary, committed co-investment is offered, a table with details about all contributing sources of co-investment, both cash and in-kind, including the rationale for selection of the contribution and the merits and risks associated with each known and anticipated contribution.

4.6.1.7 Resume(s) or CV(s)

Not to exceed 2 pages per individual. These do not contribute to the Project Narrative page limit. Resumes or CVs are required for all key personnel, including the principal investigator(s). For purposes of research security reviews, any individual whose resume is included will be deemed a covered individual. Resumes are limited to two (2) pages per individual. The resumes should highlight experience relevant to the proposed work and should provide sufficient detail for CHIPS R&D to make determinations regarding covered individuals under 42 U.S.C. §6605.

4.6.1.8 Budget Narrative and Justification

Not to Exceed 5 pages. These do not count against the Project Narrative page limit. There is no set format for the Budget Narrative and Justification; however, the written justification should include the necessity and the basis for the cost, as described below. When co-investment is included in the budget, the written justification must also identify the Federal and non-Federal portion of each cost, to include indirect costs, as applicable (see Co-Investment Section 3.2 of this NOFO for information). Proposed funding levels must be consistent with the project scope, and only allowable costs should be included in the budget.

This section will be evaluated in accordance with the evaluation criteria for Project Management, Resources, and Budget. Applicants must provide a detailed budget table[19] and budget narrative.[20] All budget tables will be reviewed to determine if all costs are allowable in accordance with Section 3.3, Allowable Costs.

[19] A budget table shows accounting information broken out by budget form object class categories in rows and summarized by performance year(s) and Federal award total in the columns.
[20] The budget should reflect the total costs, composed of both the Federal funds that will be requested and the co-investment or matching that is planned.

Information needed for each budget category is as follows (categories not listed are automatically generated by the form or are not relevant to this competition):

A. **Senior/Key Person** – At a minimum, the budget justification should include the following: name, job title, commitment of effort on the proposed project in terms of average number of hours per week or percentage of time, salary rate, total direct charges on the proposed project, description of the role of the individual on the proposed project and the work to be performed.

   Senior/Key Person Fringe Benefits – Fringe benefits should be identified separately from salaries and wages and based on rates determined by organizational policy. The items included in the fringe benefit rate (e.g., health insurance, parking, etc.) should not be charged under another cost category.

B. **Other Personnel** – Data is requested at the project role level, and not at the individual level for Other Personnel. The budget justification should include the following: job title, commitment of effort on the proposed project in terms of average number of hours per week or percentage of time, salary rate, total direct charges on the proposed project, description of the role of the position on the proposed project and the work to be performed.

   Other Personnel Fringe Benefits – Fringe benefits should be identified separately from salaries and wages and based on rates determined by organizational policy. The items included in the fringe benefit rate (e.g., health insurance, parking, etc.) should not be charged under another cost category.

C. **Equipment Description** – Equipment is defined as an item of property that has an acquisition cost of $5,000 or more (unless the organization has established lower levels) and an expected service life of more than one year. The budget justification should list each piece of equipment, the cost, and a description of how it will be used and why it is necessary to the successful completion of the proposed project. Please note that any general use equipment (computers, etc.) charged directly to the award should be allocated to the award according to expected usage on the project. Any items that do not meet the threshold for equipment can be included under the Materials and Supplies line item in Section F, Other Direct Costs (see below).

D. **Travel** – For all travel costs required by the applicant to complete the project, including attendance at any relevant conferences and/or meetings, the budget justification for travel should include the following: destination; names or number of people traveling; dates and/or duration; mode of transportation, lodging and subsistence rates; and description of how the travel is directly related to the proposed project. For travel that is yet to be determined, please provide best estimates based on prior experience. If a destination is not known,

an approximate amount may be used with the assumptions given for the location of the meeting. Applicants should build into travel budgets anticipated travel and related costs for planned team meetings.

E. **Participant/Trainee Support Costs** – Participant support costs are stipends, subsistence allowances, travel, and registration fees paid to or on behalf of participants or trainees, who are not employees of your organization, for conferences or training projects. The budget justification should indicate the names or number of participants or trainees, a description and calculation of costs per person, a description and date of the event, and a description of why the cost is necessary for the successful completion of the proposed project.

F. **Other Direct Costs** – For costs that do not easily fit into the other cost categories, please list the cost, and the breakdown of the total costs by quantity or unit of cost. Include the necessity of the cost for the completion of the proposed project. Only allowable costs can be charged to the award. Each subaward or contractual cost should be treated as a separate item in the Other Direct Costs category. Describe the services to be provided and the necessity of the subaward or contract to the successful performance of the proposed project. Contracts are for obtaining goods and services. Subrecipients perform part of the project scope of work. For each subaward, applicants must provide budget detail justifying the cost of the work performed on the project.

H. **Indirect Costs** – Commonly referred to as Facilities & Administrative (F&A) Costs, **Indirect** Costs are defined as costs incurred by the applicant organization that cannot otherwise be directly assigned or attributed to a specific project. For more details, see Section 4.6.1.9 of this NOFO.

4.6.1.9 Indirect Cost Rate Agreement

If indirect costs are included in the proposed budget, provide a copy of the approved negotiated agreement if this rate was negotiated with a cognizant Federal audit agency. If the rate was not established by a cognizant Federal audit agency provide a statement to this effect. If the successful applicant includes indirect costs in the budget and has not established an indirect cost rate with a cognizant Federal audit agency, the applicant will be required to obtain such a rate upon award in accordance with Section B.06 of the Department of Commerce Financial Assistance Standard Terms and Conditions, dated November 12, 2020.

Alternatively, applicants that do not have a current negotiated (including provisional) indirect cost rate may elect to charge a de minimis rate of 10 percent of modified total direct costs (MTDC). Applicants proposing a 10 percent de minimis rate should note this election as part of the budget portion of the application.

4.6.1.10 Subaward Budget Form

The Research & Related Subaward Budget Attachment Form is required if subrecipients and contractors are included in the application budget.

Instructions for completing subaward budget forms are available by visiting the R & R Family section of the Grants.gov Forms Repository and scrolling down to the R & R Subaward Budget Attachment(s) Form and selecting "Instructions."

4.6.1.11 Letters of Commitment and Interest

CHIPS R&D requires the inclusion of letters of commitment and encourages letters of interest specifically relevant to the applicant's CVMD plan or the applicant's Broader Impact Statement, particularly as it regards community impact and support. While letters of commitment and letters of interest do not contribute to the Project Narrative page limit, CHIPS R&D further encourages the applicant to limit the number of such letters to those absolutely required to strengthen the application and, where applicable, to consider consolidating letters of interest to include multiple entities.

Letters of commitment commit specific resources or funding to the proposed project, if the application is funded. Letters of commitment are required in the following situations:

- If the application includes subawards or contracts to known third parties, a letter of commitment from an authorized organization representative of each known proposed subrecipient and contractor must be included. Each letter should indicate the submitting organization's willingness to participate as a subrecipient or contractor, as applicable, describe the work they will do in relation to the Project Narrative, and confirm that the subrecipient is a participant in no more than two applications under this NOFO as a subrecipient.
- Letters of commitment from subrecipients that are operators of an FFRDC (See Section 3.1.1) or are Federal entities must include, in addition to the information above, documentation demonstrating that the proposed work does not compete with the private sector and documentation from the FFRDC's sponsoring institution citing the FFRDC's eligibility to participate in competitive Government funding opportunities, the FFRDC's compliance with the sponsor agreement, and confirmation from the sponsoring agency that they can receive Federal funds from NIST.
- Letters of commitment from subrecipients that are Federal entities (See Section 3.1.2) must include, in addition to the information above, documentation demonstrating that the proposed work does not compete with the private sector and/or citing the specific statutory authority and contractual authority, if relevant, establishing their ability to receive Federal award funds and compete with industry

- If key personnel who are willing to fill vacancies on the applicant's or subrecipient's staff are identified by the applicant, a letter of commitment from each of the relevant key-personnel individuals must be included. The letter from each such individual, or group of individuals, should indicate the relationship of the writer to the applicant and how the writer will help fulfill the efforts described in the Funding Opportunity Description (see Section 1.4).
- Applicant and Third-Party Non-Federal Co-investment: Letters of commitment for all sources of non-Federal co-investment must be included.
    - Applicant Non-Federal Co-investment (Cash and In-kind): A letter of commitment is required from an authorized representative of the applicant, stating the total amount of co-investment to be contributed by the applicant towards the proposed team. This letter includes a per year break-out of cash co-investment and in-kind (non-cash) contributions for the duration of the award.
    - Third Party Co-investment (Cash and In-kind): The applicant must include a letter of commitment from an authorized representative of each third-party organization providing cash or in-kind contributions that are being committed to the proposed project, subject to the application being funded. Any such letter(s) should clearly state: whether the third-party contribution will consist of cash contributions, in-kind contributions, or a combination thereof; the total amount or value of the contribution, including a break-out of cash versus in-kind contributions (as applicable); the time period over which the third-party contribution will be made; any interim performance requirements for phased contributions; and all contingencies or pre-conditions to which the contribution is subject.
    - Letters of commitment should not be letters submitted by non-proposing entities wishing to vouch for the applicant's (or entities associated with the applicant) knowledge, skills, and abilities or entities to conduct the proposed work. These letters should be in the form of a letter of interest. Letters of Commitment from education and workforce development partners should describe the specific role of the partner.

Letters of interest are optional and, where included, should indicate willingness from any third party to support this proposed effort. Letters of Interest should outline the nature and importance of the collaboration or involvement being offered. Letters of interest may also be from non-proposing entities wishing to vouch for the applicant's knowledge, skills, or abilities to conduct the proposed work or to express interest as potential customers for or users of the technologies to be developed under the project plan, including those with commercial, national security, or critical infrastructure interests.

4.6.1.12 Data Management Plan

Consistent with NIST Policy 5700.00[21], Managing Public Access to Results of Federally Funded Research, and NIST Order 5701.00[22], Managing Public Access to Results of Federally Funded Research", applicants must include a Data Management Plan (DMP).

All applications for activities that will generate scientific data using CHIPS R&D funding are required to adhere to a DMP or explain why data sharing and/or preservation are not within the scope of the project. For the purposes of the DMP, NIST adopted the definition of "research data" at 2 C.F.R. § 200.315(e)(3).

The DMP must include, at a minimum, a summary of proposed activities that are expected to generate data; a summary of the types of data expected to be generated by the identified activities; a plan for storage and maintenance of the data expected to be generated by the identified activities, including after the end of the award's period of performance; and a plan describing whether and how data generated by the identified activities will be reviewed and made available to the public.

A template for the DMP, an example DMP, and the rubric against which the DMP will be evaluated for sufficiency is available at https://www.nist.gov/open. An applicant is not required to use the template as long as the DMP contains the required information.

If an application stands a reasonable chance of being funded and the DMP is determined during the review process to be insufficient, the program office may reach out to the applicant to resolve deficiencies in the DMP. If an award is issued prior to the deficiencies being fully rectified, the award will include a term and condition stating that no research activities shall be initiated or costs incurred for those activities under the award until the NIST Authorizing Officer amends the award to indicate the term and condition has been satisfied. Reasonable costs for data preservation and access may be included in the application.

4.6.1.13 Current and Pending Support Form

Applicants must identify all sources of current and potential funding, including this proposal, for all investigators, researchers, and key personnel. Any current project support (e.g., Federal, state, local, public or private foundations, etc.) must be listed on this form. The proposed project and all other projects or activities requiring a portion of time of the Principal Investigator(s) (PI), co-PI (s), and key personnel must be included, even if no salary support is received. The total award amount for the entire award period covered, including indirect costs, must be shown as well as the number of person-months per year to be devoted to the project, regardless of the source of support. Similar information must

[21] https://www.nist.gov/system/files/documents/2018/06/19/final_p_5700.pdf
[22] https://www.nist.gov/system/files/documents/2019/11/08/final_o_5701_ver_2.pdf

be provided for all proposals already submitted or that are being submitted concurrently to other potential funders.

Applicants must complete the Current and Pending Support Form, using multiple forms as necessary to account for all activity for each individual identified in the PI, co-PI and key personnel roles. A separate form should be used for each identified individual.

Applicants must download the Current and Pending Support Form from the NIST website at https://www.nist.gov/oaam/grants-management-division/current-and-pending-support and reference the guidance provided as it contains information to assist with accurately completing the form.

4.6.2 Attachment of Required Documents

Items 4.6.1.1 through 4.6.1.4 above are part of the standard application package in Grants.gov and can be completed through the download application process.

Item 4.6.1.5 the SF-LLL, Disclosure of Lobbying Activities form, is an optional application form which is part of the standard application package in Grants.gov. If item IV.2.a.(5), the SF-LLL, Disclosure of Lobbying Activities form is applicable to this proposal, attach it to field 18 of the SF-424 (R&R), Application for Federal Assistance.

Item 4.6.1.6, the Project Narrative, should be attached to field 8 (Project Narrative) of the Research and Related Other Project Information form by clicking on "Add Attachment".

Item 4.6.1.8, the Budget Narrative and Justification, should be attached to field L (Budget Justification) of the Research and Related Budget (Total Fed + Total Non-Fed) form by clicking on "Add Attachment".

Items 4.6.1.7, Resume(s) or CV(s), 4.6.1.9, the Indirect Cost Rate Agreement, 4.6.1.11 Letters of Commitment if applicable to the submission, 4.6.1.12, the Data Management Plan, and 4.6.1.13, the Current and Pending Support Form, must be completed and attached by clicking on "Add Attachments" found in item 12 (Other Attachments) of the Research and Related Other Project Information form.

Item 4.6.1.10, the Subaward Budget Form(s), if applicable to the submission, should be attached to the Research & Related Subaward Budget (Total Fed + Non-Fed) Attachment(s) Form in the application package.

Following these directions will create zip files which permit transmittal of the documents electronically via Grants.gov.

Applicants should carefully follow specific Grants.gov instructions to ensure the attachments will be accepted by the Grants.gov system. A receipt from Grants.gov indicates

only that an application was transferred to a system. It does not provide details concerning whether all attachments (or how many attachments) transferred successfully. Applicants will receive a series of e-mail messages over a period of up to two business days before learning whether a Federal agency's electronic system has received its application.

Applicants are strongly advised to use grants.gov to access the "Download Submitted Forms and Applications" option to check that their application's required attachments were contained in their submission.

After submitting the application, check the status of your application here: CHECK APPLICATION STATUS. If any, or all, of the required attachments are absent from the submission, follow the attachment directions found above, resubmit the application, and check again for the presence of the required attachments.

If the directions found at https://www.grants.gov/help/html/help/index.htm#t=GetStarted%2FGetStarted.htm are not effective, please contact the Grants.gov Help Desk immediately. If calling from within the United States or from a U.S. territory, please call 800-518-4726. If calling from a place outside the United States or a U.S. territory, please call 606-545-5035. E-mails should be addressed to support@grants.gov. Assistance from the Grants.gov Help Desk will be available around the clock every day, with the exception of Federal holidays. Help Desk service will resume at 7:00 a.m. Eastern Time the day after Federal holidays.

Applicants can track their submission in the Grants.gov system by following the procedures at the Grants.gov site (CHECK APPLICATION STATUS). It can take up to two business days for an application to fully move through the Grants.gov system to CHIPS R&D.

CHIPS R&D uses the Tracking Numbers assigned by Grants.gov and does not issue Agency Tracking Numbers.

4.6.3 Full Application Format and Guidelines

Table 4. Full Application Format and Guidelines

Paper, Email, and Facsimile (fax) Submissions	Will not be accepted
Figures, Graphs, Images, and Pictures	Should be of a size that is easily readable or viewable and may be displayed in landscape orientation. Any figures, graphs, images, or pictures will count toward the page limits for the Project Narrative
Font	Use one of the following fonts: • Arial (not Arial Narrow), Courier New, or Palatino Linotype at a font size of 10 points or larger; • Times New Roman at a font size of 11 points or larger; or

	• Computer Modern family of fonts at a font size of 11 points or larger
Page Limit	The Project Narrative is limited to twenty (20) pages, noting the limit of two (2) pages for the Executive Summary
Page Limit Exclusions	SF-424 (R&R), Application for Federal Assistance; Research & Related Budget (Total Fed + Non-Fed); CD-511, Certification Regarding Lobbying; Research and Related Other Project Information; SF-LLL, Disclosure of Lobbying Activities; Executive Summary; Table of Contents; Research Security Plan; IP Rights Management Plan; Physical Infrastructure; Project Performance/Site Locations(s); Table of Abbreviations and Acronyms; Bibliographic List of References; Compliance Matrix; Fundamental Research Declaration; Table of Funded Participants and Unfunded Collaborators; Table of Co-investment Components; Resume(s) or CV(s); Budget Narrative and Justification; Indirect Cost Rate Agreement; Subaward Budget Form; Letters of Commitment and/or Interest; Data Management Plan; Current and Pending Support Form
Page Layout	The Project Narrative must be in portrait orientation
Page size	21.6 centimeters by 27.9 centimeters (8 ½ inches by 11 inches) with 2.5 centimeter (1 inch) margins
Page numbering	Number all pages sequentially within each section of the application, in a format that is clear and consistent. CHIPS R&D suggests formatting such as 'Project Narrative page 1 of 10' for ease of reference
Application language	All documents must be in English, including but not limited to the initial application, any additional documents submitted in response to a CHIPS R&D request, all reports, and any correspondence with CHIPS R&D
Typed document	All applications, including forms, must be typed

4.7 FULL APPLICATION REPLACEMENT PAGES

Applicants may not submit replacement pages and/or missing documents once a full application has been submitted. Any revisions must be made by submission of a new full application that must be received by CHIPS R&D by the submission deadline.

4.8 UNIQUE ENTITY IDENTIFIER AND SYSTEM FOR AWARD MANAGEMENT (SAM)

Pursuant to 2 C.F.R. part 25, applicants and recipients are required to: (i) be registered in SAM before submitting its application; (ii) provide a valid unique entity identifier in its application; and (iii) continue to maintain an active SAM registration with current information at all times during which it has an active Federal award or an application or plan under consideration by a Federal awarding agency, unless otherwise excepted from these requirements pursuant to 2 C.F.R. § 25.110. NIST will not make a Federal award to an applicant until the applicant has complied with all applicable unique entity identifier and SAM requirements and, if an applicant has not fully complied with the requirements by the time that NIST is ready to make a Federal award pursuant to this NOFO, NIST may determine that the applicant is not qualified to receive a Federal award and use that determination as a basis for making a Federal award to another applicant.

4.9 SUBMISSION DATES AND TIMES

4.9.1 Concept Papers

Applicants must send an email to research@chips.gov with "2024-NIST-CHIPS-NAPMP-01 Concept Papers" in the subject line to request instructions for submitting Concept Papers. Applicants are strongly advised not to wait until the last minute to request submission instructions. The CHIPS R&D Program will respond by email with instructions for securely submitting a Concept Paper. Concept Papers must be received no later than 11:59 p.m. Eastern Daylight Time, April 12, 2024. Concept papers received after this deadline will not be reviewed or considered. Review of the concept papers and feedback to applicants is expected to be completed on or about May 10, 2024.

4.9.2 Full Applications

Full applications must be received at Grants.gov no later than 11:59 p.m. Eastern Time, July 3, 2024. CHIPS R&D will consider the date and time recorded by Grants.gov as the official submission time. Applications received after this deadline will not be reviewed or considered.

CHIPS R&D strongly encourages applicants to begin the process of registering for SAM.gov as early as possible. While this process ordinarily takes between three days and two weeks,

in some circumstances it can take six or more months to complete due to information verification requirements.

Applicants should be aware, and factor in their application submission planning, that the Grants.gov system closes periodically for routine maintenance. Applicants should visit Grants.gov for information on any scheduled closures.

Please note that an award cannot be issued if the designated recipient's registration in the System for Award Management (SAM.gov) is not current at the time of the award.

4.10 INTERGOVERNMENTAL REVIEW

Applications under this Program are not subject to Executive Order 12372.

4.11 FUNDING RESTRICTIONS

Construction activities are not an allowable cost under this program. However, costs related to internal modifications of existing buildings that would be necessary to carry out the proposed research tasks may be allowed, at NIST discretion.

In addition, recipients and subrecipients may not charge profits, fees, or other increments above cost to an award issued pursuant to this NOFO.

5 APPLICATION REVIEW INFORMATION

5.1 CONCEPT PAPER EVALUATION CRITERIA

The CHIPS R&D merit review process will assess concept papers against the following four criteria: Relevance to economic and national security; Overall scientific and technical merit; Project management; and Transition and impact strategy. The evaluation will be qualitative, not numerical.

5.1.1 Relevance to economic and national security

This criterion addresses relevance of the proposal to enhancing U.S. economic or national security competitiveness and to achieving the CHIPS R&D mission and goals (See Section 1.1.1). Reviewers will consider the extent to which the project is likely to:

1. Advance domestic semiconductor development capabilities;
2. Generate substantial economic benefits to the Nation that extend beyond the direct return to participants in the program; and

3. Support the development of semiconductors necessary to the U.S. Department of Defense, other government systems, or critical infrastructure.

5.1.2 Overall Scientific and Technical Merit

This criterion addresses the quality, innovativeness, and feasibility of the proposed Concept Paper Narrative and the potential for meeting the objectives of this NOFO, as expressed in Section 1.1.3. Reviewers will consider the extent to which:

1. The proposed activities are innovative, original, or potentially transformative;
2. The proposal demonstrates knowledge of the current state of the art in relevant fields and the feasibility of the proposed technologies to be advanced, including gaps, constraints, and significant challenges that must be addressed; and
3. The plans for Project-Level Technical Targets, including any Embedded Substrate Features, represent a significant advance relative to the state of the art globally.

5.1.3 Project Management

This criterion addresses the degree to which applicants demonstrate that they have the appropriate personnel and access to required equipment and facilities. Reviewers will consider the extent to which the concept paper:

1. Identifies key staff, leadership, and technical experts with qualifications and experience appropriate to the proposed work, including prior experience and results in efforts similar in nature, purpose, or scope of proposed activities;
2. Identifies equipment and facilities required to support the project and demonstrates either access to or a clear plan to obtain access to such equipment and facilities; and
3. Convincingly demonstrates existing or planned substrate manufacturing capability by the applicant and component integration and workforce capabilities by the applicant and/or other committed project participants.

5.1.4 Transition and Impact Strategy

This criterion addresses the project's potential for supporting the commercialization and domestic production of funded semiconductor innovations, as well as beneficial impacts to workforce development and the broader domestic research, development, and innovation ecosystem. Reviewers will consider the extent to which the proposal provides:

1. A reasonable approach for transitioning the proposed technology to commercial deployment; and
2. Outlines an education and workforce development plan appropriate to developing a workforce relevant to domestic advanced substrate manufacturing capabilities.

The evaluation may also consider the applicant's history of transitioning (or plans to transition) technologies to foreign governments or to companies that are foreign owned, controlled, or influenced.

5.2 CONCEPT PAPER SELECTION FACTORS

The selection factors for concept papers in this competition are:

1. Merit Review. Results of the merit reviewers' evaluations, including technical comments, and the evaluation panel's evaluations and adjectival rankings.
2. Relevance to Program and Mission. Alignment with the objectives of the NOFO as well as the objectives and priorities of the NAPMP program and the mission, goals, and priorities of the CHIPS Research and Development Office.
3. Non-Duplication. The degree to which the proposed project duplicates other projects funded by NIST or other Federal sources.
4. Diversity of Projects and Participants. The degree to which the proposed team and project provides for a diversity of proposed project topics, regional diversity, and institutional diversity (including small and medium enterprises, universities, non-profit research organizations, etc.) in the overall NAPMP materials and substrates projects portfolio.
5. Broader Impacts and Workforce Development. The potential for the proposed project to contribute to broader U.S. research, development, innovation, manufacturing, education, workforce development, environmental responsibility, and regional economic development goals, including plans for broader impact consistent with Sections 1.6.1 and 1.9 of this NOFO.

5.3 FULL APPLICATION EVALUATION CRITERIA

The CHIPS R&D merit review process will assess full applications against the following four criteria: Relevance to economic and national security; Overall scientific and technical merit; Project management, resources, and budget; and transition and impact strategy. The first two criteria—economic and national security and overall scientific and technical merit—will receive the greatest and approximately equal weight. The remaining criteria will receive approximately equal weight to each other. The evaluation will be qualitative, not numerical. Applications will only be recommended for award if each criterion is adequately addressed in the application materials.

5.3.1 Relevance to economic and national security

This criterion addresses relevance of the proposal to enhancing U.S. economic or national security competitiveness and to achieving the CHIPS R&D mission and goals (See Section 1.1.1). Specifically, the applicant must clearly demonstrate its plans and capabilities to enable domestic invention, development, prototyping, manufacture, and deployment of foundational semiconductor technologies. Reviewers will therefore evaluate the extent to which the project is likely to:

1. Advance domestic semiconductor research and development capabilities;

2. Create a more resilient U.S. semiconductor supply chain, such as by addressing the risks associated with geographic concentration of current semiconductor production;
3. Generate substantial economic benefits to the Nation that extend beyond the direct return to participants in the program;
4. Support the production of semiconductors necessary to the U.S. Department of Defense, other government systems, or critical infrastructure; and
5. Increase non-Federal investment in advanced substrate research and manufacturing capabilities in the United States.

5.3.2 Overall Scientific and Technical Merit

This criterion addresses the quality, innovativeness, and feasibility of the proposed Project Narrative and the potential for meeting the objectives of this NOFO, as expressed in Section 1.1.3. Specifically, the proposal must be clear and concise and identify the core innovation, technical approach, and major technical hurdles and risks, as well as clearly establish the feasibility of the project through adequately detailed plans linked to major technical barriers. Reviewers will therefore evaluate the extent to which:

1. The proposed activities are innovative, original, or potentially transformative;
2. The proposed activities, goals, objectives, and strategies are well-reasoned, well-organized, and presented in sufficient technical detail;
3. The proposal demonstrates knowledge of the current state of the art in relevant fields and the feasibility of the proposed technologies to be advanced, including gaps, constraints, and significant challenges that must be addressed;
4. The proposal incorporates effective mechanisms to assess success, including meaningful milestones and effective demonstration device design; and
5. The plans for Project-Level Technical Targets, including any Embedded Substrate Features, represent a significant advance relative to the state of the art globally.

5.3.3 Project Management, Resources, and Budget

This criterion addresses the reasonableness, appropriateness, and cost-effectiveness of the proposed budget, management strategy, and resources, relative to the work and objectives of the Project Narrative. Applicants must demonstrate that they have the appropriate personnel and management structure to complete the work, access to the required equipment/facilities, and that the budget requested matches the need. Reviewers will therefore evaluate the extent to which the proposal:

1. Provides a clear picture of annual expenditures and a budget that is cost-effective, reasonable, and consistent with the proposed scope of work;
2. Clearly describes targets, milestones, and a project management approach that supports the objectives of this NOFO, including schedule and budget risk and mitigation strategies;

3. Identifies key staff, leadership, and technical experts with qualifications and experience appropriate to the proposed work, including prior experience and results in efforts similar in nature, purpose, or scope of proposed activities;
4. Identifies equipment and facilities required to support the project and demonstrates either access to or a clear plan to obtain access to such equipment and facilities; and
5. Convincingly demonstrates existing or planned substrate manufacturing capability by the applicant and component integration and workforce capabilities by the applicant and/or other committed project participants.

5.3.4 Transition and Impact Strategy

This criterion addresses the project's potential for supporting the commercialization and domestic production of funded semiconductor innovations, as well as beneficial impacts to workforce development and the broader domestic research, development, and innovation ecosystem. Reviewers will therefore evaluate the extent to which the proposal:

1. Includes a Commercial Viability and Domestic Production Plan that demonstrates an understanding of competing commercial and emerging technologies and how the proposed innovation would provide a significant, marketable improvement over these competing technologies, as applicable;
2. Provides a reasonable approach for transitioning the proposed technology to commercial deployment, including an Intellectual Property Rights Management Plan;
3. Includes an Education and Workforce Development Plan, including plans with rational and feasible targets, milestones, and metrics (e.g., students trained, graduated, and/or hired), appropriate to developing a diverse and skilled workforce to support domestic advanced packaging capabilities;
4. Includes a Broader Impacts Statement that, in combination with the Commercial Viability and Domestic Production Plan, demonstrates a credible commitment to the domestic R&D and manufacturing ecosystem, such as plans to leverage or contribute to regional assets, such as shared domestic facilities, manufacturers, infrastructure, and suppliers; and
5. Describes the potential for the proposed work to contribute to establishing sustainable domestic substrate innovation and manufacturing capability such as contributions to the development of new or existing regional semiconductor industry clusters.

The evaluation may also consider the applicant's history of transitioning (or plans to transition) technologies to foreign governments or to companies that are foreign owned, controlled, or influenced.

5.4 SELECTION FACTORS

The selection factors for this competition are:

1. Merit Review. Results of the merit reviewers' evaluations, including technical comments, and the evaluation panel's evaluations and adjectival rankings.
2. Relevance to Program and Mission. Alignment with the objectives of the NOFO as well as the objectives and priorities of the NAPMP program and the mission, goals, and priorities of the CHIPS Research and Development Office, which may include considerations related to research security, domestic production, and domestic control of intellectual property.
3. Funding. The availability of funding.
4. Non-Duplication. The degree to which the proposed project duplicates other projects funded by NIST or other Federal sources.
5. Diversity of Projects and Participants. The degree to which the proposed team and project provides for a diversity of proposed project topics, regional diversity, and institutional diversity (including small and medium enterprises, universities, non-profit research organizations, etc.) in the overall NAPMP materials and substrates projects portfolio.
6. Broader Impacts and Workforce Development. The potential for the proposed project to contribute to broader U.S. research, development, innovation, manufacturing, education, workforce development, environmental responsibility, and regional economic development goals — including plans for broader impact consistent with Sections 1.6.1 and 1.9 of this NOFO — in addition to any commitment to co-investment from specific, known and anticipated non-Federal sources.

5.5 REVIEW AND SELECTION PROCESS

Proposals, reports, documents, and other information related to applications submitted to CHIPS R&D and/or relating to awards issued by CHIPS R&D will be reviewed and considered by Federal employees, or non-Federal personnel who have entered into conflict of interest and confidentiality agreements covering such information, when applicable.

5.5.1 Initial Review of Applications

Concept papers and full applications received by the respective deadlines will be reviewed to determine eligibility, completeness, and responsiveness to this NOFO and stated program objectives. Concept papers and full applications determined to be ineligible, incomplete, and/or nonresponsive may be eliminated from further review. However, CHIPS R&D, in its sole discretion, may continue the review process for any concept paper or full application that is missing non-substantive information, the absence of which may easily be rectified during the review process.

Applicants are reminded that it is a crime to knowingly make false statements to a Federal agency. Misrepresentation of material facts may be the basis for denial of an application. Penalties upon conviction may include fine and imprisonment. For details, please refer to 18 U.S.C. §1001.

5.5.2 Review of Concept Papers

Concept papers that are determined to be eligible, complete, and responsive will proceed for full reviews in accordance with the review and selection process below:

5.5.2.1 Merit Review

At least three (3) independent, objective reviewers, who may be Federal employees or non-Federal personnel, with appropriate professional and technical expertise relating to the topics covered in this NOFO, will each provide a written evaluation and adjectival ratings (see Section 5.5.2.3) based on the evaluation criteria (see Section 5.1). While every concept paper will have at least three (3) reviewers, concept papers may have more than three (3) reviewers if specialized expertise is needed. During the review process, the reviewers may discuss concept papers with each other, but ratings will be determined on an individual basis.

5.5.2.2 Evaluation Panel

Following the merit review, an evaluation panel consisting of CHIPS R&D staff and/or other Federal employees with the appropriate technical expertise will conduct a panel review of the concept papers. The evaluation panel may contact applicants via e-mail to clarify contents as needed.

5.5.2.3 Adjectival Rating

The evaluation panel will provide a final adjectival rating and written evaluation of each concept paper to the Selecting Official for further deliberation, considering:

- All concept paper materials.
- Results of the merit reviewers' evaluations, including written assessments.
- Any relevant publicly available information.
- Any clarifying information obtained from the applicants.

The adjectival ratings that will be assigned are:

- Outstanding
- Very Good
- Average
- Deficient

For decision-making purposes, concept papers receiving the same adjectival rating will be considered to have an equivalent ranking.

5.5.2.4 Selection of Successful Concept Papers and Invitations to Submit Full Applications

The NIST Director or designee will serve as the Selecting Official and will make final determinations regarding which concept papers to invite to submit full applications. The Selecting Official shall generally select the most meritorious concept papers for invitation based upon the adjectival ratings and one or more of the Selection Factors. The Selecting Official retains the discretion to select concept papers from a lower adjectival category based on one or more of the Selection Factors. The decisions of the Selecting Official regarding the selection of concept papers are final and may not be appealed.

5.5.3 Review of Full Applications

Applications that are determined to be eligible, complete, and responsive will proceed for full reviews in accordance with the review and selection process below:

5.5.3.1 Merit Review

At least three (3) independent, objective reviewers, who may be Federal employees or non-Federal personnel, with appropriate professional and technical expertise relating to the topics covered in this NOFO, will each provide a written evaluation and adjectival ratings (see Section 5.5.3.4 based on the evaluation criteria (see Section 5.3). While every application will have at least three (3) reviewers, applications may have more than three (3) reviewers if specialized expertise is needed to evaluate an application. During the review process, the reviewers may discuss the applications with each other, but evaluations will be determined on an individual basis.

5.5.3.2 Evaluation Panel

Following the merit review, an evaluation panel consisting of CHIPS R&D staff and/or other Federal employees with the appropriate technical expertise will conduct a panel review of the ranked applications. The evaluation panel may contact applicants via e-mail to clarify contents of an application.

5.5.3.3 Pre-selection Interviews and Site Visits

At CHIPS R&D's discretion, applicants may be requested to participate in Pre-Selection Interviews and/or Site Visits during the evaluation panel phase, either at CHIPS R&D, the applicant's site, or a mutually agreed upon location, or via conference call or webinar. The interviews and site visits are intended to allow the applicant to provide clarifications on the

contents of the application and to provide CHIPS R&D an opportunity to ask questions and collect relevant information. Information provided during the interview and/or site visit will contribute to CHIPS R&D's evaluation of the applications.

5.5.3.4 Adjectival Rating

The evaluation panel will provide a final adjectival rating and written evaluation of each full application to the Selecting Official for further deliberation, considering:

- All application materials.
- Results of the merit reviewers' evaluations, including written assessments.
- Any relevant publicly available information.
- Any clarifying information obtained from the applicants.

The adjectival ratings that will be assigned are:

- Outstanding
- Very Good
- Average
- Deficient

For decision-making purposes, applications receiving the same adjectival rating will be considered to have an equivalent ranking.

5.5.3.5 Selection

The Selecting Official, the NIST Director or designee, will make final award recommendations to the NIST Authorizing Officer. The Selecting Official shall generally select and recommend the most meritorious applications for an award based upon the adjectival ratings and one or more of the Selection Factors. The Selecting Official retains the discretion to select and recommend an application from a lower adjectival category based on one or more of the Selection Factors.

CHIPS R&D reserves the right to negotiate the budget costs with any applicant selected to receive an award, which may include requesting that the applicant removes certain costs. Additionally, CHIPS R&D may request that successful applicants modify objectives or work plans and provide supplemental information required by the agency prior to award.

CHIPS R&D also reserves the right to reject an application where information is uncovered that raises a reasonable doubt as to the responsibility of the applicant. CHIPS R&D may select some, all, or none of the applications, or part(s) of any application. The final approval of selected applications and issuance of awards will be by the NIST Authorizing Officer. The award decisions of the NIST Authorizing Officer are final and may not be appealed.

5.5.3.6 Federal Awarding Agency Review of Risk Posed by Applicants

To inform the review by the Selecting Official, NIST will also conduct the research security review described in Section 2.7.6 and the results will be provided to the Selecting Official. Applicants with proposals that have been assessed as having high risk may be given an opportunity to mitigate the risk, as described in Section 2.7.8 .

After applications are proposed for funding by the Selecting Official, the NIST Grants Management Division (GMD) performs pre-award risk assessments, which may include a review of the financial stability of an applicant, the quality of the applicant's management systems, the history of performance, and/or the applicant's ability to effectively implement statutory, regulatory, or other requirements imposed on award recipients.

In addition, prior to making an award where the total Federal share is expected to exceed the simplified acquisition threshold (currently $250,000), NIST GMD will review and consider the publicly available Responsibility/Qualification records about that applicant in SAM.gov (formerly available via the Federal Awardee Performance and Integrity Information System (FAPIIS)). An applicant may, at its discretion, review and comment on information about itself previously entered into SAM.gov by a Federal awarding agency. As part of its review of risk posed by applicants, NIST GMD will consider any comments made by the applicant in SAM.gov in making its determination about the applicant's integrity, business ethics, and record of performance under Federal awards. Upon completion of the pre-award risk assessment, the NIST Authorizing Officer will make a responsibility determination concerning whether the applicant is qualified to receive the subject award and, if so, whether appropriate specific conditions that correspond to the degree of risk posed by the applicant should be applied to an award.

5.6 ADDITIONAL INFORMATION

5.6.1 Safety

Safety is a top priority at NIST. Employees and affiliates of award recipients who conduct project work at NIST will be expected to be safety-conscious, to attend NIST safety training, and to comply with all NIST safety policies and procedures, and with all applicable terms of their guest research agreement.

5.6.2 Notification to Unsuccessful Applicants

Unsuccessful applicants will be notified by e-mail and will have the opportunity to receive a debriefing after the opportunity is officially closed. Applicants must request within 10 business days of the email notification to receive a debrief from the program office. The program office will then work with the unsuccessful applicant in arranging a date and time of the debrief.

5.6.3 Retention of Unsuccessful Applications

Unsuccessful applications will be retained in accordance with the General Record Schedule 1.2/021.

6 Federal Award Administration Information

6.1 FEDERAL AWARD NOTICES

Successful applicants will receive an award package from the NIST Authorizing Officer.

6.2 ADMINISTRATIVE AND NATIONAL POLICY REQUIREMENTS

6.2.1 Terms and Conditions

The complete terms and conditions of each award will be contained in the award package signed by the NIST Authorizing Officer.

6.2.1.1 NIST/CHIPS R&D Discretion

Awards in this program require significant ongoing involvement from CHIPS R&D staff and provides NIST the flexibility to alter the course of the project in real-time to meet the overarching goals. This will generally include collaboration with the recipient organization in developing and implementing the approved scope of work.

6.2.1.2 Management Systems and Procedures

Recipient organizations are expected to have systems, policies, and procedures in place by which they manage funds and activities. Recipients may use their existing systems to manage federal award funds and activities as long as they are consistently applied regardless of the source of funds and across their business functions. To ensure that an organization is committed to compliance, recipient organizations are expected to have in use clearly delineated roles and responsibilities for their organization's staff, both programmatic and administrative; written policies and procedures; training; management controls and other internal controls; performance assessment; administrative simplifications; and information sharing.

6.2.1.3 Financial Management System Standards

Recipients must have in place accounting and internal control systems that provide for appropriate monitoring of other transaction accounts to ensure that obligations and expenditures are congruent with programmatic needs and are reasonable, allocable, and

allowable. In addition, the systems must be able to identify unobligated balances, accelerated expenditures, inappropriate cost transfers, and other inappropriate obligation and expenditure of funds, and recipients must notify CHIPS R&D when problems are identified. A recipient's failure to establish adequate control systems constitutes a material violation of the terms of the award.

6.2.2 Funding Availability and Limitation of Liability

Funding for the program listed in this NOFO is contingent upon the availability of appropriations. NIST or the Department of Commerce will not be responsible for application preparation costs, including but not limited to if this program fails to receive funding or is cancelled because of agency priorities. Publication of this NOFO does not oblige NIST or the Department of Commerce to award any specific project or to obligate any available funds.

As specified in Section 2.2 of this document, when a proposal for a multi-year award is approved, funding will be provided for only the first phase of the project and incrementally thereafter. If a project is selected for funding, NIST has no obligation to provide any additional funding in connection with that award. Continued funding of an award will be contingent upon satisfactory performance and the availability of funds.

6.2.3 Collaborations with CHIPS R&D and Other Federal Agencies

CHIPS R&D employees may not participate in the preparation of any application in response to this funding opportunity. After award, the team is expected to interact with CHIPS R&D and with Federal government organizations and FFRDCs, as appropriate and consistent with their respective missions, objectives and operational structures.

The award recipient is encouraged to collaborate with Federal entities to support the program goals and to ensure that the Federal investment in this team can be leveraged to the extent appropriate for national priorities.

If an applicant proposes collaboration with NIST, the statement of work should include a statement of this intention, a description of the collaboration, and prominently identify the NIST employee(s) involved, if known. Any collaboration by a NIST employee must be approved by appropriate NIST management and is at the sole discretion of NIST. Prior to beginning the merit review process, NIST will verify the approval of the proposed collaboration. Any unapproved collaboration will be stricken from the application prior to the merit review. Any collaboration with an identified NIST employee that is approved by appropriate NIST management will not make an application more or less favorable in the competitive process.

6.2.4 Post-Award Involvement of Foreign Entities

Once an award has been issued, on a case-by-case basis and subject to a determination by CHIPS R&D, majority foreign-owned or foreign-controlled entities may be allowed as subrecipients or contractors, based on the unique and specific needs of the team. CHIPS R&D's determination of whether a specific foreign-owned or foreign-controlled entity will be allowed to participate as a subrecipient or contractor will be based on information provided by the team and by other Federal agencies. CHIPS R&D will consider whether the foreign entity's participation is in the best interest of the team and the United States, including the domestic economy generally, U.S. industry, and U.S. manufacturing competitiveness. CHIPS R&D will also consider whether the team has sufficiently demonstrated that, among other items, adequate intellectual property and data protection protocols exist between the proposed entity and its foreign parent organization(s).

6.2.5 Use of Federal Government-Owned Intellectual Property

If the applicant anticipates using any Federal government-owned intellectual property, in the custody of CHIPS R&D or another Federal agency, to carry out the work proposed, the applicant should clearly identify such intellectual property in the proposal. This information will be used to ensure that no Federal employee involved in the development of the intellectual property will participate in the review process for that competition. In addition, if the applicant intends to use the Federal Government-owned intellectual property, the applicant must comply with all statutes and regulations governing the licensing of Federal government patents and inventions, described in 35 U.S.C. §§200-212, 37 C.F.R. Part 401, 2 C.F.R. §200.315. Questions about these requirements may be directed to the Chief Counsel for NIST, (301) 975-2803, nistcounsel@nist.gov.

Any use of Federal government-owned intellectual property by a recipient of an award under this announcement is at the sole discretion of the Federal government and will need to be negotiated on a case-by-case basis by the recipient and the Federal agency having custody of the intellectual property if a project is deemed meritorious. The applicant should indicate within the statement of work whether it already has a license to use such intellectual property or whether it intends to seek a license from the applicable Federal agency.

If any inventions made in whole or in part by a NIST employee arise in the course of an award made pursuant to this NOFO, the United States Government may retain its ownership rights in any such invention.

Licensing or other disposition of the Federal government's rights in such inventions will be determined solely by the Federal government, through CHIPS R&D as custodian of such inventions and include the possibility of the Federal government putting the intellectual property into the public domain.

6.2.6 Export Controls

Some activities may require access to export-controlled items and therefore be subject to export control laws and regulations. If an applicant is selected for award, the applicant and all subrecipients agree to comply with United States export laws and regulations, including, but not limited to, the International Traffic in Arms Regulations and the Department of Commerce Export Regulations. Under no circumstances may foreign entities (organizations, companies, or persons) obtain access to export-controlled items unless proper procedures have been satisfied and such access is authorized pursuant to law or regulation. If involvement of foreign entities is approved by CHIPS R&D under Section 6.2.4, awardees must develop measures to properly protect export-controlled information, as appropriate.

6.3 REPORTING

6.3.1 Reporting Requirements

The following reporting requirements apply to awards in this program:

6.3.1.1 Financial Reports

Each award recipient will be required to submit an SF-425, Federal Financial Report on a quarterly basis for the periods ending March 31, June 30, September 30, and December 31 of each year. Reports will be due within 30 days after the end of the reporting period. A final financial report is due within 120 days after the end of the project period.

6.3.1.2 Research Performance Monitoring and Reporting

Award recipients will be required to submit quarterly research progress reports within 30 days of the close of the reporting period. CHIPS R&D expects the recipient to include similar content to that requested in the Research Performance Progress Report (see 2 C.F.R. § 200.329). However, CHIPS R&D may approve the use of a different format at the request of the recipient.

A final consolidated report shall be submitted within 120 days after the expiration date of the award. The recipient is required to submit publication citation information, links to publicly available data, and other public outputs as soon as they become available.

In addition to the formal quarterly progress reports, the award recipient will be expected to meet quarterly with the Federal Program Officer to discuss operational, technical, and strategic plans. It is expected that the recipient will additionally establish regular and ongoing cadence of informal communication with the Federal program team to ensure timely awareness of issues and achievements.

Information submitted in the course of applying for funding under this program or provided in the course of its grant management activities, will be subject to analysis and evaluation for official Government or statistical purposes, including but not limited to assessing performance and evaluating program outcomes.

6.3.1.3 Patent and Property Reports

In accordance with the terms and conditions governing the award, the recipient may need to submit property and patent reports. The award recipient is required to notify CHIPS R&D of any patents or other intellectual property issuing from work performed within this award. CHIPS R&D requires periodic reporting on the utilization or efforts at obtaining utilization that are being made by the awardee or its licensees or assignees: *Provided*, that any such information as well as any information on utilization or efforts at obtaining utilization shall be treated by the Federal agency as commercial and financial information obtained from a person and privileged and confidential and not subject to disclosure.

6.3.1.4 Recipient Integrity and Performance Matters

In accordance with section 872 of Public Law 110-417 (as amended; see 41 U.S.C. §2313), if the total value of a recipient's currently active grants, cooperative agreements, and procurement contracts from all Federal awarding agencies exceeds $10,000,000 for any period of time during the period of performance of an award made under this NOFO, then the recipient shall be subject to maintaining the currency of information reported to SAM that is made available in FAPIIS about certain civil, criminal, or administrative proceedings involving the recipient.

6.3.2 Audit Requirements

Any recipient that expends Federal awards of $750,000 or more in the recipient's fiscal year must conduct a single or program specific audit in accordance with the requirements set out in the 2 C.F.R. Part 200 Subpart F. Additionally, unless otherwise specified in the terms and conditions of the award, entities that are not subject to Subpart F of 2 C.F.R. Part 200 (e.g., for-profit commercial entities) that expend $750,000 or more in DOC funds during their fiscal year must submit to the assigned NIST Authorizing Officer either: (i) a financial related audit of each DOC award or subaward in accordance with Generally Accepted Government Auditing Standards; or (ii) a project specific audit for each award or subaward in accordance with the requirements contained in 2 C.F.R. §200.507. Applicants are reminded that CHIPS R&D, the Department of Commerce Office of Inspector General, or another authorized Federal agency may conduct an audit of an award at any time.

6.3.3 Federal Funding and Accountability Transparency Act of 2006

In accordance with 2 C.F.R. Part 170, all recipients of a Federal award made on or after October 1, 2010, are required to comply with reporting requirements under the Federal

Funding Accountability and Transparency Act of 2006 (Public Law No. 109-282). In general, all recipients are responsible for reporting sub-awards of $25,000 or more. In addition, recipients that meet certain criteria are responsible for reporting executive compensation. Applicants must ensure they have the necessary processes and systems in place to comply with the reporting requirements should they receive funding. Also see the Federal Register Notice published September 14, 2010, at 75 FR 55663.

7 AGENCY CONTACTS

Questions should be directed to the following:

Subject Area	Point of Contact
Programmatic and Technical Questions	E-mail: research@chips.gov with "2024-NIST-CHIPS-NAPMP-01 Questions" in subject line
Technical Assistance with Grants.gov Submissions	grants.gov Phone: 800-518-4726 E-mail: support@grants.gov
Award Management Inquiries	Gilberto Castillo Phone: 202-281-8505 E-mail: gilberto.castillo@nist.gov with "2024-NIST-CHIPS-NAPMP-01 Questions" in subject line

8 OTHER INFORMATION

8.1 PERSONAL AND BUSINESS INFORMATION

The applicant acknowledges and understands that information and data contained in applications for other transactions, as well as information and data contained in financial, performance and other reports submitted by applicants, may be used by CHIPS R&D in conducting reviews and evaluations of its financial assistance programs. For this purpose, applicant information and data may be accessed, reviewed and evaluated by Department of Commerce employees, other Federal employees, and also by Federal agents and contractors, and/or by non-Federal personnel, all of whom enter into appropriate conflict of interest and confidentiality agreements covering the use of such information. As may be provided in the terms and conditions of a specific other transaction award, applicants are expected to support program reviews and evaluations by submitting required financial and performance information and data in an accurate and timely manner, and by cooperating with Department of Commerce and external program evaluators. Applicants are reminded that they must take reasonable measures to safeguard protected personally identifiable

information and other confidential or sensitive personal or business information created or obtained in connection with a Department of Commerce financial assistance award.

In addition, Department of Commerce regulations implementing the Freedom of Information Act (FOIA), 5 U.S.C. Sec. 552, are found at 15 C.F.R. Part 4, Public Information. These regulations set forth rules for the Department regarding making requested materials, information, and records publicly available under the FOIA. Applications submitted in response to this Federal Funding Opportunity may be subject to requests for release under the Act. If an application contains information or data that the applicant deems to be confidential commercial information that should be exempt from disclosure under FOIA, that information should be identified, bracketed, and marked as Privileged, Confidential, Commercial or Financial Information. In accordance with 15 CFR §4.9, CHIPS R&D and the Department of Commerce will protect from disclosure confidential business information contained in other transaction applications and other documentation provided by applicants to the extent permitted by law.

8.2 PUBLIC WEBSITE

CHIPS R&D has a public website that provides a "Frequently Asked Questions" page and other information pertaining to this Funding Opportunity. Any amendments to this NOFO will be announced through Grants.gov.

Applicants must submit all questions pertaining to this funding opportunity in writing to research@chips.gov with "2024-NIST-CHIPS-NAPMP-01 Questions" in the subject line.