UNITED STATES DEPARTMENT OF COMMERCE
National Institute of Standards and Technology
Gaithersburg, Maryland 20899-6830

Semiconductor Metrology Research & Development: Workshop 1

April 6, 2022 – April 7, 2022

April 6, 2022: Panel Discussion Sessions

Workshop Facilitators: Tim McBride (NIST), Anita Balachandra (NIST)

10:00 am – 10:15 am (EDT)	**Welcome and Opening Remarks**	James Olthoff (NIST)
10:15 am – 10:45 am (EDT)	**CHIPS Act Overview**	Michael Molnar (NIST)
10:45 am – 11:25 am (EDT)	**Plenary Speaker**	Todd Younkin (SRC)

11:30 am – 12:30 pm (EDT) **Panel 1 – Metrology for Materials and Dimensional Scaling**

Discuss the metrology needed for extending leading-edge CMOS, materials characterization, structure function relationships, in addition to accelerating beyond CMOS technologies.

Moderator: George Orji (NIST)

Panelists: Alain Diebold (SUNY Poly), Ofer Adan (Applied Materials), Andy Antonelli (Onto), and Nelson Felix (IBM)

12:30 pm – 1:00 pm (EDT) **Break for Lunch**

1:00 pm – 2:00 pm (EDT) **Panel 2 – In-line Metrology for High-Throughput Manufacturing**

Discuss in-line metrology needed for high-volume manufacturing of leading-edge devices. The use of new materials, introduction of new lithography techniques and complex device structures into high-volume manufacturing have increased the need for in-line metrology for process control.

Moderator: Bryan Barnes (NIST)

Panelists: Alok Vaid (Global Foundries), Chris Deeb (Intel), Qinghuang Lin (Lam Research), and Zhengquan Tan (KLA)

2:00 pm – 3:00 pm (EDT) **Panel 3 – Materials Quality for Suppliers**

Discuss the metrology requirements and challenges pertaining to supplier material quality as advanced processing nodes continue to add new substances to the fab and necessitate more stringent requirements for contamination and purity.

Moderator: R. Joseph Kline (NIST)

Panelists: Roya Lahiji (Intel), Stuart Tison (Entegris), Rama Puligadda (Brewer Science), and Ganesh Vijayaraghavan (Air Products)

3:15 pm – 4:15 pm (EDT) **Panel 4 – Digital Enablers to Improve Design and Manufacturing**

Discuss industry use of digital enablers, such as artificial intelligence, machine learning, digital twins, simulation and optimization tools, data management and analysis for big data sets, and standards for data representation and integration, to improve semiconductor product and process design and semiconductor manufacturing processes.

Moderator: Kevin Jurrens (NIST)

Panelists: Regina Freed (Applied Materials), Victor Moroz (Synopsys), John Allgair (BRIDG), Marc Swinnen (Ansys), and Zhengquan Tan (KLA)

4:15 pm – 4:20 pm (EDT) **Closing Remarks** Tim McBride (NIST)

4:30 pm – 6:00pm (EDT) **RFI: National Semiconductor Technology Center Questions**

Moderators: David Gundlach (NIST), George Orji (NIST), and Joe Kline (NIST)

April 7, 2022: Breakout Discussion Sessions

Breakout Session Lead Facilitator: Joan Pellegrino (Energetics)

10:00 am – 11:15 am (EDT) **Panel 1 Breakout – Metrology for Materials and Dimensional Scaling**

Identify future materials and dimensional metrology needs that could become showstoppers within the next 10- 15 years.

11:30 am – 12:45 pm (EDT) **Panel 2 Breakout – In-line Metrology and High-Throughput Manufacturing**

Identify key metrology methods and tools needed for high volume manufacturing and process control.

12:45 pm – 1:15 pm (EDT) **Break for Lunch**

1:15 pm – 2:30 pm (EDT) **Panel 3 Breakout – Materials Quality for Suppliers**

Identify key areas where improvements in metrology for materials quality and supply are needed.

2:45 pm – 4:00 pm (EDT) **Panel 4 Breakout – Digital Enablers to Improve Design and Manufacturing**

Understand industry's current use of Digital Enablers, identify existing industry challenges, needs, and priorities, and determine how NIST can best help to advance the industry in these areas

April 6 Workshop Speaker and Moderator Bio's

Workshop Facilitators: Tim McBride (NIST) - Tim McBride is with the NIST Information Technology Laboratory his current role is Deputy Division Chief for the Applied Cybersecurity Division. Mr. McBride has held several positions at NIST including Deputy Director of the National Cybersecurity Center of Excellence. Prior to NIST Mr. McBride was with the Department of Homeland Security.

Workshop Co-Facilitator: Anita Balachandra (NIST) - Anita Balachandra is a Resource Manager with the Hollings Manufacturing Extension Partnership. Her portfolio includes the manufacturing extension Centers in Hawaii, Oregon, Arizona, Kansas, Missouri, Minnesota, and Mississippi. Prior to joining NIST, Ms. Balachandra spent many years as a private-sector consultant, where she worked extensively with the semiconductor industry.

Plenary Speaker: Todd Younkin (SRC) - Dr. Todd Younkin is the CEO of Semiconductor Research Corporation (SRC). Through SRC's $90M/yr. commitment to global research and workforce development, he is bringing innovators together to drive next-gen heterogeneous electronics for a smarter, shared future.

Panel 1 – Metrology for Materials and Dimensional Scaling

Panel Moderator: George Orji (NIST) - George Orji is currently with the NIST Program Coordination office. He is a project leader in the Microsystems and Nanotechnology Division of the Physical Measurement laboratory at NIST, where he works on nanoscale dimensional and optical metrology, calibration methods, traceability, and uncertainty analysis in dimensional metrology.

Alain Diebold (SUNY Poly) - Alain C. Diebold is Professor Emeritus and Empire Innovation Professor of Nanoscale Science at SUNY Polytechnic Institute. He is a SPIE Fellow and an AVS Fellow. He co-led the Metrology Roadmap Technical Working Group for the International Technology Roadmap for Semiconductors which he started. His current research covers both nanoscale materials properties and semiconductor metrology. These efforts now include the application of machine learning to materials characterization and metrology. He is a co-author of Optical and Electrical Properties of Nanoscale Materials which was published by Springer Nature by the end of 2021.

Ofer Adan (Applied Materials) – Ofer Adan is the Head of Patterning Control Technology at Applied Materials. Adan has held various roles, leading solutions in metrology inspection and process control since 2001. Adan has several patents including the first patent on using high energy for SEM Overlay, and over 50 publications on metrology, inspection, process control, failure analysis, and fracture. Adan was awarded several best paper awards at various conferences among them the SPIE Diana Nyyssonen Memorial Award. Adan received an M.Sc. degree in electronic materials engineering from Ben Gurion University.

Andy Antonelli (Onto) - Andy Antonelli holds a PhD in physics from Brown University and 25 years of experience in the semiconductor industry including time at Intel, Novellus Systems, and Lam Research. He is currently Senior Director of Research & Development and Fellow at Onto Innovation where he directs pathfinding metrology development. He has made contributions to metrology, deposition process technology, and process integration including being one of the founding architects of the Rudolph MetaPULSE™ technology and the principal architect of the Onto Aspect™ technology, an innovator in low-k interlayer dielectric, dielectric barrier, and hardmask materials synthesis and analysis, and novel plasma sources.

Nelson Felix (IBM) - Nelson Felix joined IBM in 2008 and is currently the Director of Process Technology at IBM Research in Albany, NY. In this role, Nelson is responsible for the demonstration and enablement of new tooling, processes, materials, and metrology to support IBM's leading-edge CMOS device and AI hardware roadmap. Nelson received his B.S. from the University of Massachusetts, Amherst (2002) and his Ph.D. from Cornell University (2007), both in chemical engineering.

Panel 2 – In-line Metrology for High Throughput Manufacturing

Panel Moderator: Bryan Barnes (NIST) - Dr. Bryan Barnes is a Physicist at the National Institute of Standards and Technology, working on optical methods for semiconductor metrology since 2005. Among other roles, he chairs the North America chapter of the SEMI Standards Microlithography Committee.

Alok Vaid (Global Foundries) - Alok Vaid is Dep. Director of Metrology process module at GLOBALFOUNDRIES's Fab8 site located in New York. He has been performing/leading R&D and manufacturing in the field of metrology and process control for 17 years. He has published several scientific papers (> 75) in various conference and journals and holds ~ 20 US patents. Alok currently serves as committee member and session chair at SPIE and IEEE/SEMI ASMC conferences.

Chris Deeb (Intel) - Chris Deeb has been in different areas of FAB metrology, inspection, and characterization at Intel for the past 18 years. He is currently a Principal Engineer in Intel's Global Supply Chain focused on electron beam inspection and metrology.

Qinghuang Lin (Lam Research) - Dr. Qinghuang Lin is Director in the Advanced Technology Development at Lam Research, Fremont, California. He is an SPIE Fellow, an ACS Fellow, a PMSE Fellow and a POLY Fellow. For more than 20 years, he has held technical and executive positions in photoresist development, advanced lithography, BEOL materials & integration, 3D integration and semiconductor technology strategy for several nodes of CMOS technology research and development at Lam Research, IBM, and ASML. He holds more than 120 granted US patents and is the author and co-author of over 100 technical papers. Dr. Lin is the recipient of Industrial Polymer Scientist Award (2018) and the Roy W. Tess Award (2020) and several IBM Awards. He is Co-Chair of the SPIE Advanced Lithography and Patterning (2021-2022) and serves as an associate editor of Journal of Micro/Nanopatterning, Materials, and Metrology (JM3).

Zhengquan Tan (KLA) - Dr. Zhengquan Tan is a physicist and a Senior Director at KLA, with 20 years of experience in optical films and critical-dimension shape metrology for process control in semiconductor integrated circuit development and production. He has led product development and fab process-control solutions, covering logic / foundry devices for 65nm to 2nm nodes, dynamic random-access memory (DRAM) 45nm to 10nm, plus 2D and 3D NAND flash memory. His prior experience includes extreme ultraviolet (EUV) lithography development, extreme ultraviolet (EUV) interferometry, and chemical vapor deposition in semiconductor processing.

Panel 3 – Materials Quality for Suppliers

Panel Moderator: R. Joseph Kline (NIST) - R. Joseph Kline leads the Metrology for Nanolithography project at NIST and his research interests include X-ray based dimensional metrology of nanostructures. He received his Ph.D. in Materials Science and Engineering at Stanford University. He has published more than 100 articles, given more than 50 invited presentations, and has received awards including the Presidential Early Career Award for Science and Engineering, the Department of Commerce Gold Award, and the Arthur S. Flemming Award.

Roya Lahiji (Intel) - Roya is a director of Strategic Quality Engineering (SQE) Group within Fab Materials Organization (FMO), at Intel Corp. She has 15 years' experience in R&D, technology development, process engineering, and program management. Roya has played critical role in successfully introducing and developing FOK toolsets to enable thin film and e-NVM metrology for different programs within Intel in partnership with OEM suppliers as a senior TD Engineer. In her current role she leads a diverse and talented team of engineers and technologists focused on E2E traceability, predictivity, defectivity reduction and development of next generation of advance metrology platforms to detect and control defects in materials for advance tech nodes. Roya has a PhD in Physics-Nanotechnology from Purdue University and worked as postdoctoral researcher at University of Alberta, Canada.

Stuart Tison (Entegris) - Stuart Tison is currently Senior Vice President of the Specialty Chemicals and Engineered Materials (SCEM) Division for Entegris. In this position he is responsible for leading Entegris's material businesses including specialty gases, deposition materials, wet chemistries, coatings, and other specialty materials. He holds 13 patents and numerous publications in the area of instrumentation, materials and contamination control. He is involved in leadership positions at ASTM, ISO, and the American Vacuum Society.

Rama Puligadda (Brewer Science) - Rama Puligadda earned a Master of Science in Chemistry from the Indian Institute of Technology (IIT), Delhi, India (1990), a Master of Technology in Polymer Science and Technology from IIT Delhi, India (1992), and a Master of Science in Chemical Engineering from the University of Cincinnati (1995). Rama began her career at Brewer Science in 1995 as a Research Chemist. She has led and managed several programs at Brewer Science including product development projects and collaborative work with partnering companies, universities, and research institutions. She now serves as Chief Technical Officer, providing leadership for the design, development, and engineering of innovative solutions for the semiconductor packaging industry.

Ganesh Vijayaraghavan (Air Products) - Ganesh Vijayaraghavan is currently the technology manager for analytical systems and electrolysis with the global operations team at Air Products. In this role he supports Air Products' global operating facilities with design, fabrication, commissioning, operations, maintenance and troubleshooting of analytical systems and electrolysis applications.

Panel 4 – Digital Enablers to Improve Design and Manufacturing

Panel Moderator: Kevin Jurrens (NIST) - Kevin Jurrens is the Acting Chief of the Intelligent Systems Division in the NIST Engineering Laboratory. He is a mechanical engineer with more than 30 years dedicated to advanced manufacturing. Kevin has served in a variety of technical and management roles for NIST manufacturing programs, including as researcher, technical project leader, program manager, and division chief.

Regina Freed (Applied Materials) - Regina Freed is the Vice President of AIx Solutions at Applied Materials. She has more than 20 years of experience in the semiconductor industry, managing semiconductor process and equipment development for both logic and memory processes, including co-optimization between deposition and etch, lithography, metrology, and defect inspection. At Applied Materials, Regina leads the AIx program that enables accelerated development and ramp, as well as improved process windows through Actionable Insights, enabling Applied's customers to scale faster and at lower cost, while optimizing device performance.

Victor Moroz (Synopsys) - Dr. Victor Moroz is a Fellow at Synopsys, and he is engaged in a wide variety of projects on modeling Design-Technology Co-Optimization, stress engineering, 3D integrated circuits, transistor scaling, cryogenic devices, random and systematic variability, junction leakage, and many other efforts. His achievements are reflected in three book chapters, more than 100 technical papers, and over 300 US and international patents. Victor has been involved in many technical committees across the community, including the International Technology Roadmap for Semiconductors and the International Conference on Simulation of Semiconductor Processes and Devices (SISPAD), where he was the Technical Chair in 2018. He currently serves as an Editor of IEEE Electron Device Letters.

John Allgair (BRIDG) - Dr. John Allgair is the Director of BRIDG, a not-for-profit, public-private partnership, where he leads the Advanced System Integration and Packaging Program which provides robust, cost-effective platforms for the heterogeneous integration of silicon and photonic devices to enable smart sensor integration. Over his twenty-year career in the semiconductor industry, John has worked in roles focused on business growth, innovation, and bringing new products to market during tenures at GLOBAL FOUNDRIES, AMD, SEMATECH, Freescale, and Motorola.

Marc Swinnen (Ansys) - Marc Swinnen is Product Marketing Director for semiconductor products at Ansys. Before joining Ansys, Marc was Director of Product Marketing at Cadence Design Systems and has worked in Marketing and Technical Support positions at Synopsys, Azuro, and Sequence Design, where he gained experience with a wide array of digital and analog design tools. Marc holds a Master's in Electrical Engineering and a Master's in Industrial Management from KU Leuven, Belgium and an MBA from San Jose State University, California.

Zhengquan Tan (KLA) - Dr. Zhengquan Tan is a physicist and a Senior Director at KLA, with 20 years of experience in optical films and critical-dimension shape metrology for process control in semiconductor integrated circuit development and production. He has led product development and fab process-control solutions, covering logic / foundry devices for 65nm to 2nm nodes, dynamic random-access memory (DRAM) 45nm to 10nm, plus 2D and 3D NAND flash memory. His prior experience includes extreme ultraviolet (EUV) lithography development, extreme ultraviolet (EUV) interferometry, and chemical vapor deposition in semiconductor processing.

RFI - National Semiconductor Technology Center Questions

Moderator: David Gundlach (NIST) - David J. Gundlach joined National Institute of Standards and Technology in 2005 as the leader of the Thin Film Electronics Project in the Semiconductor Electronics Division. In 2018 he became Chief of the Nanoscale Device Characterization Division, where he provides leadership in developing and advancing measurements and fundamental knowledge to characterize nano- and atom-scale engineered materials and solid-state devices for innovation in information processing, sensing, and future quantum technologies. Dr. Gundlach is a member of the IEEE and APS, and a former editorial board member for IEEE Transactions on Electron Devices.

Moderator: George Orji (NIST) - George Orji is currently with the NIST Program Coordination office. He is a project leader in the Microsystems and Nanotechnology Division of the Physical Measurement laboratory at NIST, where he works on nanoscale dimensional and optical metrology, calibration methods, traceability, and uncertainty analysis in dimensional metrology.

Moderator: R. Joseph Kline (NIST) - R. Joseph Kline leads the Metrology for Nanolithography project at NIST and his research interests include X-ray based dimensional metrology of nanostructures. He received his Ph.D. in Materials Science and Engineering at Stanford University. He has published more than 100 articles, given more than 50 invited presentations, and has received awards including the Presidential Early Career Award for Science and Engineering, the Department of Commerce Gold Award, and the Arthur S. Flemming Award.