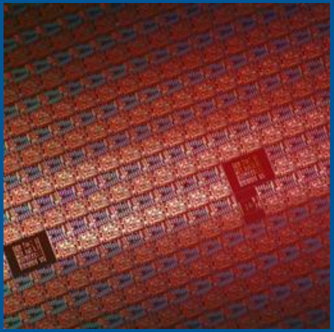
Accelerating the next technology revolution

Overview of Next Generation Lithography, Advanced Patterning, EUV and Self Assembly

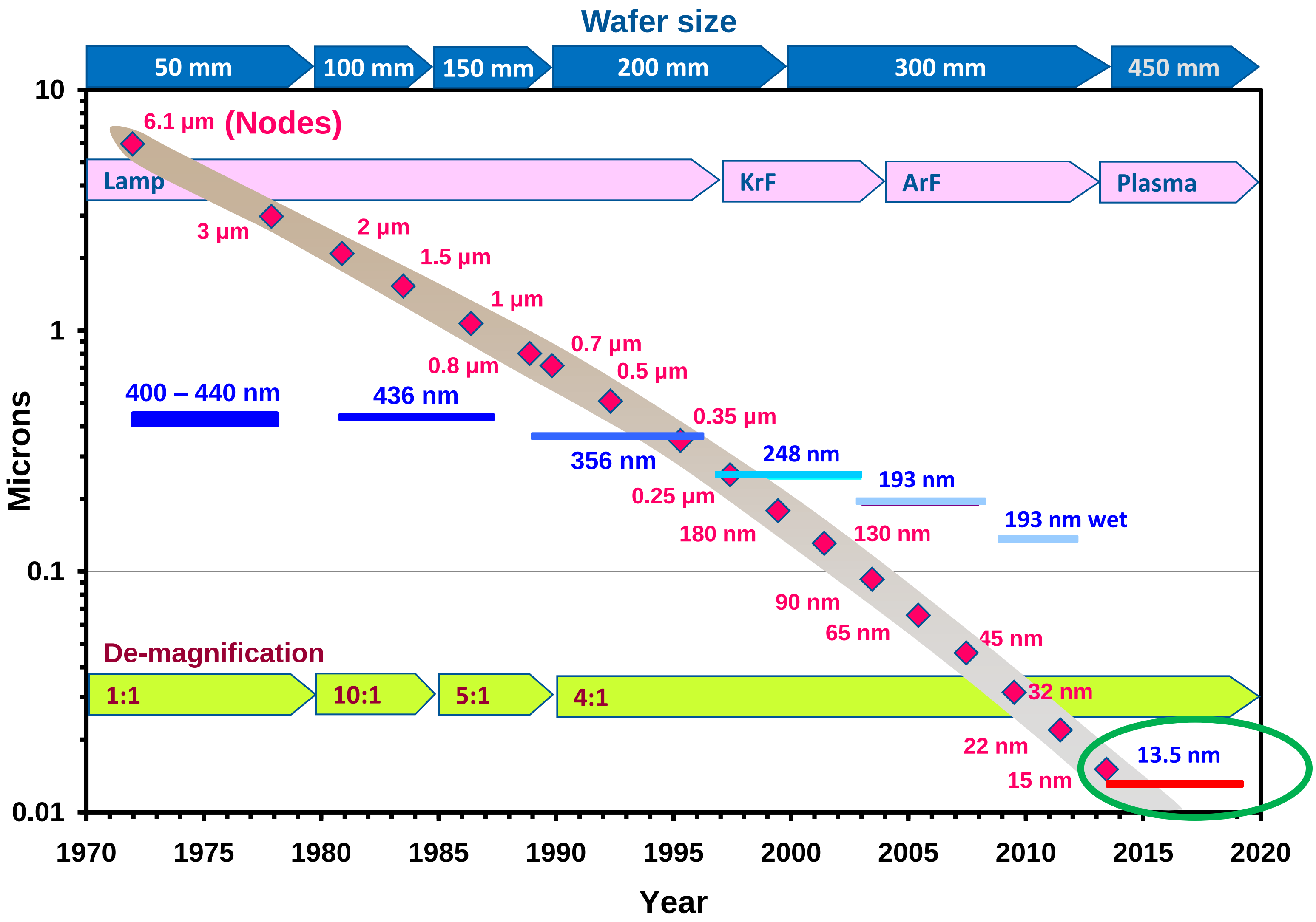
2013 International Conference on Frontiers of Characterization and Metrology
Gaithersburg, Maryland



Mark Neisser & Stefan Wurm
SEMATECH
March 28, 2013

INTRODUCTION

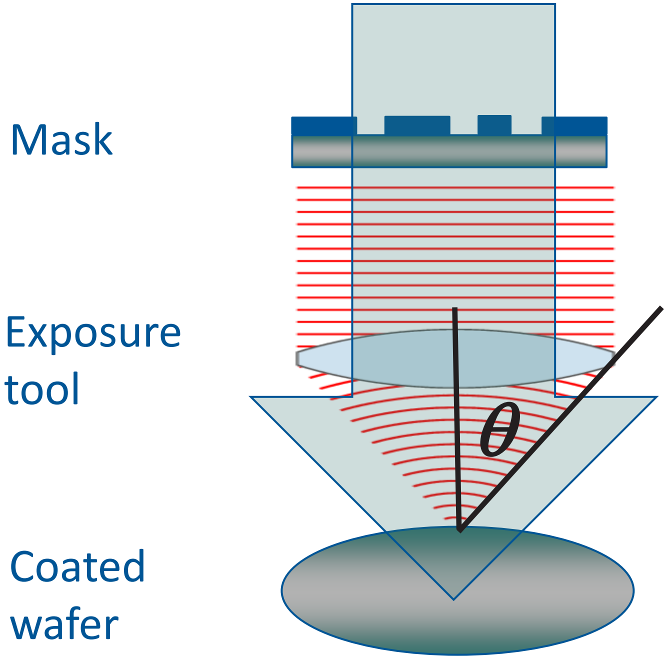
Lithography Scaling



ITRS Roadmap Requirements

Specifications are in nm	2012	2013	2014	2015	2016	2017	2018	2019	2020	2021	2022
Minimum critical level half pitch	20	18	17	15	14	13	12	11	10	9	8
Minimum hole dimension	32	28	25	23	20	18	16	14	13	11	10
LWR	2.5	2.2	2.0	1.8	1.6	1.4	1.3	1.1	1.0	0.9	0.8
Minimum patterned defect size	20	20	20	10	10	10	10	10	10	10	10
Overlay	6.4	5.4	4.8	4.2	3.8	3.4	3.0	2.7	2.4	2.1	1.9
Minimum hole CD uniformity	1.2	1.0	0.8	0.6	0.5	0.5	0.4	0.4	0.3	0.3	0.3
Double patterning CD uniformity	0.6	0.4	0.3	0.3	0.3	0.3	0.2	0.2	0.2	0.2	0.2
Spacer defined CD uniformity		0.4	0.3	0.3	0.3	0.3	0.2	0.2	0.2	0.2	0.2

Conventional Lithography



$$NA = \sin\,\theta$$

$$resolution\ (half\ pitch) = \mathrm{k}_1 \frac{\lambda}{NA}$$

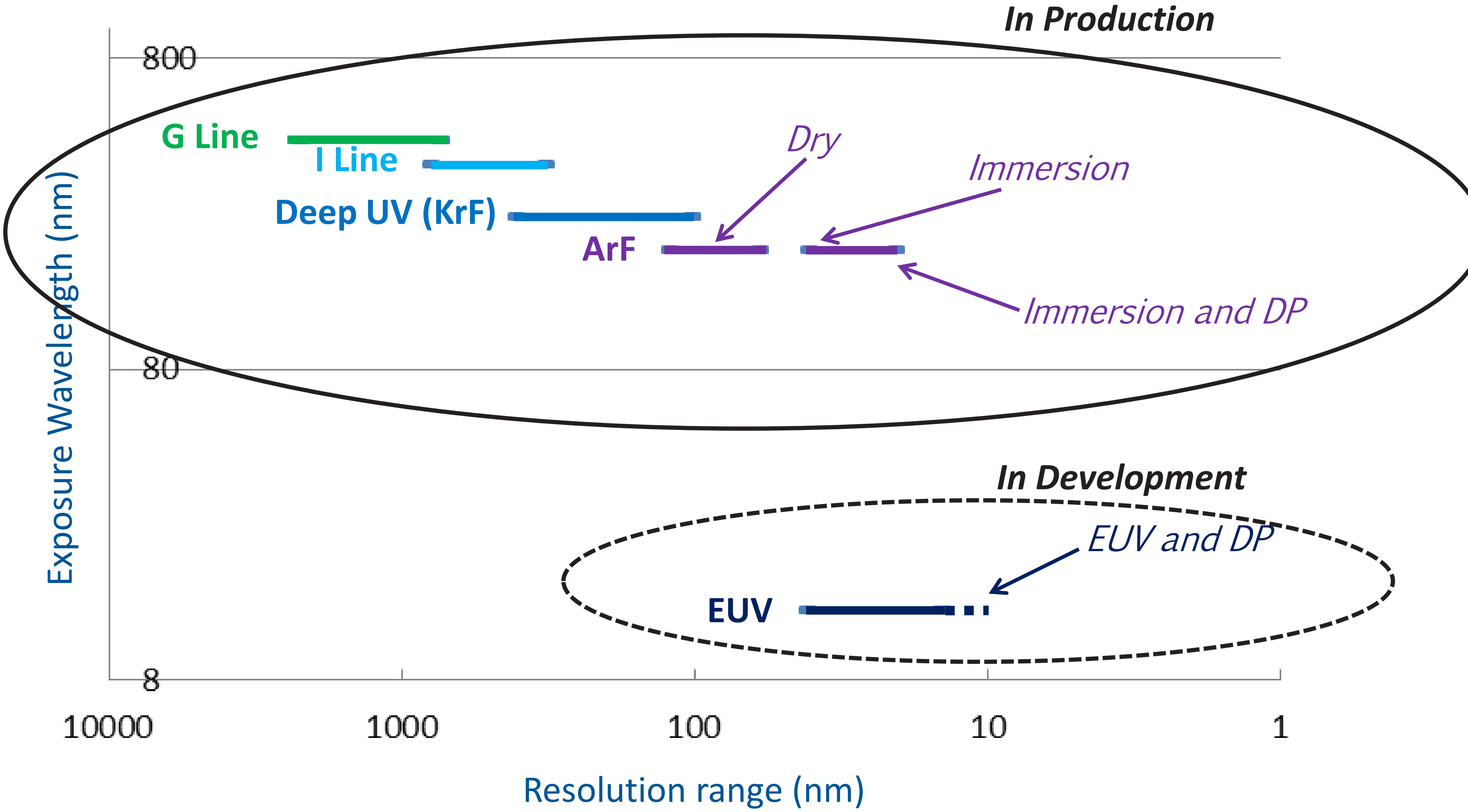
- Improve Resolution by:
  - Shorter Wavelength
  - Higher NA
  - Improved tolerances and processing (lower k_1)
- *But!*

Physics limits resolution

- Can‘t go below $k_1 = 0.25$ in a single exposure (all light will diffract outside the lens)

Improvement through Litho Wavelength and NA

(Historical data per Burn Lin)



Improvement of k_1

- Better exposure tool tolerances
  - Aberrations
  - Flare
  - Control of wafer plane
  - Scan accuracy
  - Etc.

- Improvement of processing
  - Better resolving photoresists
  - Anti-reflective coatings
  - Planarized substrates
  - Ancillary coatings

- The k_1 resolution limit for single patterning with ArF immersion lithography is 36nm for 1.35 NA exposure tool (the highest NA available)

- Pitch Multiplication is used to go past this limit

The Aerial Image View Today

(with dipole illumination for 43nm)

Significant Material Improvement!

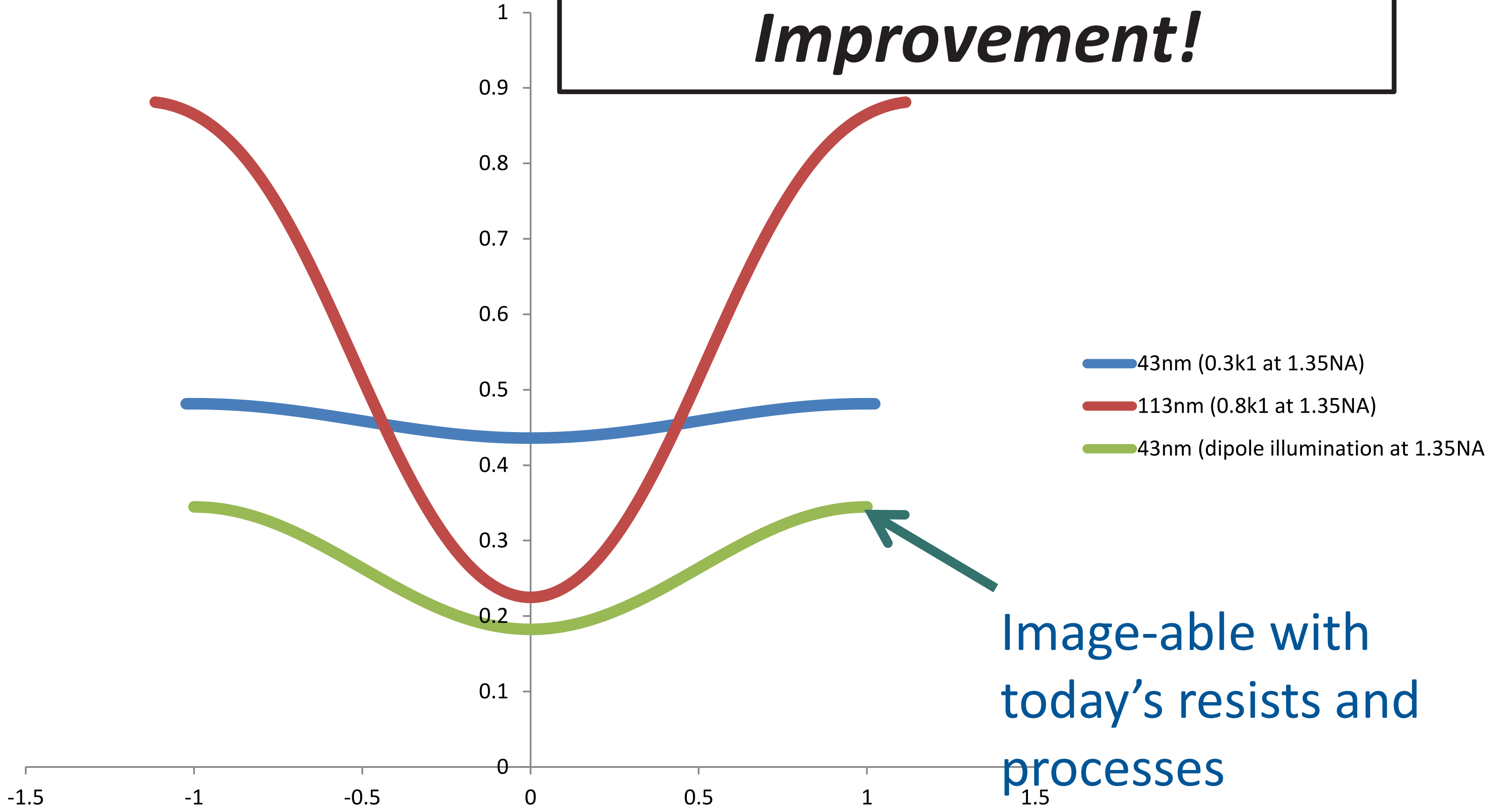


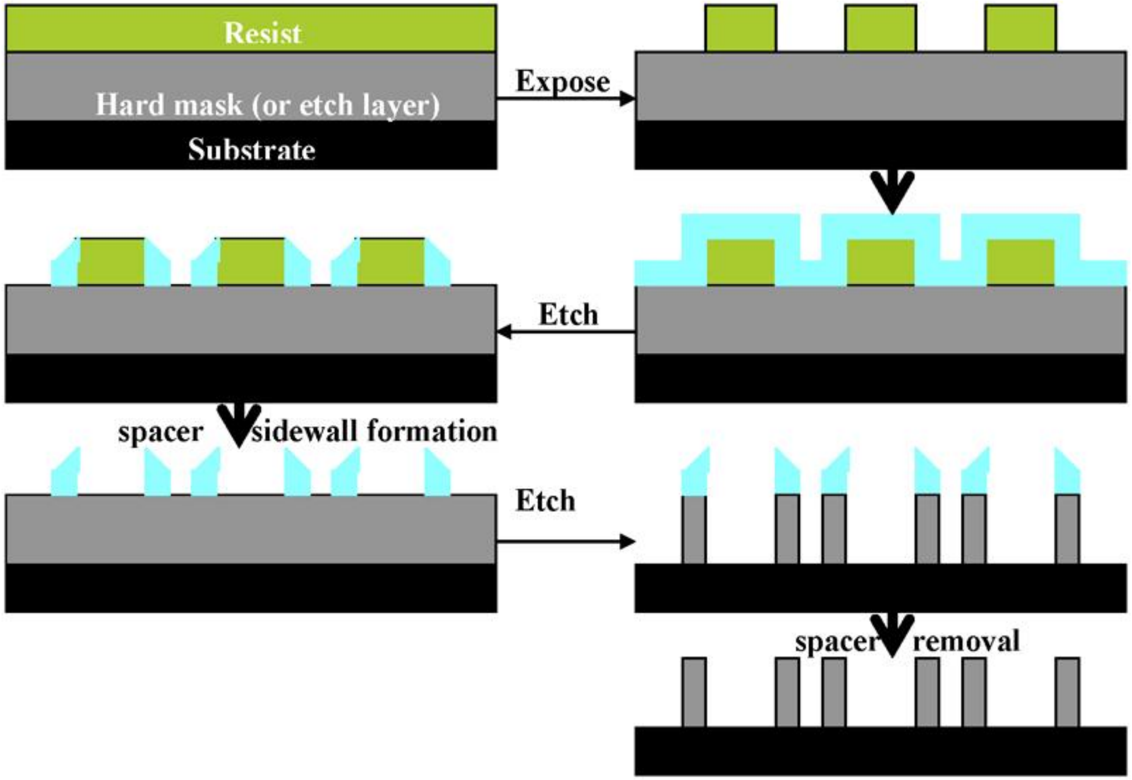
Image-able with today’s resists and processes

Metrology Challenges for Extending Conventional Lithography

- CD measurement including sidewall and profile
- LWR
- Overlay
  - Normally measured optically
  - Need accuracy with optics for <3 nm overlay budget
- Defects
  - Some specifications reflect tool capability rather than need.

DOUBLE AND MULTIPLE PATTERNING

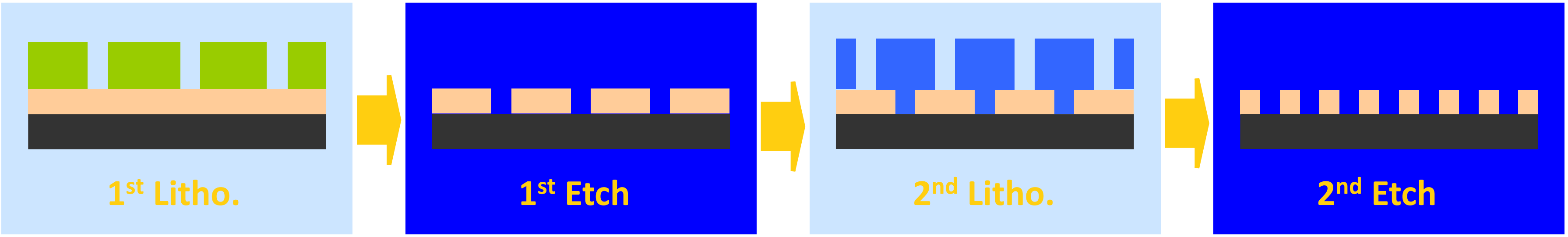
Self Aligned Double Patterning (SADP) -- Pitch multiplication by process



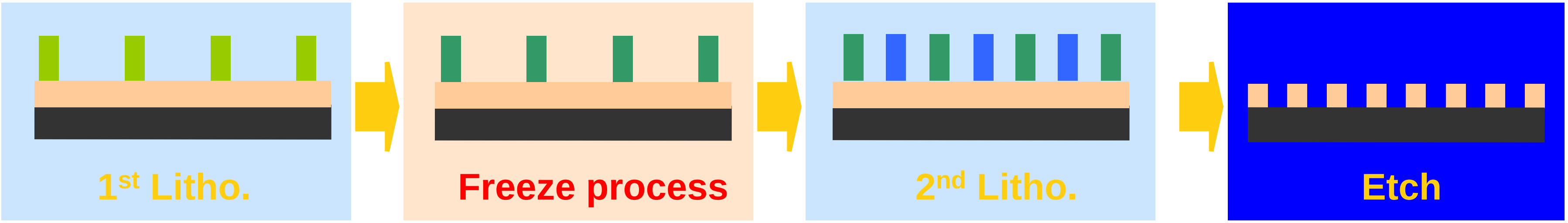
- One exposure with substantial extra processing turns edges into lines and doubles the pitch
- Pattern types that can be produced after doubling are very limited
- Can come close to doubling the pitch. In practice, gives a 30% reduction in pitch (about one semiconductor generation’s worth).

Double Patterning -- Two exposures

Litho – Etch – Litho - Etch



Litho – Freeze – Litho - Etch

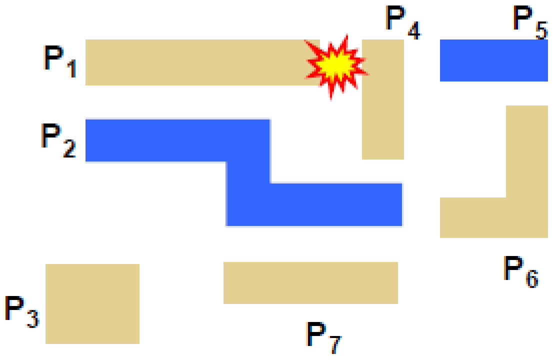


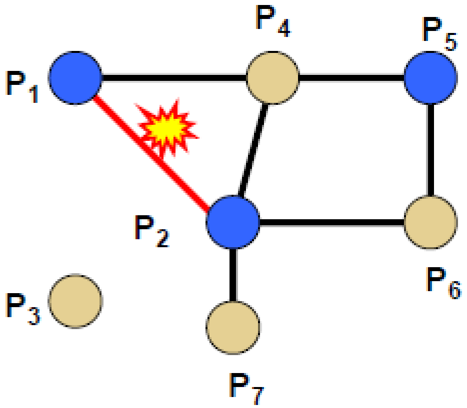
- Two exposure used giving twice the information through the lens
- Pattern types that can be produced are more flexible than SADP, but still need complicated design
- Can come close to doubling the pitch. In practice, gives a 30% reduction in pitch (about one semiconductor generation’s worth).

Double Exposure Design Issues

- 1 D type designs split into two exposures easily

- 2 D type designs can be impossible and require design change

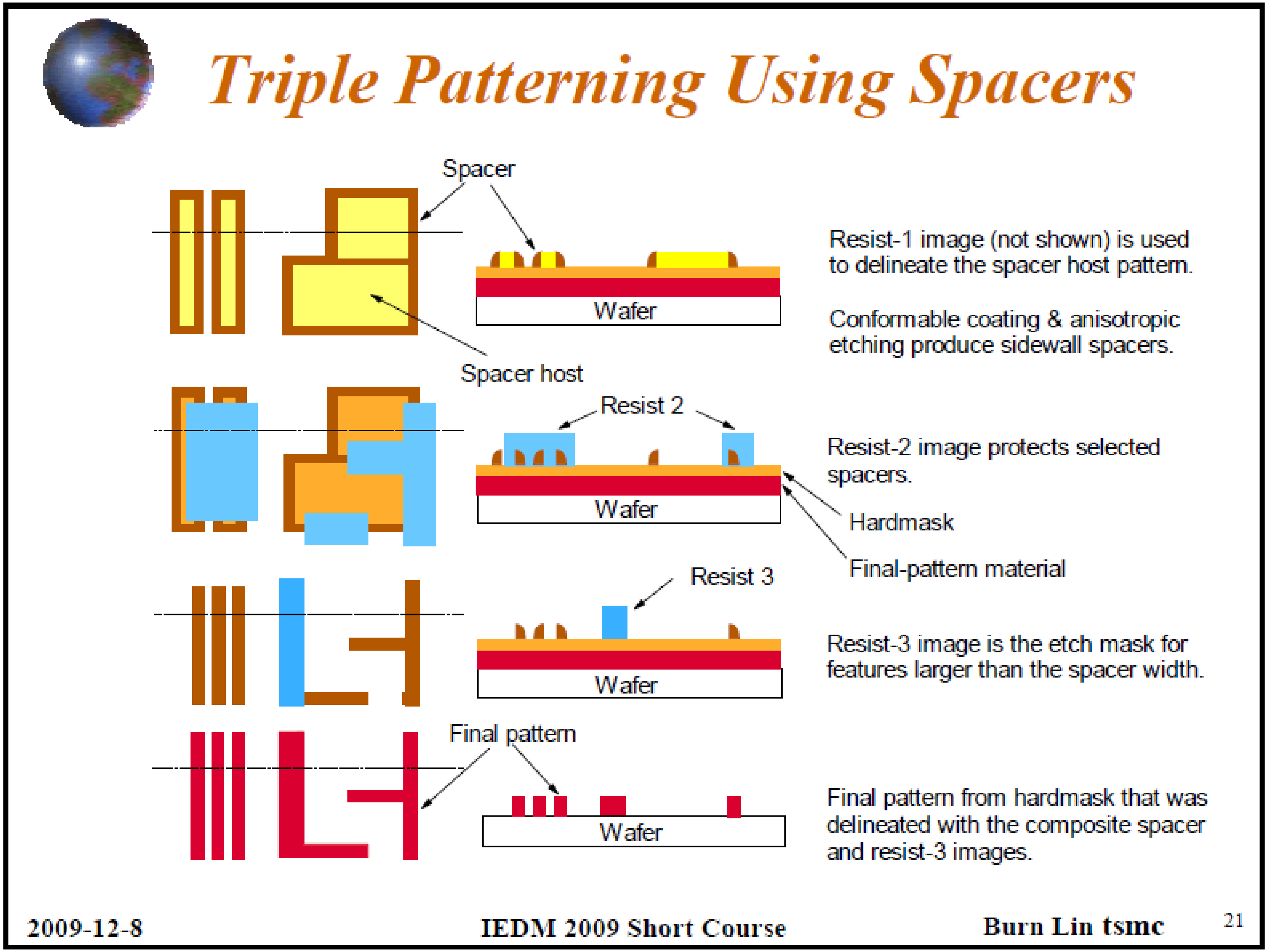




Multiple Patterning (MP)

- Needed for half pitches below roughly 22nm if ArF immersion lithography is to be extended
- Requires “Double” Double patterning
  - Many process options
  - All potential processes complicated and expensive processes
- Expect substantial design restrictions
- Overlay still shrinks with final feature size
  - Many more overlay parameters for multiple patterning
  - Interaction between CDs and OL

Triple Patterning Complexity



Triple Patterning Using Spacers

Resist-1 image (not shown) is used to delineate the spacer host pattern.

Conformable coating & anisotropic etching produce sidewall spacers.

Resist-2 image protects selected spacers.

Resist-3 image is the etch mask for features larger than the spacer width.

Final pattern from hardmask that was delineated with the composite spacer and resist-3 images.

2009-12-8 **IEDM 2009 Short Course** **Burn Lin tsmc** 21

Inspection Challenges with Multiple Patterning

- Many more targets per layer (3 to 6X)
- Exposure 2 to exposure 1 metrology
- Confounding of overlay and CD error
- Multiple CD distributions

EUV

Suppliers execute against roadmap

EUV Product Roadmap

2006	2010	2012	2013
ADT	**NXE:3100**	**NXE:3300B**	**NXE:3350C**
Resolution = 32 nm	Resolution = 27 nm	Resolution = 22 nm	Resolution = 16* nm
NA = 0.25, σ = 0.5	NA = 0.25, σ = 0.8	NA = 0.32, σ = 0.2-0.9	NA = 0.32, OAI
Overlay < 7 nm	Overlay < 4.5 nm	Overlay < 3.5 nm	Overlay < 3 nm
Throughput 5 WPH	Throughput 60 WPH	Throughput 125 WPH	Throughput 150 WPH
@ 5mJ/cm^2	@ 10mJ/cm2	@ 15mJ/cm2	@ 15mJ/cm2
~8W	>100W	>350W	>550W

Main improvements
1) New EUV platform :NXE
2) Improved low flare optics
3) New high σ illuminator
4) New high power LPP source
5) Dual stages

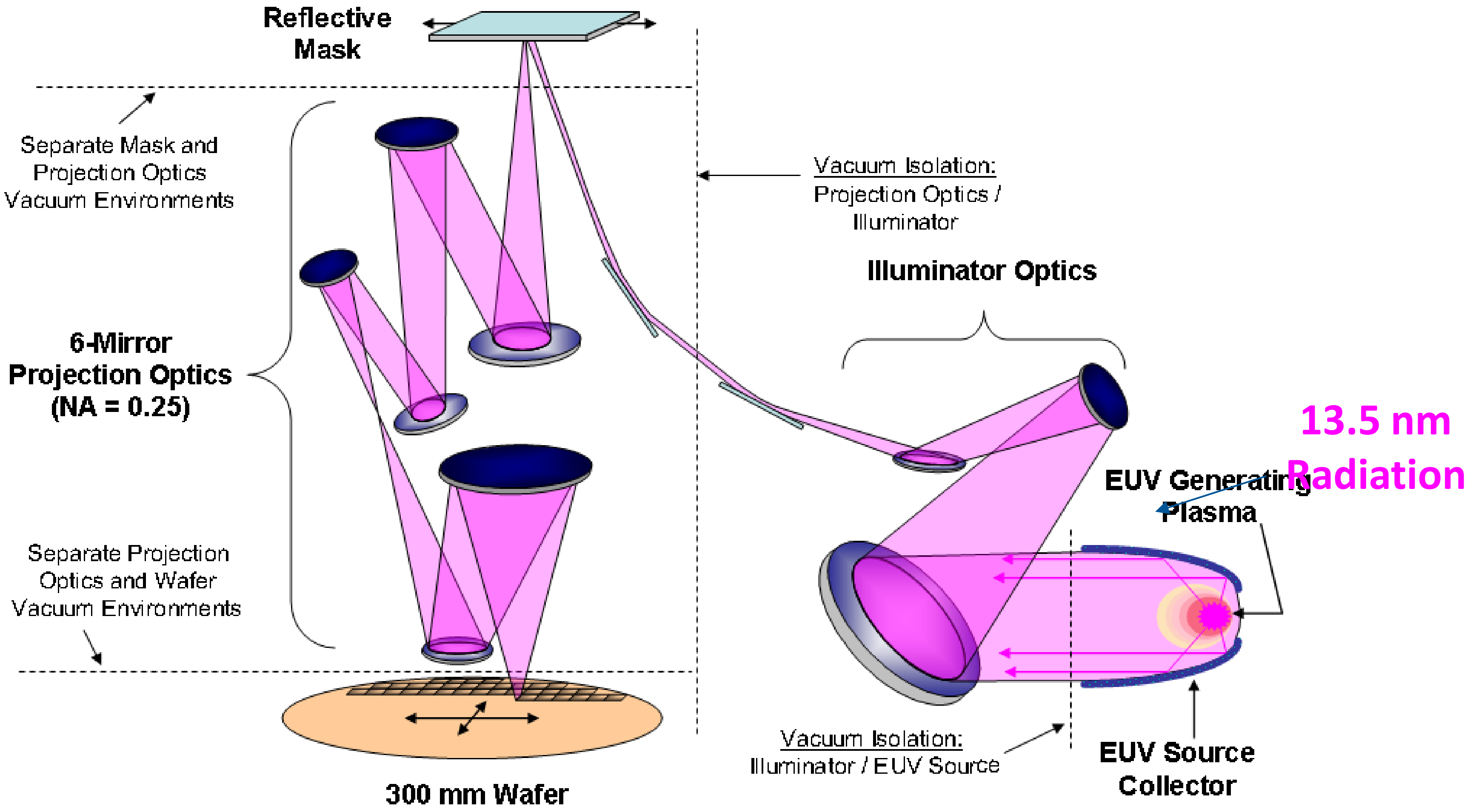
Main improvements
1) New high NA 6 mirror lens
2) New high efficiency illuminator
3) Off-Axis illumination option
4) Source power increase
5) Reduced footprint

Platform enhancements
1) Source power increase

**** Requires <7nm resist diffusion length***

ASML Roadmap, SPIE 2010

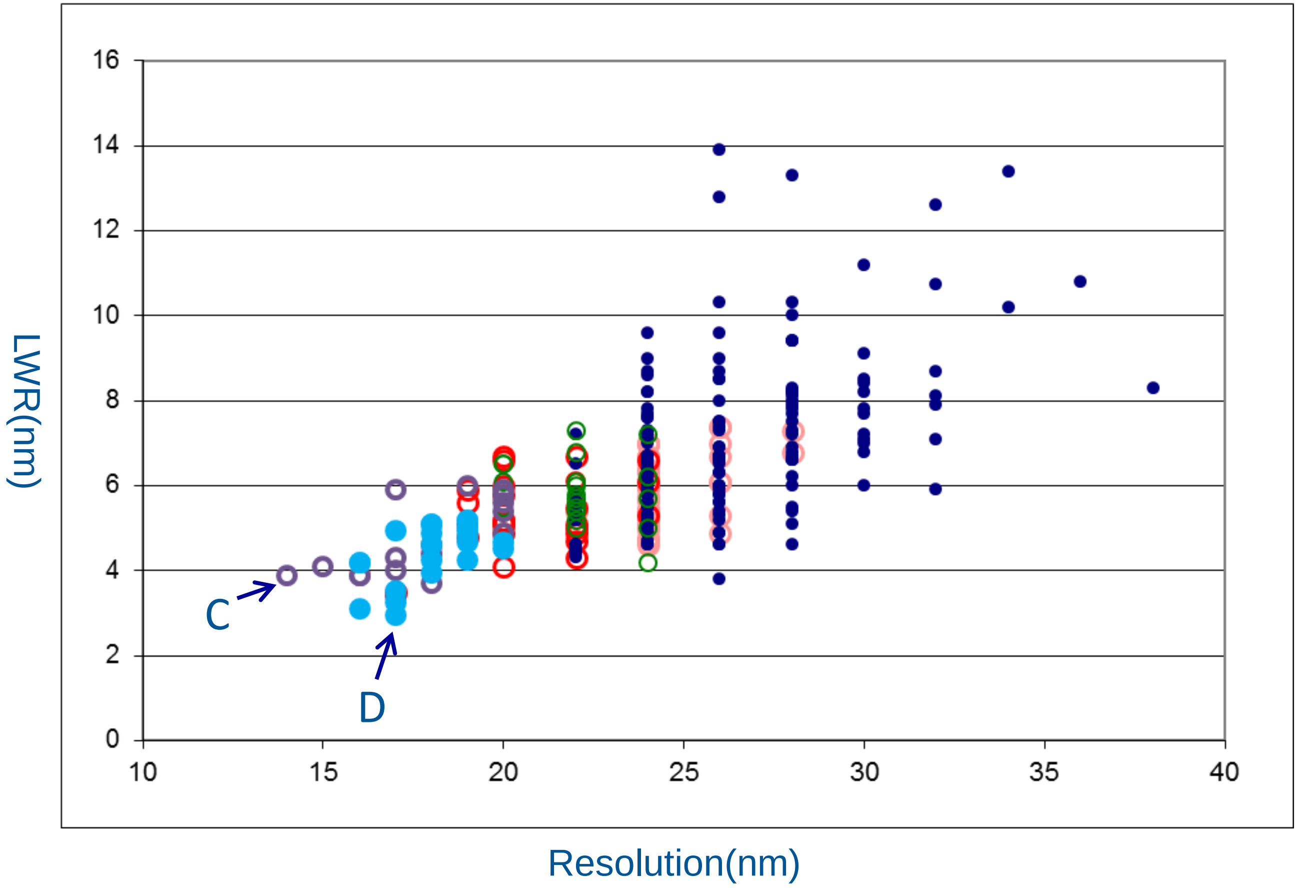
EUV Lithography Exposure System



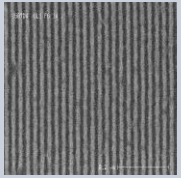
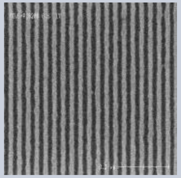
- All Reflective Optics
- Optical train is in a vacuum

EUV Resist Performance Status

Line Width Roughness (LWR) vs. Resolution



● ~2010
○ 2011, Albany Quad
○ 2011, Albany Dipole
○ 2011, LBNL 18nm Dipole
○ 2011, LBNL Pseudo PSM
● 2011, LBNL Pseudo PSM

	C	D
Image		
Size	14nm HP	17nm HP
LWR	3.8nm	2.9nm
Speed	33.6mJ/cm2	26.5mJc/m2

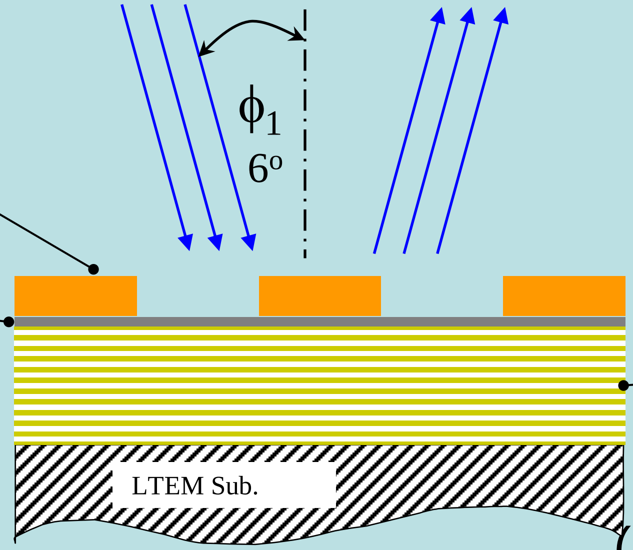
- Resolution of EUV has improved over time, both through resist and imaging tool improvements

EUV Metrology Challenges

- Same ones as for optical extensions
  - CD measurement including sidewall and profile
  - LWR
  - Overlay
  - Defects

- Plus:
  - Actinic substrate, blank, and mask inspection during mask manufacture
  - Defect review after mask cleaning

Typical current EUV mask structure



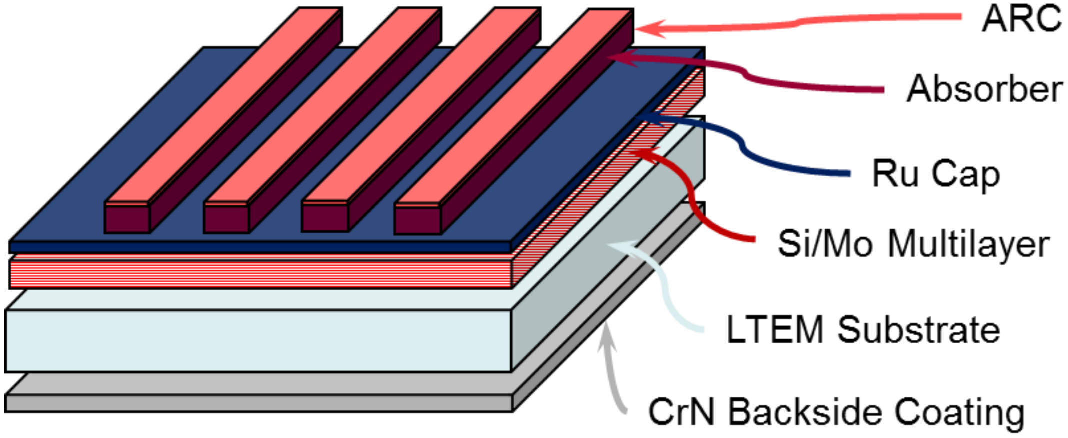
Patterned Absorbers
~ 50 to 70 nm thick
(typically Cr or TaN)

Ruthenium
cap
2.5 nm thick

Reflective
Multilayers
~ 280 nm thick
(Mo/Si pair = 7nm)
40 Pairs

Hard EUV Mask Blank Challenges

Substrate and Blank



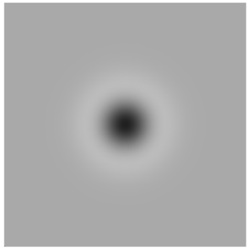
- Absorber/ARC Stack
  - Optical Properties at EUV
  - Properties at Inspection Wavelengths
  - Particle Defects
  - Etch Performance

- Ru Cap
  - Particle Defects
  - Film Loss from Etch
  - Metrology
- Multilayer
  - Particle Defects
  - Uniformity
  - Reflectivity and Centroid Wavelength
  - Metrology (Defect Detection)

This is difficult!

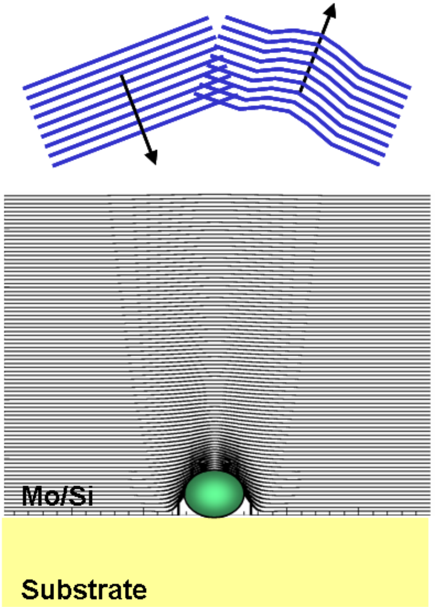
- Substrate
  - Thermal Properties
  - Particle and pit defects
  - Subsurface polishing damage
  - Flatness and Surface Roughness
  - Metrology (Defect Detection)
- Backside Coating
  - Electrical Properties
  - Defectivity

EUV Mask Blank Defects and their Repair

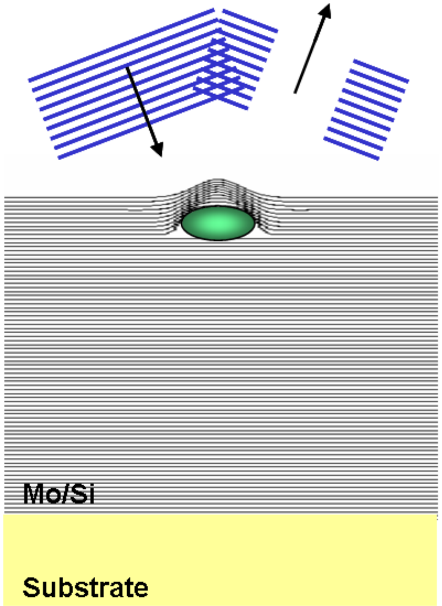


Phase defect wafer plane image

Amplitude defect wafer plane image

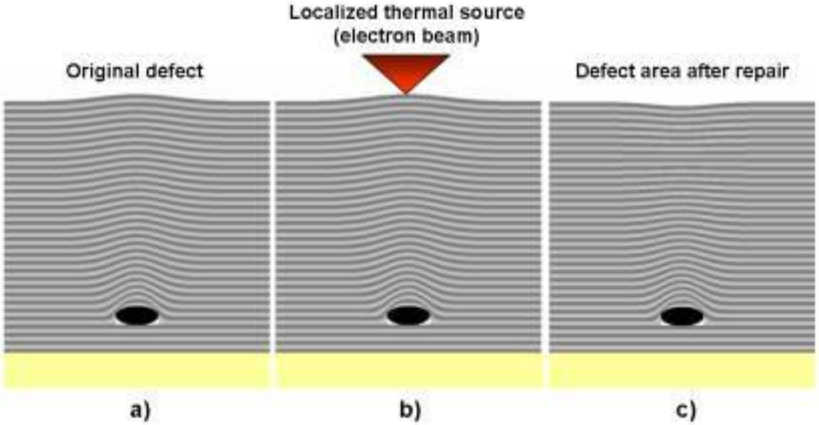


b) Phase defect

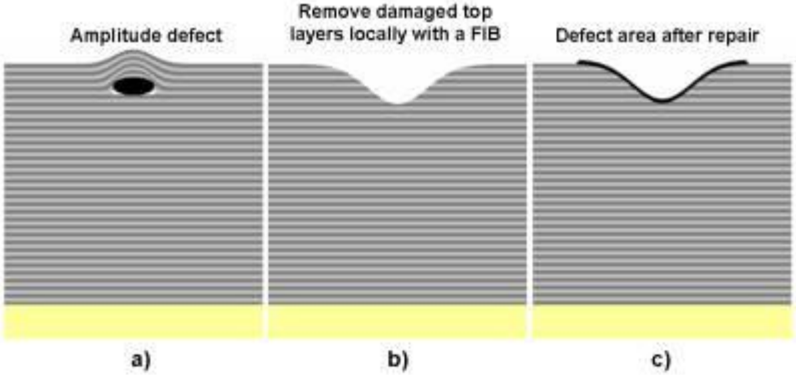


b) Amplitude defect

Phase defect repair technique



Amplitude defect repair technique

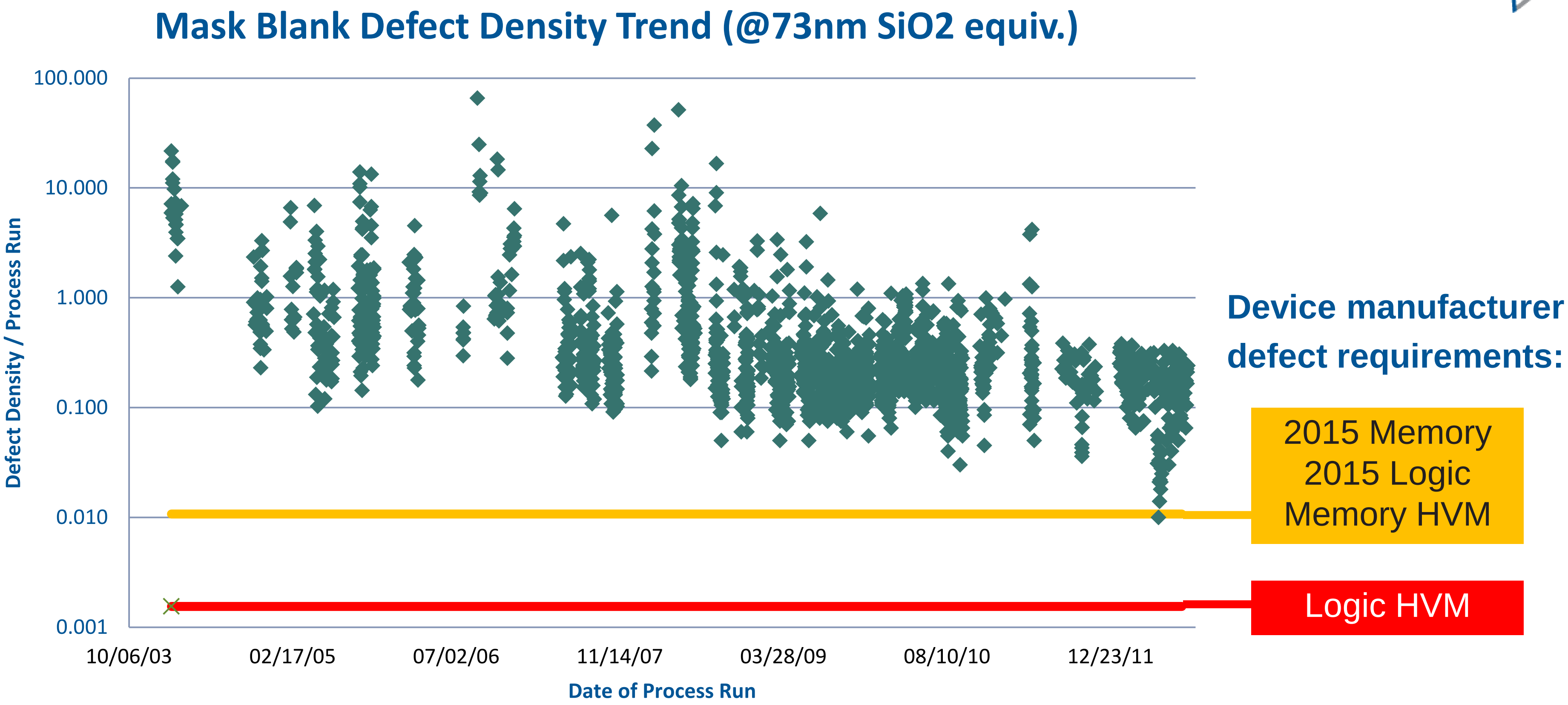


Graphics courtesy to S.P. Hau-Riege, Lawrence Livermore National Labs

EUV Actinic Inspection issues

- Buried defects in masks and optics need actinic inspection to detect
  - Light sources are dim and give slow inspection
  - Defects much smaller than printed feature size can give unacceptable patterning
- Mask layers require atomic level precision
  - Pits and bumps in the substrate must be found and repaired or avoided
  - Flatness and smoothness of substrates are also issues
- Chemical nature of particles can matter

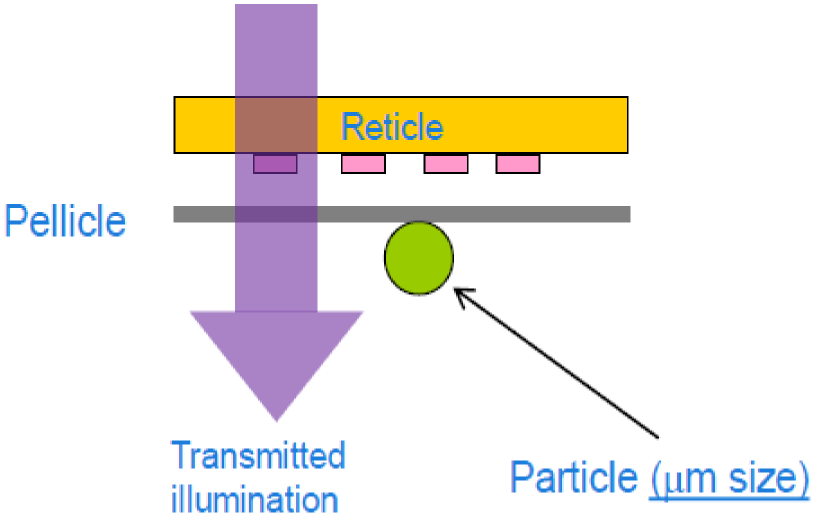
Mask Blank Defect Density Trend



- Progress has been made but more progress is needed.
  - Defects come from both the mask substrate and from layer depositions

Need for Regular Mask Cleaning

DUV Reticles (193nm)



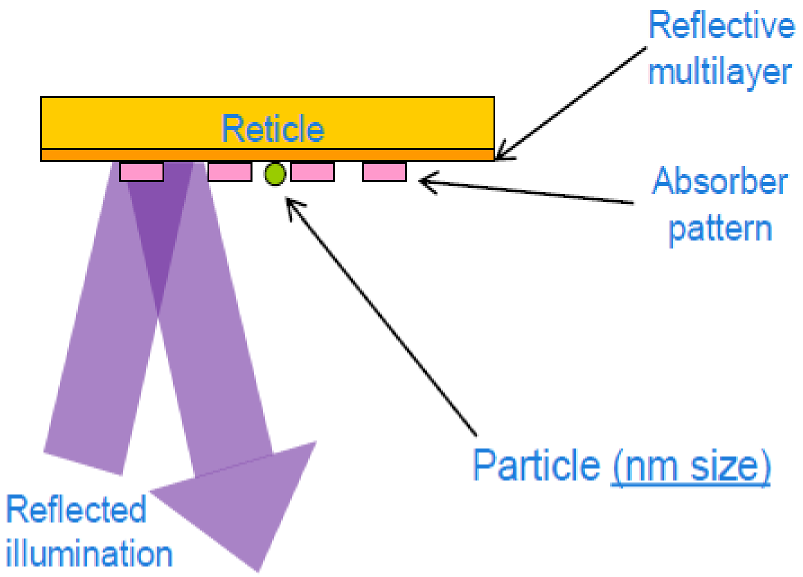
Reticle

Pellicle

Transmitted illumination

Particle (µm size)

EUV Reticles (13.5nm)



Reflective multilayer

Reticle

Absorber pattern

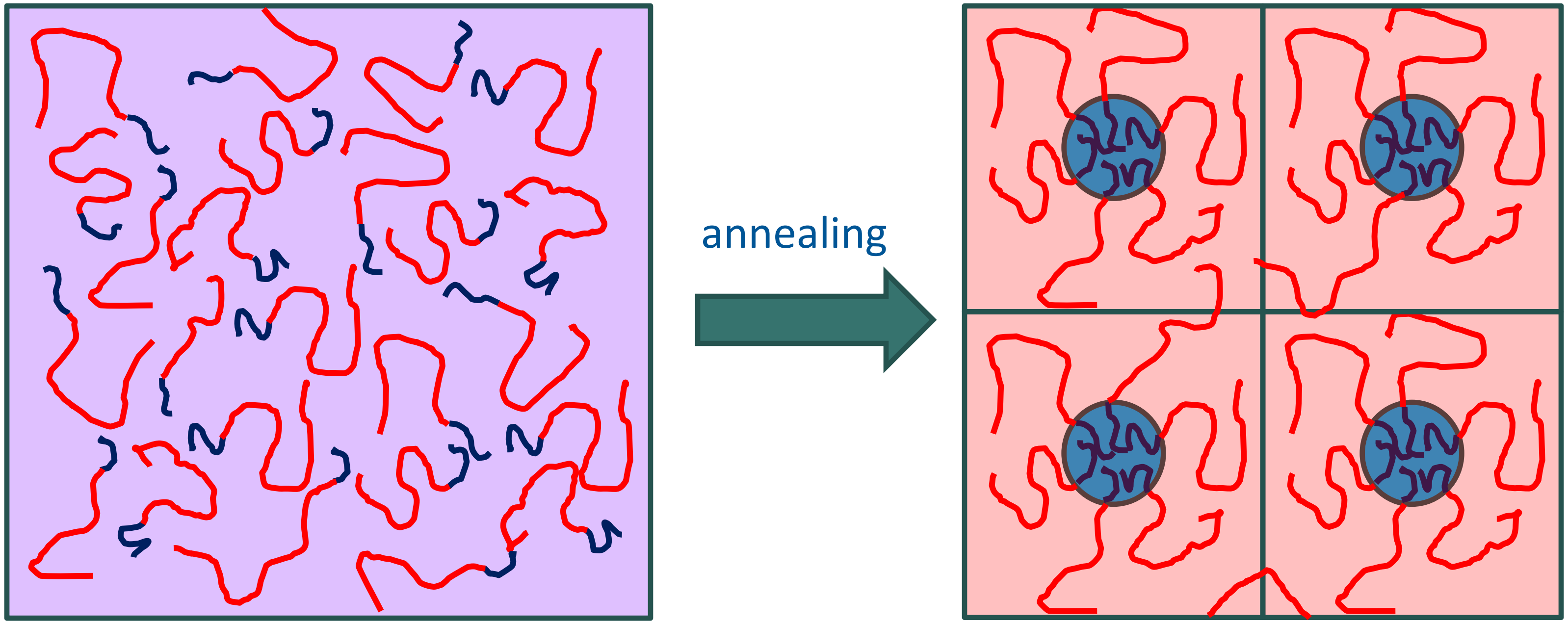
Particle (nm size)

Reflected illumination

- Pellicle for ArF lithography means small particles aren't imaged.
- Lack of pellicle for EUV means very small particles are problems

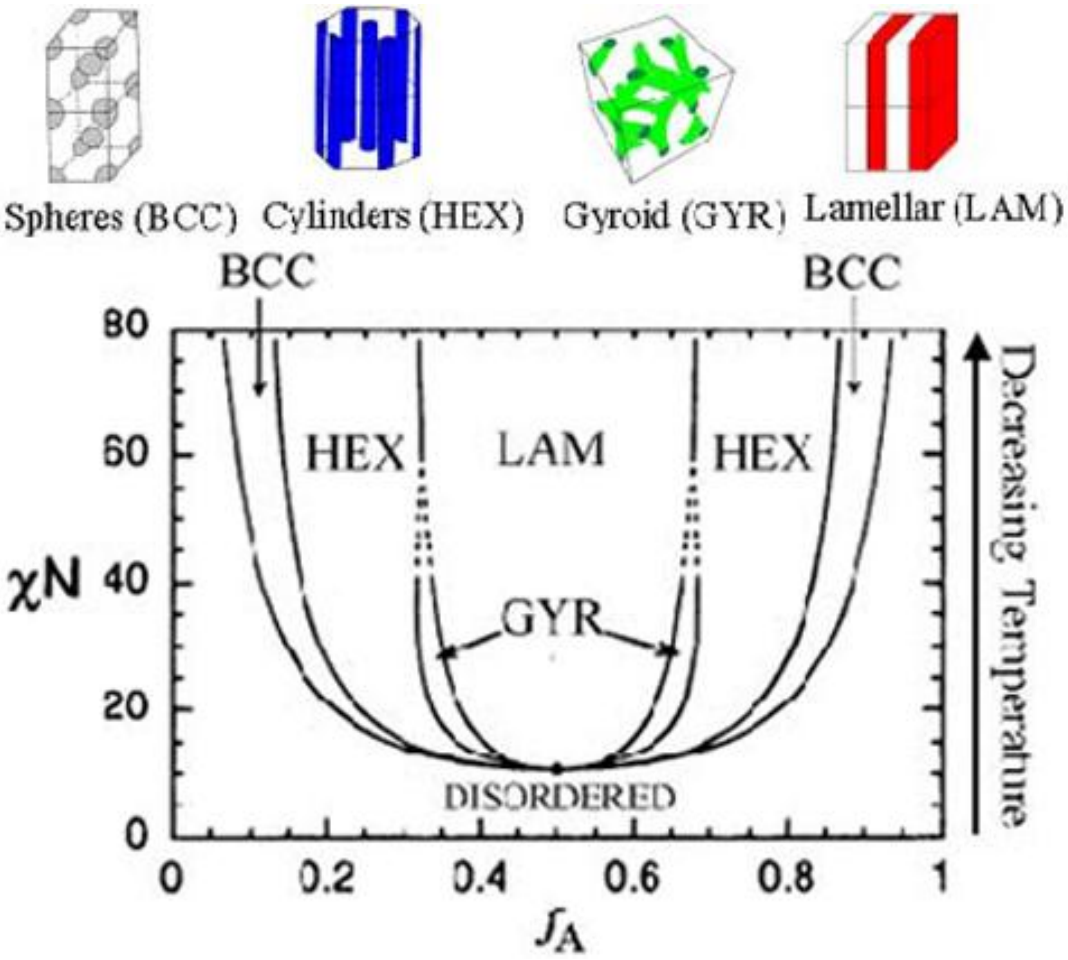
SELF ASSEMBLY

Block Copolymer Self-Assembly for Holes

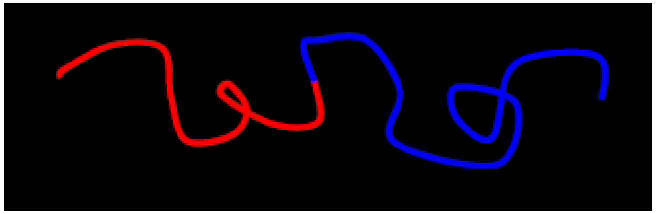


- Polymer chains have “blocks” of each monomer
- Volume ratio of monomers drives the shape of the phase domains
- Overall polymer MW drives size of domains

Block Copolymer Morphologies



Mean field phase diagram for binary BCP



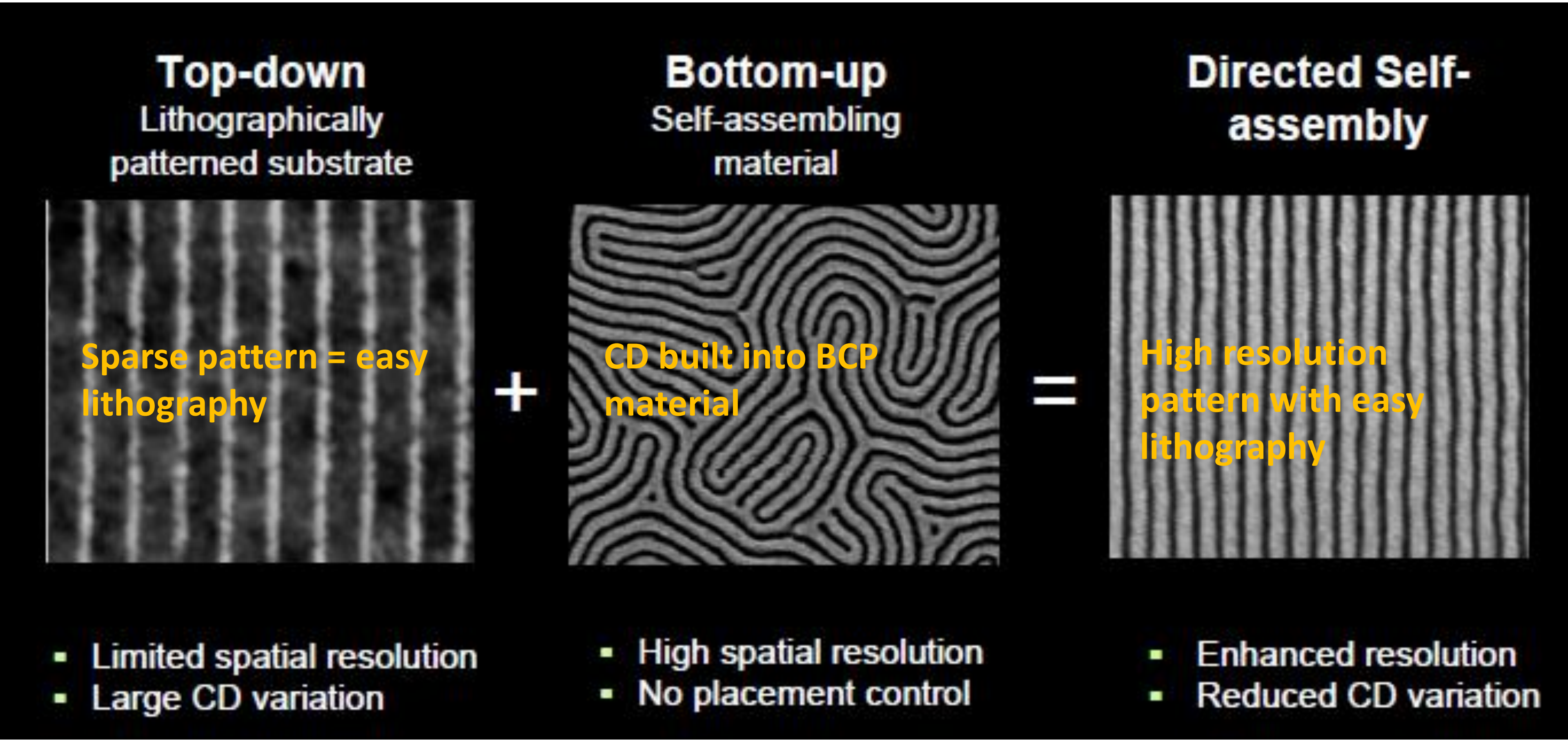
- Phase diagram depends on molecular weight (number of molecules N) and strength of interaction (χ factor)
- Cylinder phase structures look similar to lithographic contact holes.
- Lamellar phase looks similar to lithographic line and space structures.

Thermodynamic driving force for phase separation of polymers

$$\frac{\Delta G_{mix}}{kt} = \frac{f_A}{N_A}\ln\left(f_A\right) + \frac{f_B}{N_B}\ln\left(f_B\right) + f_A f_B \chi$$

The Question: How Can We Make The BCP Phases Lithographically Useful?

The Answer: Directed Self-Assembly



Top-down
Lithographically patterned substrate

Sparse pattern = easy lithography

+

Bottom-up
Self-assembling material

CD built into BCP material

=

Directed Self-assembly

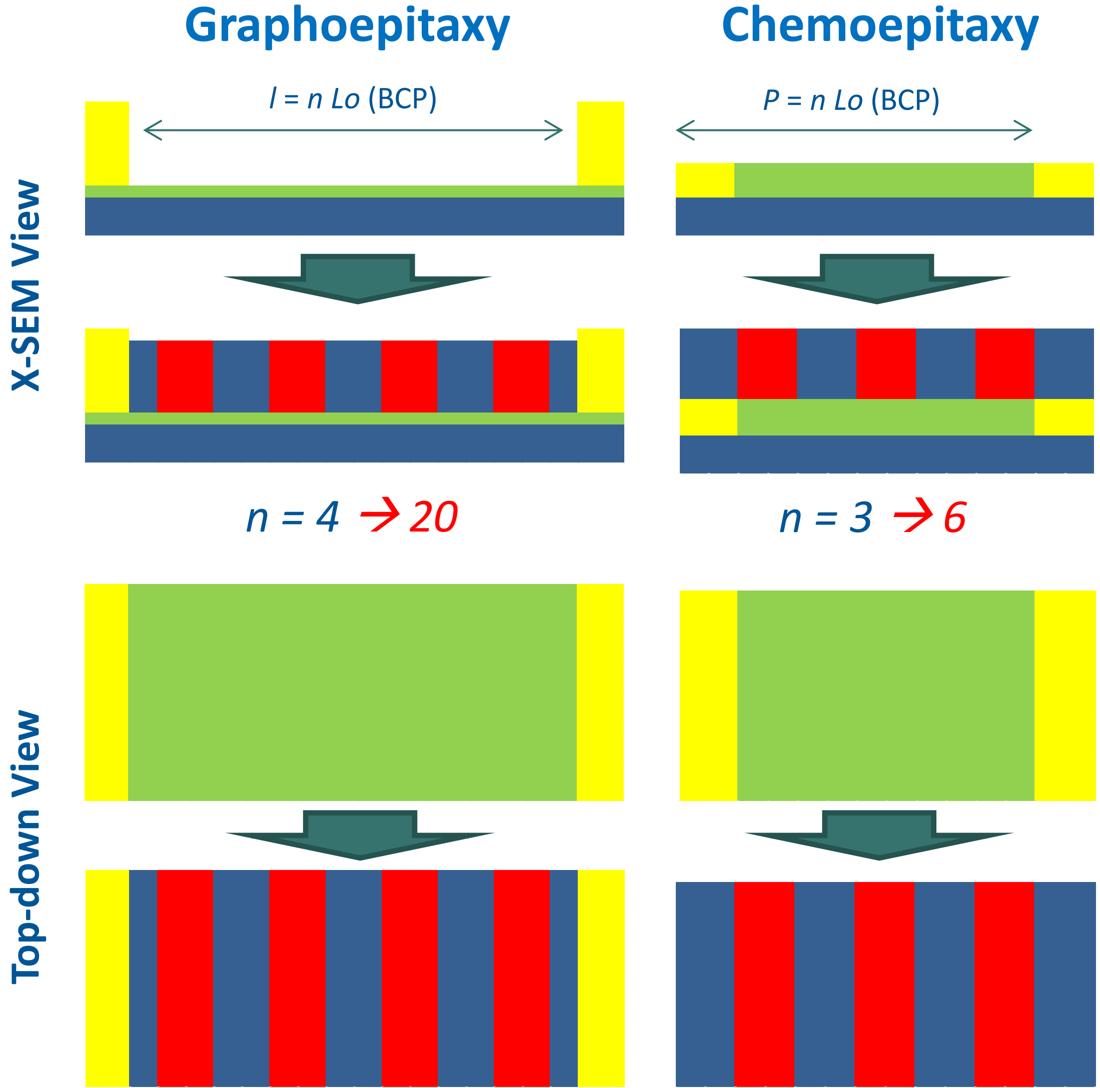
High resolution pattern with easy lithography

- Limited spatial resolution
- Large CD variation

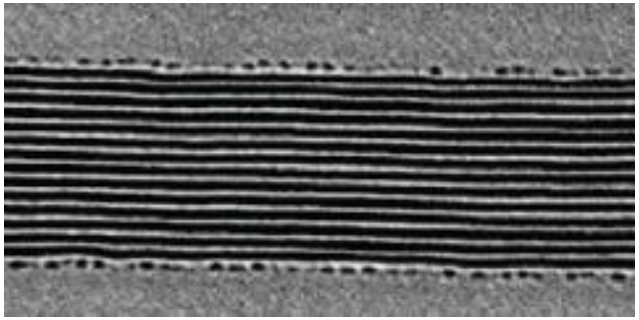
- High spatial resolution
- No placement control

- Enhanced resolution
- Reduced CD variation

Directed Self Assembly Types



- 🟩 ***Neutral surface***
- 🟨 ***Pinning surface***
- 🟦 ***PMMA Block***
- 🟥 ***PS Block***



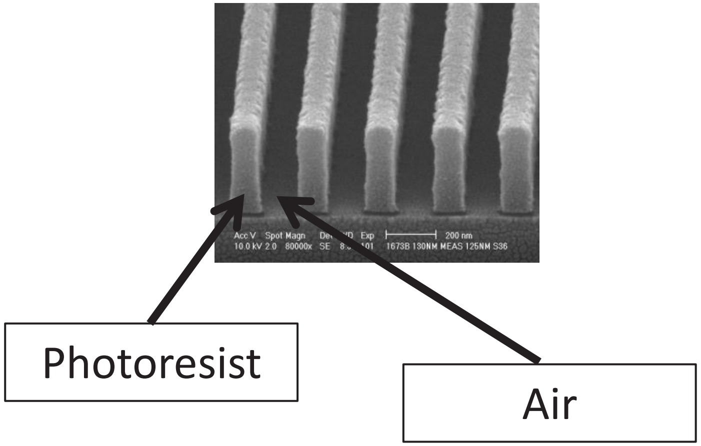
Graphoepitaxy

- Both types of directed self assembly can also be used for contact holes

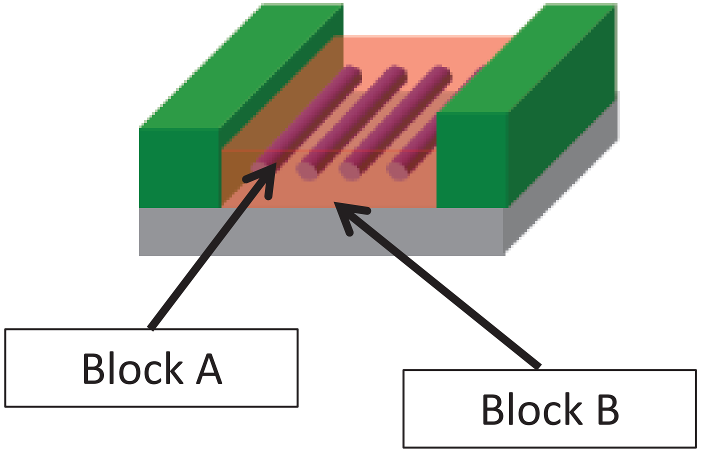
DSA Metrology Challenges

- Assembled Patterns are solid blocks of materials
  - Need inspection before etch
  - Three dimensional structure of the blocks is important
  - How to measure solid phase boundaries?

Conventional Resist



Assembled Block CoPolymer

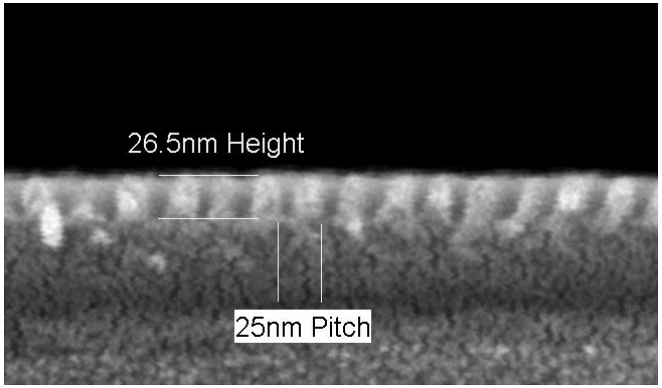


DSA Metrology Challenges

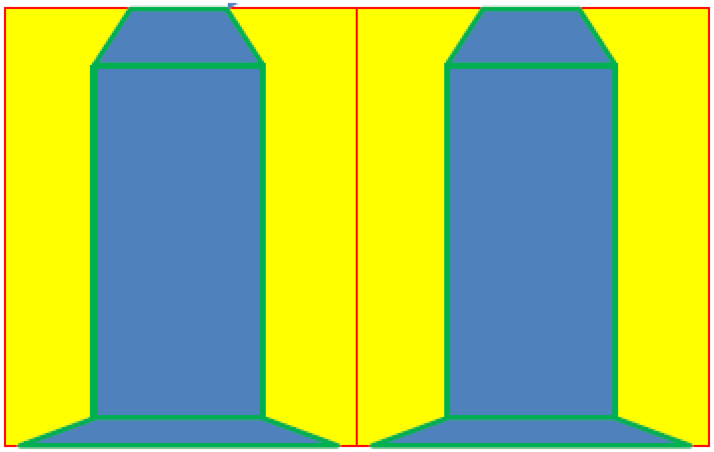
- Actual shape can be different from simple block diagram

Block Diagram

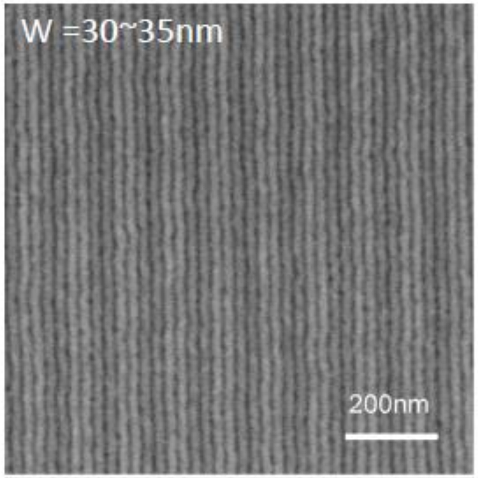
Actual Etched Shape

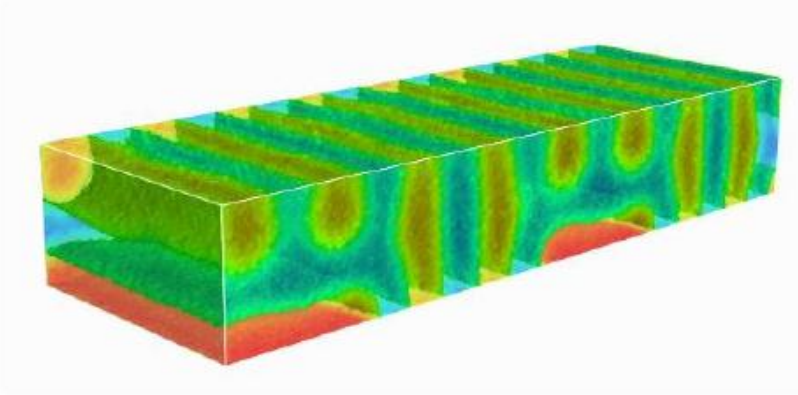


Example of Actual Shape (per Small Angle X-ray Scattering (SAXS) done at NIST)

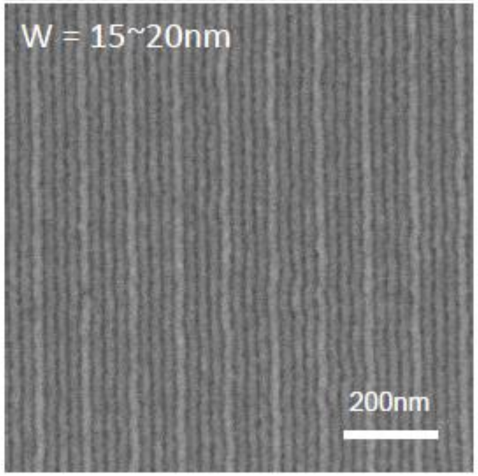


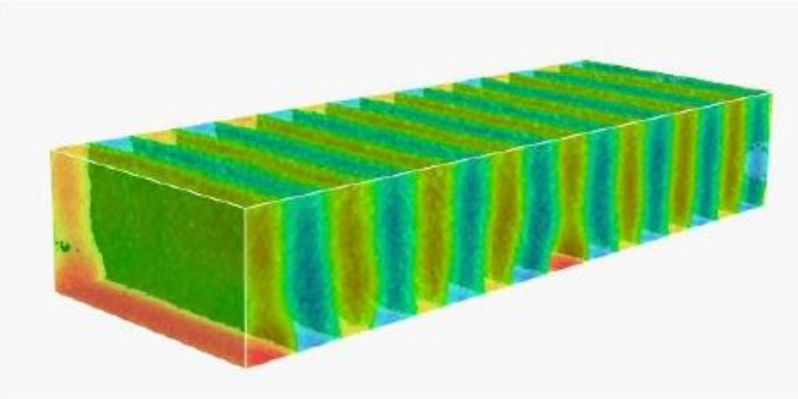
Simulated Good and Bad Annealed Structures -- how to tell the difference from above?





- Alignment features of incorrect size





- Alignment features of correct size

Work published by P. Nealey/J. DePablo

Other DSA Metrology Issues

- Overlay of annealed phases
  - Pitch multiplication results in several or more features spontaneously forming during anneal some distance for the guiding feature.
  - The exact position may vary with respect to guiding feature
  - This can be called “pattern registration”
- CD control
  - Need to check CDs before etching
- Defects
  - Defects could be buried
  - Defects that require rework could be present in annealed phase
  - Conceivably, defects in surface energy of the substrate could make be a problem, even without a physical particle
- The generally small size of the features is intrinsically hard to measure

OTHER ADVANCED PATTERNING APPROACHES

E Beam Direct Write

- Focused beam of electrons is scanned in a way to create the desired pattern in resist without a reticle
  - Has throughput issues
  - Difficult to scale to smaller sizes without losing throughput
- Tools are not available yet, but two companies are working on them
  - Each has multiple beams for writing
  - Scaling will require more and more beams
- Same metrology issues as conventional lithography except:
  - Every wafer probably needs much more inspection for defects and missing features
  - This is because there is no mask that can be inspected in advance

Nanoimprint

- A kind of microstamping and cure process
  - Uses a master template to make replicates
  - Replicates are used for wafer printing and then discarded
  - Masters and replicates are 1X, which makes them hard to make to spec.
- Tools are available for development work
  - Some work being done for disk drive master preparation
  - Some tools are used for semiconductor testing
- This is a contact printing technique
  - Physical contact creates worries about defects
  - The accumulation of particles over time needs to be worked on
- Wafer metrology similar to that of conventional metrology
- “Mask” Metrology is different, but doable
  - The masks 3-D template so position , size and depth have to be inspected
  - Mask vendor claims good progress on this

SUMMARY

Conclusions

- Standard single exposure lithography with ArF does not meet future industry needs.
- The smaller and smaller size of the pattern creates metrology challenges just by itself
- All possible options for future patterning create additional metrology challenges

Acknowledgements

- Our thanks to Alain Diebold and Ralph Dammel for inputs