Characterization and Metrology for
ULSI Technology

Interconnects, an Overview and Critical Review

Kenneth A. Monnig Phd
Associate Director, Interconnect

(03/26/03)

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OUTLINE

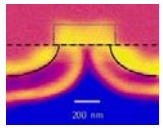
Brief Overview of Interconnect Technology Today

- Progress from 2 yrs ago
- Interconnect Measurement Challenges

Restate The Challenge;

- We need to measure Properties of the 'Sidewall'
- Flat Film Properties Decreasingly Important
- Destructive and/or Cross-section Test Increasingly Costly

The Coming Era of "Beyond Cu and Low-K"



2000 International Conference on Characterization and Metrology for ULSI Technology

NIST

The Coming & Ongoing Changes in IC Interconnect Fabrication

&

What This Has to do With Metrology

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(06/27/00)

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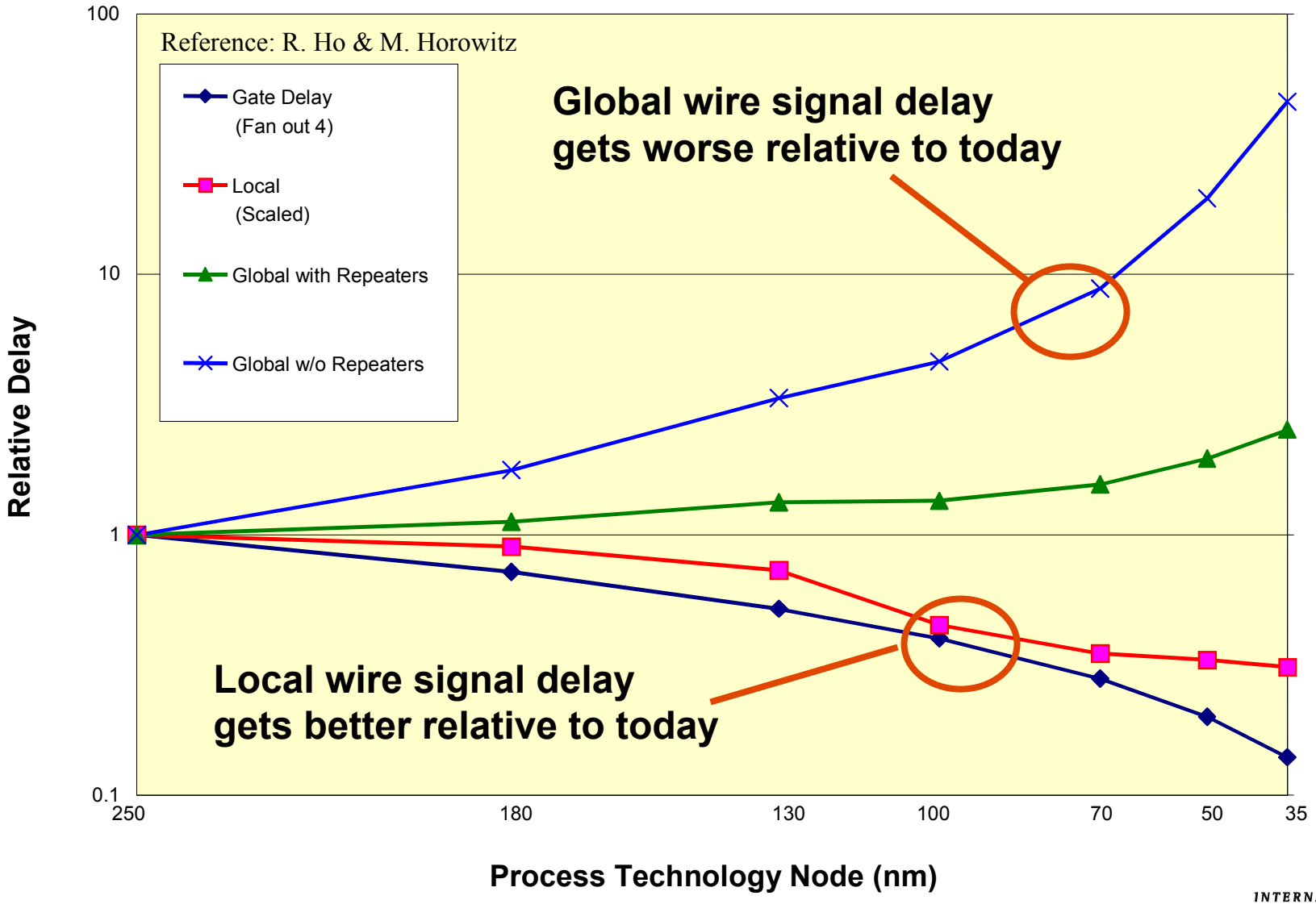
INTERCONNECT DELAY VS. DESIGN RULE



2002 *Condensed* ITRS

Year of First Product Shipment Technology Generation	2003 100	2004 90	2005 80	2006 70	2007 65	2010 45	2013 32
Number of metal levels—DRAM	4	4	4	4	4	4	4
Number of metal levels—logic	8	9	10	10	10	10	10
Jmax (A/cm^2)-wire (at 105^{o}C)	1.3E6	1.5E6	1.7E6	1.9E6	2.1E6	2.7E6	3.3E6
FITs/m legnth/cm^2 x 10^{-3} excluding global levels							
Local wiring pitch—DRAM (nm) non-contacted	200	180	160	150	130	90	64
Local wiring pitch—logic (nm)	245	210	185	170	150	105	75
Local wiring AR—logic (Cu)	1.6	1.7	1.7	1.7	1.7	1.8	1.9
Cu local wiring thinning (nm)	20	18	16	14	13	5	4
Intermediate wiring pitch—logic (nm)	320	275	240	215	195	135	95
Intrmdt wiring h/w AR-logic (Cu DD via/line)	1.7/1.5	1.7/1.5	1.7/1.5	1.7/1.6	1.8/1.6	1.8/1.6	1.9/1.7
Cu intrmdt wiring thinning (nm)	27	23	20	18	18	12	9
Global wiring pitch—logic (nm)	475	410	360	320	290	205	140
Global wiring h/w AR-logic (Cu DD via/line)	2.1/1.9	2.1/1.9	2.2/2.0	2.2/2.0	2.2/2.0	2.3/2.1	2.4/2.2
Cu global wiring thinning (nm)	168	193	176	158	172	155	148
Contact aspect ratio-DRAM, stacked cap	9.3	11.4	13	13	14.1	16.1	23.1
Conductor effective resistivity (μΩ-cm) Cu *	2.2	2.2	2.2	2.2	2.2	2.2	2.2
Barrier/cladding thickness (nm)***	12	10	9	8	7	5	3.5
Interlevel metal insulator effective dielectric constant (k) logic	3.0-3.6	2.6-3.1	2.6-3.1	2.6-3.1	2.3-2.7	2.1	1.9
Interlevel metal insulator (minimum expected) -bulk dielectric constant (k)	<2.7	<2.4	<2.4	<2.4	<2.1	<1.9	<1.7

Process and Material Solutions Can't Meet Needs

* Assumes a conformal barrier/nucleation layer

*** Calculated for a conformal layer in local wiring to meet effective conductor resistivity

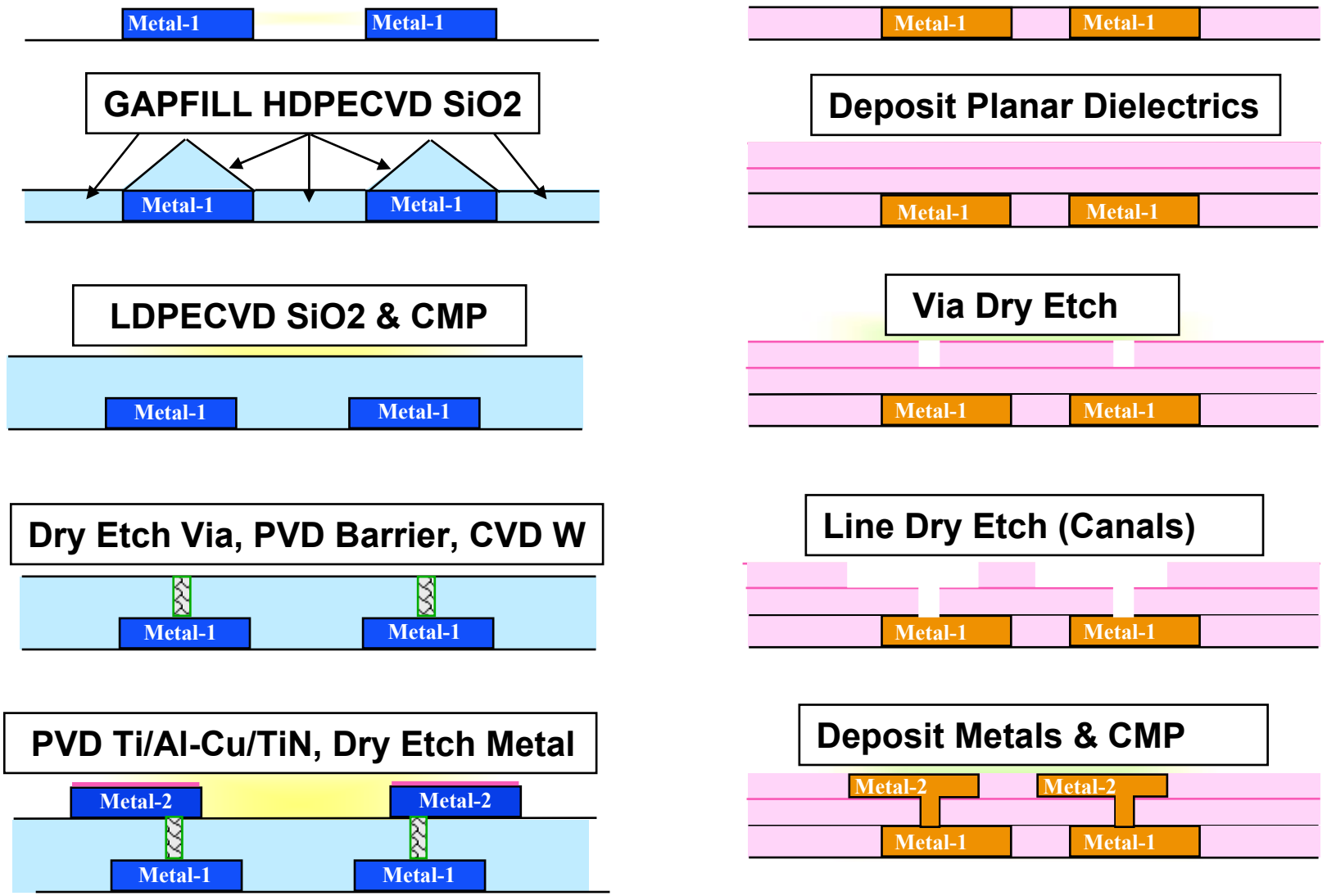
ROADMAP 'CREEP'

Roadmap		Year of First Product Shipment	1997	1999	2000	2001	2002	2003	2004	2005	2006	2007	2008	2009	2010	2011	2012	2013	2014
		Technology Node	250 nm	180 nm		150nm		130 nm			100 nm			70 nm			50 nm		
1997	NA	Interlevel metal insulator—effective dielectric constant (k)	3.0 - 4.1	2.5 - 3.0		2.0-2.5		1.5 - 2.0			1.5 - 2.0			≤ 1.5			≤ 1.5		
		Technology Node	250 nm	180 nm			130 nm			100 nm			70 nm			50 nm			35
1998 Update	NA	Minimum interlevel metal insulator—effective dielectric constant (k)	3.0 - 4.1	2.5 - 4.1			1.5 - 2.0			1.5 - 2.0			≤ 1.5			≤ 1.5			
				180 nm			130 nm			100 nm			70 nm			50			35
1999	MPU	Interlevel metal insulator—effective dielectric constant (k)		3.5-4.0	3.5-4.0	2.7-3.5	2.7-3.5	2.2-2.7	2.2-2.7	1.6-2.2			1.5			<1.5			<1.5
	SOC	Interlevel metal insulator—effective dielectric constant (k)		3.5-4.0	3.5-4.0	2.7-3.5	2.7-3.5	2.2-2.7	2.2-2.7	1.6-2.2			1.5			<1.5			<1.5
	DRAM	Interlevel metal insulator—effective dielectric constant (k)		4.1	4.1	4.1	3.0-4.1	3.0-4.1	3.0-4.1	2.5-3.0			2.5-3.0			2.0-2.5			2.0-2.3
				180 nm		130 nm			90 nm				60 nm			40			30
2000 Update	MPU	Interlevel metal insulator—effective dielectric constant (k)		3.5-4.0	3.5-4.0	2.9-3.5	2.9-3.5	2.2-2.9	2.2-2.9	1.6-2.2			1.6			<1.6			<1.3
	MPU	Interlevel metal insulator—BULK dielectric constant (k)		2.9	2.9	2.7	2.7	2	2	1.3			1.3			<1.3			1.1
	SOC	Interlevel metal insulator—effective dielectric constant (k)		3.5-4.0	3.5-4.0	2.7-3.5	2.7-3.5	2.2-2.7	2.2-2.7	1.6-2.2			1.5			<1.5			<1.5
	DRAM	Interlevel metal insulator—effective dielectric constant (k)		4.1	4.1	4.1	3.0-4.1	3.0-4.1	3.0-4.1	2.5-3.0			2.5-3.0			2.0-2.5			2.0-2.3
				180 nm		130 nm	115 nm	100 nm	90 nm	80 nm	70 nm	65 nm			45nm			32 nm	
2001	MPU	Interlevel metal insulator—effective dielectric constant (k)				3.0-3.6	3.0-3.6	3.0-3.6	2.6–3.1	2.6–3.1	2.6–3.1	2.3–2.7			2.1			1.9	
	MPU	Interlevel metal insulator (minimum expected) —bulk dielectric constant (k)				<2.7	<2.7	<2.7	<2.4	<2.4	<2.4	<2.1			<1.9			<1.7	
	DRAM	Interlevel metal insulator—effective dielectric constant (k)				4.1	3.0–4.1	3.0–4.1	3.0–4.1	3.0–4.1	2.6–3.1	2.6–3.1			2.3–2.7			2.3–2.7	

Roadmap Year	K~2.5	K~2.0
1997	2000	~2003
1998 Update	2000+	~2002
1999	Early 2004	2006
2000 Update	~2007	2006+
2001	Early 2006	~2012

INTERCONNECT PROCESS FLOWS

Traditional Flow VS *Dual Damascene*



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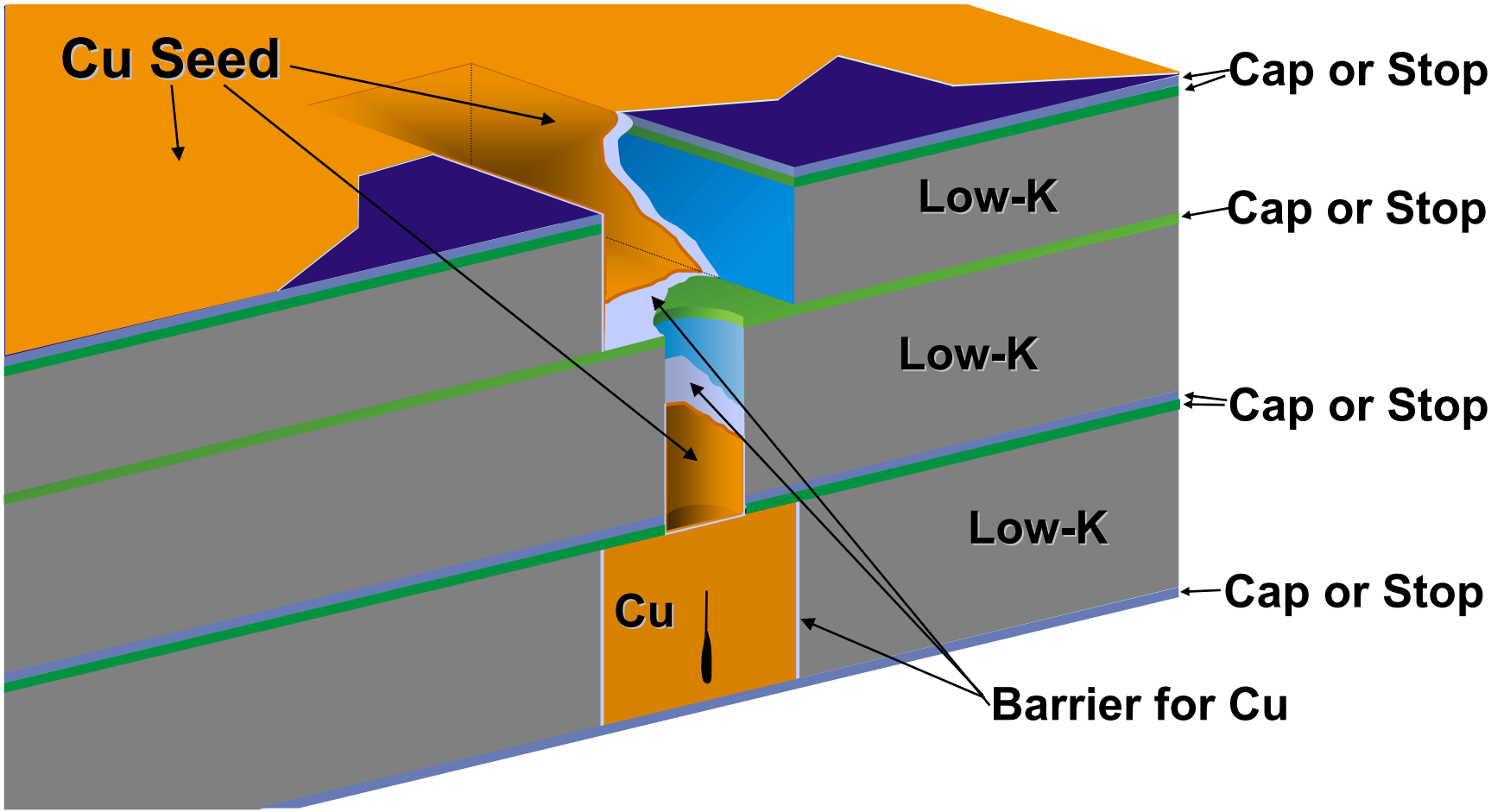
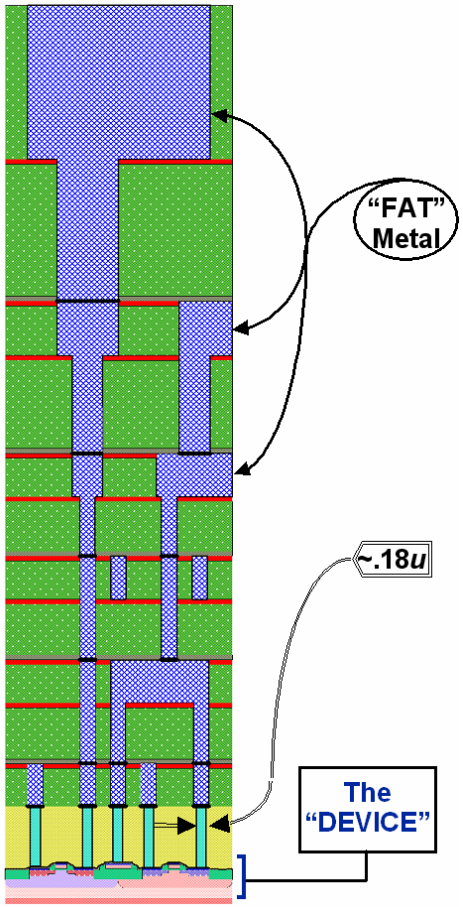
A DUAL DAMASCENE 'UNIT' STRUCTURE



COMPLEXITY

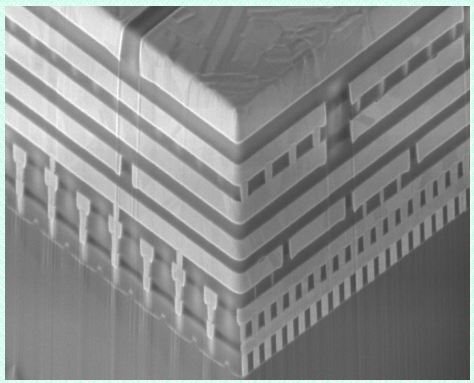
2000 Artist Concept



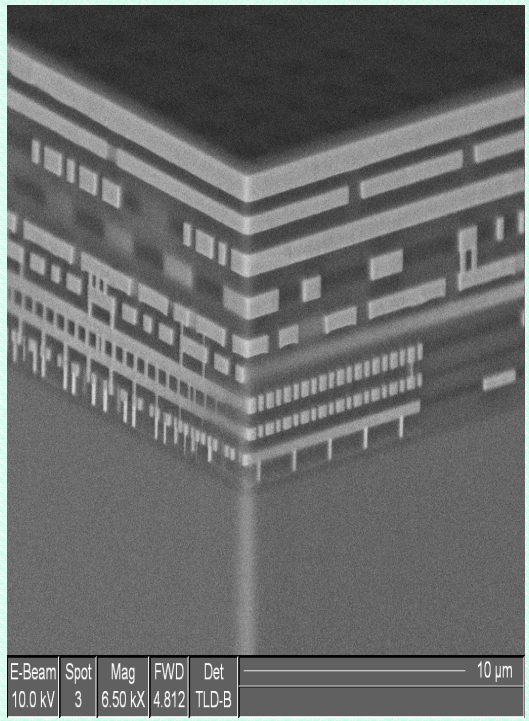
2002 REALITY

AMD

130nm – 6LM



90nm – 9LM



Devices and SEM Cross-sections Courtesy of AMD

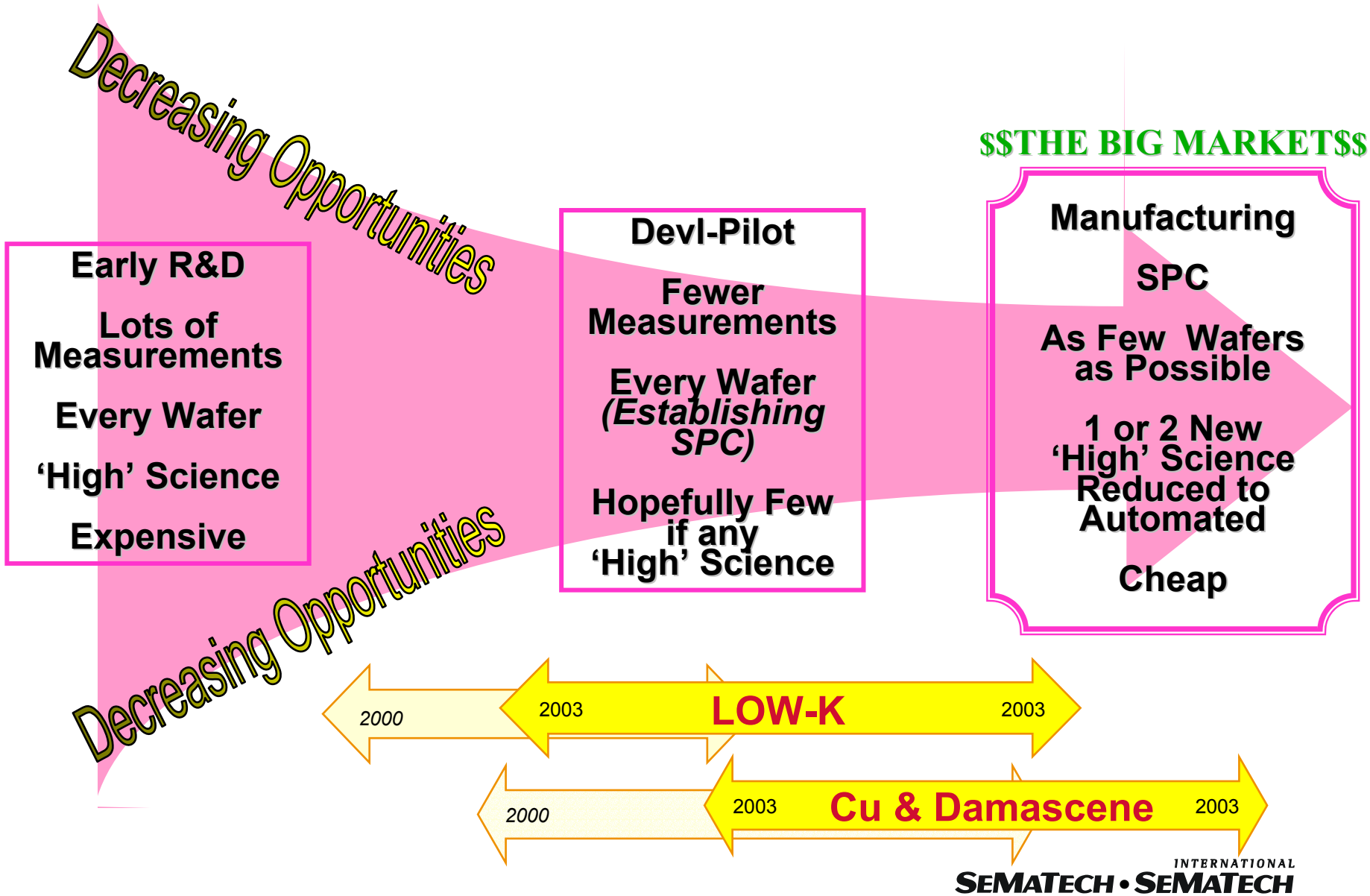
Half of the Structure and Cost of an IC is Interconnects

IMPACT OF CU, LOW-K, DAMASCENE

- **All of the Interconnect Materials Are Being Changed**
- **Most of the Process Methods Are Being Changed, Therefore Most of the Equipment Set Is Impacted**
- **To Get a Dielectric Constant Below ~2.5 'Porosity' Must Be Added**

  The Materials Become Increasingly 'Fragile'

A WORD ABOUT METROLOGY



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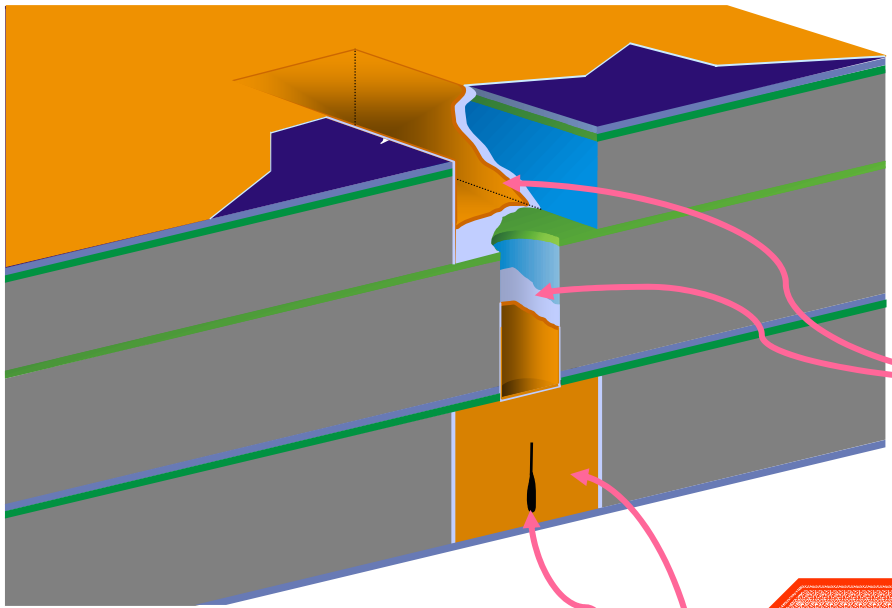
Metrology Needs (2000)

Metal Deposition



Want to Measure;
Thin Things on the Sidewalls of Deep Things

Barrier and Seed;

- Thickness (in detail)
- Resistivity
- Morphology
- Composition

Want to Measure;
Metal Properties in the "Canal"

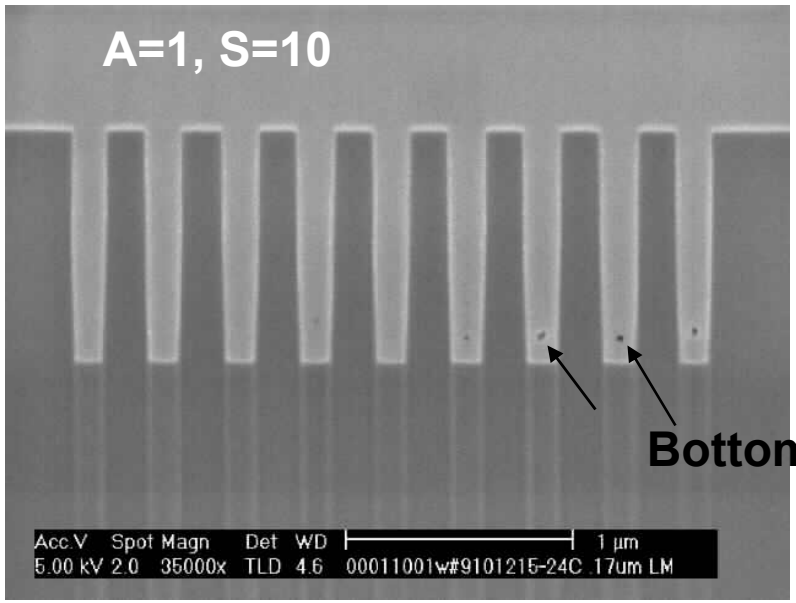
Line;

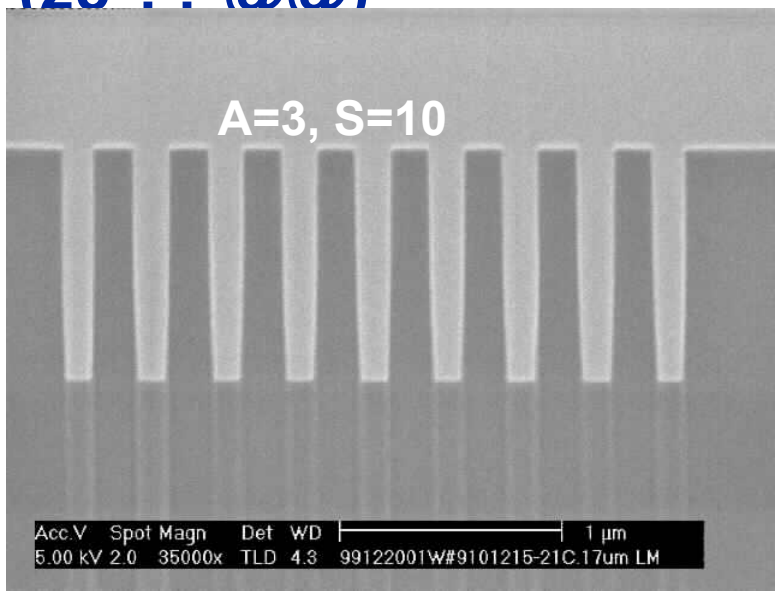
- Resistivity
- Orientation
- Voids
- Composition

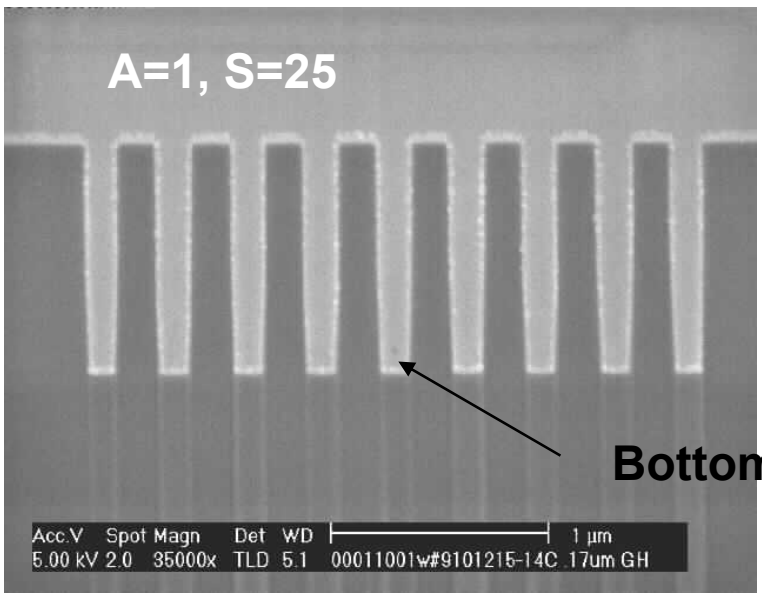
We now measure;

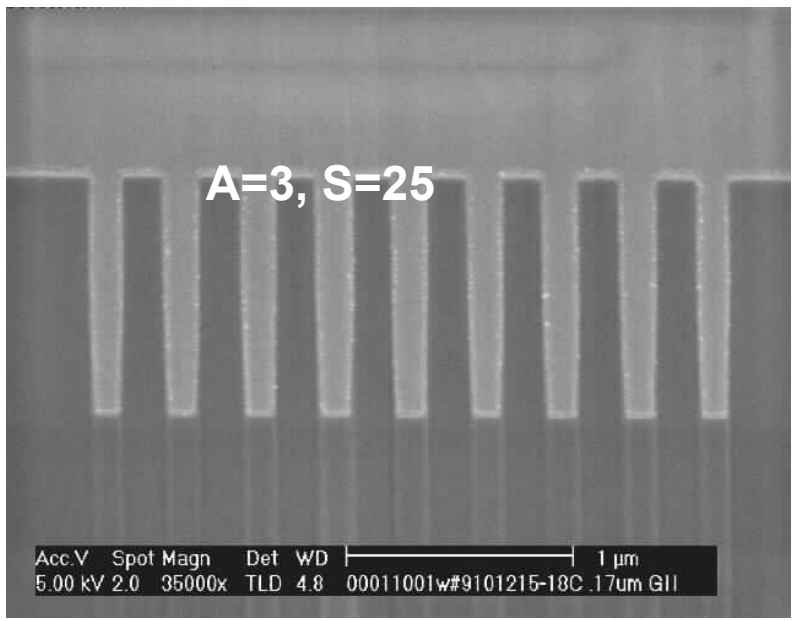
- Surface film properties
- Cross section
- Electrical Result

Additive Experiment (25 ?? @@)









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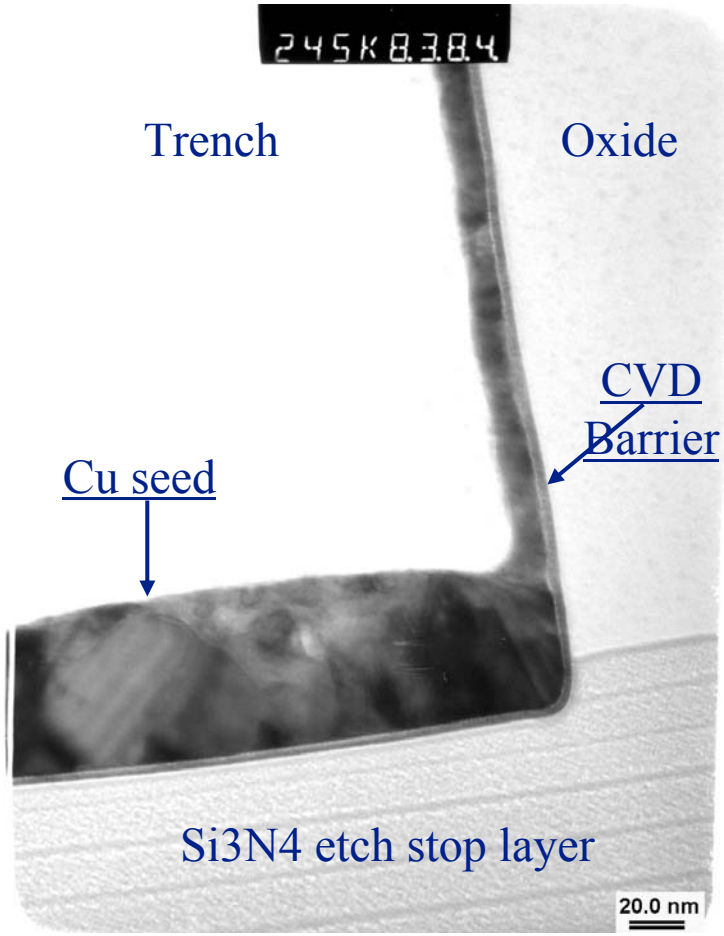
TEM IMAGE OF CVD CVD BARRIER
(100Å CVD Barrier + 1000Å 'Enhanced PVD' Cu seed)

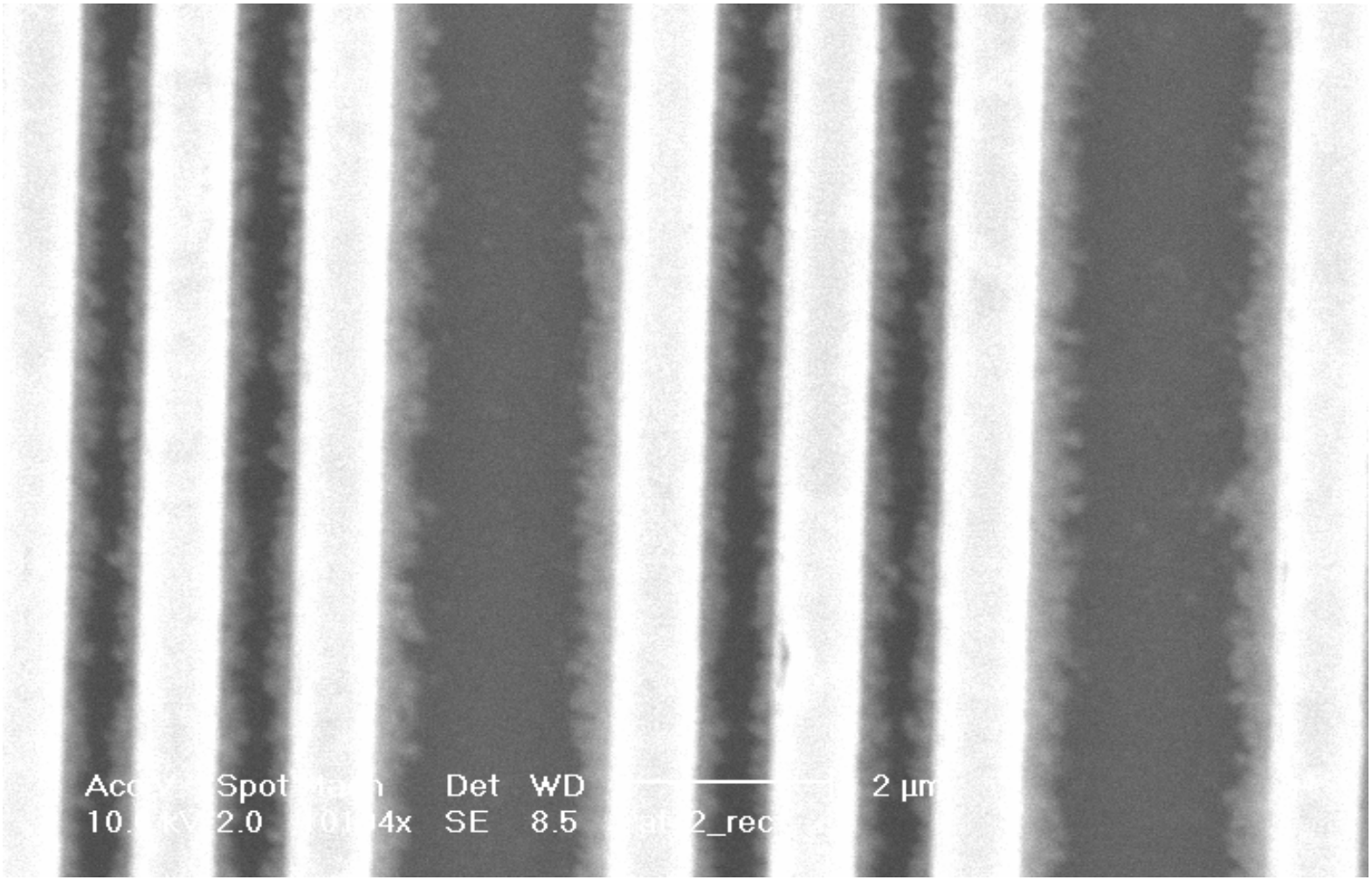


0.25µm AR ~ 3.0:1 Right edge

- Image shows good conformality of barrier (step coverage is ~69.4% on sidewall & 59.2% at bottom).
- Cu seed should be sufficient for plating (step coverage is ~ 11.0% on sidewall & 55.9% at bottom).
- Issues with sample prep at SEMATECH and Accurel.

CU DIFFUSION

Cu diffuses into Low K through sidewall



2003 METALIZATION METROLOGY CAPABILITY

Some Progress on Nondestructive Measurements For

- Film & Film Stack Thickness
- Subsurface Voids, Broken Vias
  - •Void Volume Still Too Large
- Grain Properties in Trenches

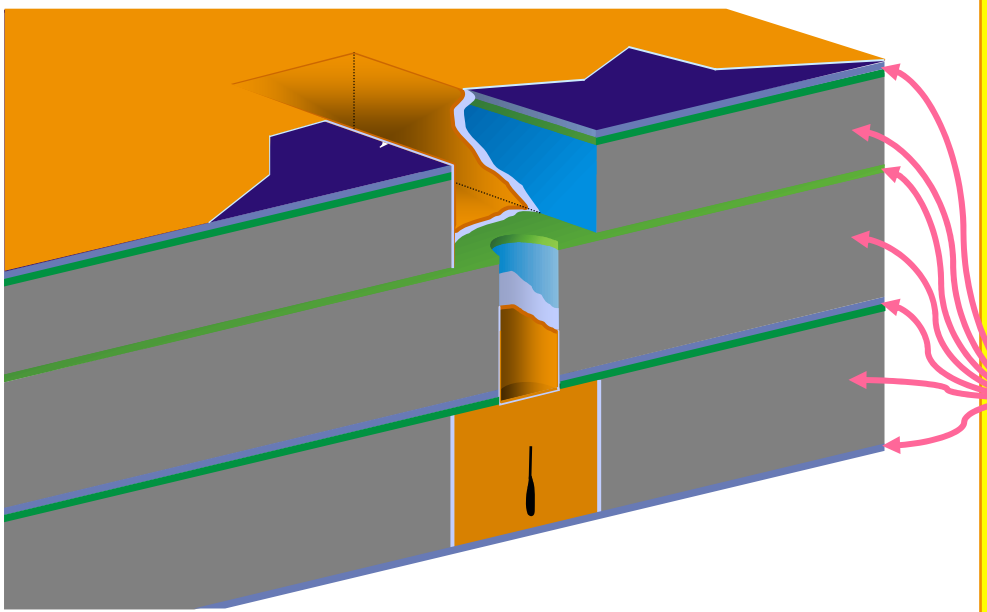
Little Progress in Other 'In Trench' Properties

- Barrier and/or Seed Properties
- Thickness
- Continuity/Density
- Texture/Orientation
- "Barrier-ness" Reliability

Have to TEM or Build a Complete Device and Life Test

Metrology Needs (2000)

Dielectric Deposition



Now Measure;
A Whole Host of Things:

- Dielectric Constant
- CTE
- Modulus
- Adhesion
- Fracture Toughness
- Thermal "Stability"
- Moisture Uptake
- Morphology
- Composition
- etc. etc.

and as a Function of Time

We Can Measure Some Things Pretty Well in Multiple Layers:

Planar Film:

- Thickness (Uniformity)
- Refractive Index

Don't Know How Many Will Be Carried into Production

2003 DIELECTRIC METROLOGY CAPABILITY

Porosity, Lots of Progress

- What Do the Porosity Measurements Mean
- The Search for the 'Killer Pore'

There Are ~10^{15} Pores/die (and Rising)

- iSMT Porosity Measurement Workshop

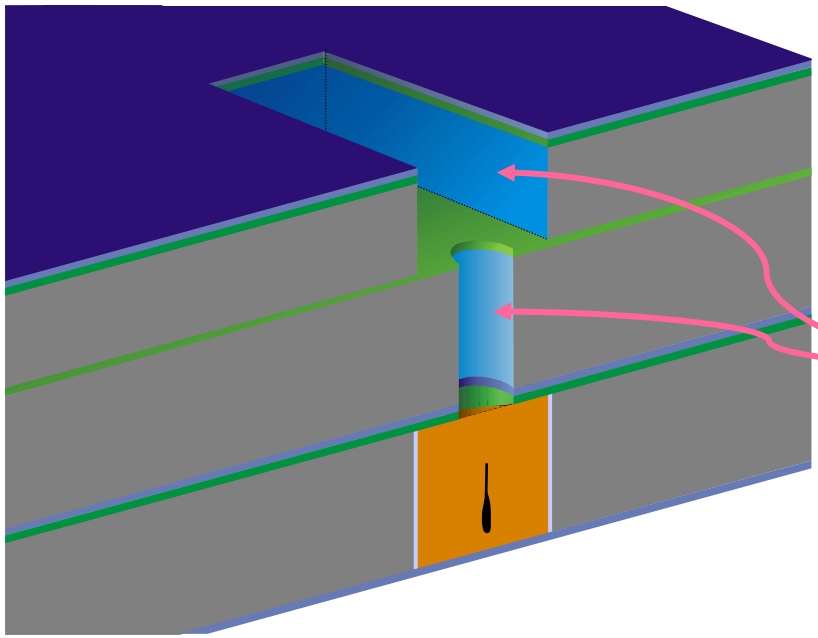
Adhesion

- A Generic Problem in Semiconductor Manufacturing
- More Problematic (now) For Dielectrics

Breaking Beams is Not a Manufacturing Solution

Metrology Needs (2000)

Etch & Strip



Want to Measure;
Thin Things on the Sidewalls and Bottoms of Deep Things

- Feature Size (in detail)
- Profile
- Residues
- Low-K 'Attack'
- Alignment
- "Depth"
- Faceting

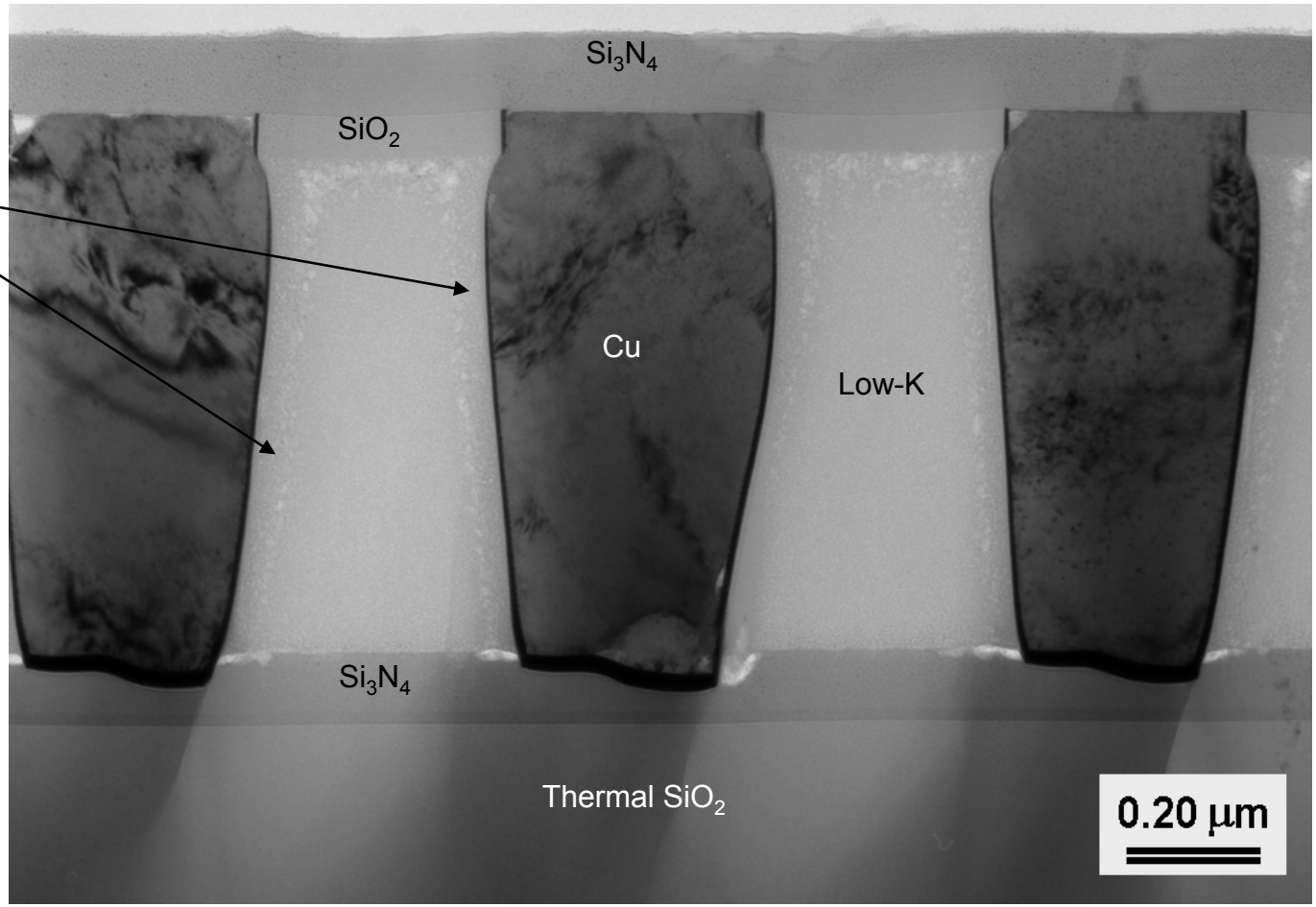
We now measure;

- Cross section
- Electrical Result

Etch Development is Paced by SEM/TEM Time

LOW-K DAMAGE

Note areas at sidewall with appearance of higher density (perhaps due to etch/ash damage).

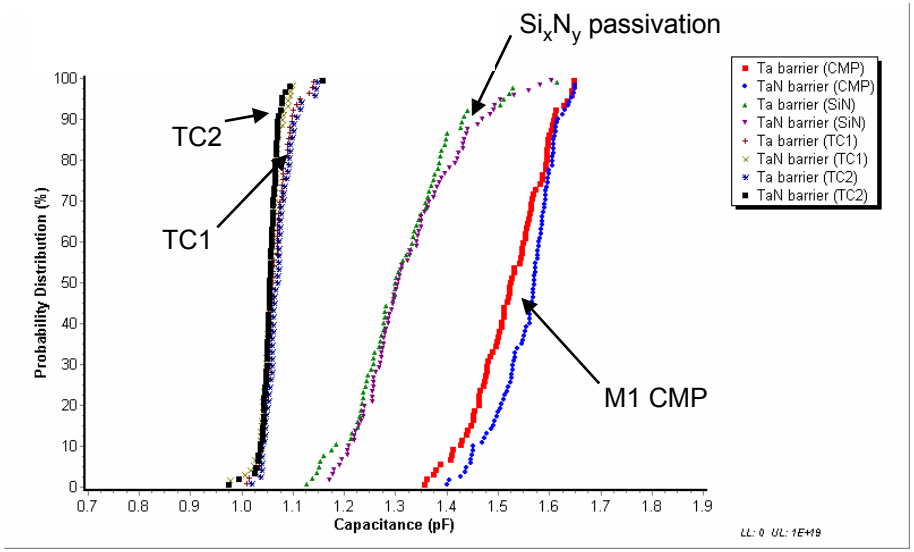


*Conventional Bright Field TEM image of completed M1 test vehicle incorporating Low-K **after TC1** (400°C, 1 hr.) anneal.*

Acknowledgement: B. Foran, D. Brazeau (SEMATECH)

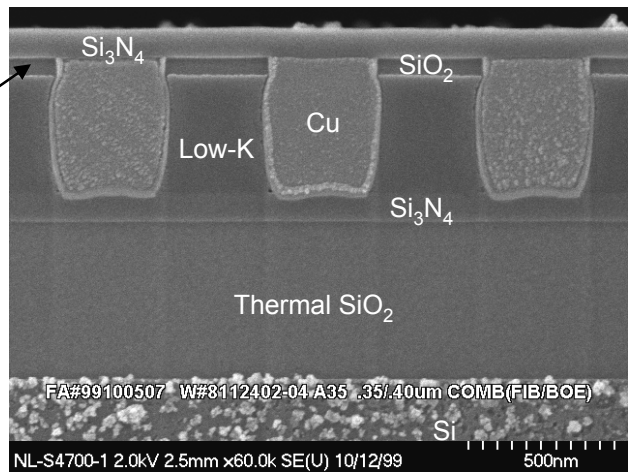
ANOTHER LOW-K wi DAMAGE

- **Electrical data**
  - Capacitance and leakage current decrease (shown in probability plots at right for 4 sequential electrical test steps) upon passivation and continued thermal cycling
  - Consistent with moisture desorption, at least through Si_xN_y passivation
  - Mechanism for capacitance decrease upon TC1, TC2 unknown

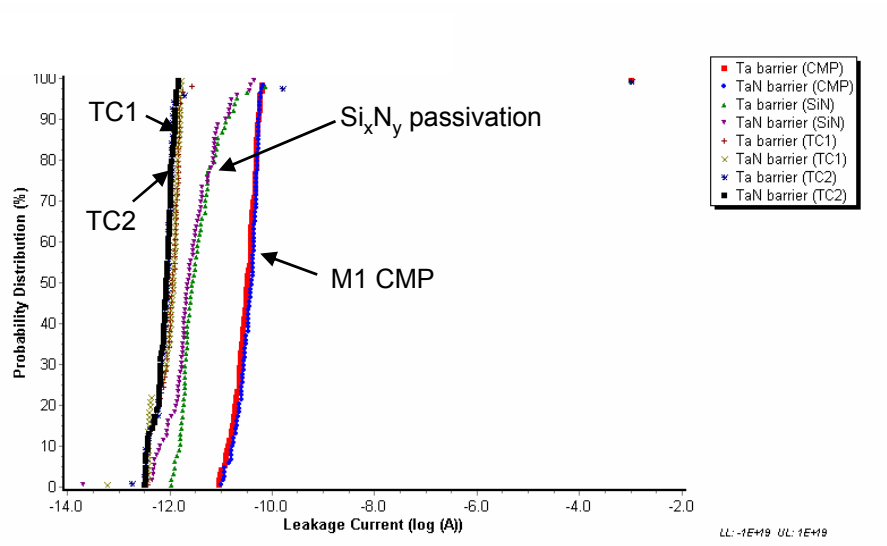


Capacitance probability plot for 4 sequential etest steps.

SiO_2 hard mask clearly present



*XSEM image (FIB/BOE) of completed 0.35μmL/0.40μmS COMB structure **after TC2.***



Leakage current probability plot for 4 sequential etest steps.

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2003 ETCH & STRIP METROLOGY CAPABILITY

Some Progress on Nondestructive Measurements For Profile

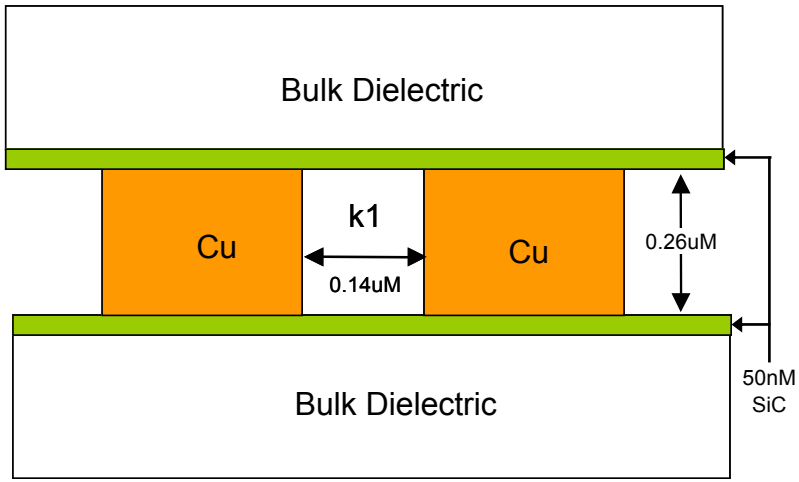
- **AFM, SEM**
- **But Seems Most Users are Still Using Cross-sections**

Little Progress on 'In Trench', Sidewall or Via Properties

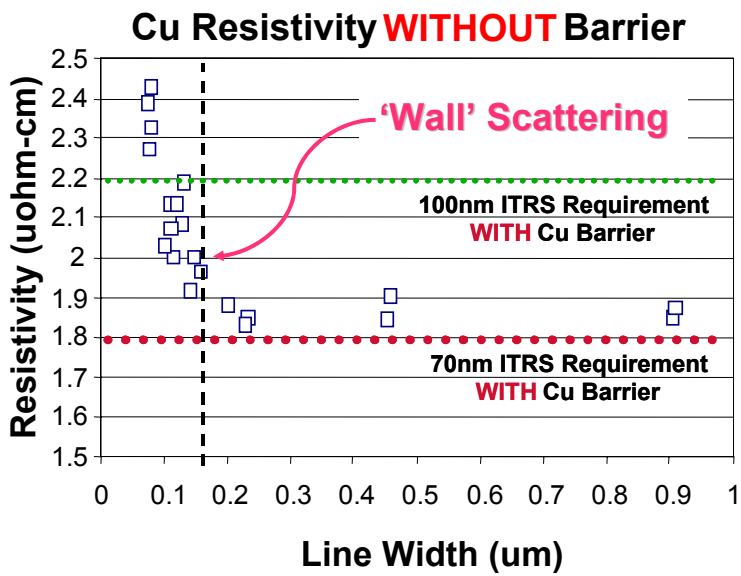
- **Polymer or 'Damage' Thickness**
- **Residues**
- **K-Value**
- **Texture**
- **Reliability**

Have to TEM or Build a Complete Device and Electrically Test

‘BEYOND Cu & LOW-K’



Properties of Metals Used in Electronic Applications		
	Resistivity @18-20C in Ohm-cm x 10-6	MP Celsius
Al, Pure	2.87	659
Al, 99.6%	2.83	660
Al, 97%; Cu 3%	>3.4	640
Au, Pure Drawn	2.44	1063
Cu, Pure	1.69 -1.77	1082
Ag, 99.98%	1.59 -1.63	960
W	5.6	3370



If bulk dielectric = 2.6 then k_{eff} = 2.94
If bulk dielectric = 2.2 then k_{eff} = 2.57
If bulk dielectric = 1.5 then k_{eff} = 1.96
If bulk dielectric = 1.0(Air) then k_{eff} = 1.5

CONVENTIONAL MATERIAL SOLUTIONS NOT AVAILABLE!

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Year of First Product Shipment Technology Generation	2003 100	2004 90	2005 80	2006 70	2007 65	2010 45	2013 32
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FITs/m legnth/cm^2 x 10^{-3} excluding global levels							
Local wiring pitch—DRAM (nm) non-contacted	200	180	160	150	130	90	64
Local wiring pitch—logic (nm)	245	210	185	170	150	105	75
Local wiring AR—logic (Cu)	1.6	1.7	1.7	1.7	1.7	1.8	1.9
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Intermediate wiring pitch—logic (nm)	320	275	240	215	195	135	95
Intrmdt wiring h/w AR-logic (Cu DD via/line)	1.7/1.5	1.7/1.5	1.7/1.5	1.7/1.6	1.8/1.6	1.8/1.6	1.9/1.7
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Contact aspect ratio-DRAM, stacked cap	9.3	11.4	13	13	14.1	16.1	23.1
Conductor effective resistivity (μΩ-cm) Cu *	2.2	2.2	2.2	2.2	2.2	2.2	2.2
Barrier/cladding thickness (nm)***	12	10	9	8	7	5	3.5
Interlevel metal insulator effective dielectric constant (k) logic	3.0-3.6	2.6-3.1	2.6-3.1	2.6-3.1	2.3-2.7	2.1	1.9
Interlevel metal insulator (minimum expected) -bulk dielectric constant (k)	<2.7	<2.4	<2.4	<2.4	<2.1	<1.9	<1.7

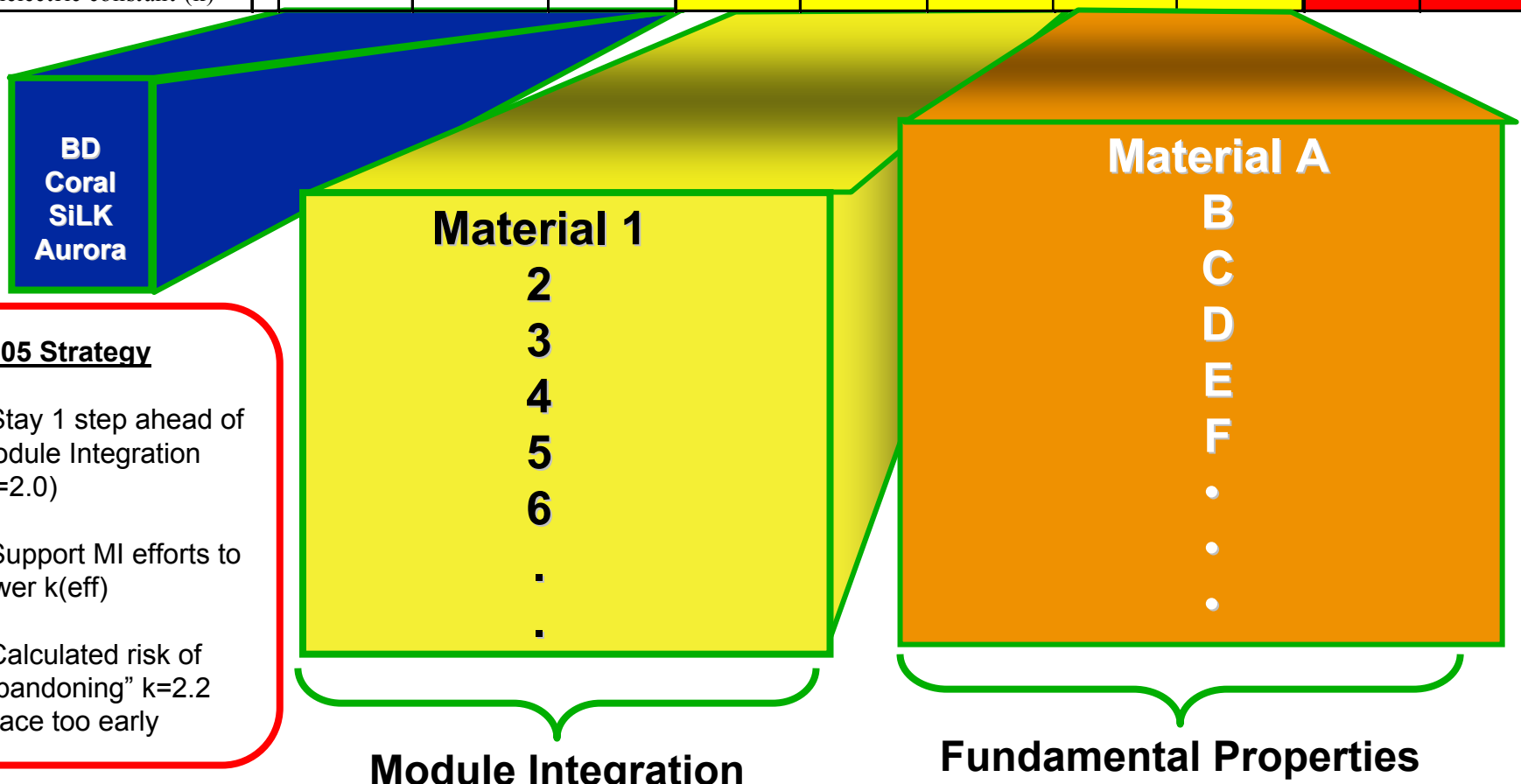
Process and Material Solutions Can't Meet Needs

* Assumes a conformal barrier/nucleation layer

*** Calculated for a conformal layer in local wiring to meet effective conductor resistivity

LOW K MATERIAL EVALUATION ACTIVITY

Year of Production	*2001*	*2002*	*2003*	*2004*	*2005*	*2006*	*2007*	*2010*	*2013*	*2016*
Interlevel metal insulator (minimum expected) —bulk dielectric constant (k)	<2.7	<2.7	<2.7	<2.4	<2.4	<2.4	<2.1	<1.9	<1.7	<1.6



J105 Strategy

- Stay 1 step ahead of Module Integration (k=2.0)
- Support MI efforts to lower k(eff)
- Calculated risk of "abandoning" k=2.2 space too early

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INTERCONNECT PROGRAM EVOLUTION

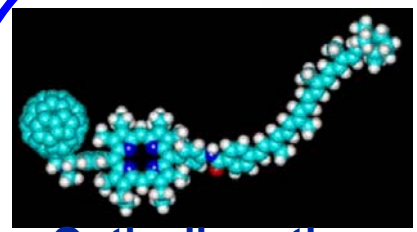
2003-2005 | 2005

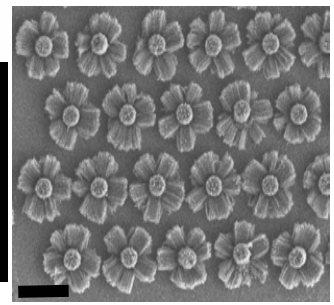
k ~ 2.3 | k ~ 1.9 | k ~ 1.0

Cu Low k & Reliability

Projects

Projects





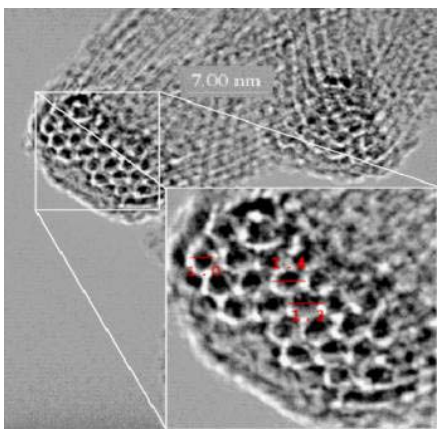
Optically active Molecules

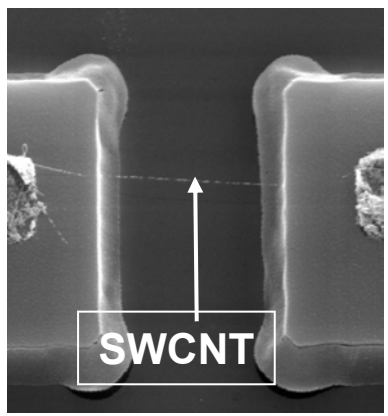
Nanotubes

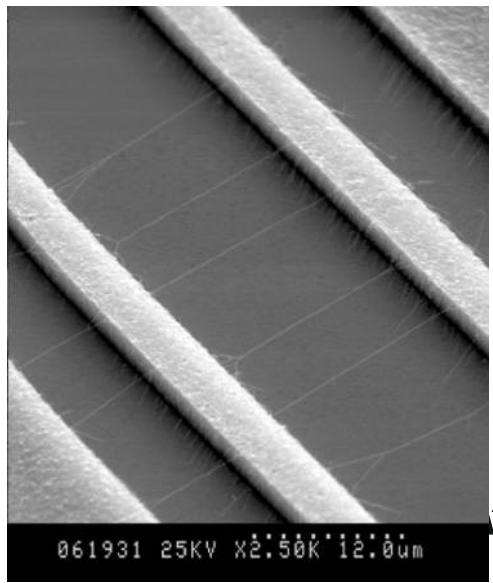
Future Connectivity

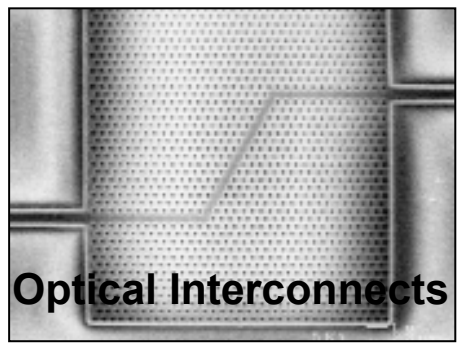
Determine;
Roadmap
Timelines
Critical Needs

Next Generation Interconnect

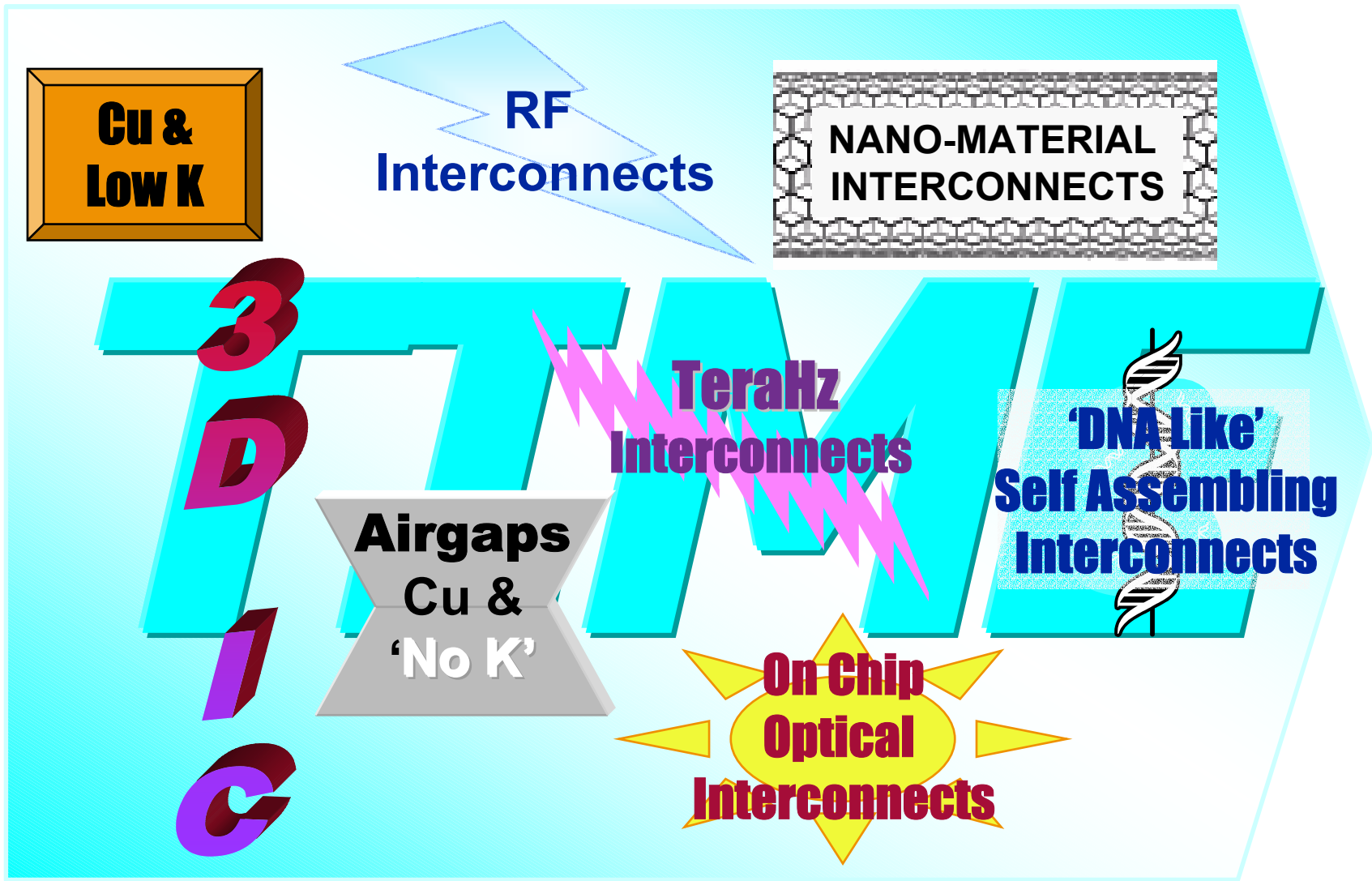








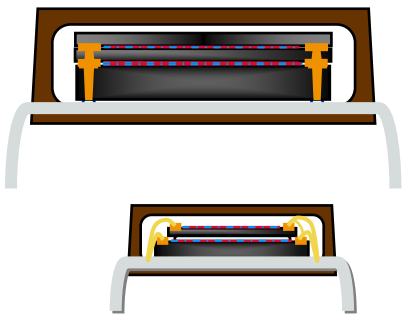
TECHNOLOGY 'AVAILABILITY' TIMELINE



3D IC APPROACHES

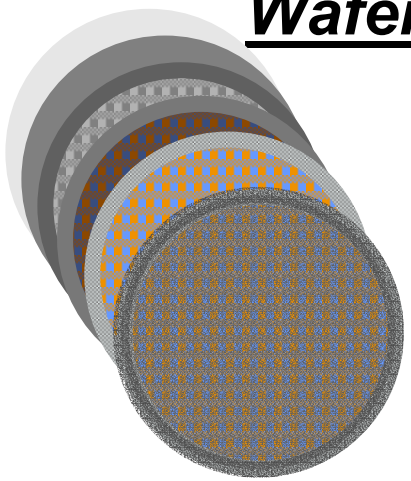
"Passive" Stacking

Chip



- Micro Spring
- Ball Bond
- Braze
- Wire Bond

Wafer



- Micro Spring
- Polymer Glue
- Oxide Bond
- Braze

"Active"

Monolithically build active devices in the Interconnects

3D IC CHALLENGES

Stacked Chip or Wafer

- $COST$
  - It's Hard to Beat
  - Monolithic Fabrication
- Known Good Die ***after separation***
- Through wafer vias
  - ¤ Etch
  - ¤ Fill
- Alignment
- Bonding Method
- Bonding Method
- Header Pitch
- Wafer Thinning
- Removal of Handle wafer
  -
  -
  -

Active

- $COST$
- Single Crystal Silicon on non Si Substrate
- All Low Temperature Transistor Fabrication Processes

3D IC BENEFITS

While 3D Is Viewed As a Problem for Interconnect, It Doesn't Do Much for the Interconnect Problem

Line Length Reduction~$\sqrt{N}$, the Number of Layers

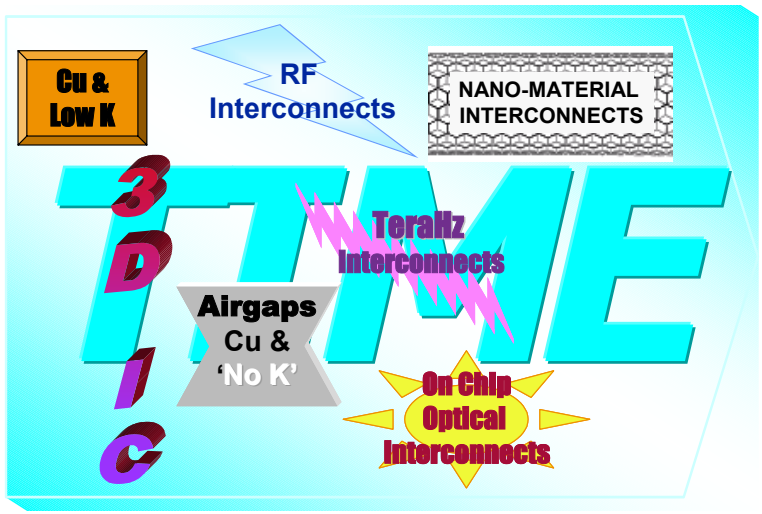
Payback Is in Other Areas

- **Mixed Process ICs**
  1. **RF, Bipolar, CMOS**
  2. **Si and Compound Semiconductor**
- **Shorter Time to Market**

CHOOSING BEYOND CU & LOW K SOLUTIONS

Not as ‘Universal as the Old Interconnect Systems

1. Everyone Used Al, SiO2, W, CMP
2. Eventually Everyone Will Use Cu & Low-K



Market Use of These Solutions Will Be More Tailored to End Product Needs

1. Smaller Markets for Suppliers
2. Smaller R&D ‘Pool’ for Development

QUESTIONS FOR A NEW TECHNOLOGY '10,000 METER'

- How does this work fit in the solution of the overall interconnect problem?
- How much of the problem does it solve? (for which products?)
- When is/will the technology be ready for implementation?
- How does the capability of this technology match needs at the projected time of implementation?
- How extendable, or for how many generations will it provide benefit?
- What other technologies will need to be developed to effectively implement the solution?
- What changes in software, hardware, manufacturing, applications, or business will need to be in place to effectively implement the solution?
- What technical problems need to be solved before implementation? and what is their current state?
- What needs to be done/added to provide the implementation on time?
- How is/will the technology transferred into the mainstream?
- Any estimates on cost?

NANOTECHNOLOGY EXAMPLE QUESTIONS ’1,000 METER’

- What defines something as a nano-technology? When does what I am doing already become nano-technology?
- What kind of resistivities are we talking about for nano-conductors?
- I have heard the I-V characteristics are quantized; true? If so how, and over what range of current (density?) or voltage?
- Most of what I hear about 'electrical' nano-technology centers around conductors or semiconductors; are there insulator opportunities as well?
- How closely could nano-conductors be spaced? Will fields in the adjacent lines affect the I-V characteristics? Are there any 'unusual' tunneling or coupling phenomena?
- In a similar vein, what about inductance? or the impact of magnetic fields?
- How do we 'scale' these things?
- Will cooling be required? How do the interconnect-relevant properties vary with temperature?
- How do the interconnect-relevant properties vary with strain?
- What would be (in general, if known) the types of reliability failure mechanisms we should be thinking about?
- What is the state of the art today? Can we fabricate with any degree of control?

SUMMARY

The Transition to Cu and Low-k is Underway

- Still Many Core Technology Challenges
- Still Many Metrology Challenges

Many Talks and Posters on These Challenges Today

- Compared to 2000 Much More Industry Focus

The Challenge of 'Measuring on the Sidewall' Still Largely Un-addressed

Cu and Low-K (Wires) Alone Will Not Sustain Moore's Law Beyond ~ 5 Generations

- If You Thought Cu and Low-K Was Tough…...