SIA SEMICONDUCTOR INDUSTRY ASSOCIATION

SEMICONDUCTOR SUPPLIERS

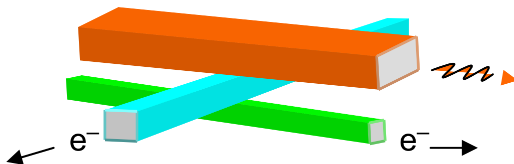
The Interconnect Era

of

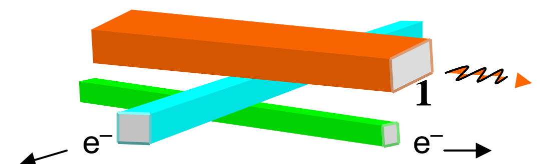
Gigascale Integration

International Conference on Characterization and Metrology for ULSI Technology

Dallas, Texas **March 16, 2005**



Interconnect Focus Center



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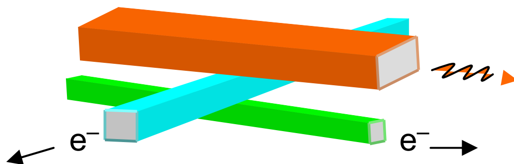
ITRS Objectives

Calendar Year	2012	2018
Interconnect One Half Pitch	35 nm	18 nm
MOSFET Physical Gate Length	14 nm	7 nm
Hi Perf. MPU Transistors/Chip	3.5 billion	14 billion
DRAM Bits/Chip (at introduction)	32 Gb	128 Gb
Number of Interconnect Levels	12-16	14-18
On-Chip Local Clock	20 GHz	53 GHz
Chip-to-Board Clock	15 GHz	56 GHz
# of Hi Perf. ASIC Signal I/O Pads	2500	3100
# of Hi Perf. ASIC Power/Ground Pads	2500	3100
Supply Voltage	0.7-0.9 Volts	0.5-0.7 Volts
Supply Current	283-220 Amperes	396-283 Amperes
Hi Perf. Chip Power Dissipation	(240)198 Watts	(300)198 Watts

[2003 ITRS, 2004 ITRS]



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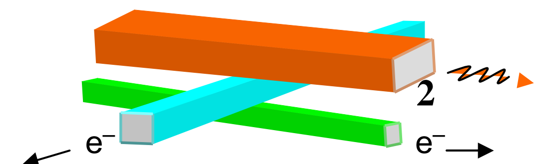

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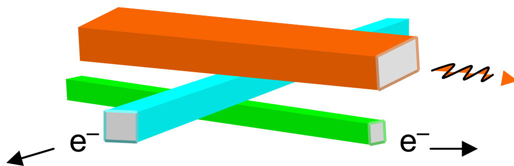
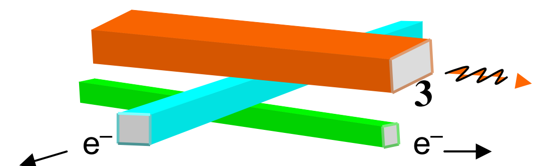
Interconnects are projected to become the principal determinants of the ***latency, energy consumption and cost*** of gigascale silicon chips.





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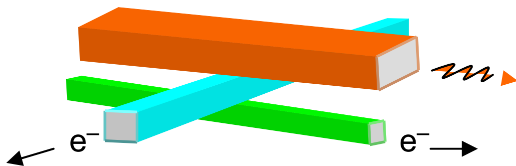
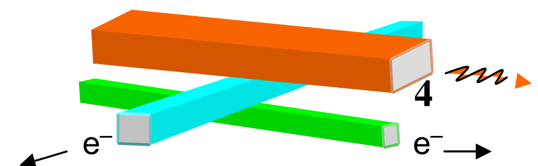
INTERCONNECT FOCUS CENTER

International Conference on Characterization and Metrology for ULSI Technology
Dallas, Texas March 16, 2005



Interconnect Focus Center

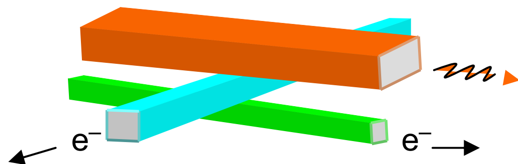


SEMICONDUCTOR SUPPLIERS

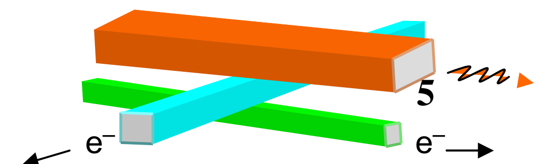
Faculty PI and Student Participation in IFC- Participation by Site

	PI's	Students
Stanford	**10**	**18**
MIT	**13**	**31**
SUNYA	**9**	**20**
Rennselaer	**9**	**31**
Georgia Institute of Technology**	**7**	**19**
Cornell	*1*	*3*
UC Santa Barbara	*1*	*2*
UT Austin	*1*	*1*
UCF	*2*	*2*
Carnegie Mellon	*1*	*2*
NCSU	*3*	*2*
UC Berkeley	*3*	*2*
Total Participation	**60**	**133**

**Lead University



Interconnect Focus Center



SEMICONDUCTOR SUPPLIERS

Interconnect Focus Center

Leadership Council

Prof. Alain Kaloyeros	SUNY at Albany
Prof. James Meindl*	Georgia Tech
Prof. Pulickel Ajayan	RPI
Prof. Anantha Chandrakasan	MIT
Prof. David A. B. Miller	Stanford

* Chairman

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SEMICONDUCTOR SUPPLIERS

Interconnect Focus Center		
Program Matrix		
	Driver 1 **High Performance Network Chips** ***Krishna Saraswat, Stanford***	**Driver 2** **Low-Energy Mixed-Signal Wireless Node** ***Anantha Chandrakasan, MIT***
Task 1 **Electrical Interconnects** ***Alain Kaloyeros, SUNYA***		
Task 2 **Optical Interconnects** ***David Miller,Stanford***		
Task 3 **Thermal Management &** **Power Delivery** ***Paul Kohl, Gerogia Tech***		
Task 4 **Circuit & System Design &** **Modeling** ***Duane Boning, MIT***		

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SEMICONDUCTOR SUPPLIERS

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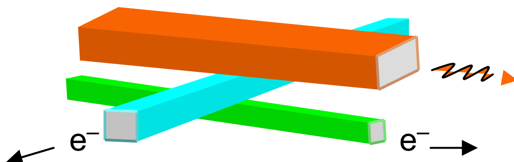

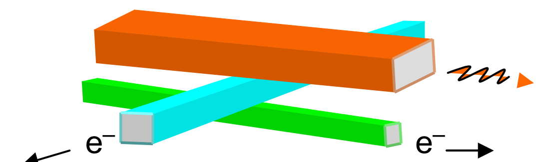

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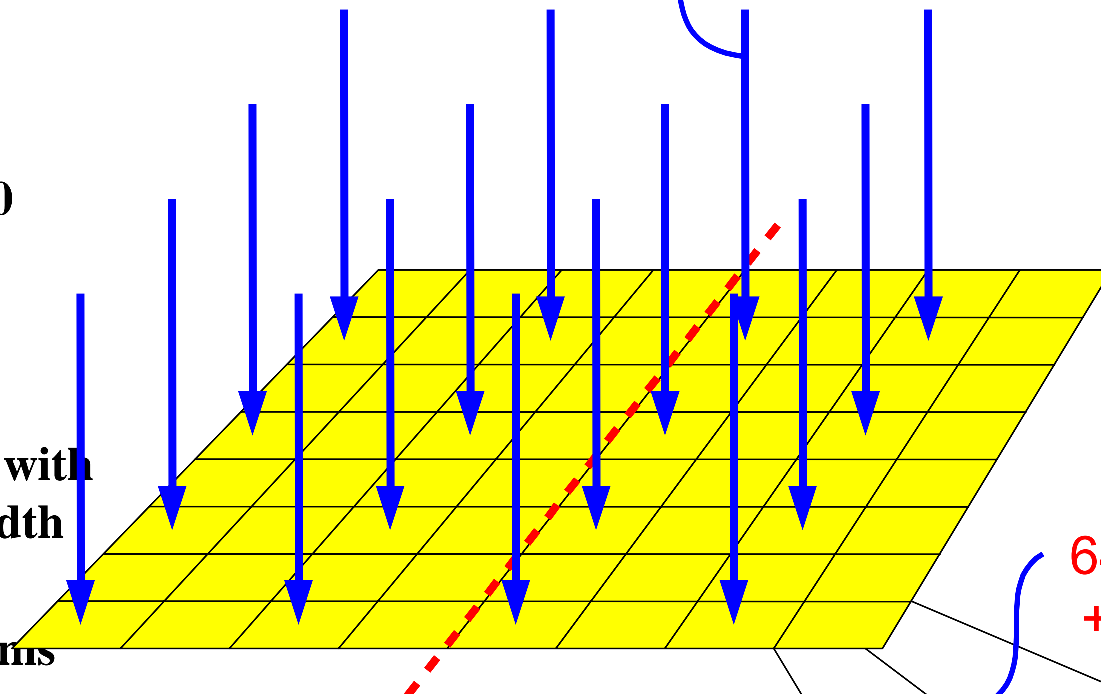
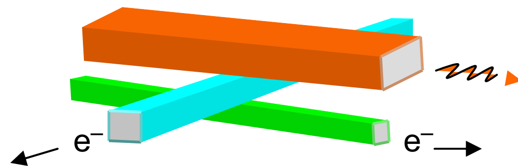
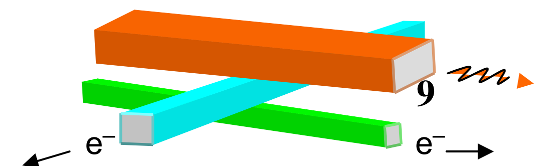
A High Performance(40Tb/s) Computing/Communication Chip

- **Enables**
  - **Scalable routers and switches**
    - **40Tb/s single-chip router**
    - **Petabit router ~ 100 chips**
  - **Supercomputers**
    - **640GFLOPS/chip**
    - **PFLOPS machines with high global bandwidth with 2K chips**
- **Prevents high-capacity systems from being limited by interconnect**



(Courtesy Prof. M. Horowitz)





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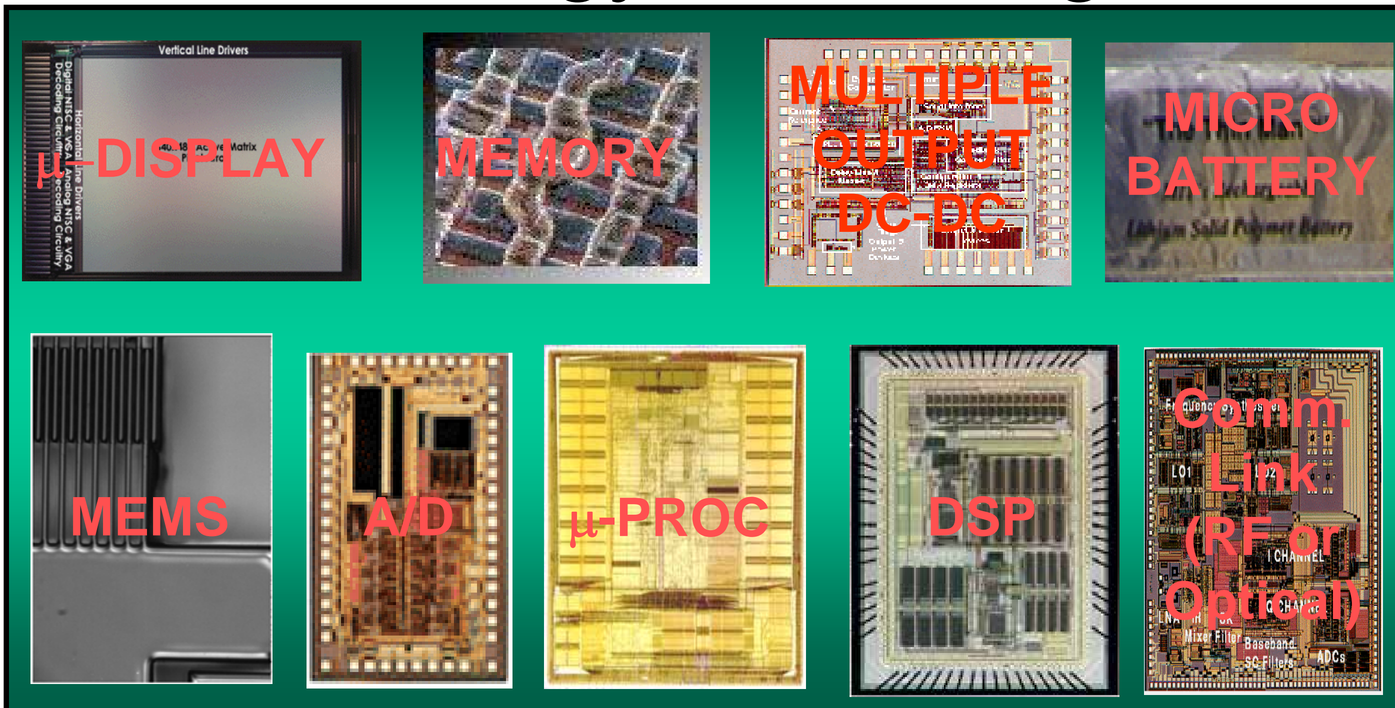
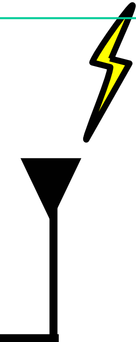
Low-Energy Mixed-Signal Wireless Node

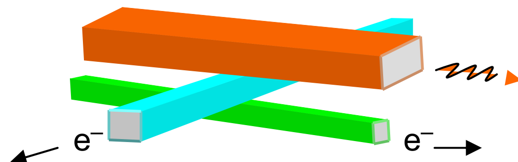


IFC, GSRC & C&SSC Collaboration

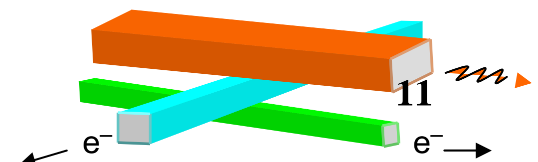


Key Requirements: **Integration of**

- **Diverse process technologies for *mixed signal* digital, analog, RF and MEMS chips**
- **Compact 3D form factor**
- **High performance, energy efficient computation and communication** (Courtesy Prof. R. Reif)



Interconnect Focus Center



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Interconnects Supersede Transistors : Latency

Technology Generation	MOSFET Switching Delay, t_d=CV/I	"RC"Response Time, L_{int}=1mm
1.0 µm (Al, SiO2)	~ 20 ps	~ 1 ps
100 nm (Cu, κ=2.0)	~ 5 ps	~ 30 ps
35 nm (Cu, κ=2.0)	**~ 2.5 ps**	**~ 250 ps** (best case)

"Size Effects": Surface/Roughness & Grain Boundary Scattering of Electrons in Metal Interconnects

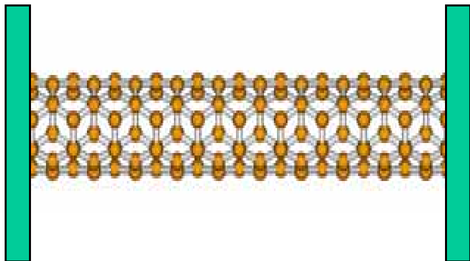
Physics predicts no known methodology to eliminate quantum mechanical scattering at boundaries in ultra-narrow conductors

Potential Solution: Interconnect Nanotechnology

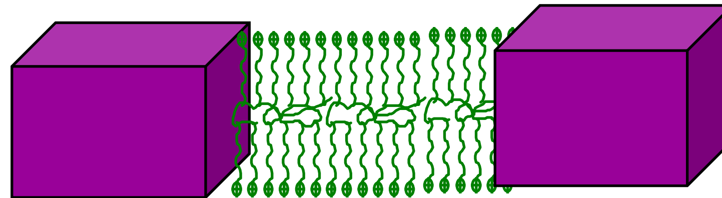
Exploit novel nanoscale electronic transport phenomena, such as:

- Ballistic electron transport in nanotubes, carbon chains, and molecules.
- Conduction occurs via quantum channels.
- Potential for ballistic transport at localization lengths ≥ 10 μm.

Carbon Nanotubes



Molecular Wires



Spintronics

(Courtesy of Prof. A. Kaloyeros)

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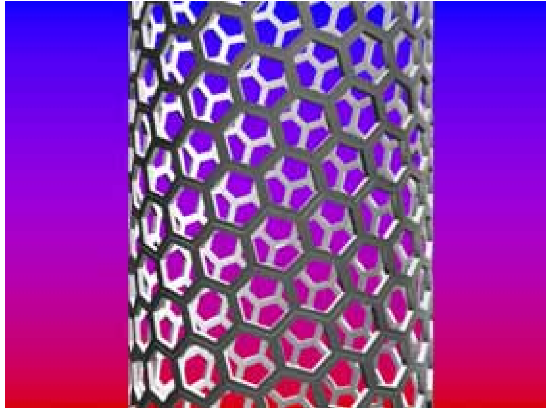
Designing Carbon Nanotubes for Interconnect Applications

New Paradigm for Future Interconnect Technology

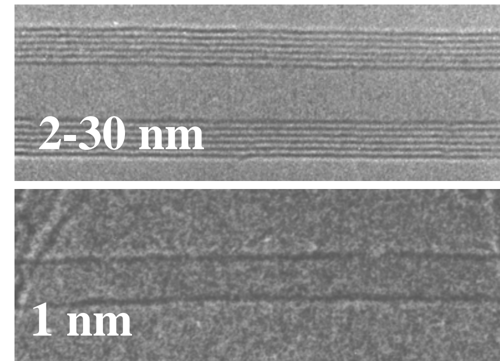


3-D Architectures, Growth, Integration
Tailoring Nanotube Structure, Properties
Creating and Characterizing Junctions, Networks

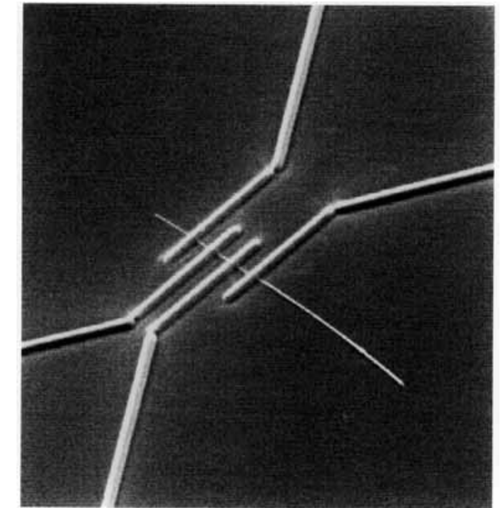
Why Carbon Nanotubes ?

- Low Resistivity
- Small Dimensions
- Mechanically Robust
- High Current Densities
- No Electromigration
- High Thermal Conductivity

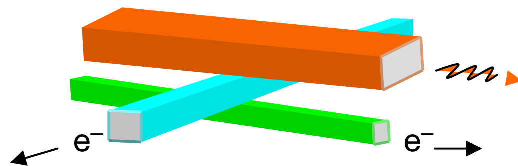
(Courtesy Prof. P. Ajayan)



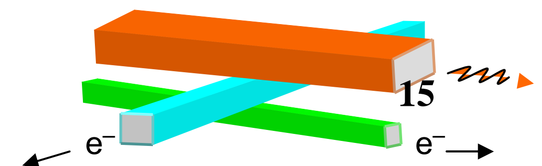
Near Perfect Nanotubes
Multiwalled and Singlewalled



Nanotube-Contacts



Interconnect Focus Center



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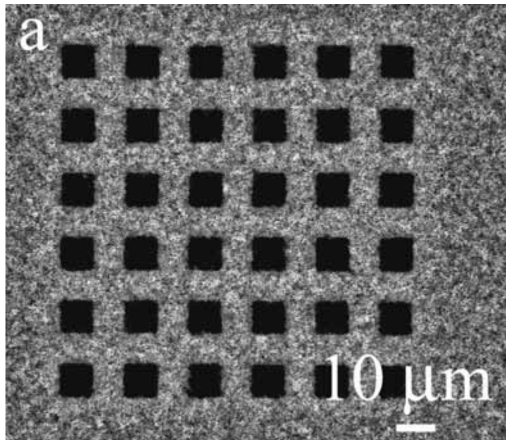
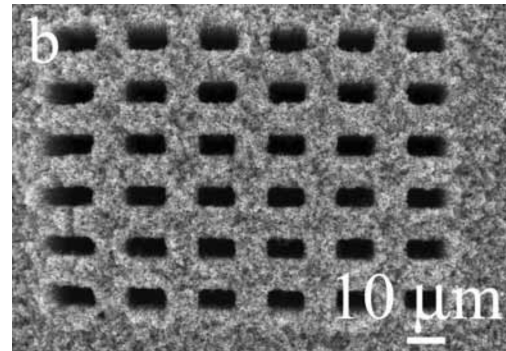
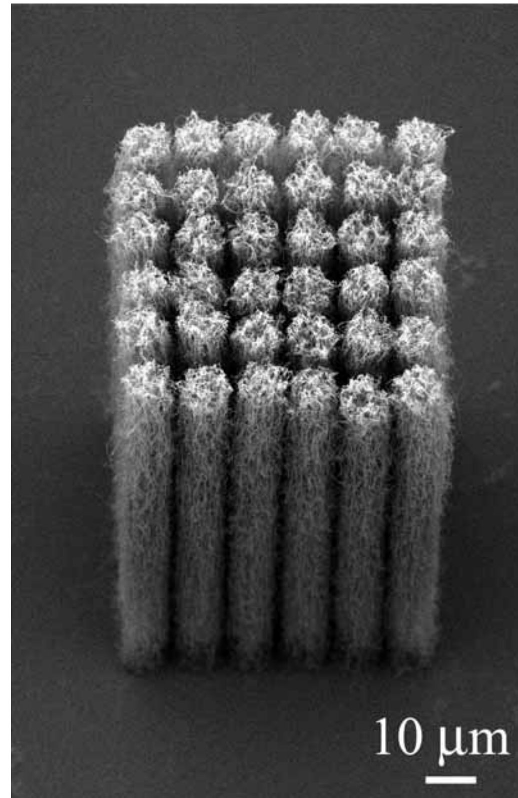
Controlled Assembly of Carbon Nanotube Architectures for Interconnects

MSDC & IFC Collaboration

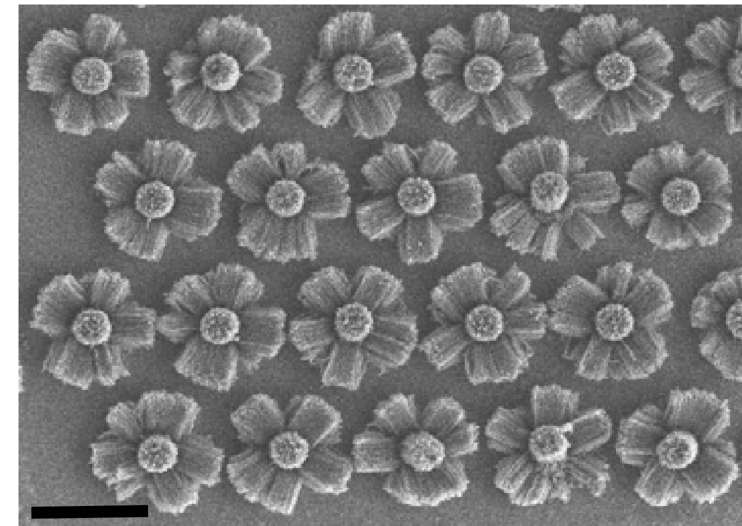
Directed Assembly Based on Substrate Selection







Vertical and Horizontal

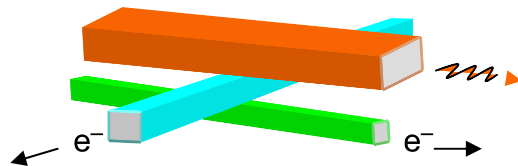


50 μm

SiO_2 layer on Si Substrate

Control: Location, Density, Orientation, Dimensions

(Courtesy Prof. P. Ajayan)



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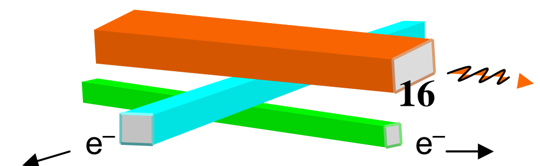

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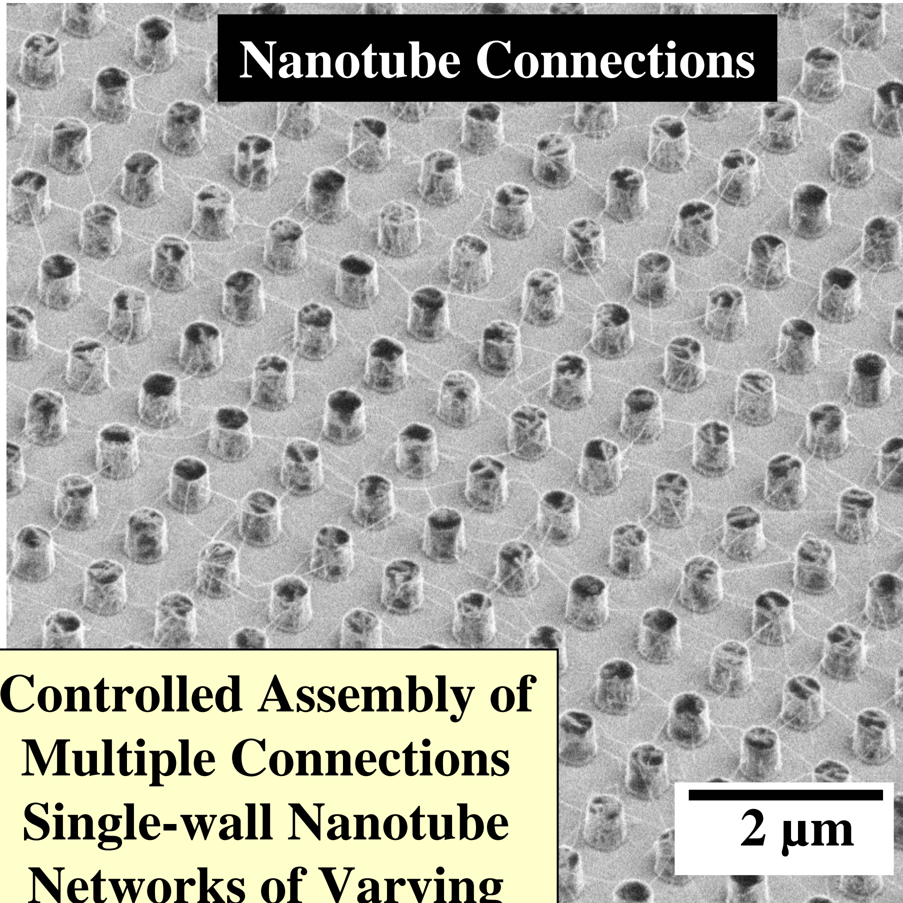
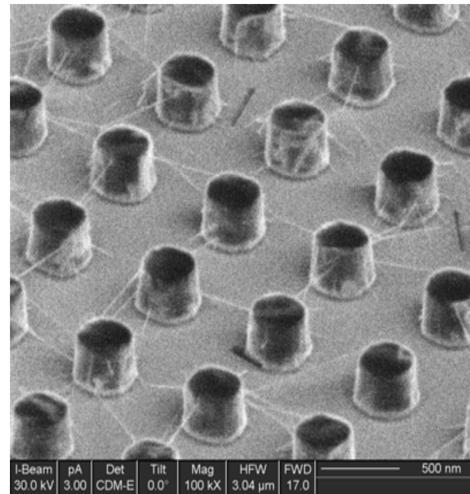
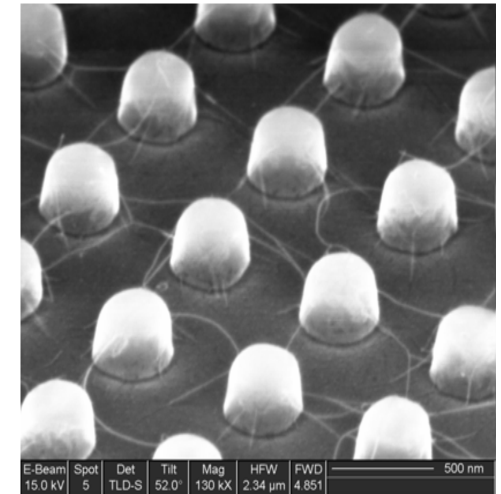
Demonstration of 2-D Carbon Nanotube Wiring Network



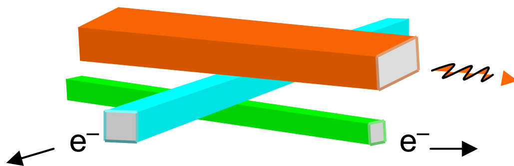




Controlled Assembly of Multiple Connections Single-wall Nanotube Networks of Varying Density/Pitch

(Courtesy Prof. P. Ajayan)

500nm



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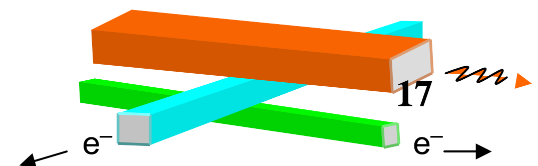
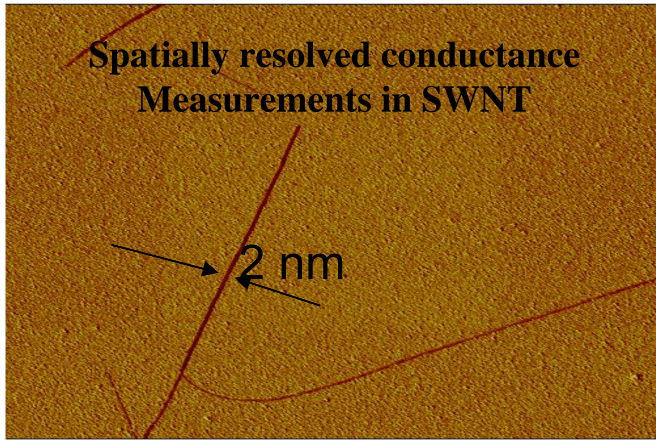
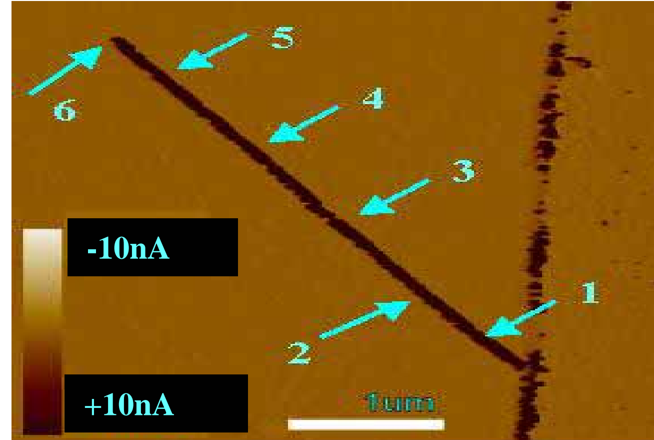
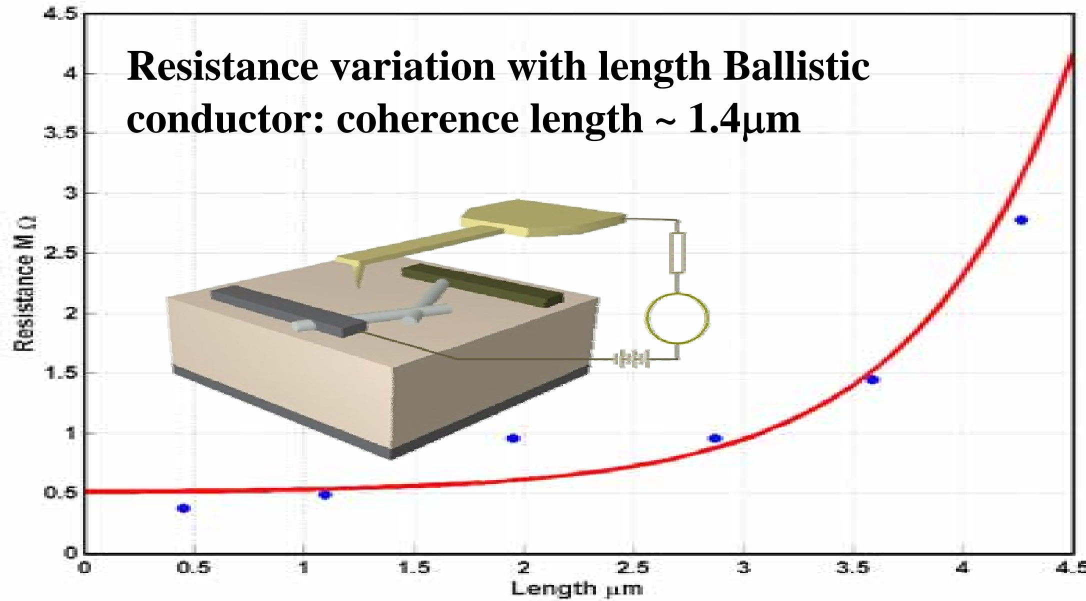


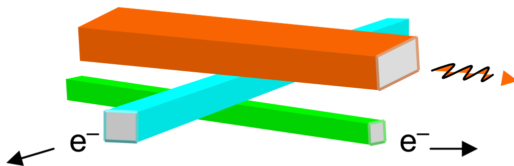
Carbon Nanotube Interconnects





(Ajayan, RPI)





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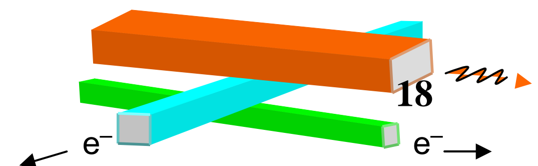

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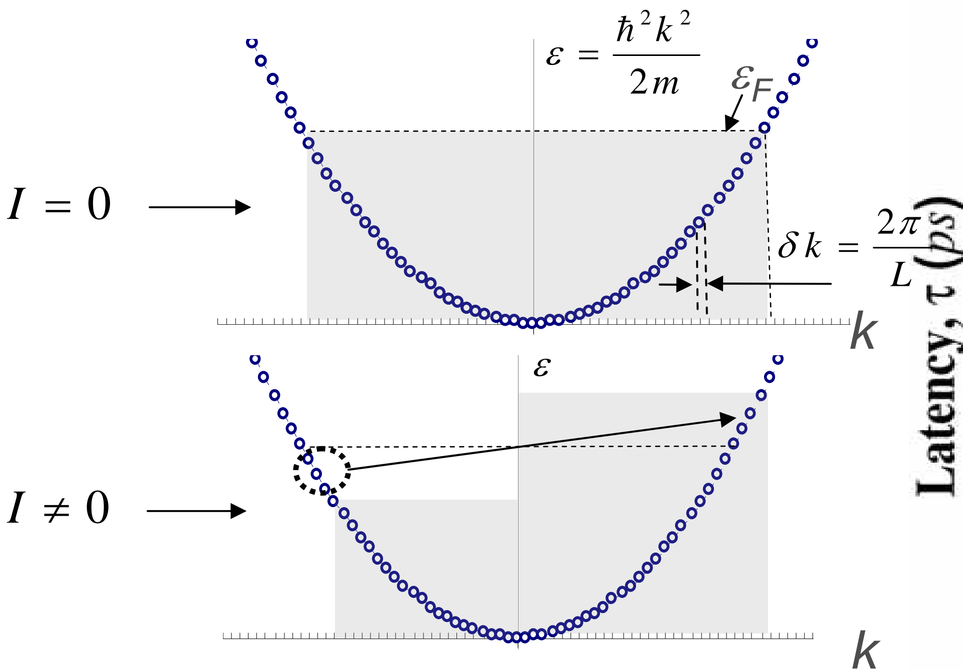
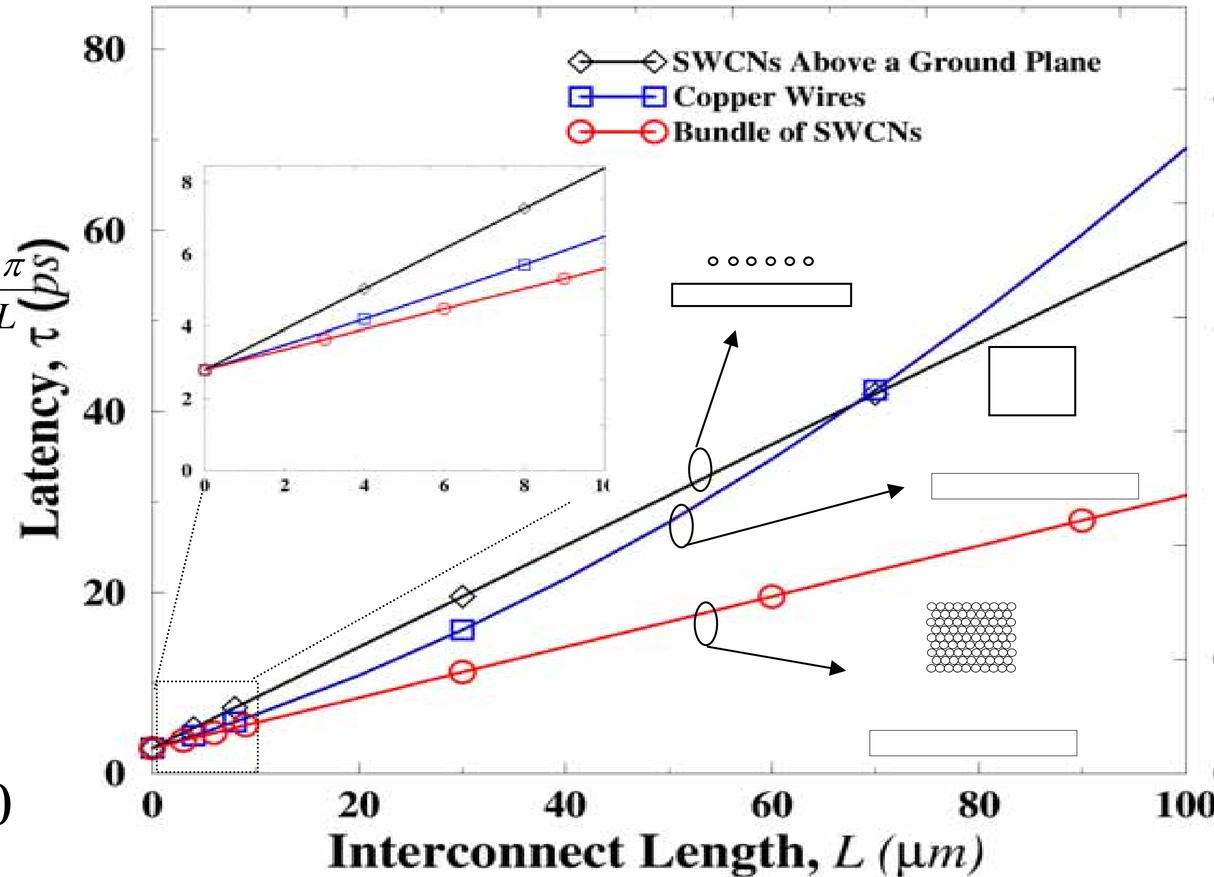
Ideal Carbon Nanotubes versus Copper Wires in 2016 (22nm Node)

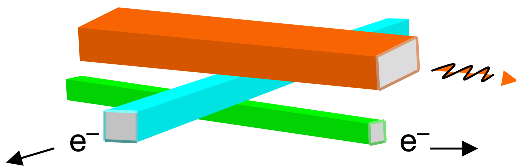




In a single CNT: $v = \sqrt{\frac{1}{lc}} < c_0/100$

Bundles of carbon nanotubes should be used for interconnect applications to avoid very slow signal propagation.

(Naeemi, Meindl – GIT)



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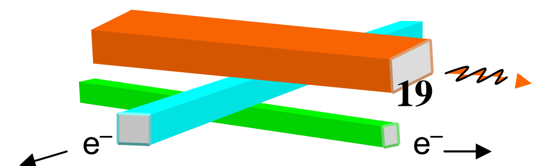

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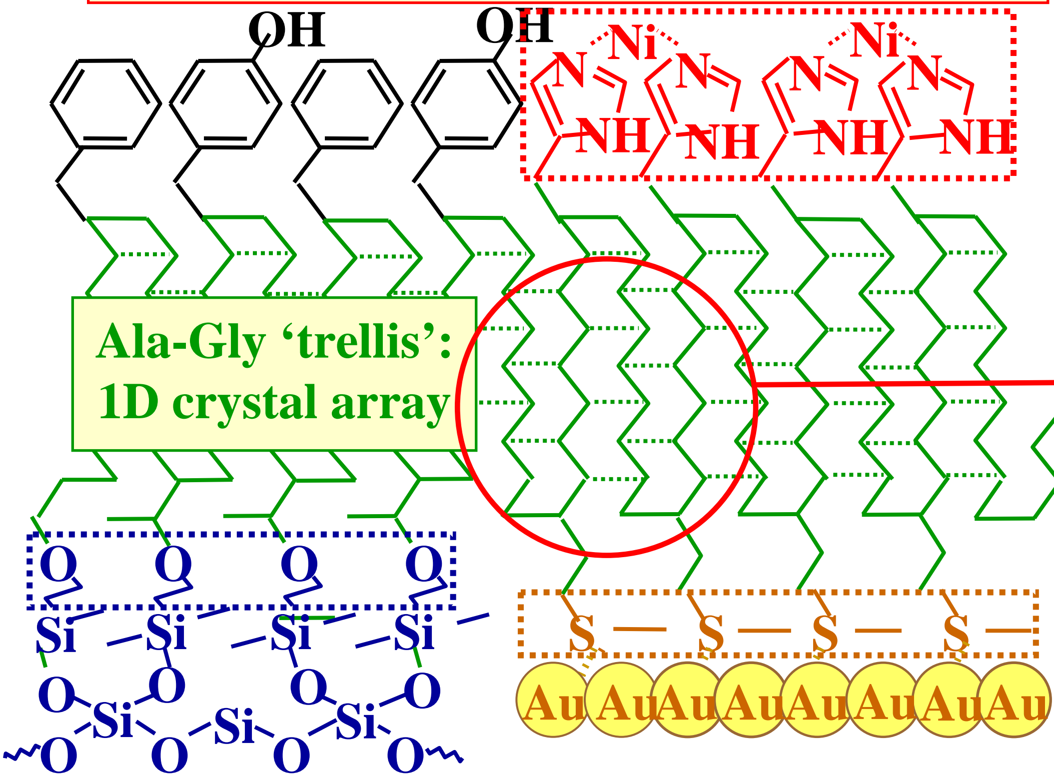
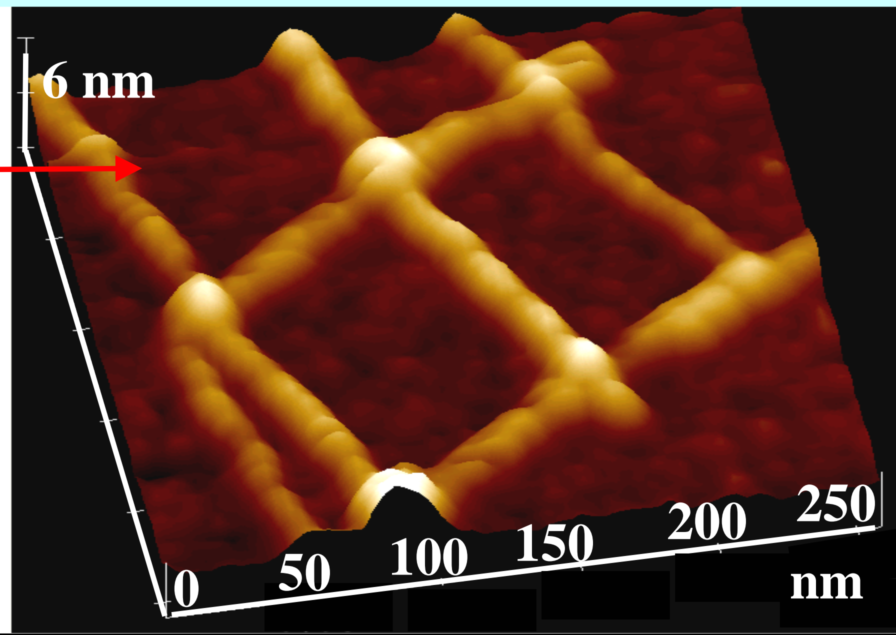
Demonstration of CMOS Compatible Polypeptide Molecular Wire

Self-assembly of functional molecular building blocks using bottom-up science + directed assembly on patterned surfaces using top-down nanotechnology

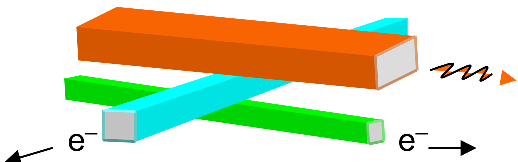


Alkylsilane linkage for SiO_2 attachment

Alkylthiol linkages for metal attachment



Successful Directed Self-Assembly of Molecular Polypeptide Backbone



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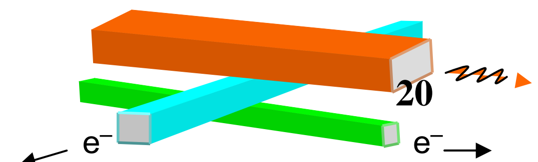

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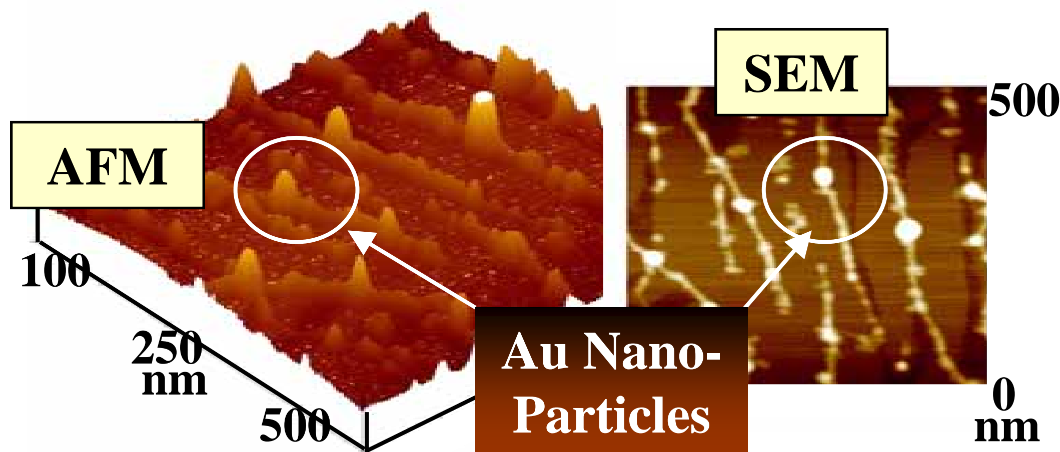
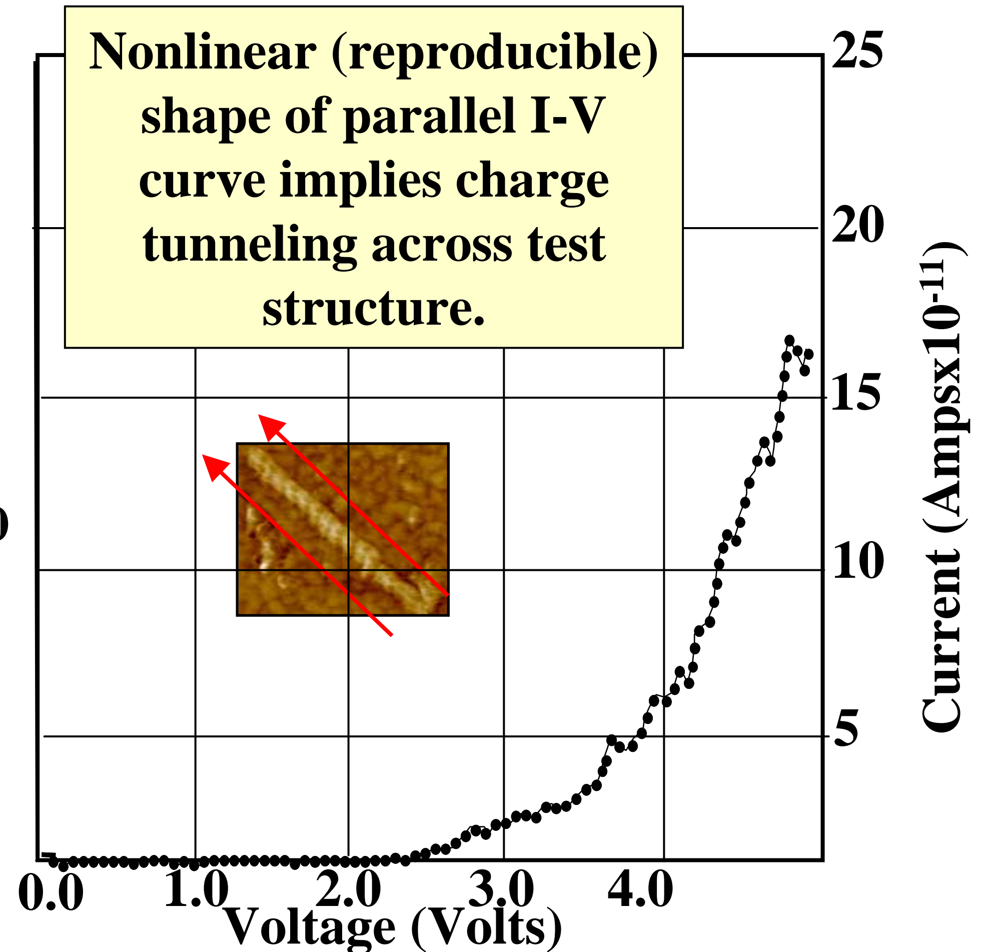
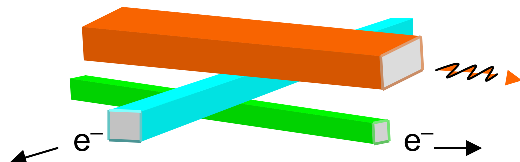
Controlled Self-Assembly of Metal Nanoparticle/Polypeptide Interconnects

- -Metal nanoparticle self-assembly demonstrated on polypeptide backbones.
- -Combines genetic engineering of polypeptide backbone with conductivity of metal nanoparticles.
- -Employs spin-on techniques consistent with CMOS fabrication flows.

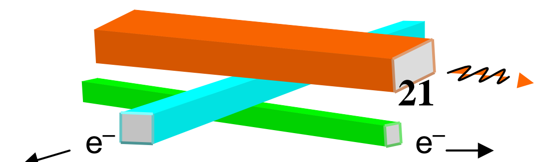




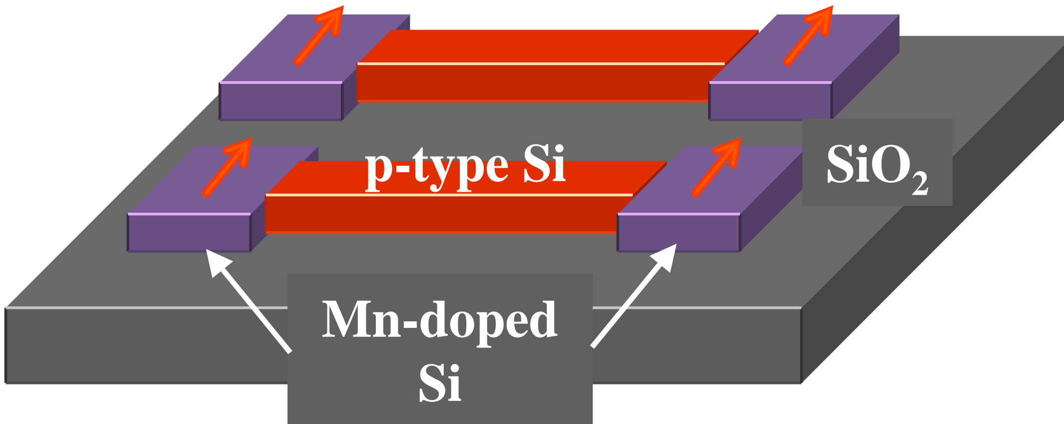
(Kaloyeros, Geer, Welch, Eisenbraun, UAlbany)



Interconnect Focus Center



Spintronics: Signal transmission via electron spin packets

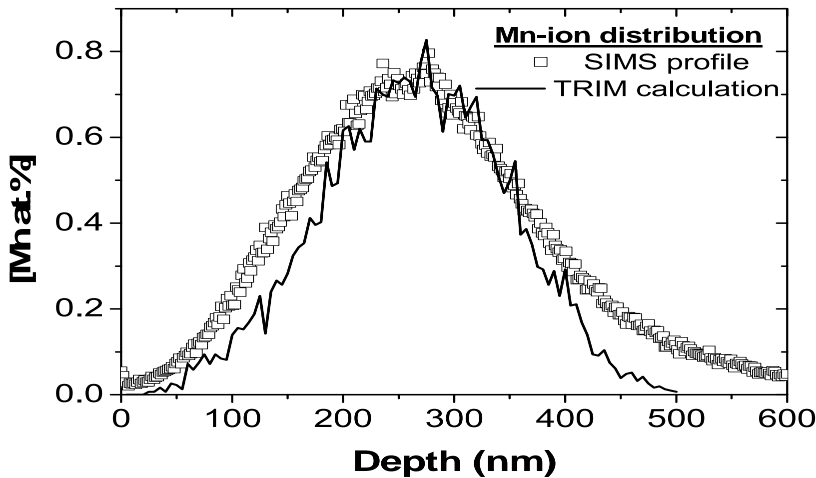


Advantages:

- All CMOS compatible → Si.
- Single crystal → no grain boundaries.
- Potentially as fast as metals without scaling issues.

Potential Challenges:

- Temperature?
- Interface Issues?
- Scattering Issues?
- What speeds can be achieved?
- What lengths can be achieved?



Mn-ion implanted p-type (~10^{19}/cm^3) Si crystal
300-keV Mn^{2+}, 350 °C
Doses: (1, 3, 6, 10) x 10^{15} ions/cm^2
Annealing at 800°C for 5 min under N_2 ambient

(Courtesy of Prof. V. LaBella)

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SEMICONDUCTOR SUPPLIERS

Interconnect Focus Center

Program Matrix

	Driver 1 High Performance Network Chip *Krishna Saraswat*	Driver 2 Low-Energy Mixed Signal Wireless Node *Anantha Chandrakasan*
Task 1 Electrical Interconnects *Alain Kaloyeros*		
Task 2 Optical Interconnects *David Miller*		
Task 3 Thermal Management & Power Delivery *Paul Kohl*		
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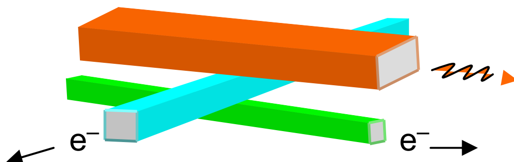
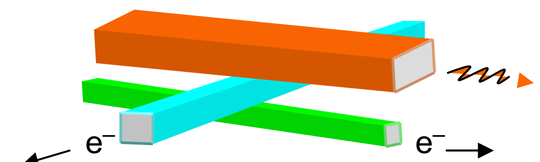


Interconnect Focus Center



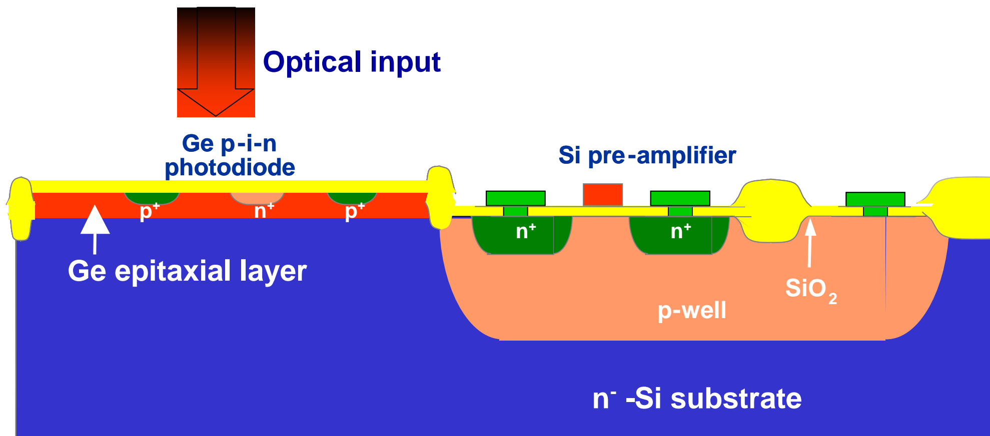
Critical Objectives

- **Ultra-high bandwidth, high speed, high density chip-to-chip and (subsequently on-chip) optical interconnects**
- **Interfacing gigascale Si chips(GSI) with optical network-like interconnects to enable "fiber-to-the-chip"**
- **Optical clock injection for GSI**
- **Implementation of the preceding advances with low voltage, low power, low cost optoelectronics**

SEMICONDUCTOR SUPPLIERS

Integrated Optical Receivers: Ge

CMOS Electronics and Ge PIN Photodiode



Successful fabrication of Ge PIN photodiodes on Si substrate

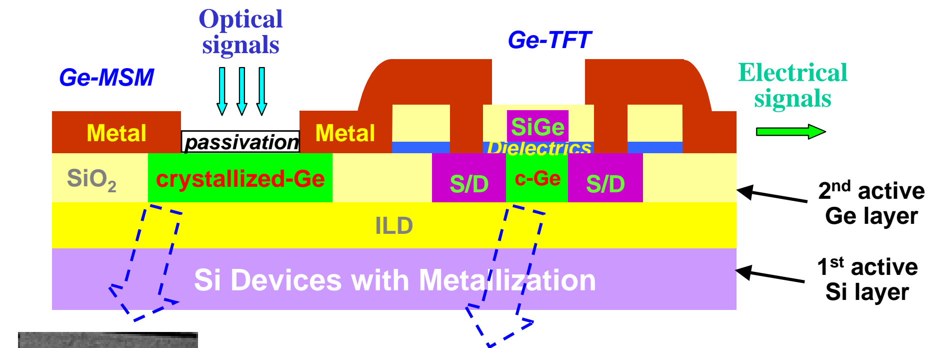
- Dark current: I_d = 1 mA @10V; diameter = 24mm
- Responsivity: 0.57A/W @2V and l = 1.3 mm
- Bandwidth: 8 GHz @ 10V

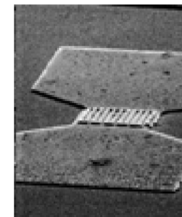
Future plans

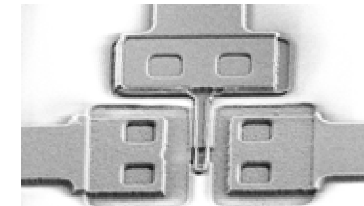
- Improve and optimize Ge PIN and adjacent CMOS devices
- Develop compatible process technology

(Campbell, UT-Austin)

3D Integration of Ge Optoelectronic Devices on Si



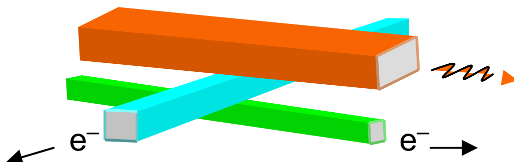




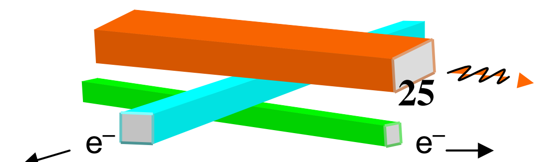
¥Piecewise technologies ready for the monolithic receiver integration in the near future

- Employ recrystallization or layer transfer technique for Ge on Si
- Integration of optical receiver in the upper active (Ge) layer
- ⇒ On-chip optical clock distribution in 3D-ICs

(Saraswat – Stanford)

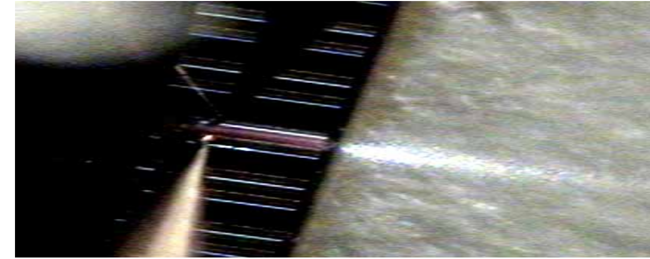


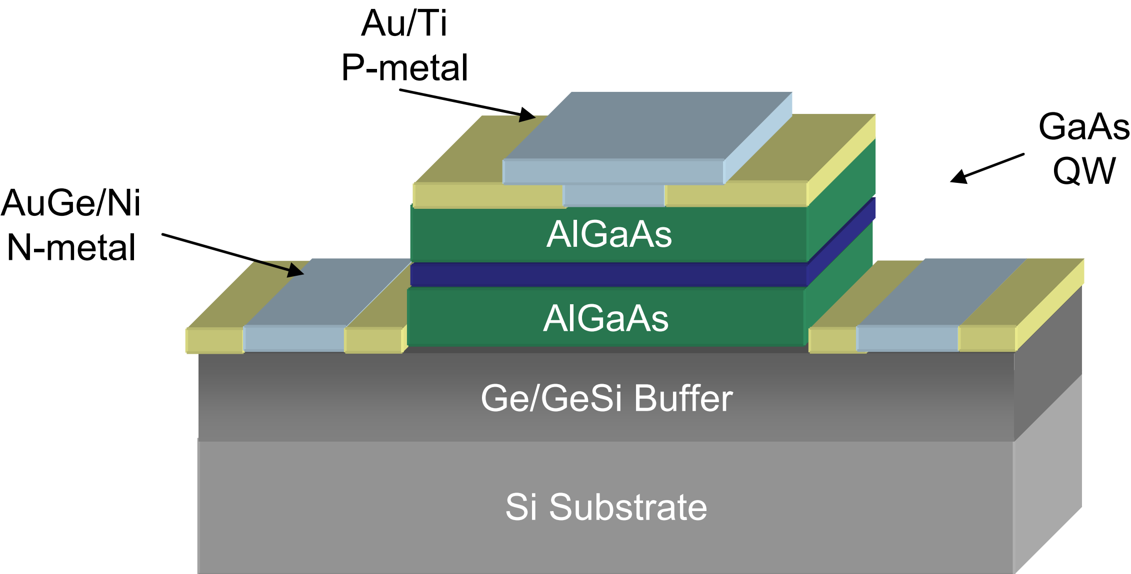
Interconnect Focus Center



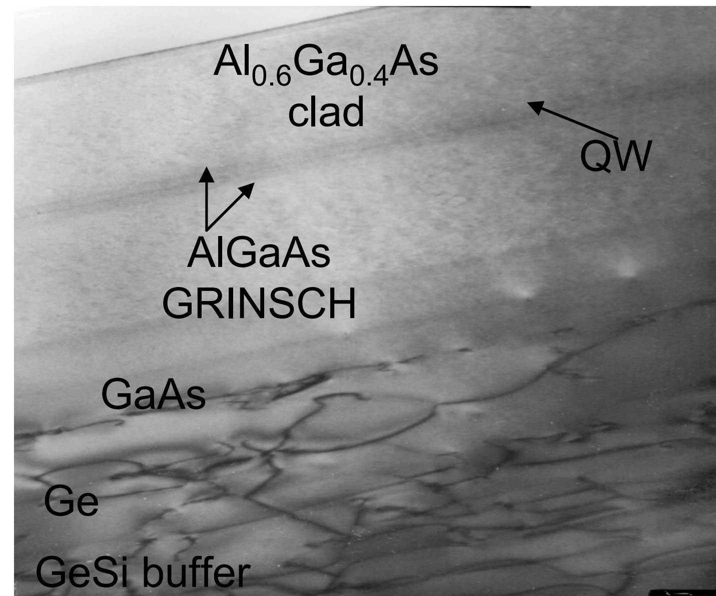
Silicon-Compatible Laser Design (MOCVD Heteroepitaxy)

- AlGaAs/GaAs and AlGaAs/GaAs/InGaAs GRINSCH quantum well on Si substrate
- CW, 28°C operation for > four hours
- Uncoated gain-guided lasers, no heatsinking
  - 5-20 μm stripes, L≈1mm





Graded-index separate confinement heterostructures

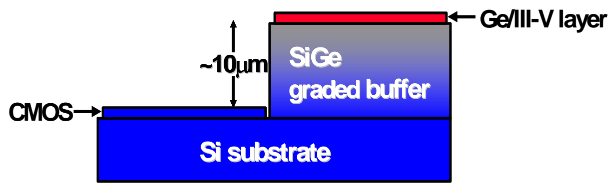


Cross-section TEM 200nm

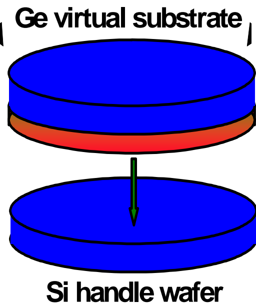
(Courtesy Prof. Gene Fitzgerald)

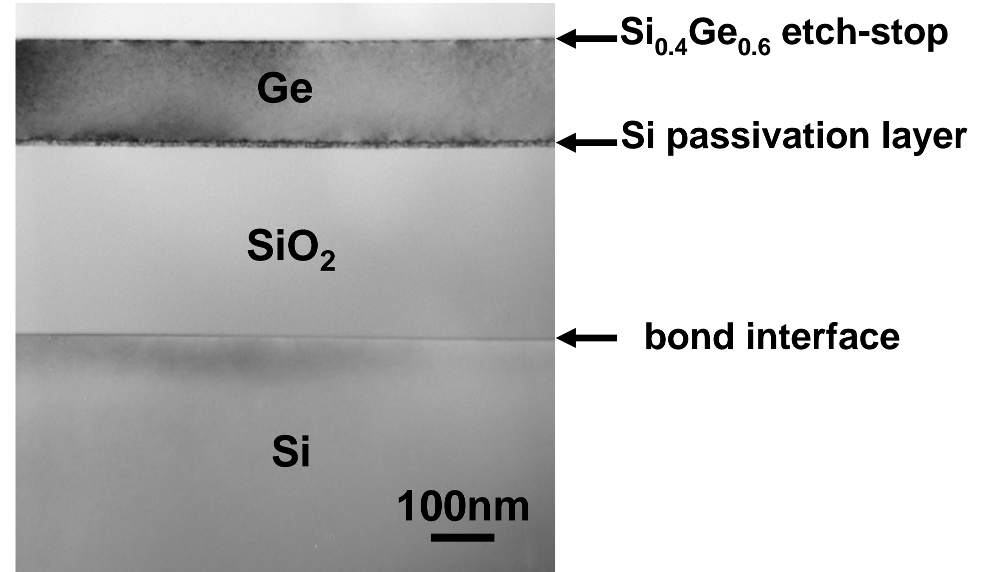
SEMICONDUCTOR SUPPLIERS

Heteroepitaxy *Plus* Wafer-to-Wafer Bonding for III-V/Si Integration



- **Virtual Substrate Bonding:**
  - Allows coplanar integration using large, Si-sized wafers
  - Bulk Si to Si bonding introduces negligible thermal stress

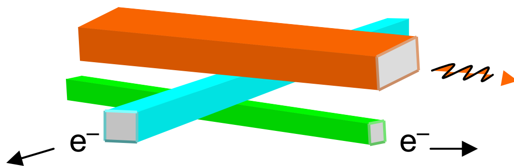


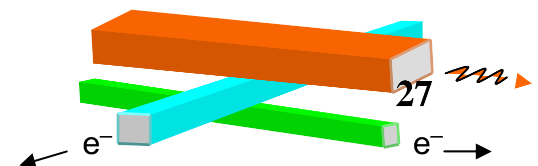


Example of Germanium on insulator that can be created using relaxed buffer bonding

- **Increase reliability of III-V lasers**
  - **Low threadhold laser design**
  - **Improved Ge/SiGe/Si relaxed buffers so that III-V's have even lower dislocation density**
- **Creation of substrate materials compatible with producing such devices with Si CMOS**
  - **Use relaxed buffer bonding to create Si CMOS-compatible platforms with embedded optical planes**

(Courtesy of Prof. E. Fitzgerald)





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SEMICONDUCTOR SUPPLIERS

Coupling

from

Fiber-to-the- Chip

Optical Fiber

Light

Silicon Chip

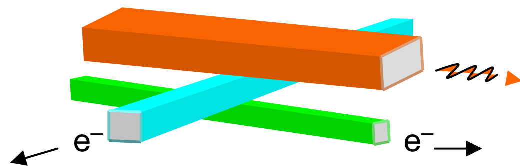
Silicon Waveguide
(High refractive index)

Mode-size mismatch

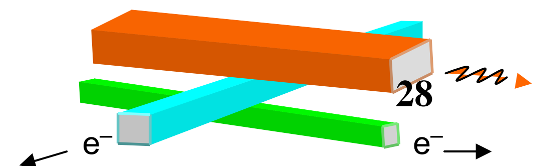
Effective index mismatch

(Courtesy Prof. M. Lipson)

~3% Transmission



Interconnect Focus Center



Proposed Solution: *Evanescent Field Matching*

sub-micron

tens of nanometers

common approach

tens of microns

microns

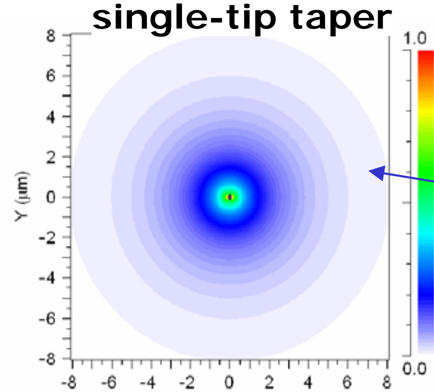
- **Same mode-size**
- **Same effective index**

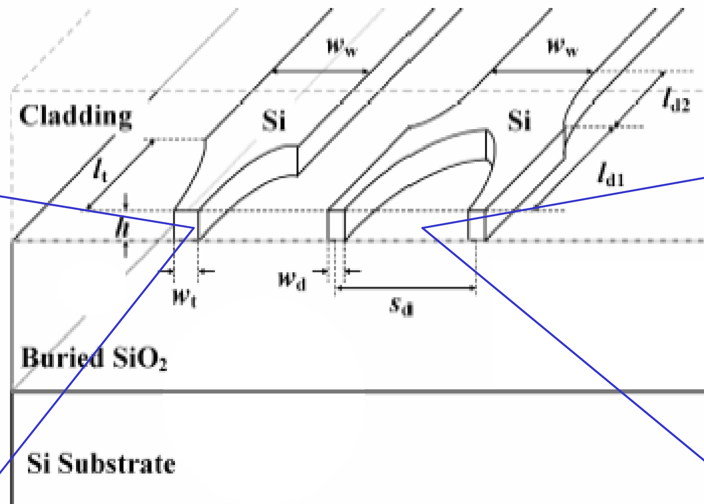
(Courtesy Prof. M. Lipson)

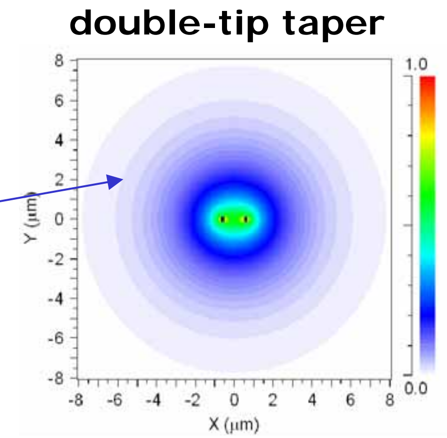
Compact Optical Soldering: Nanotaper Coupler

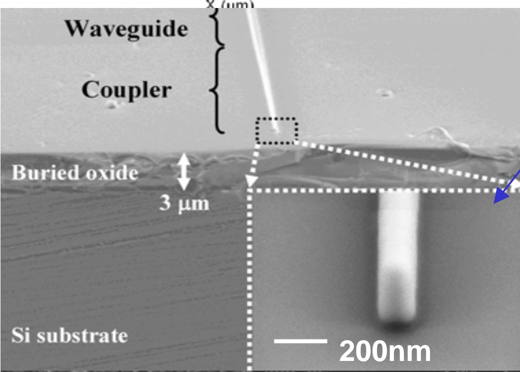
98% Efficient mode conversion achieved within only tens of μm :

- Mode field expands outside the high index core into the low index cladding thus matching both shape and effective index of fiber mode (Courtesy Prof. M. Lipson)
- Double-tip taper allows *mode shape engineering*



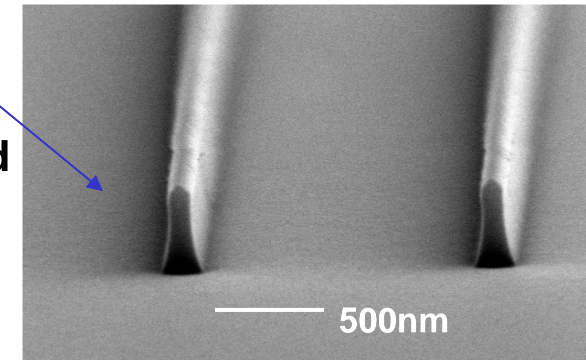






Coupling enhancement factor measured over 1520-1620nm wavelength range:

TE: 7.0 ± 0.4
TM: 8.2 ± 0.5



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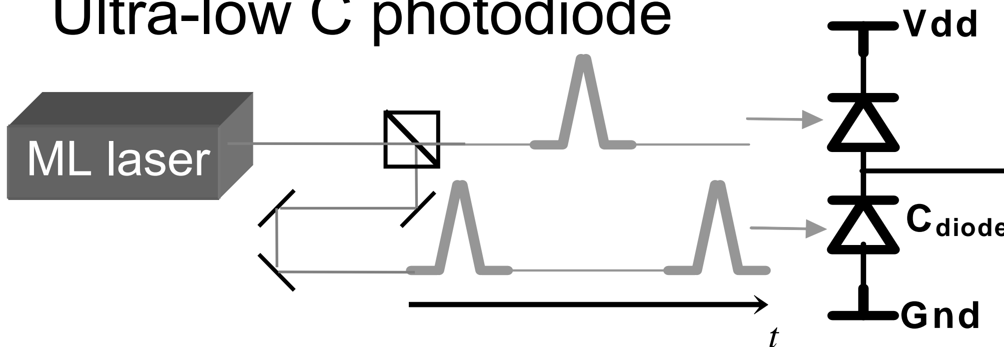
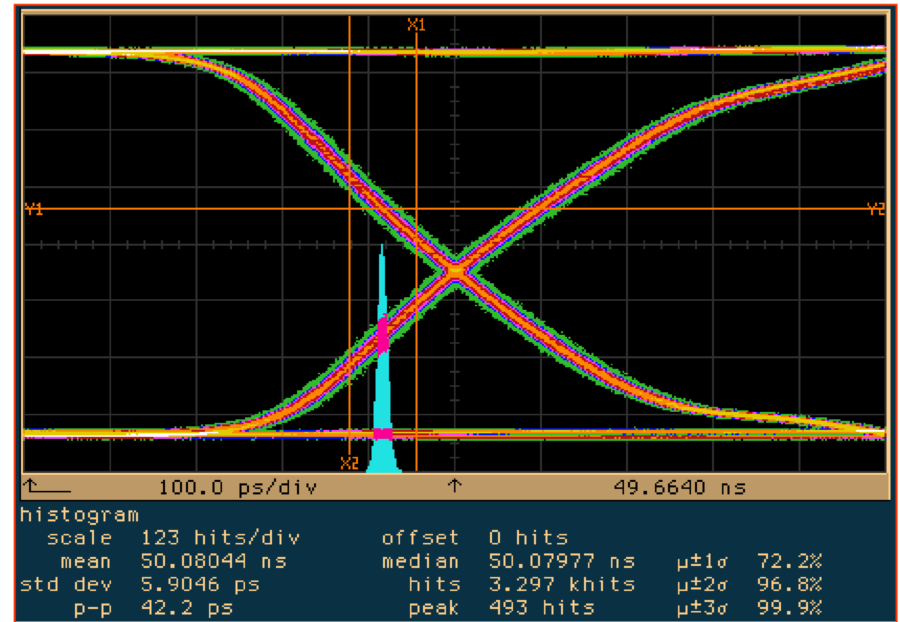
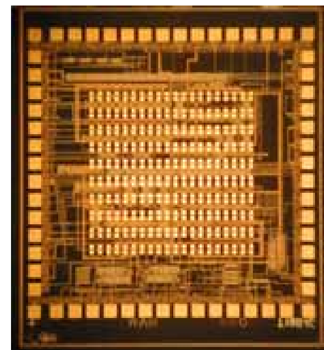
Optical Clock Injection Using Modelocked Short Pulse Lasers

- Modelocked lasers can provide low-jitter, GHz clocks for electronics
- Receiver-less direct optical injection produces low-jitter digital clock
- Ultra-low C photodiode

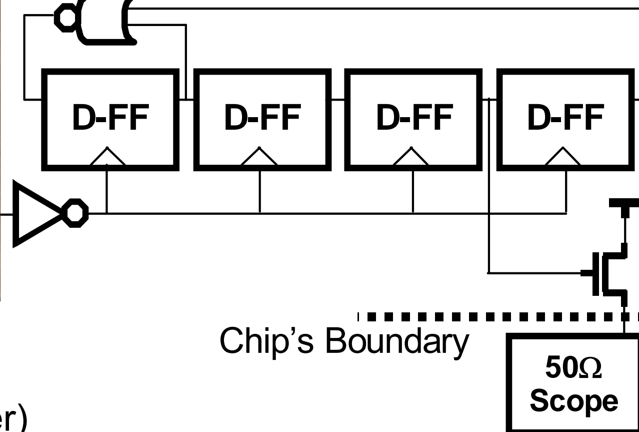




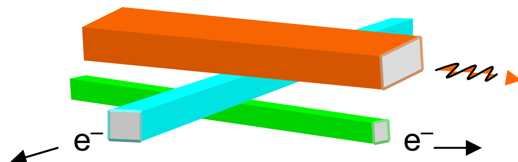


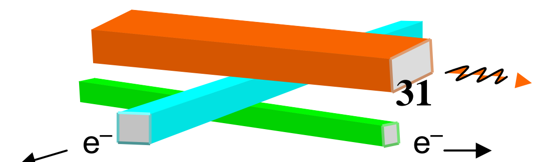
SOI Test Chip

(Courtesy Prof. D. Miller)



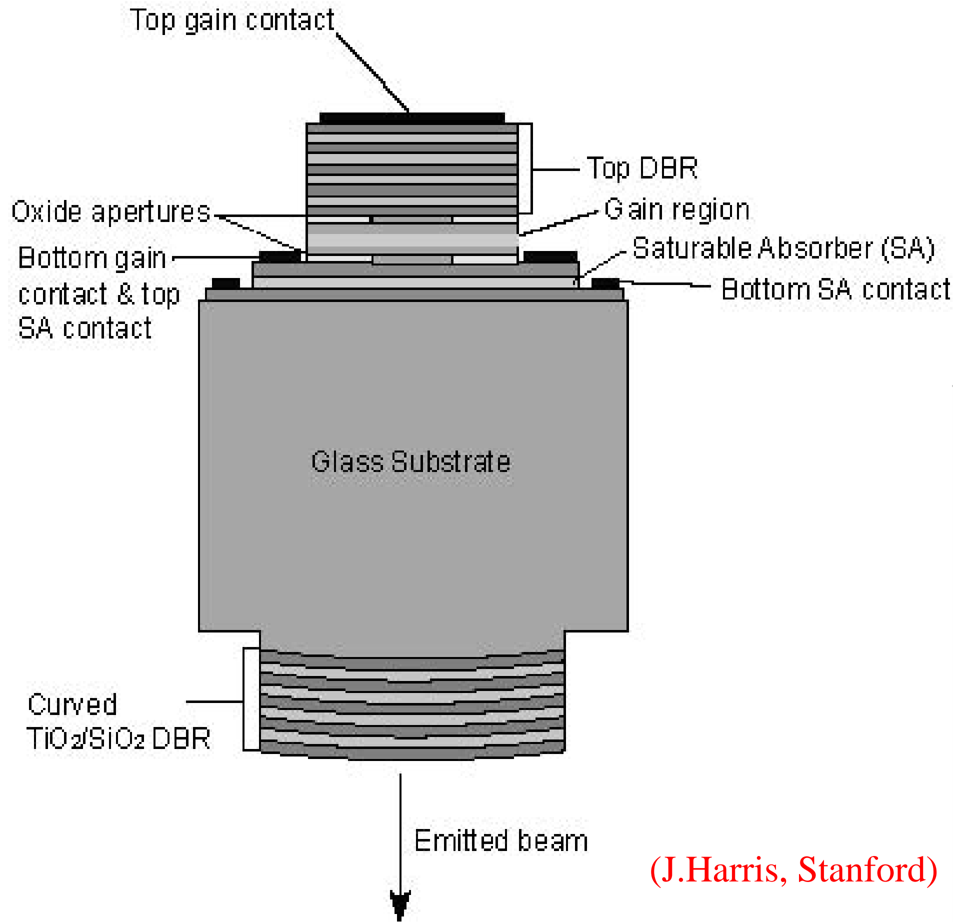
6 ps rms jitter measured on optical clock is < 31 ps rms jitter on electrical clock.





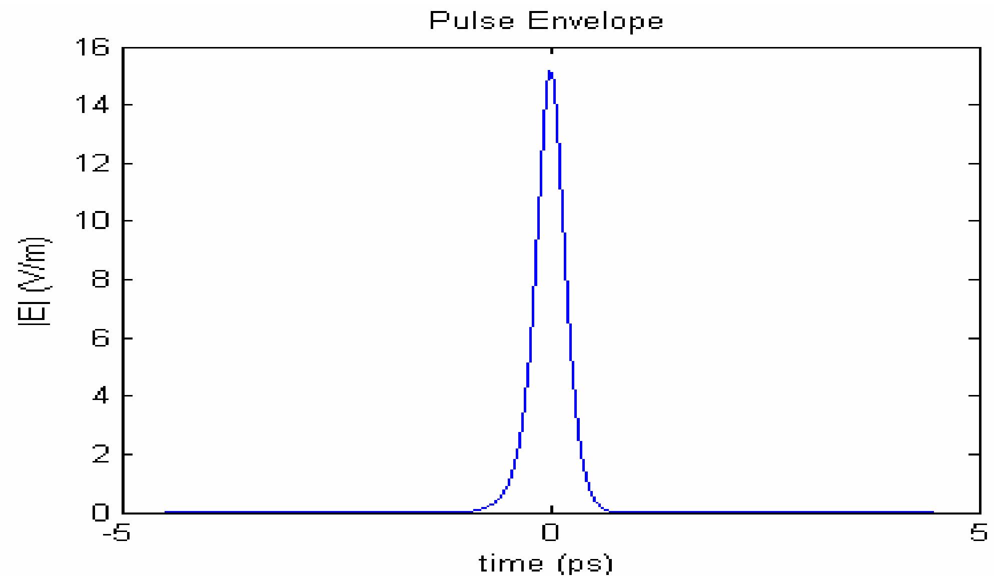
Mode-Locked Vertical Cavity Surface Emitting Laser

- ***Objective:*** to mode-lock a VCSEL to generate a train of sub-picosecond pulses at 10-80 GHz repetition rates.
- ***Applications:*** OTDM, WDM and Optical Clock Distribution.



(J.Harris, Stanford)

Schematic of Mode-Locked VCSEL



Mode-locking simulations of the device

Interconnect Focus Center

Program Matrix

	Driver 1 High Performance Network Chip *Krishna Saraswat*	Driver 2 Low-Energy Mixed Signal Wireless Node *Anantha Chandrakasan*
Task 1 Electrical Interconnects *Alain Kaloyeros*		
Task 2 Optical Interconnects *David Miller*		
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Task 4 Circuit & System Design & Modeling *Duane Boning*		

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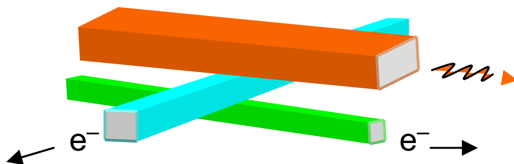
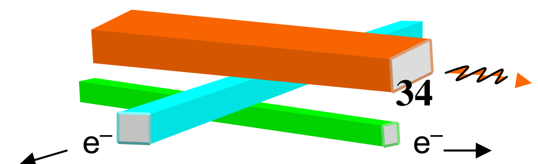
Singular Objective:

Wafer Level, Batch Fabricated, High Density, Compliant,

Compatible Electrical, Optical & Thermofluidic

Input/Output Interconnects





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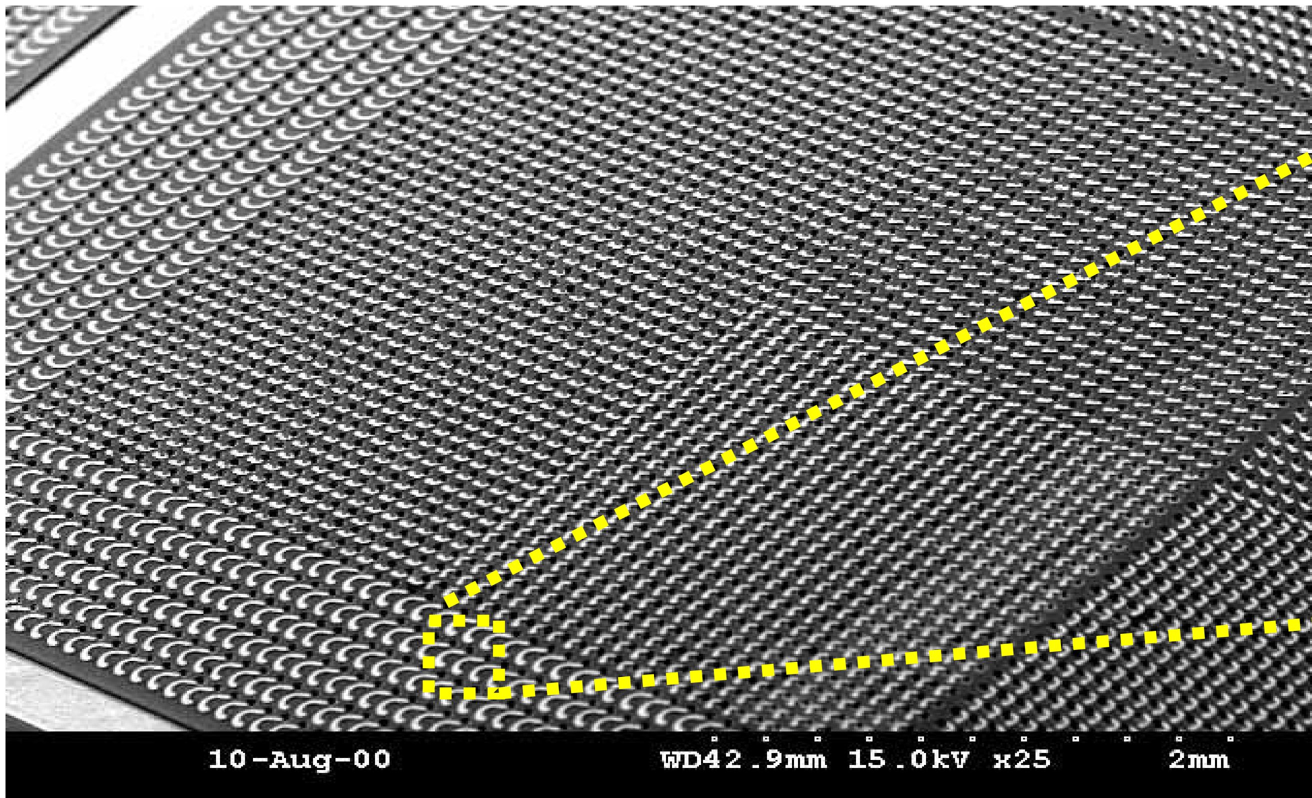
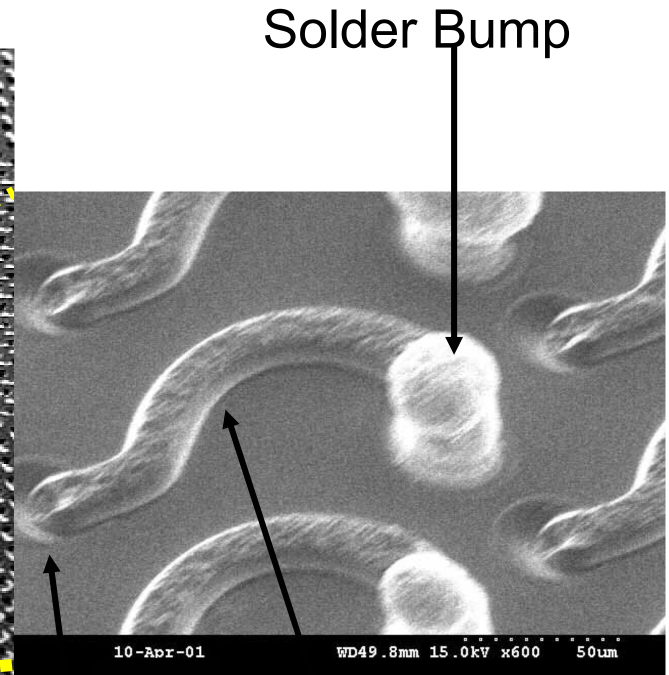
SEMICONDUCTOR SUPPLIERS

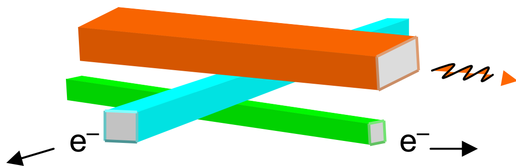
Sea of Leads

Ultra High Density **Flexible** Electrical I/O: 12,000 leads/cm^2





(Courtesy of Dr. M. Bakir) XX



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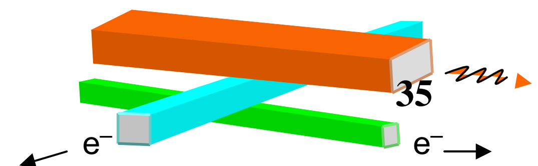

Advanced SoL Compliant Interconnects

UBM

Releasing gap

Polymer solder dam

SE 18-May-04 WD39.1mm 10.0kV x450 100um

- Complete bumping solution includes:
  - Solder dam to protect the metal leads (wicking)
  - Ni-UBM as a reliable soldering base for C4

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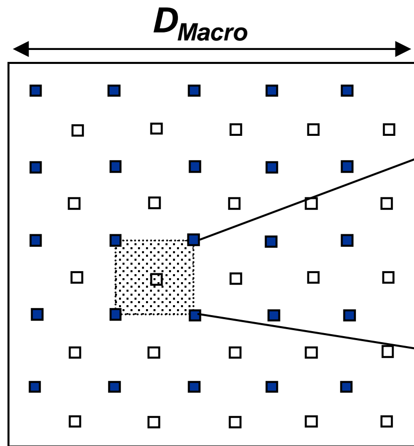
SEMICONDUCTOR SUPPLIERS

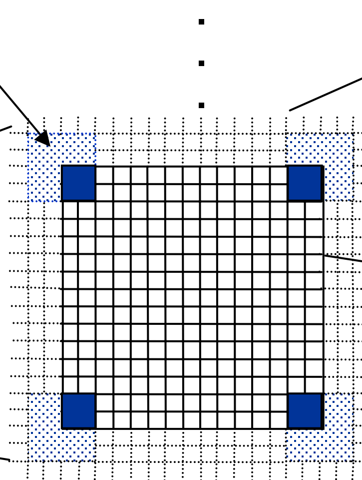
The Fundamental Equation for Co-Design of the Chip-Package *Power Delivery* Network

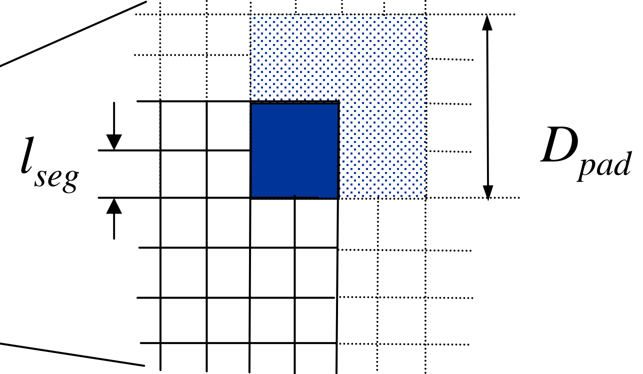
Area Array Package



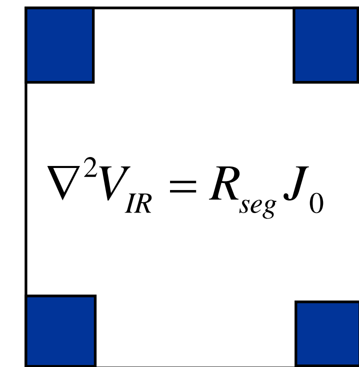
Power Pads ■ Ground Pads □

Pad





A cell surrounded by four pads

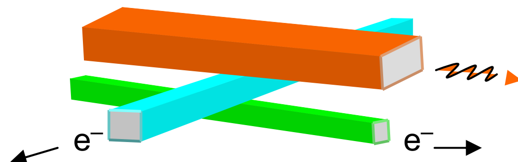


Boundary condition for each Cell

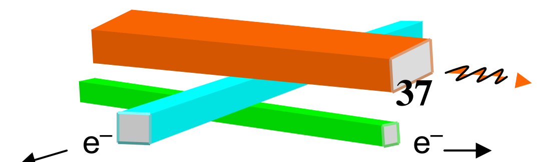
$$V_{IR} = \frac{R_{seg} \cdot I_{Total}}{2\pi \cdot n_{pg}} \ln\left(\frac{0.65 \cdot D_{Macro}}{\sqrt{n_{pg}} \cdot D_{pad}}\right)$$

$$R_{seg} = \rho \frac{l_{seg}}{W \cdot h}$$

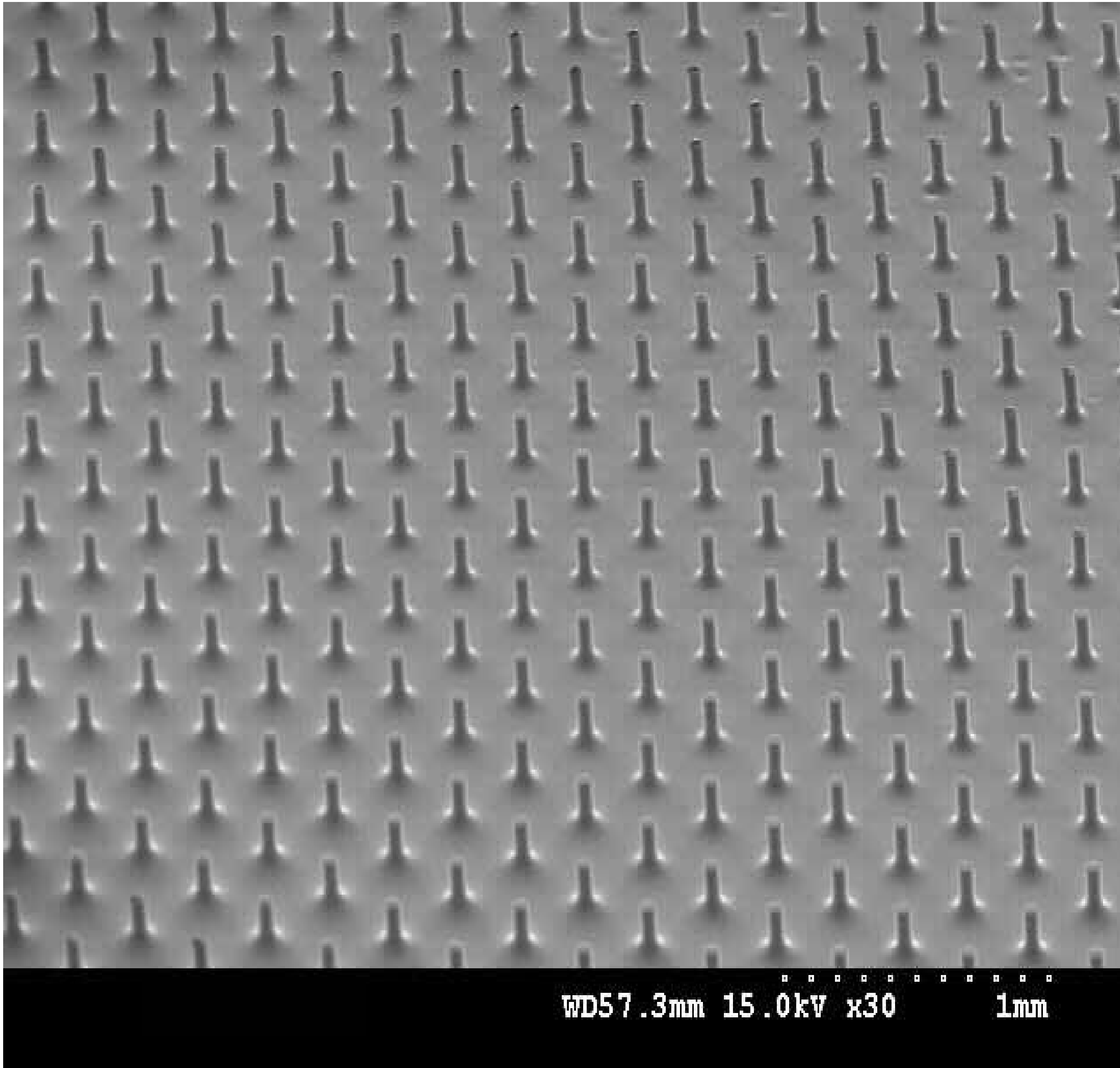
- V_{IR}: IR-drop voltage on V_{dd} or ground
- I_{Total}: Total macro block or chip current
- R_{seg}: Resistance of a segment
- n_{pg}: Number of power or ground pads in a macro block or chip
- D_{Macro}: Edge dimension of the macro block or chip in cm
- D_{pad}: Size of the pad in cm
- ρ: Resistivity of the metal
- W: Width of the interconnect
- h: Height of the interconnect



Interconnect Focus Center



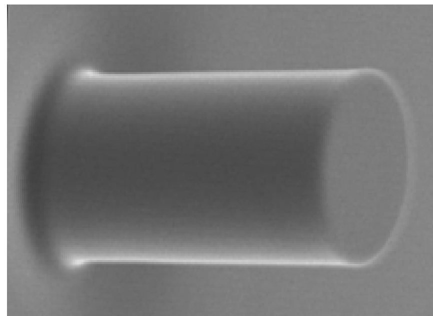
Second Generation *Sea of Leads:Compliant Polymer Pillars for Compatible* ***Optical & Electrical*** *I/O Interconnects*



50 µm x 150 µm tall photo-defined pillars using Avatrel (Promerus LLC and GT projects)

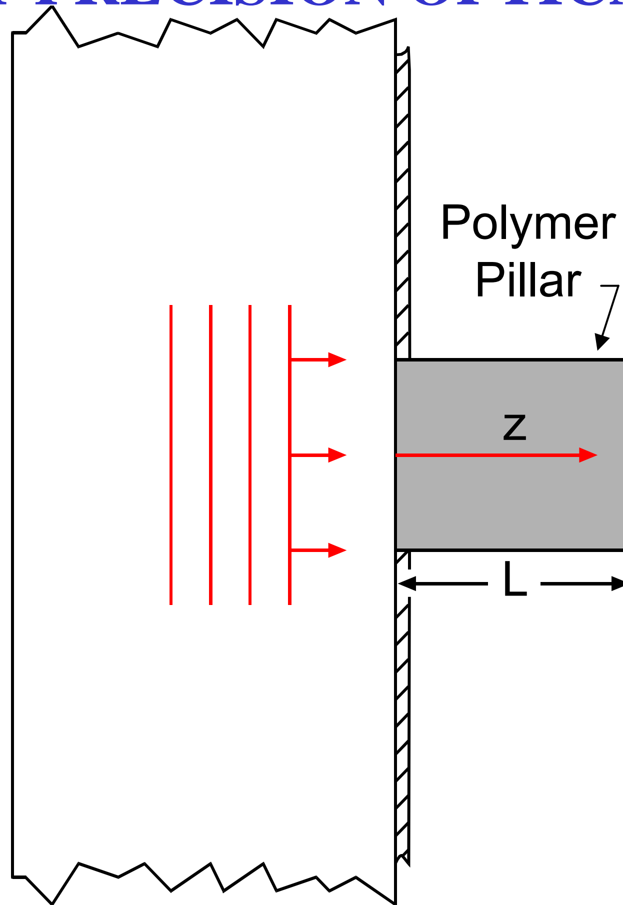
(Courtesy of Dr. M. Bakir)

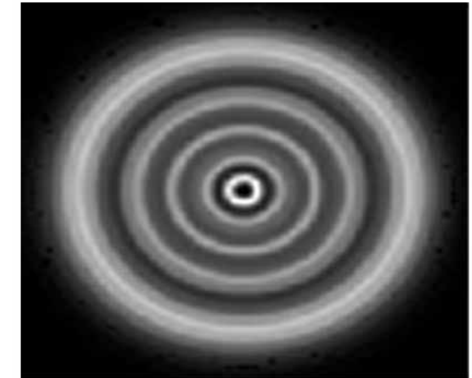
POLYMER PILLARS AS COMPLIANT HIGH-QUALITY PRECISION OPTICAL WAVEGUIDES



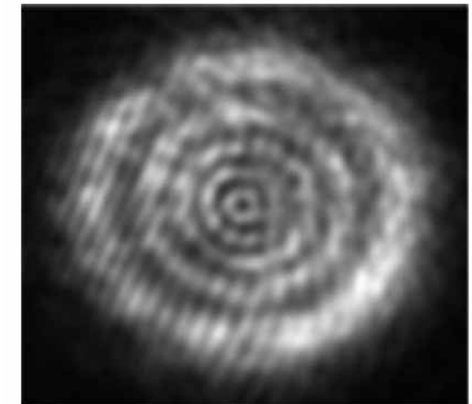
Polymer Pillar

(Courtesy Prof. T. Gaylord)



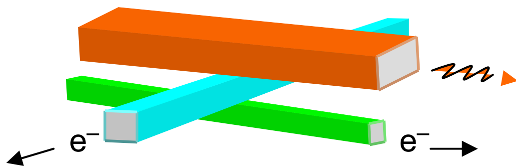


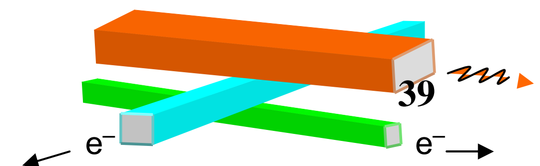
Calculated



Measured

Analysis and measurement of optical transmission of polymer pillar.





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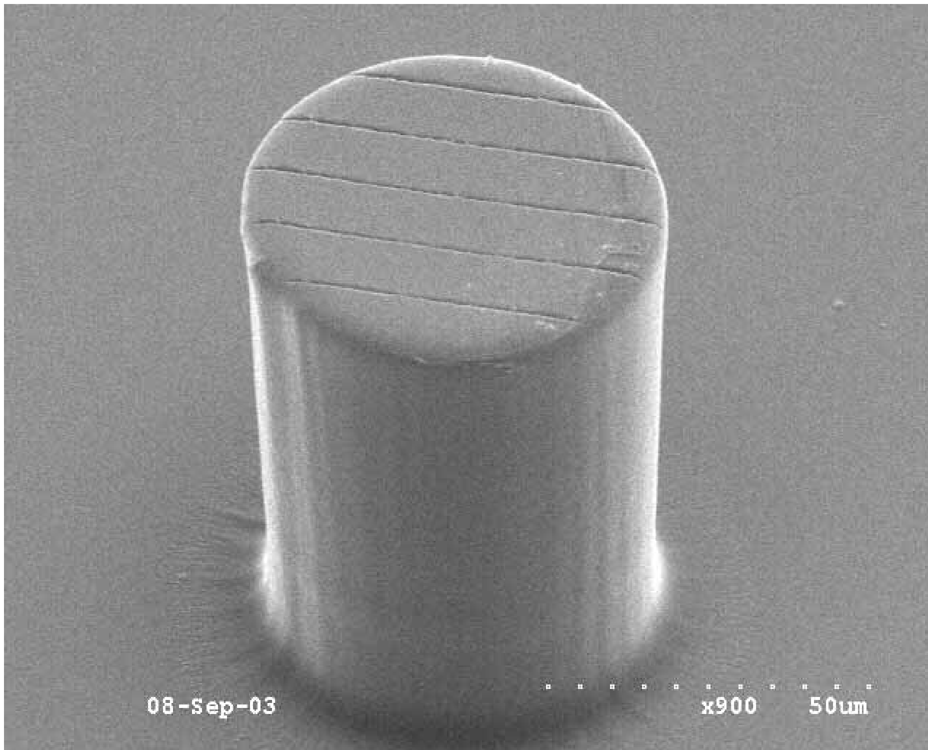
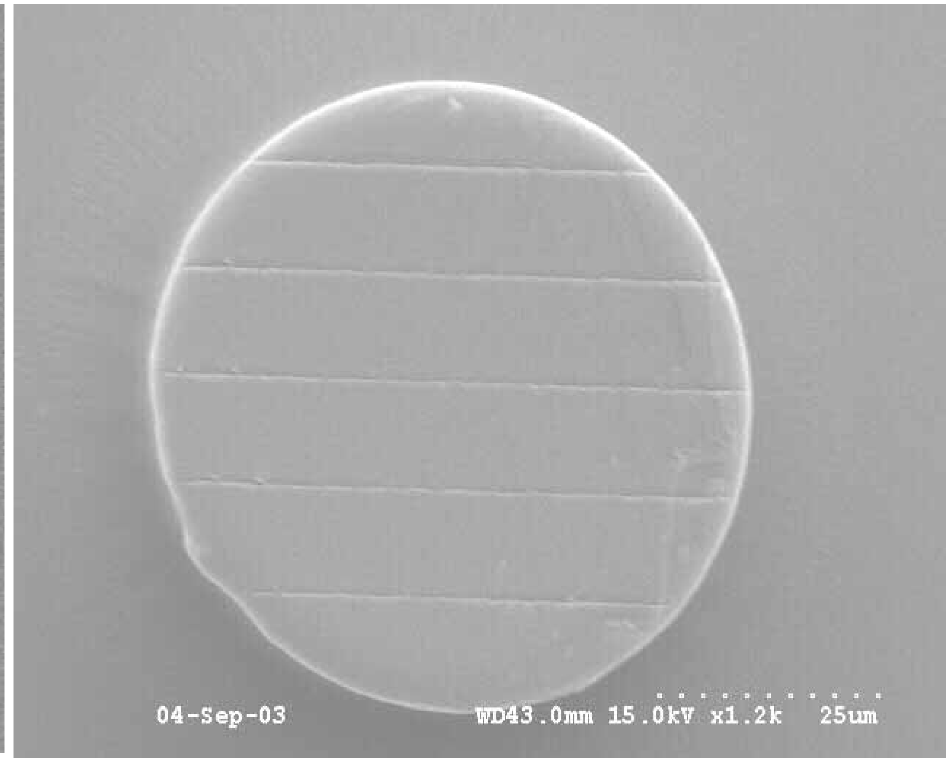
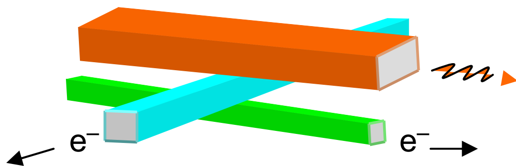
Diffraction Gratings on Top of Compliant Pillars

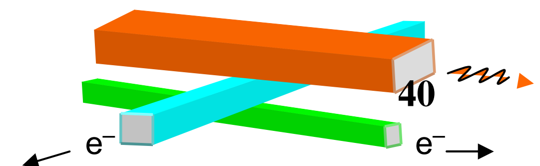




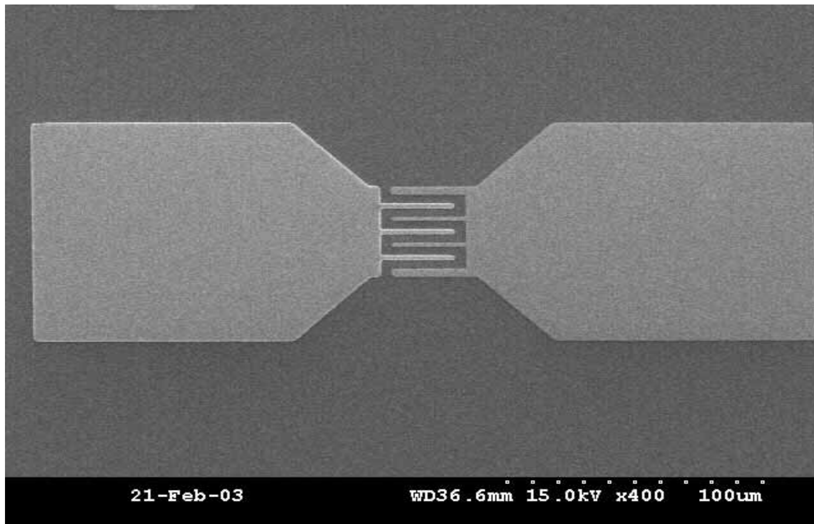
Integration of (GIT) optical pillars with optical detectors (GIT & Stanford) & emitters (GIT &UA,NY)



Interconnect Focus Center

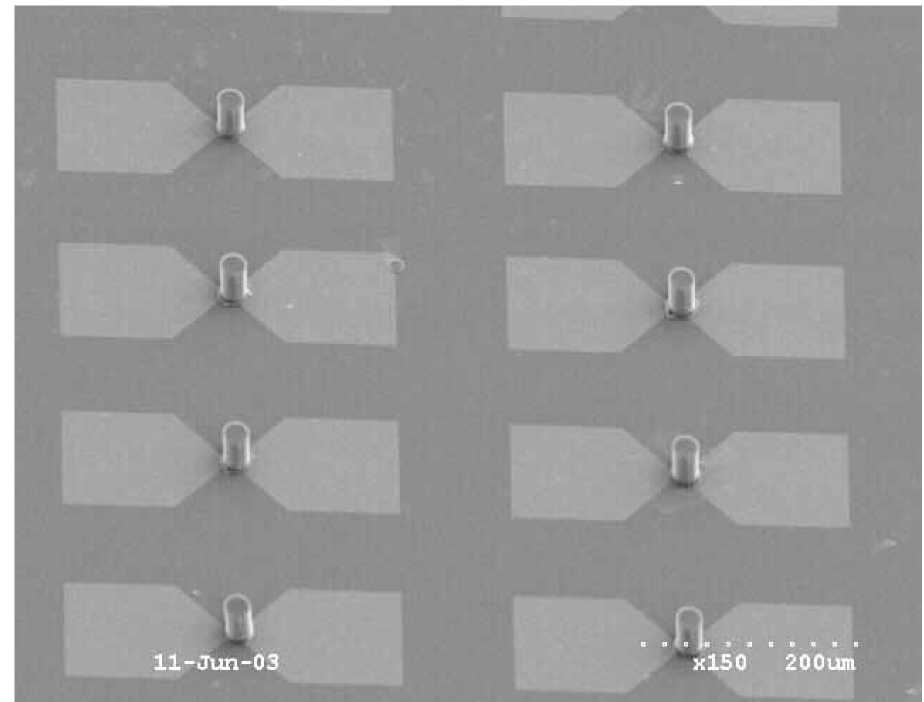


Integration of Compliant Polymer I/O with Photodetectors



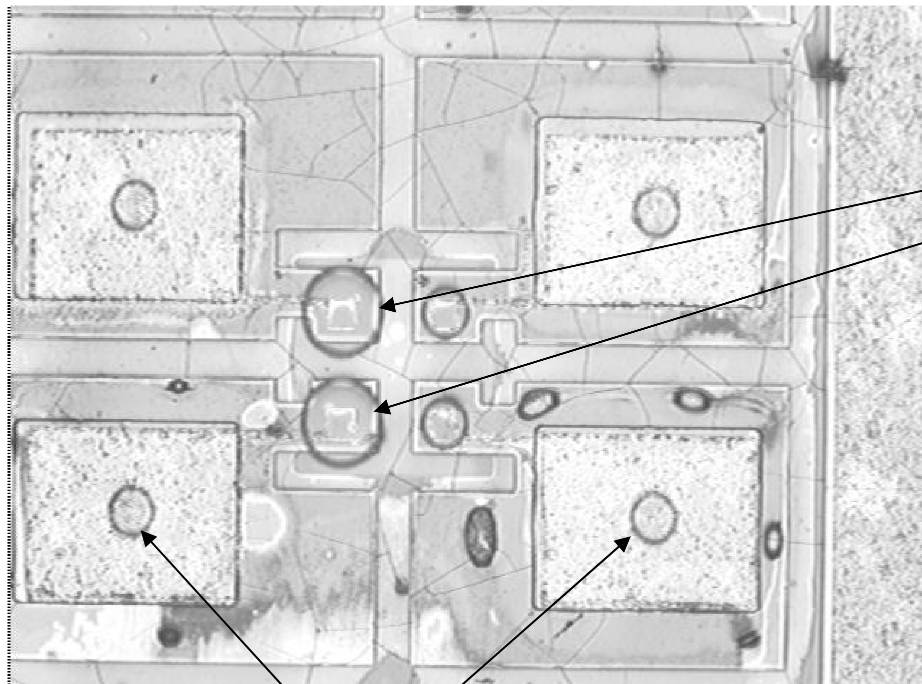
MSM photodetectors

(GIT & Stanford)



Polymer pins on photodectectors

Integration of Optical I/O Pillars with GaAs VCSELs

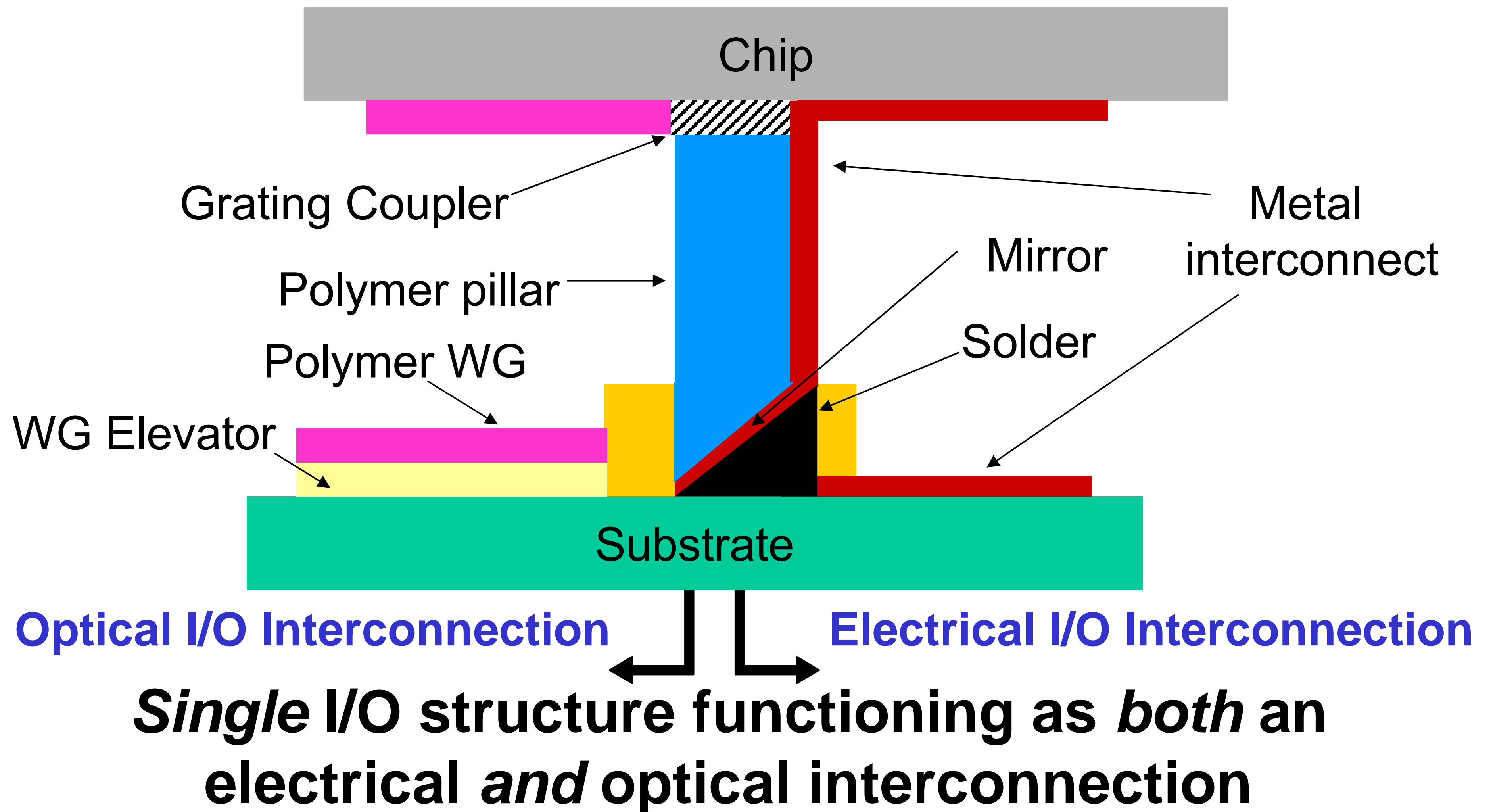


Optical pillars

Electrical pillars (not yet metallized)

(GIT with SUNY Albany)

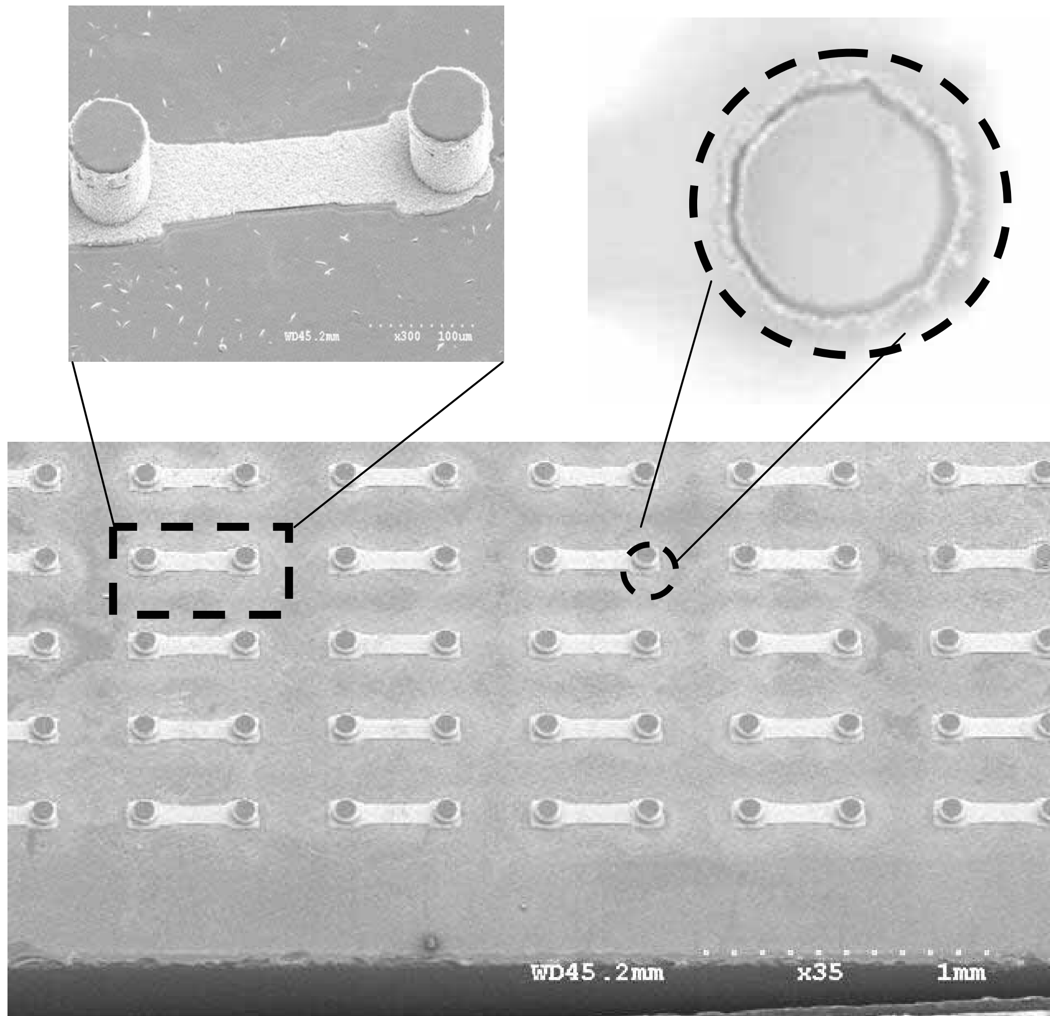
Dual Function Electrical/Optical Compliant Polymer Pillar I/O



Single **I/O structure functioning as *both* an electrical *and* optical interconnection**

(Courtesy of Dr. M. Bakir)

Dual Function Compliant Polymer Pillars



Dual-mode polymer pillar: optically transparent tip

Thermofluidic Input/Output Interconnects

Microchannel Modules

Electrical Connections

targeted, on-demand microchannel cooling

Integrated EO Pump/controller

Fluid: Water or Liquid Air

High Performance CMOS Chip

(Courtesy of Prof. Ken Goodson)

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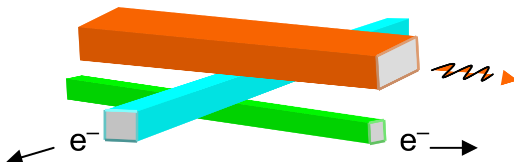
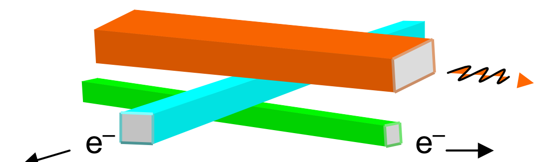
Interconnect Focus Center

Program Matrix

	Driver 1 High Performance Network Chip *Krishna Saraswat*	Driver 2 Low-Energy Mixed Signal Wireless Node *Anantha Chandrakasan*
Task 1 Electrical Interconnects *Alain Kaloyeros*		
Task 2 Optical Interconnects *David Miller*		
Task 3 Thermal Management & Power Delivery *Paul Kohl*		
Task 4 Circuit & System Design & Modeling *Duane Boning*		



Interconnect Focus Center



SEMICONDUCTOR SUPPLIERS

Key Objectives: Novel Circuits, Systems & CAD Tools

Electrical

Signalling

- Extended Electrical Signalling
- Clock-Data Recovery
- Substrate Noise Estimation
- RLCM Impulse Response Extraction
- E-M Analysis of Rough Surfaces

Clocking

- Standing Wave Clock

Power

- Energy in FPGAs
- Power Delivery in Stacked Logic

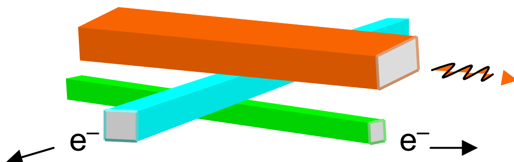
Optoelectronic

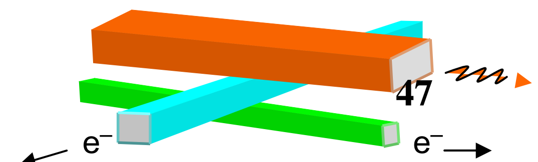
Signalling

- TIA-less Optical Receiver
- 3D E-M Reduced Order Models
- Sensitivity Analysis in Photonic Devices
- Variation in Optical Splitters
- Simulation of Mode-Locked Laser Dynamics
- Modeling Photonic Crystals
- 3D Maxwell Solution for Optical IR

Clocking

- PLL-Based Active Optical Clock





MARCO | SIA Semiconductor Industry Association | SEMICONDUCTOR SUPPLIERS | Department of Defense | DARPA

Extend Electrical Signaling

(Horowitz, Stanford)

Multi-tone data rates with thermal noise
Nelco 64Gb/s
FR4 38Gb/s
#bits/Hz
frequency [GHz]

data0 → LPF | data1 → LPF ⊗ BPF (e^{jw1t}) | ... | dataN → LPF ⊗ BPF (e^{jwNt})

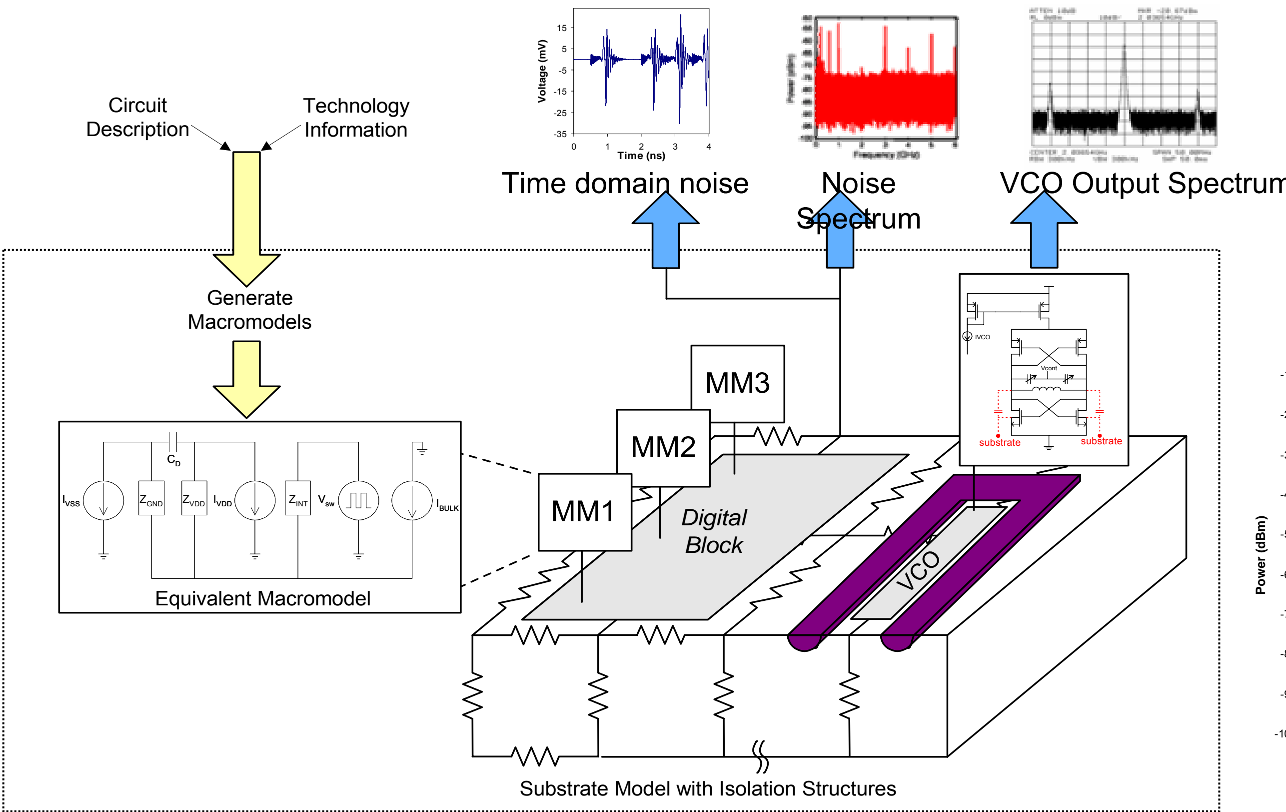
levels vs f

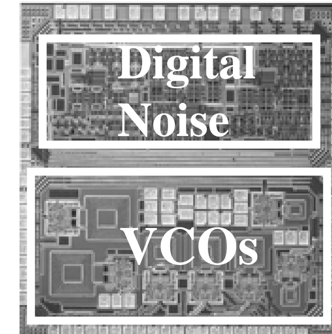
LPF → data0 | BPF ⊗ LPF → data1 (e^{jw1t}) | ... | BPF ⊗ LPF → dataN (e^{jwNt})

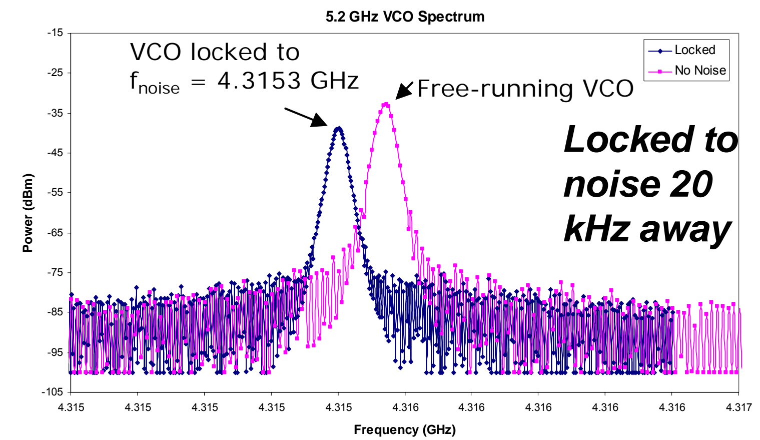
-Today’s links are baseband limited by intersymbol interference (ISI) – can’t afford enough equalization

-Extend performance by multi-tone transmission but must be simple: can’t afford discrete multitone (DMT) circuits – explore analog methods

Substrate Noise Estimation *Framework*

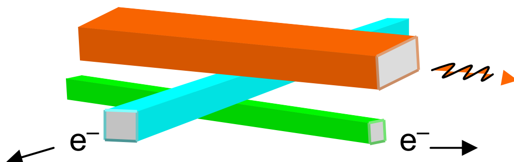


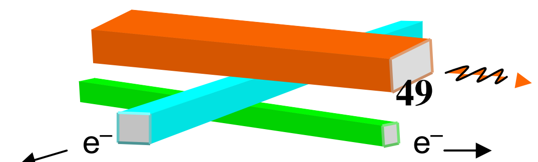




(N. Checka, A. Chandrakasan, R. Reif; MIT)

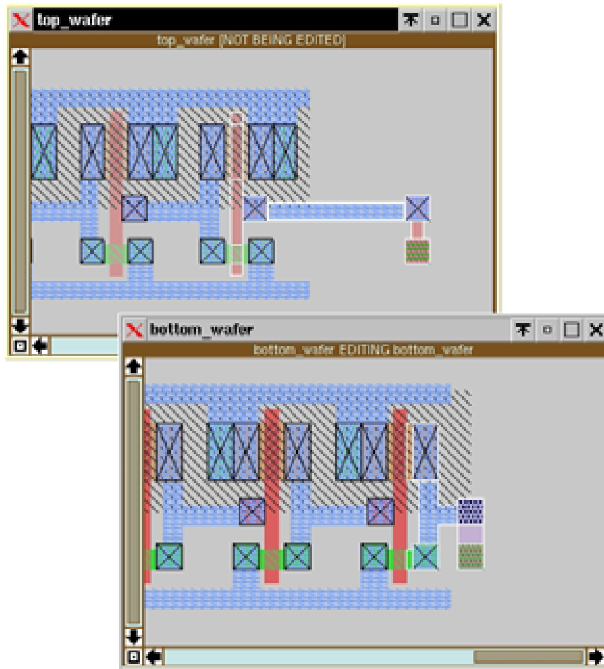
- **Testchip fabricated and tested to study the impact of substrate coupling**
- **Framework: Demonstrated < 5% error with Spice for key benchmark circuits**
- **Framework expected to be released in 2005**





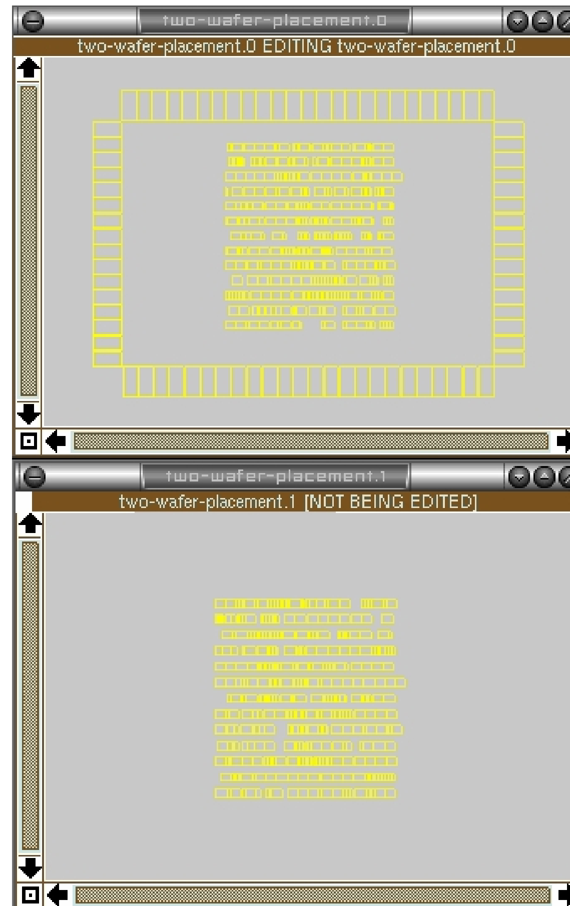
Physical Design Tools for 3D Integration

3D Magic

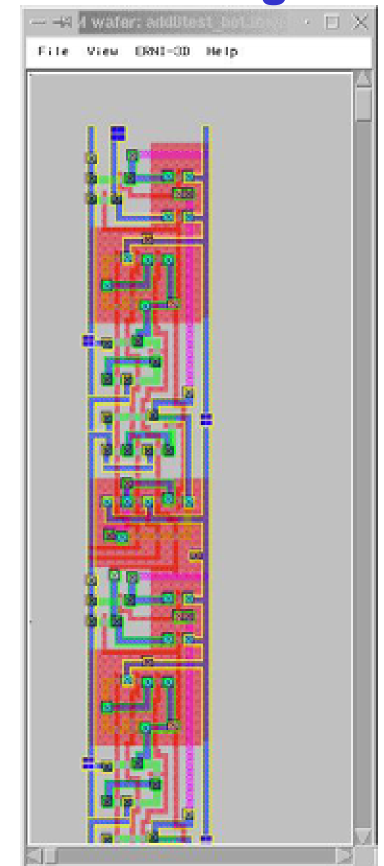


(A. Chandrakasan & R. Reif; MIT)

3D Standard Cell Placement and Routing



ERNI 3D Reliability Testing



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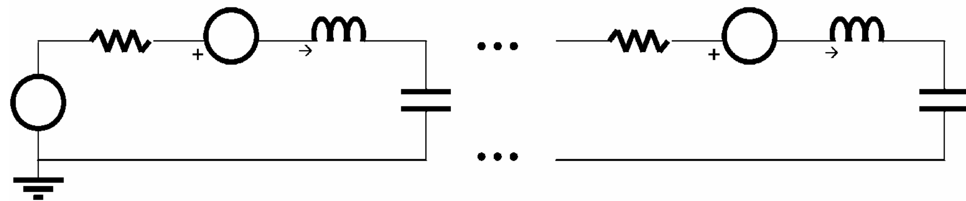
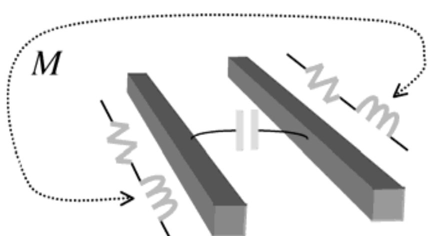
3D Design Tools

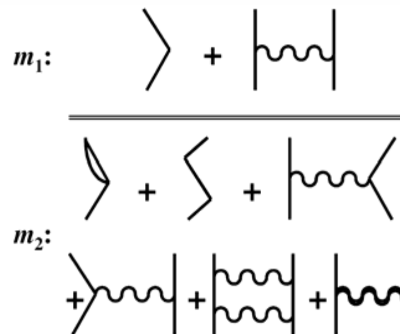
Electrical & Optical Interconnect Impulse-Response Simulator

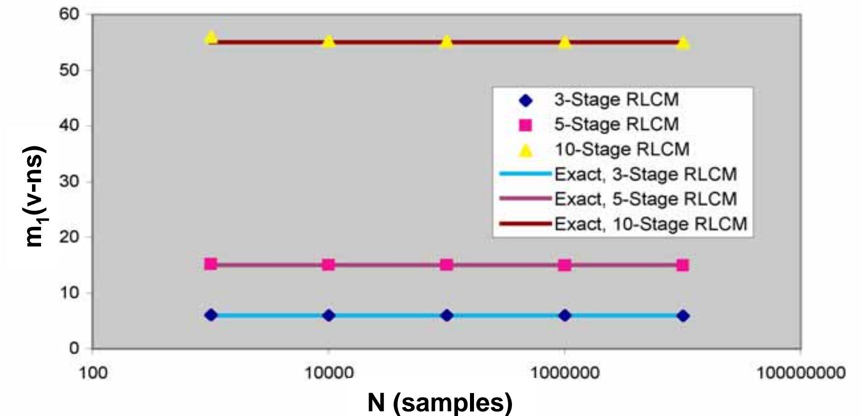
- *Challenge*—**create efficient stochastic (random-walk/Monte Carlo) algorithms for IC-interconnect impulse-response (IR) simulation.**
- ***Results*—created and validated a new algorithm for electrical IR extraction of uncoupled & coupled *RLCM* lines; created a new algorithm for optical IR extraction.**
- ***Future Work*—analyze *RLCM* bus lines with 1G mutual-inductance couplings; test the optical IR-extraction algorithm.**

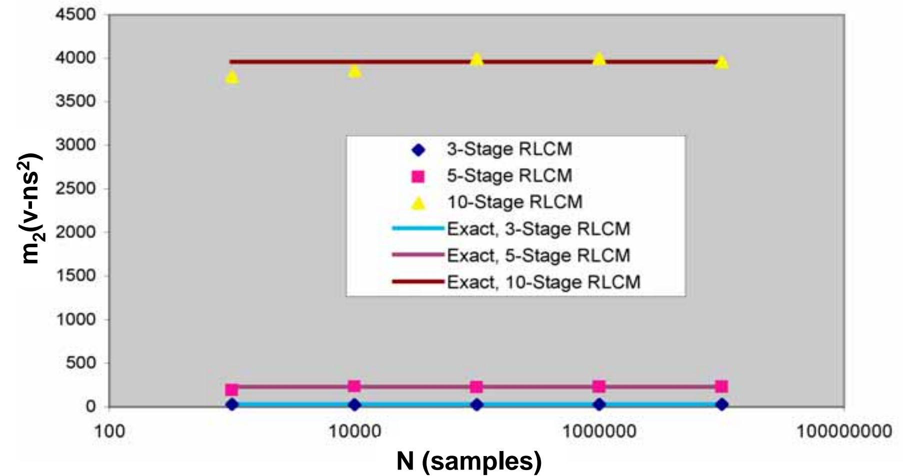




(Y.L. Le Coz, RPI)







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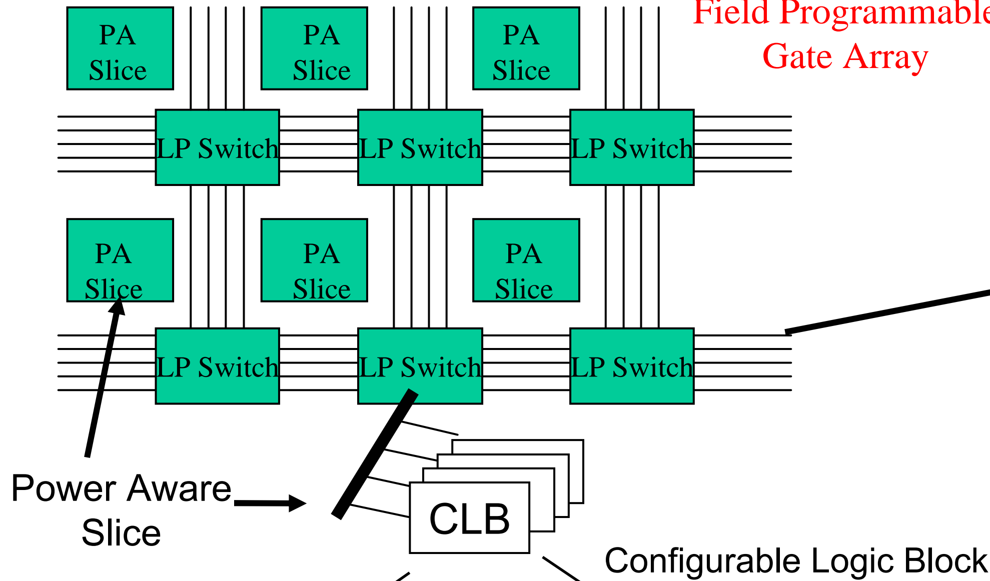
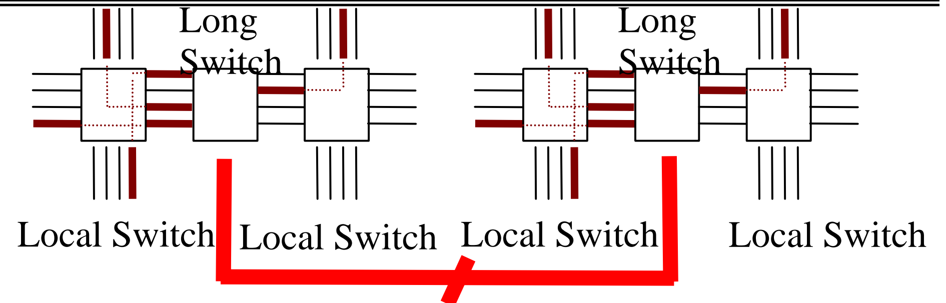
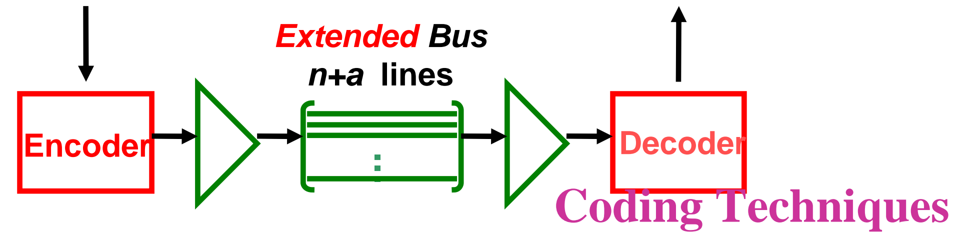
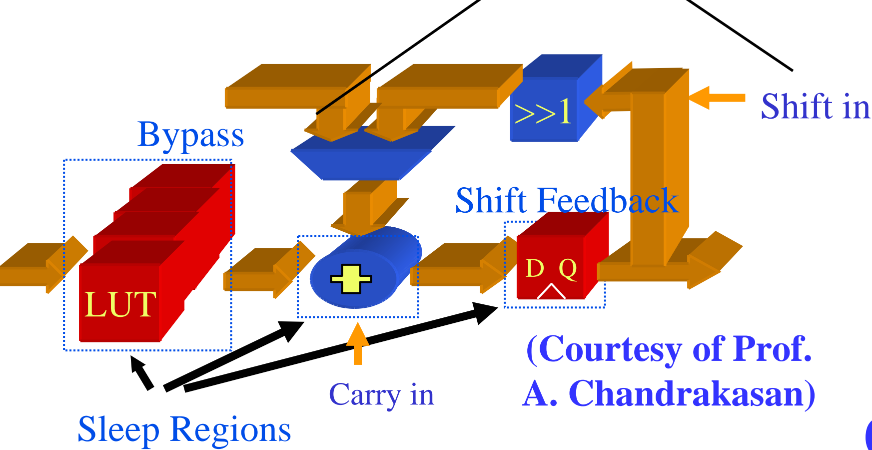
A Low Power FPGA Architecture







Coding Techniques



(Courtesy of Prof. A. Chandrakasan)

0.13μm testchip

- Significant component of the power in FPGA structures is dissipated in wires (eg 60%)
- New CLB architecture, power gating & coding minimize power dissipation (eg 50% improvement in logic utilization & 9x less leakage .

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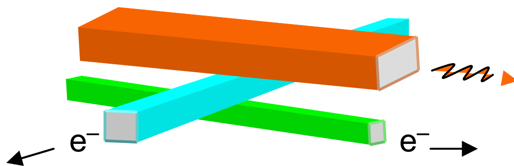
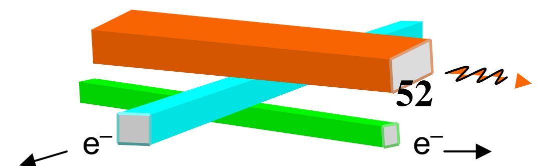
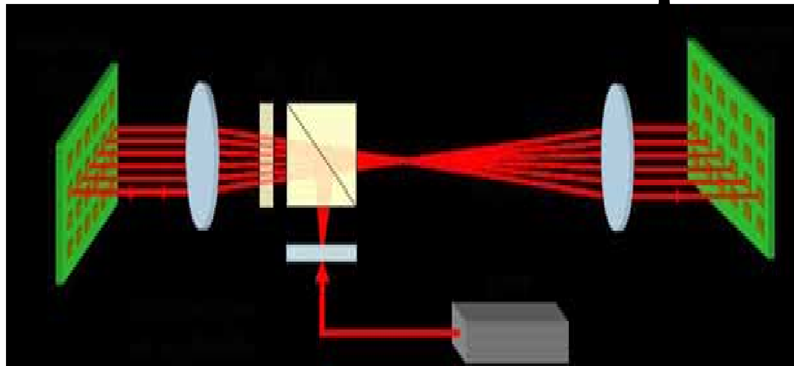


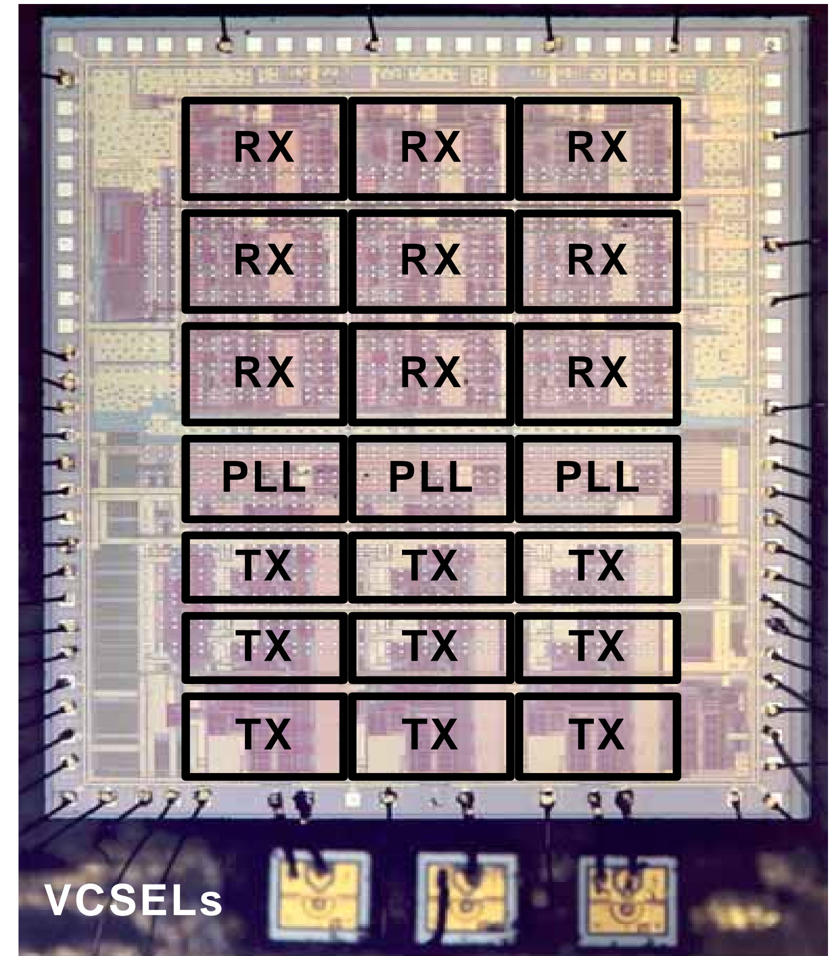
Interconnect Focus Center



Parallel Optical Interconnect



Transmitter chip laser Receiver chip



- **Optical transceiver in CMOS**
  - **5 G/b in 0.25μ technology**
  - **Used flip-chip MQW diodes**
  - **In 90nm, > 15Gb/s, < 30mW**
- **Uses novel receiver architecture**
  - **No TIA in forward path**
  - **Integrating receiver**

(M.Horowitz)

Optical Receiver Block Diagram

V_{dd}

V_{in}

I_{DC}

LPF

ϕ_1

ϕ_2

C1

C2

$V_{in}(n+1)$

$V_{in}(n)$

+ Latch -

+ Latch -

D_{out}

Double-sampler

•*IFC & CSSFC*

(Courtesy Prof. M. Horowitz)

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PROPHET: Optoelectronic Simulation of OE/QW Structures

Device and Simulation Parameters

Calculate Band Structure and Optical Matrix Elements (k•p method)

Electronic Solver (PROPHET): Simultaneous Sol'n:
- **Poisson,**
- **Carrier Continuity,**
- **Photon Rate Equations**

Output

Optical Solver (FDTD): Compute Field Pattern, Photon D.O.S., Resonant Frequency and Optical Loss

* Hot Cavity Consideration

p-Contact
p-DBR (mirror)
Oxide
Quantum Wells (QW)
n-DBR (mirror)

(Courtesy Prof. R. Dutton)

Optical Power-vs-I
V-vs-I
light output power (mW): 0, 5, 10, 15, 20
voltage (V): 0.9, 0.95, 1, 1.05, 1.1
current bias (mA): 0, 10, 20

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Conclusion--Overarching Challenge of Interconnect Era:

To Provide a Hierarchy of Electrical, Optical & Thermofluidic Interconnect Solutions

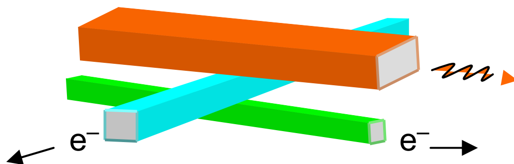
5. System: **Innovative interconnect-centric system architectures that "keep interconnects short"**

4. Circuit: **Original circuit concepts & physical design tools**
(eg "amplifier-less" optical receivers & 3D design tools)

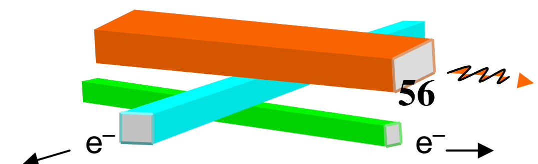
3. Device: **Novel optoelectronic device & interconnect structures**
(eg mode-locked VSCELs & batch-fabricated polymer optical I/O pins)

2. Material: **New materials and processes (eg carbon nanotubes and molecular wires)**

1. Fundamental: Previously untapped fundamental principles (eg on-chip photonics)

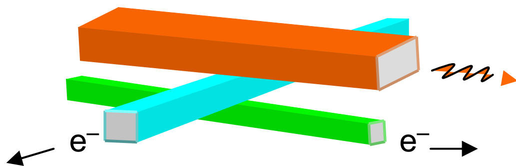


Interconnect Focus Center



SEMICONDUCTOR
SUPPLIERS

THANK YOU



Interconnect Focus Center