Emerging Technologies and Moore's Law: Prospects for the Future

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Economics, Technology, & Innovation

"*No exponential is forever … but we can delay 'forever'*."

Technologies on Deck

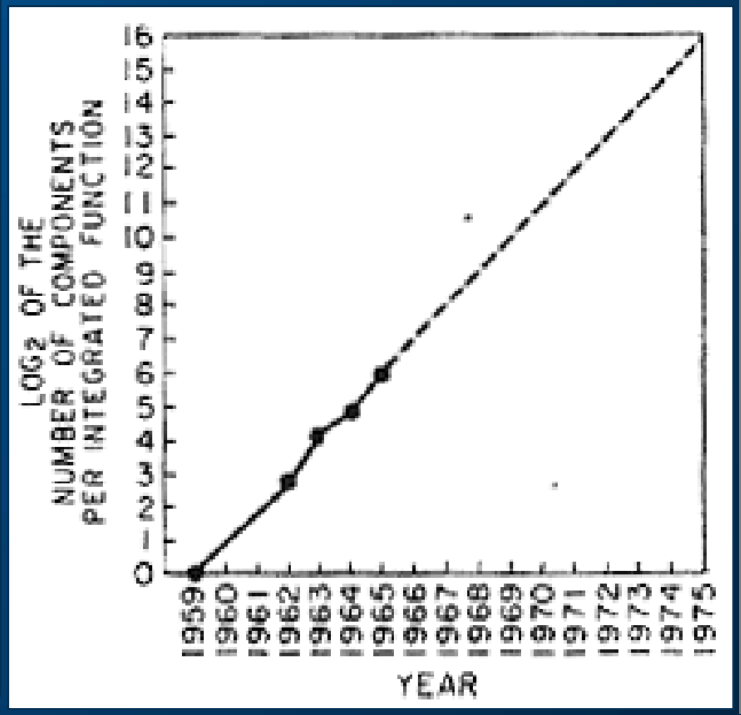
Opportunities for Future Products

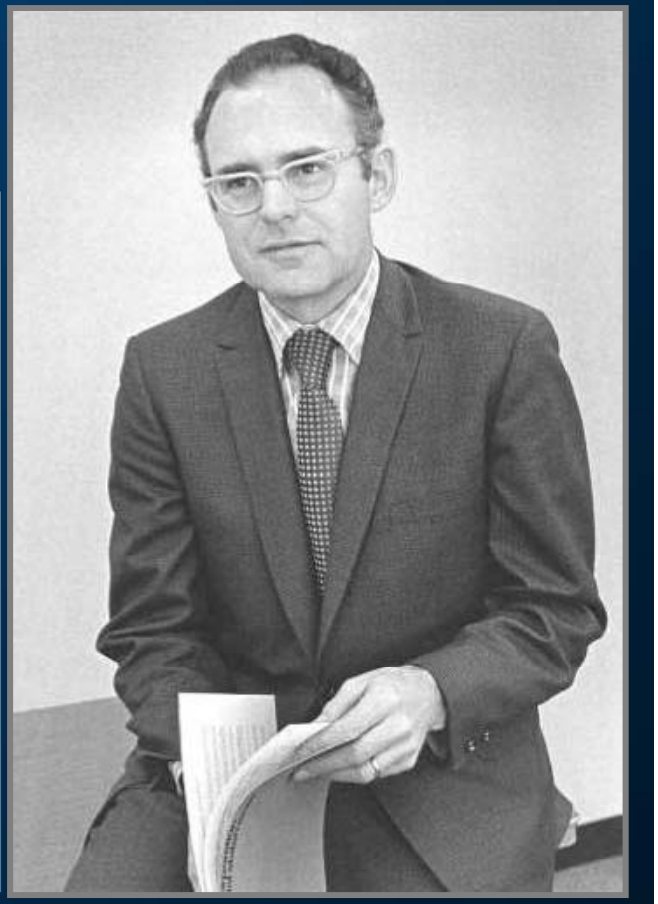
Visible Horizon and Beyond

Moore's Law - 1965

"**<u>Reduced cost</u>** is one of the big attractions of integrated electronics, and the cost advantage continues to increase as the technology evolves toward the production of larger and larger circuit functions on a single semiconductor substrate."

Electronics, Volume 38, Number 8, April 19, 1965

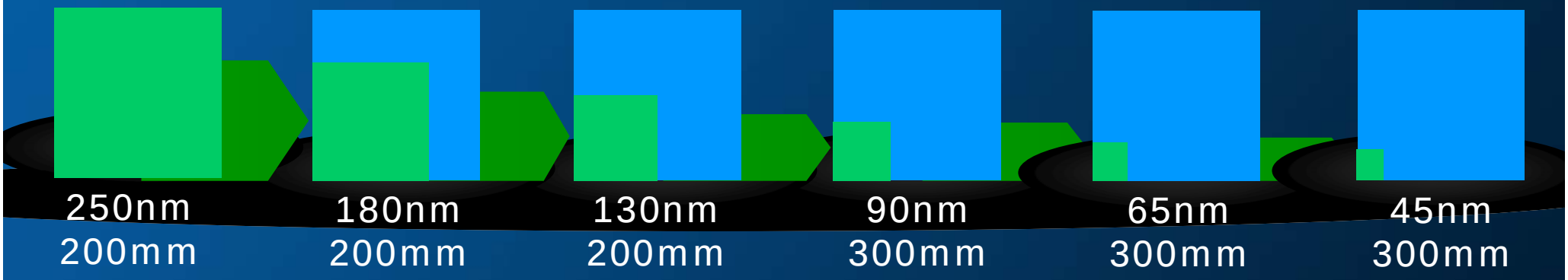




Integrated circuits = Parallel fabrication

Parallel fabrication = Lower cost per function

Enabling Innovation and Cost Reductions



Same circuitry half the space (cost reduction)

OR

Twice the circuitry in the same space (architectural innovation)

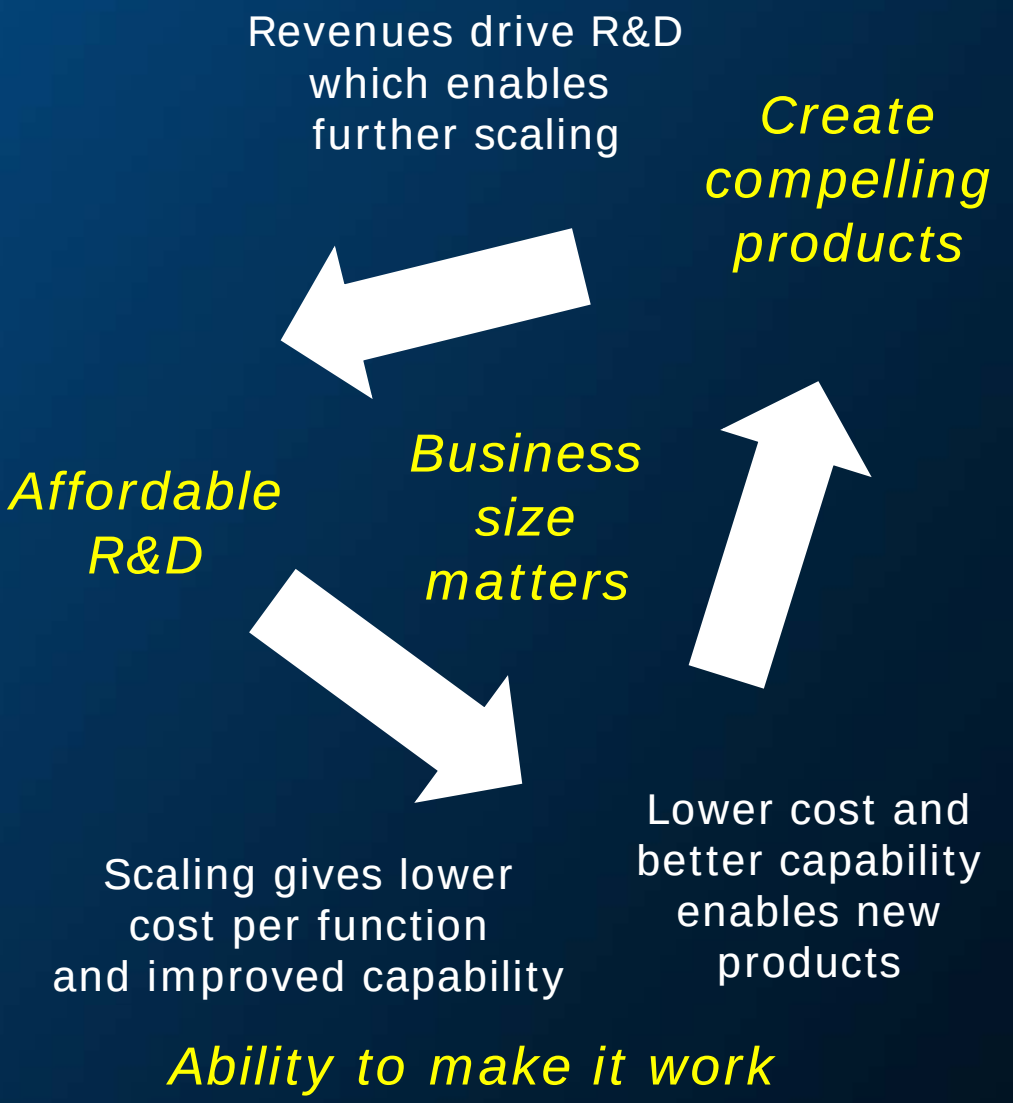
=

Option to design for optimal performance/cost

Source: Intel

Key Economics: Scaling is Better under almost all circumstances

- If you can scale then you should
  - Compelling products command higher prices
  - Leading technology delivers lower costs
  - Enables necessary investment in R&D
- If you can't scale then hope your competitors can't either



Economics, Technology, & Innovation

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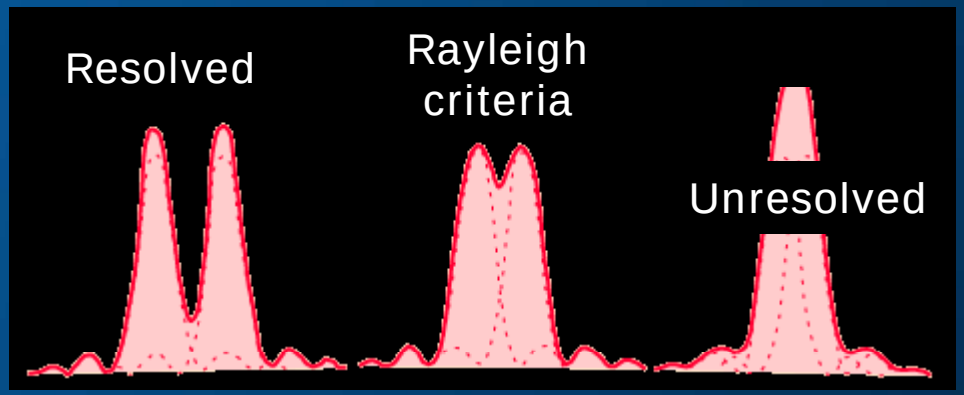
Technologies on Deck

Opportunities for Future Products

Visible Horizon and Beyond

"We're limited by the wavelength of light"

Feature >> Wavelength



Feature << Wavelength

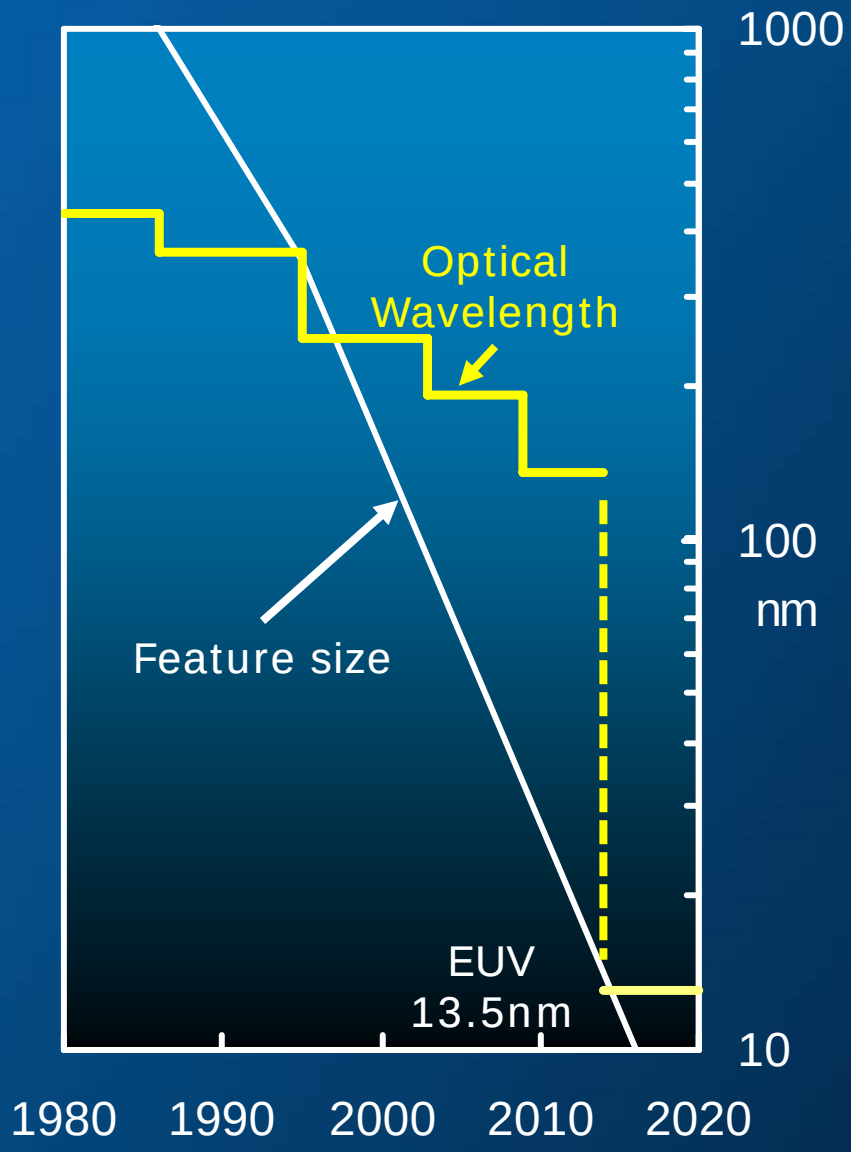
Feature = 0.6 x Wavelength / numerical aperture

In the limit, microscope objectives with 0.95 N.A. are available and, provided very small fields (200μ x 200μ) are adequate, linewidths < 0.4μ should be achievable under carefully controlled laboratory conditions, and in very thin resist layers.

Depth of field will be reduced to about ± 0.2μ. Deep U.V. (λ = 200nm - 260nm) lenses will be difficult to build because of the lack of materials that are transparent at these wavelengths and yet have relatively high refractive indices.

Lithography Scaling Limitations
From Broers [1] IEDM Plenary Session 1980

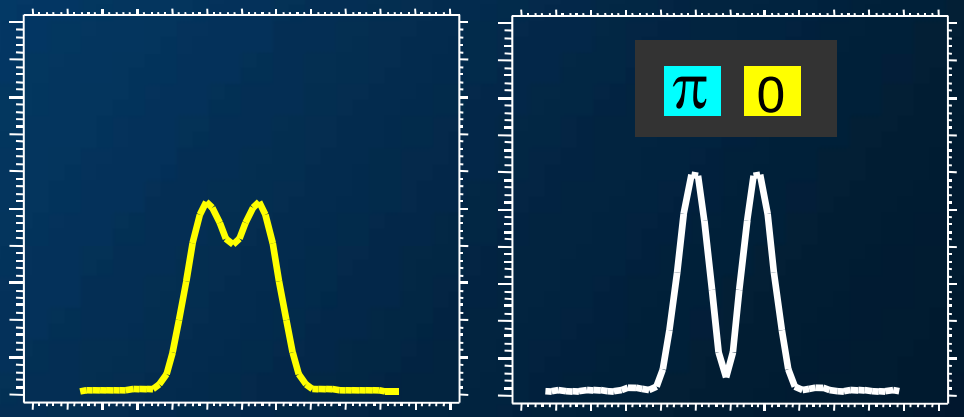
Breaking through the Wall



New lens materials enabled shorter wavelengths

365nm in mid 80s
193nm immersion (145nm eqv) today

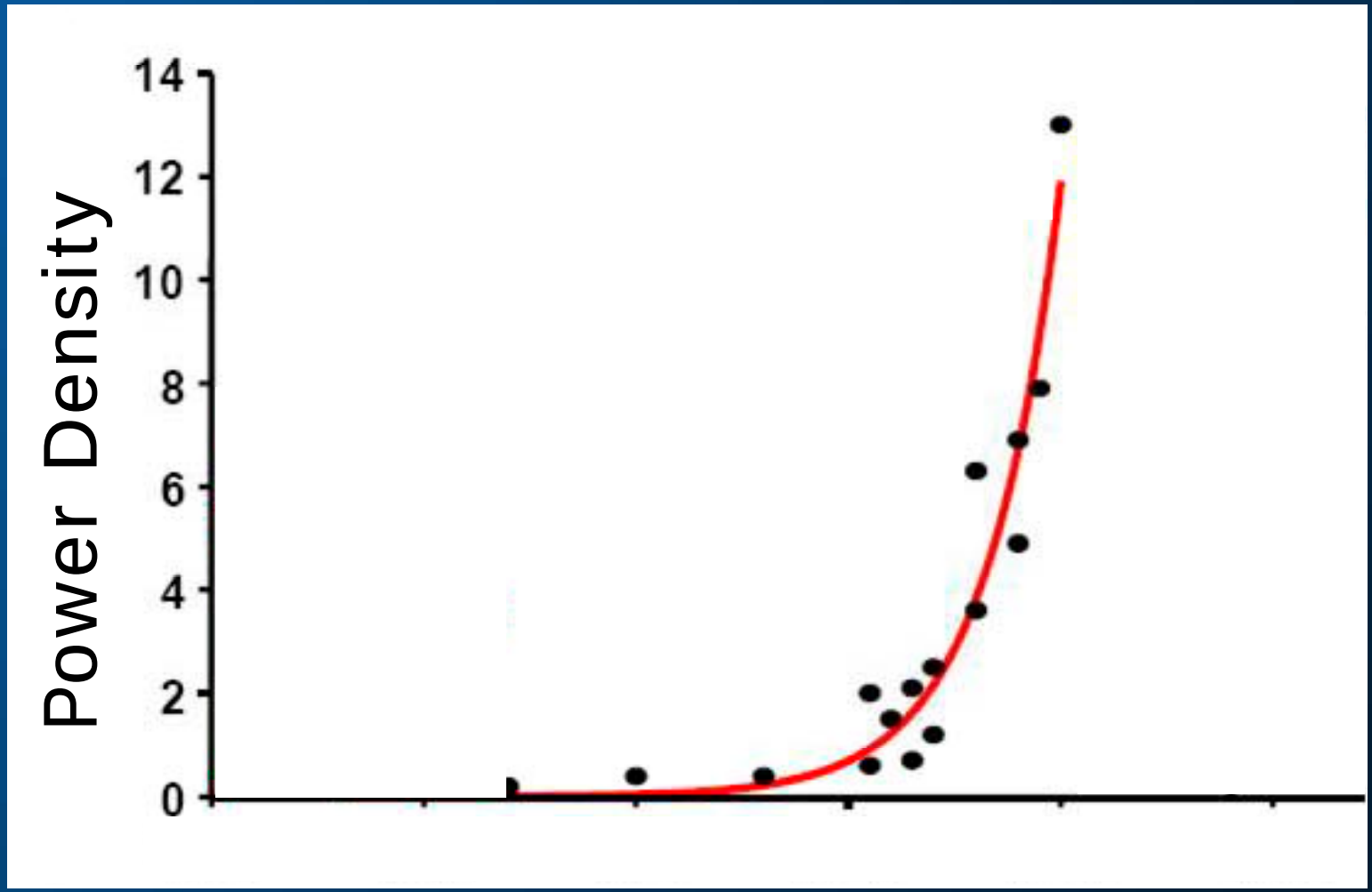
New mask techniques enabled smaller features



Conventional Mask Structure

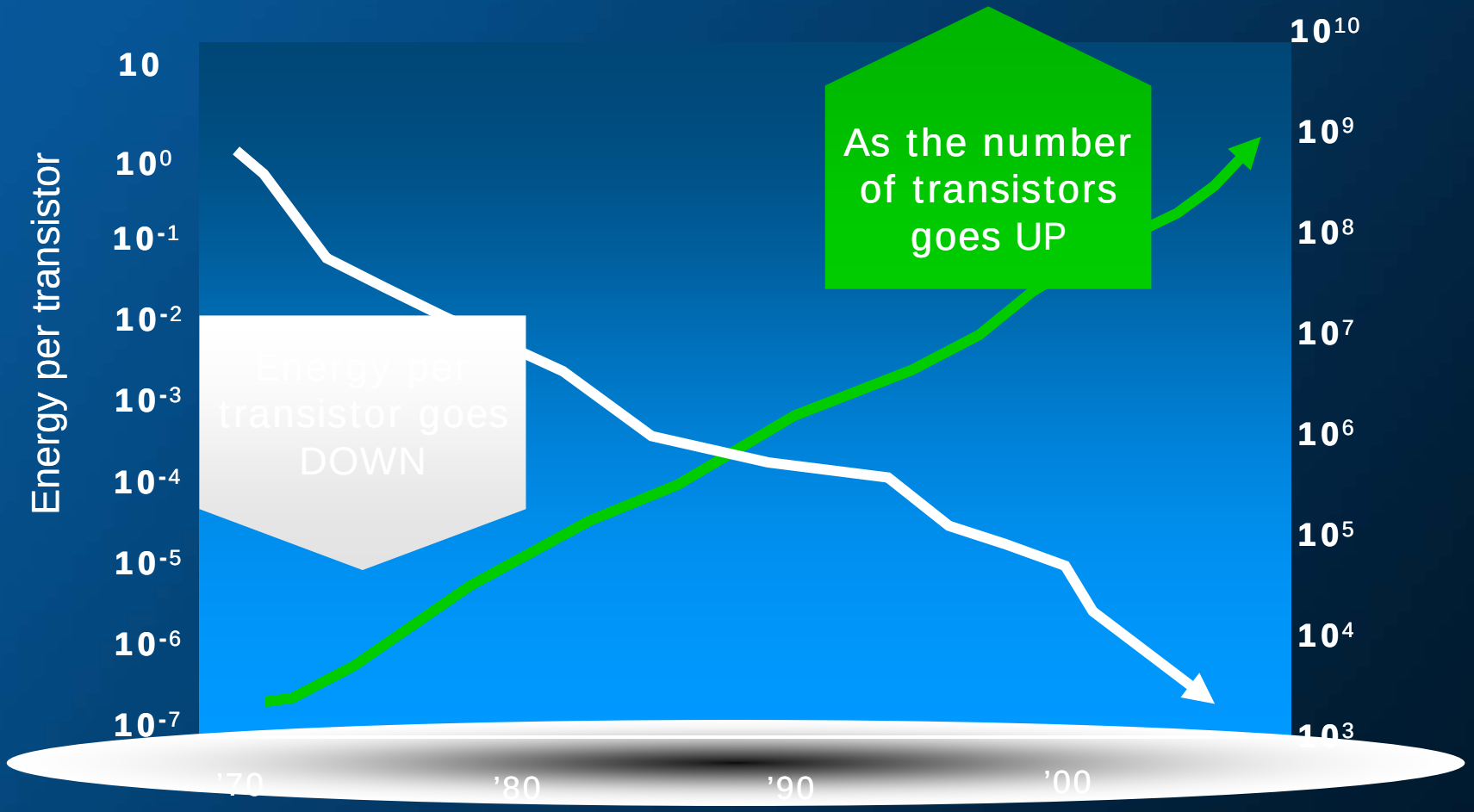
Alternate Phase Shift

"We're hitting the power wall"



Source: IBM 2004

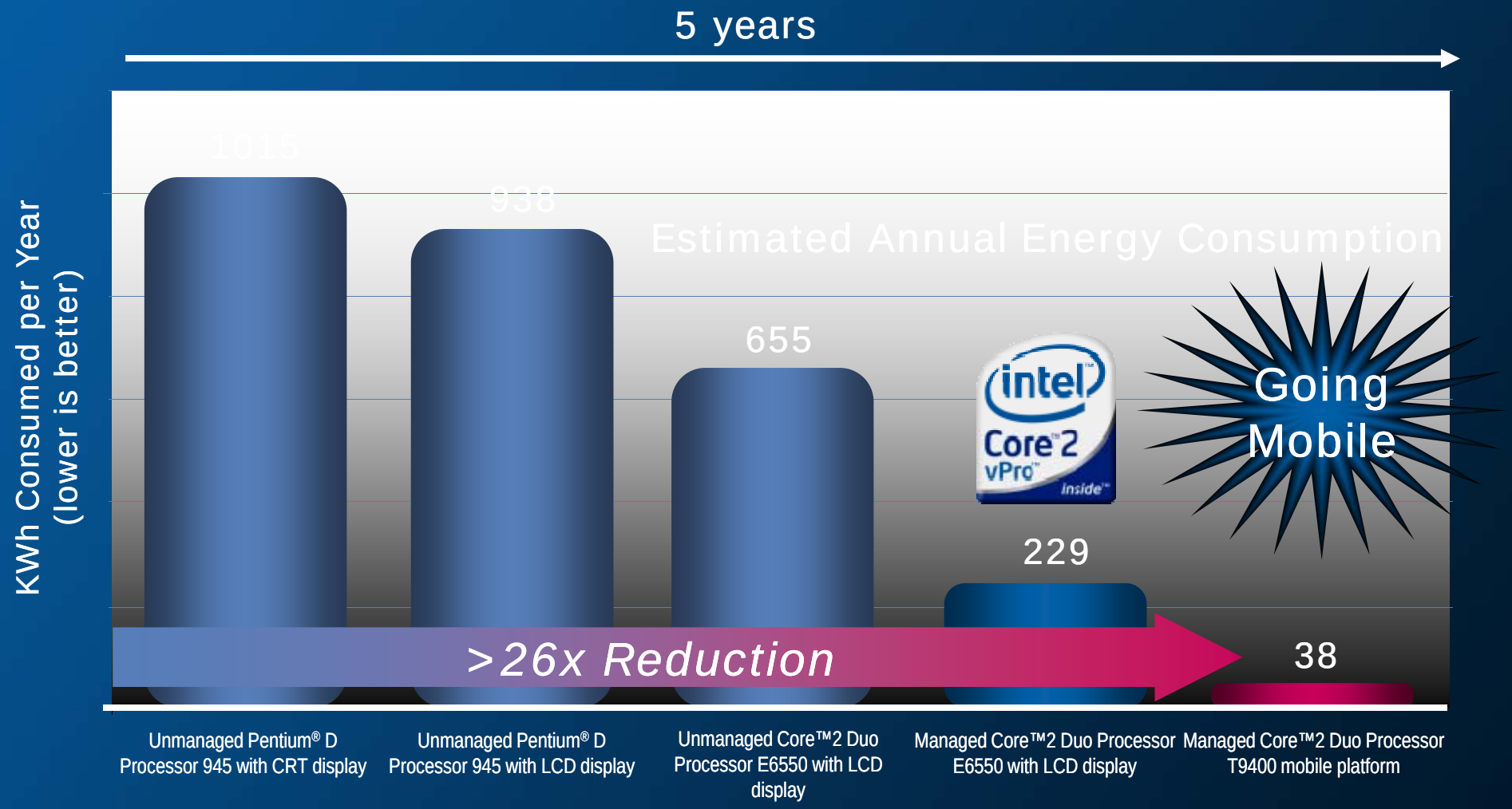
Energy per Transistor Continues to Drop



Source: WSTS/Dataquest/Intel

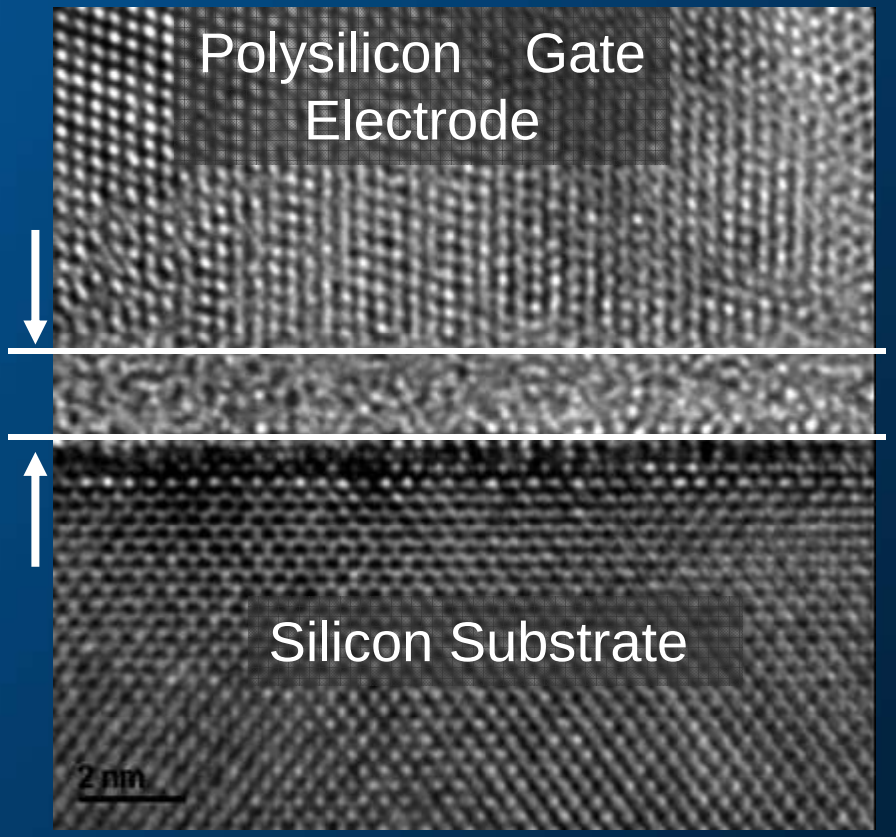
~ 1 Million Factor Reduction In Energy/Transistor Over 30+ Years

Energy Consumption is about System Optimization

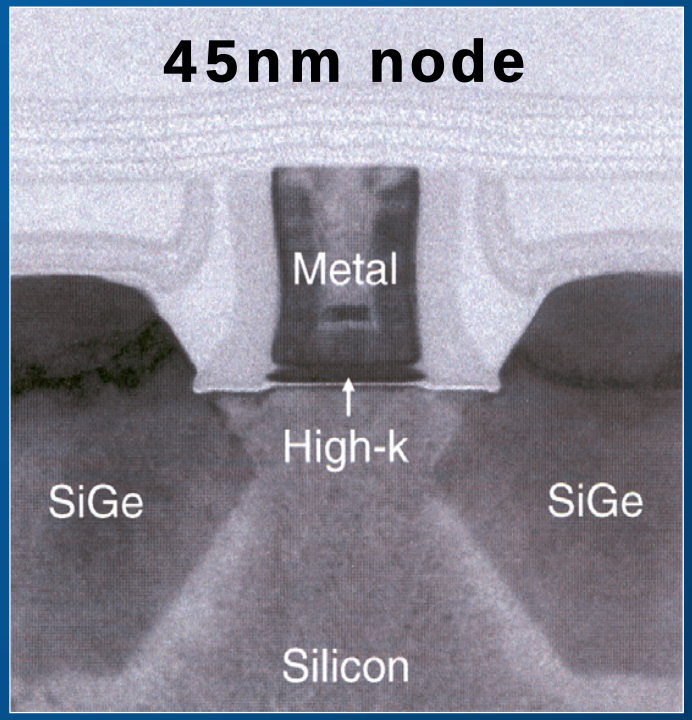


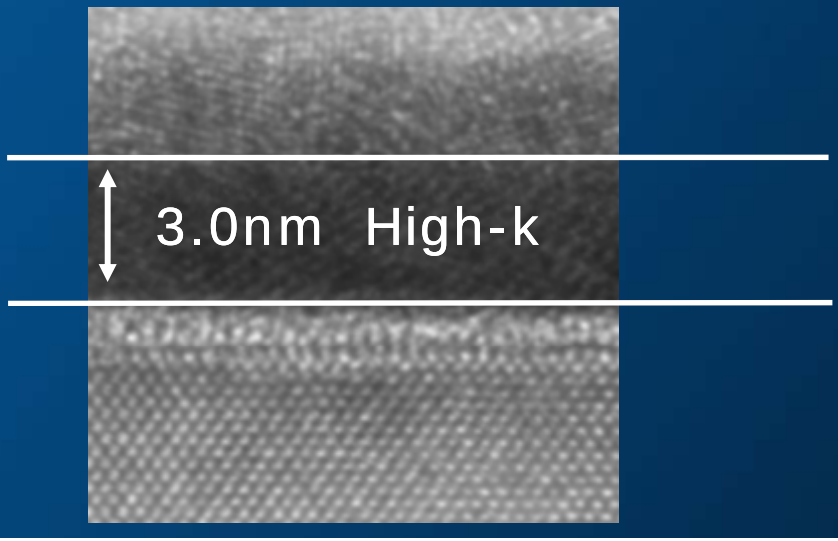
Energy savings comes from combination of transistor scaling and architectural innovations

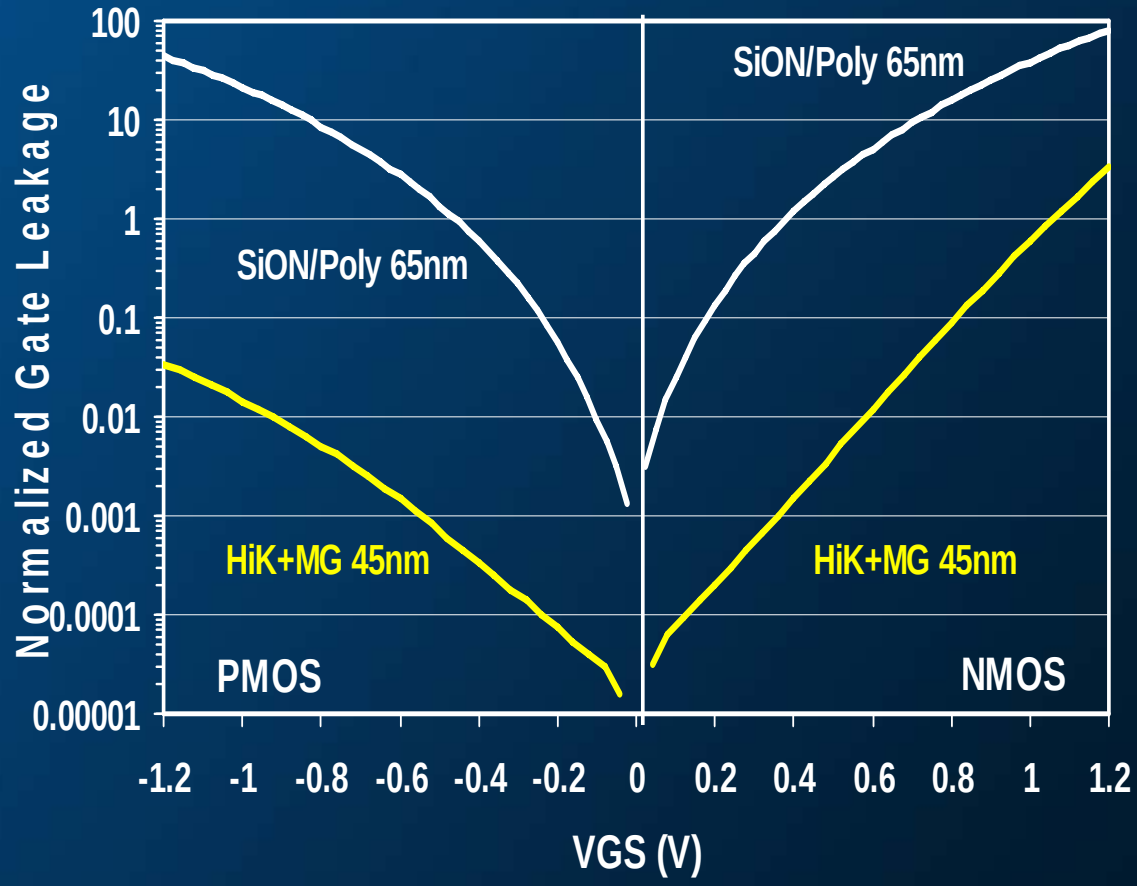
“We’re running out of atoms”



New Materials and New Fabrication







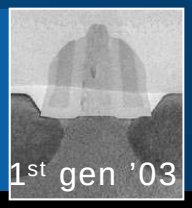
45 nm HK+MG provides >25x gate leakage reduction

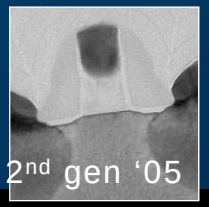
The Timing of Research Is Not Always Predictable But a Commitment to Research is Required

1999 2001 2003 2005 2007

Strained Silicon

Development '01- '02

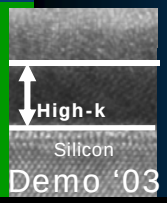




High-k Metal Gate

Materials selected 2000

Metal gates research 2001



Development '05- '06

Intel 45nm High-k Metal Gate

Ten Years, Millions of Hours

Dead Ends, Failures

Unwavering Focus

Source: Intel

Meanwhile despite these worries Innovations continued on product side

- Personal computing replacing shared computers
- Portable computing
- Connected computers, sharing data, Internet
- Wireless connectivity
- Smaller form factors, pocket computers
- Special purpose devices

...





Economics, Technology, & Innovation

"No exponential is forever … but we can delay 'forever'."

Technologies on Deck

Opportunities for Future Products

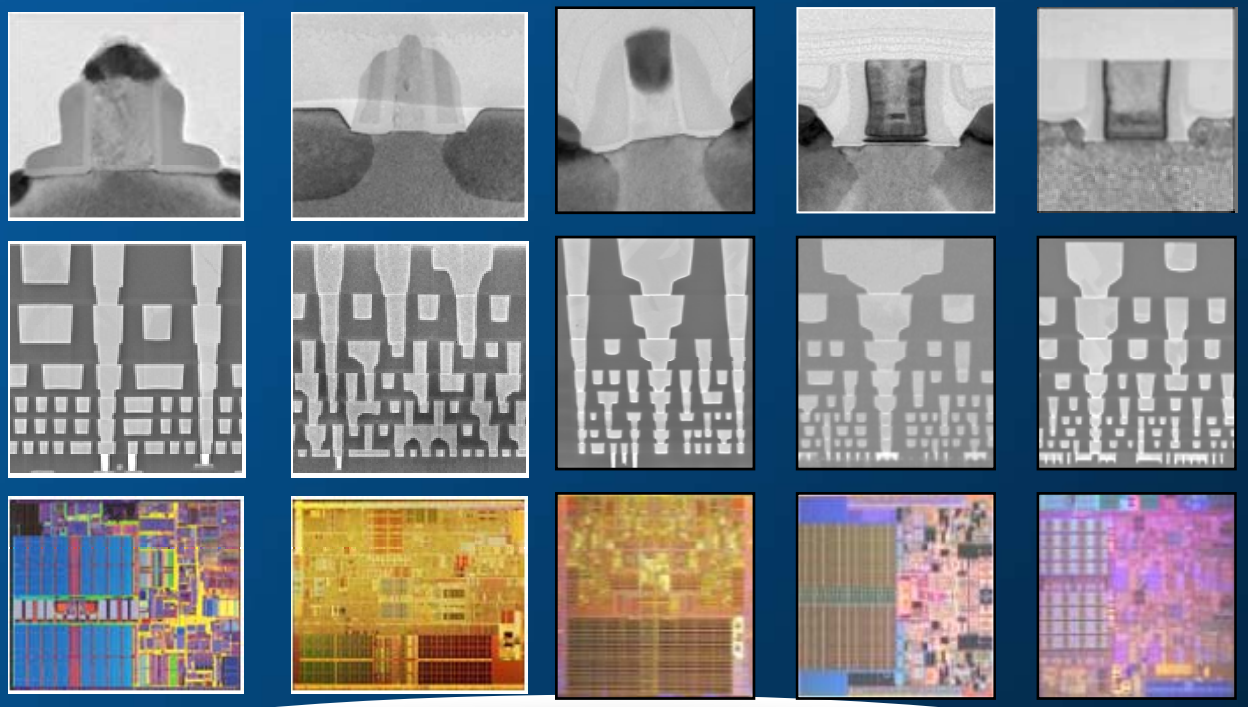
Visible Horizon and Beyond

Steady Technology Cadence

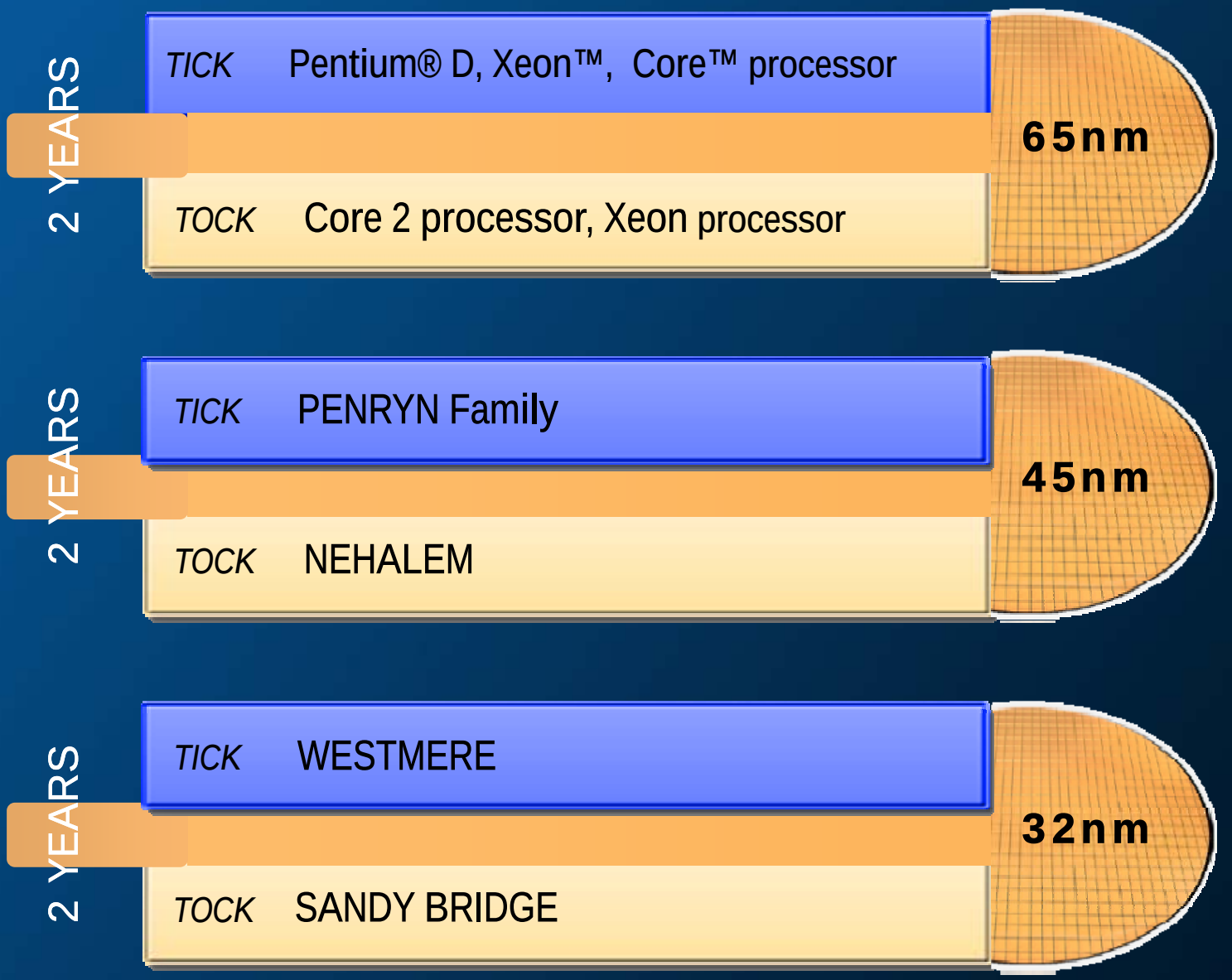
TECHNOLOGY GENERATION

130nm	90nm	65nm	45nm	32nm
2001	2003	2005	2007	2009

MANUFACTURING



Product Cadence for Sustained Leadership



All product information and dates are preliminary and subject to change without notice

So What ?

Generational benefits
don’t just add,

they multiply

Energy Efficiency Improvement

(Same Performance Footprint)

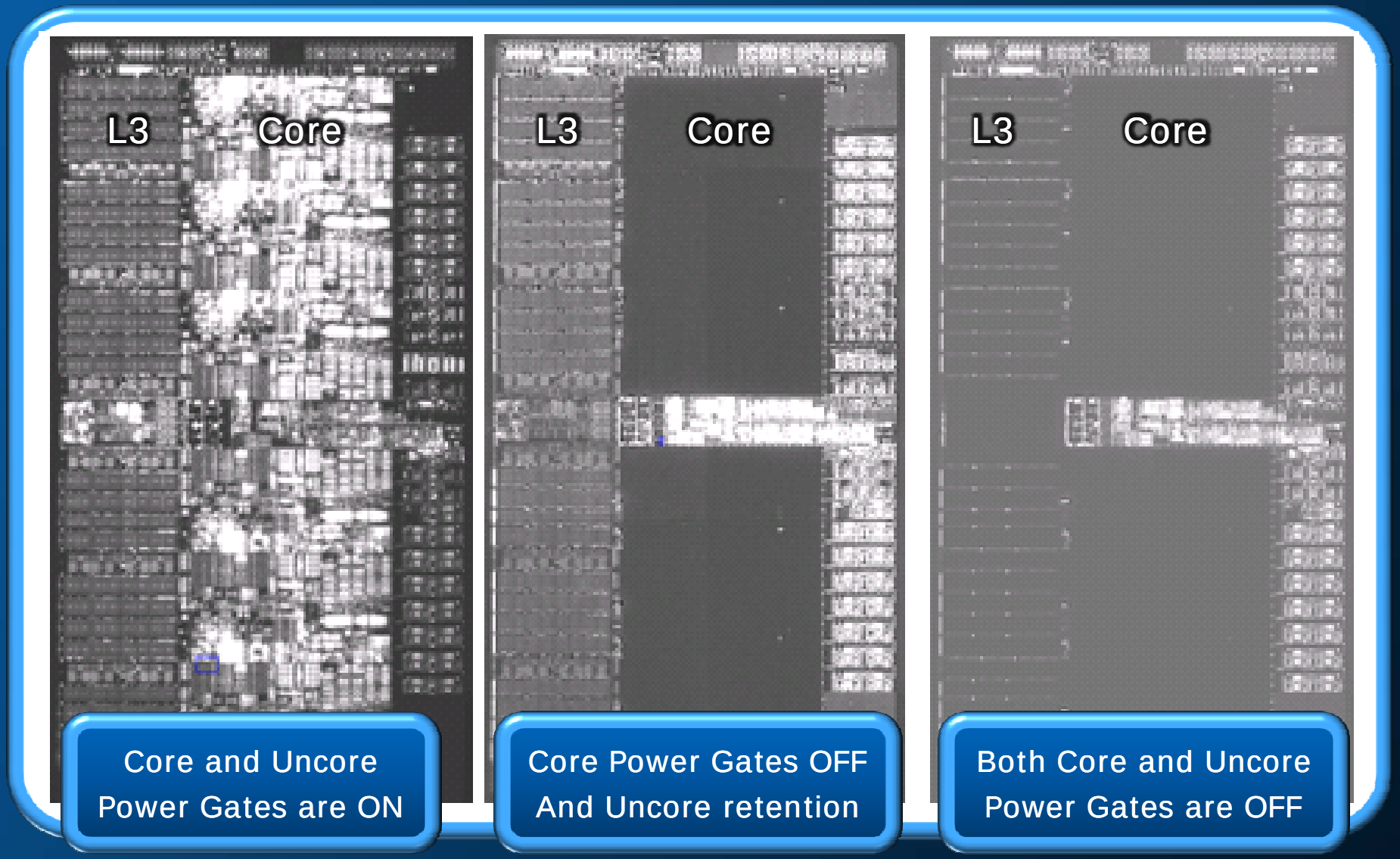
2005 — 184 single core servers

2009 — 21 Intel® Xeon® 5500 based servers

Up to	Up to	Annual Energy Costs
8 month	9X	92%
Return on Investment	Server Reduction	Estimated Reduction

Source: Intel estimates as of Nov 2008. Performance comparison using SPECjbb2005 bops (business operations per second). Results have been estimated based on internal Intel analysis and are provided for informational purposes only. Any difference in system hardware or software design or configuration may affect actual performance. For detailed calculations, configurations and assumptions refer to the legal information slide in backup.

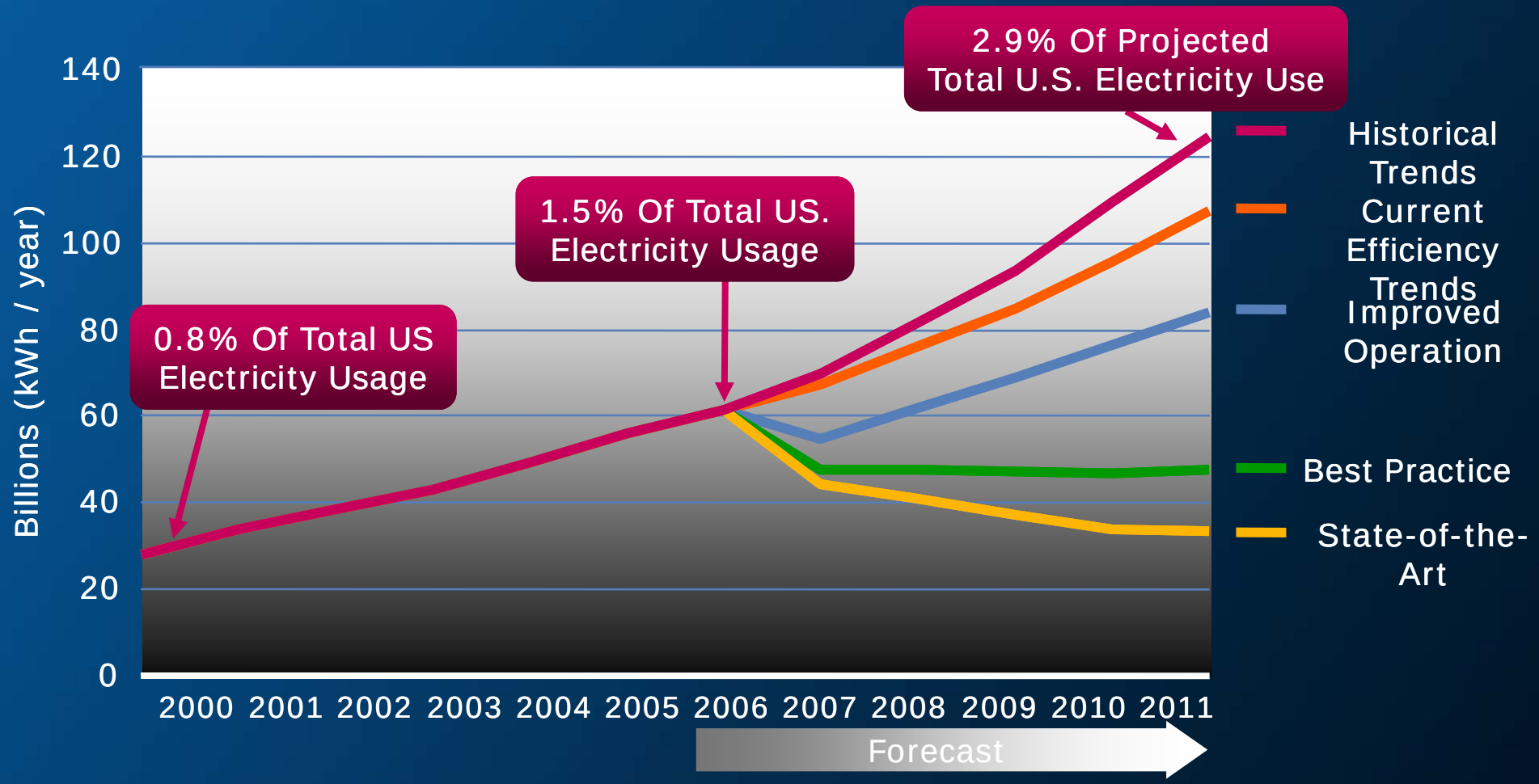
New Fabrication enables New Product Opportunities



Westmere 6 cores, Infrared imaging showing advanced power management

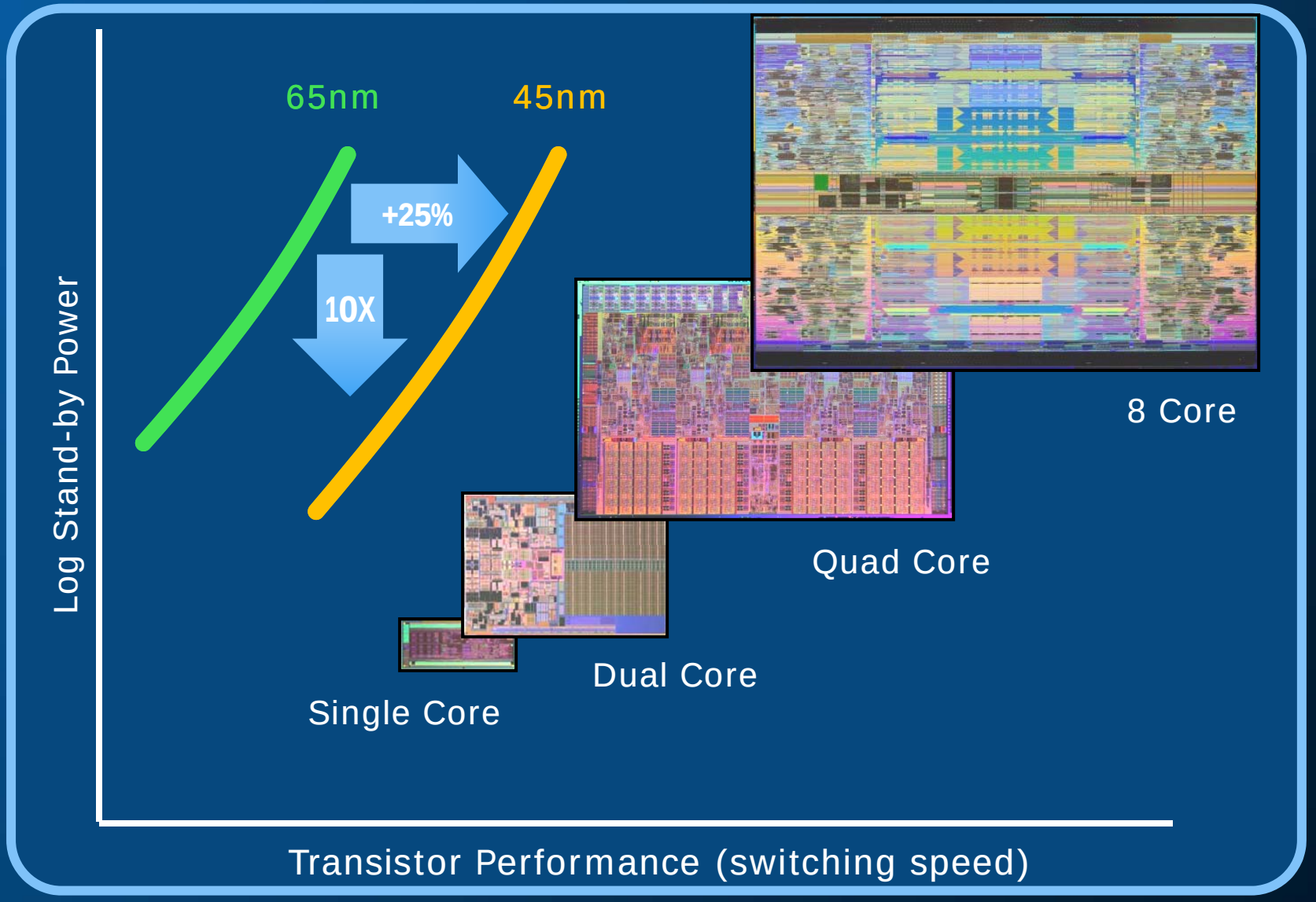
The Opportunity for Data Center Efficiency

Projected Data Center Energy Use Under Five Scenarios



Source: EPA Report to Congress on Server and Data Center Energy Efficiency; August 2, 2007

Technology Advances Enable <u>Both</u> Better Products and a Wider Range



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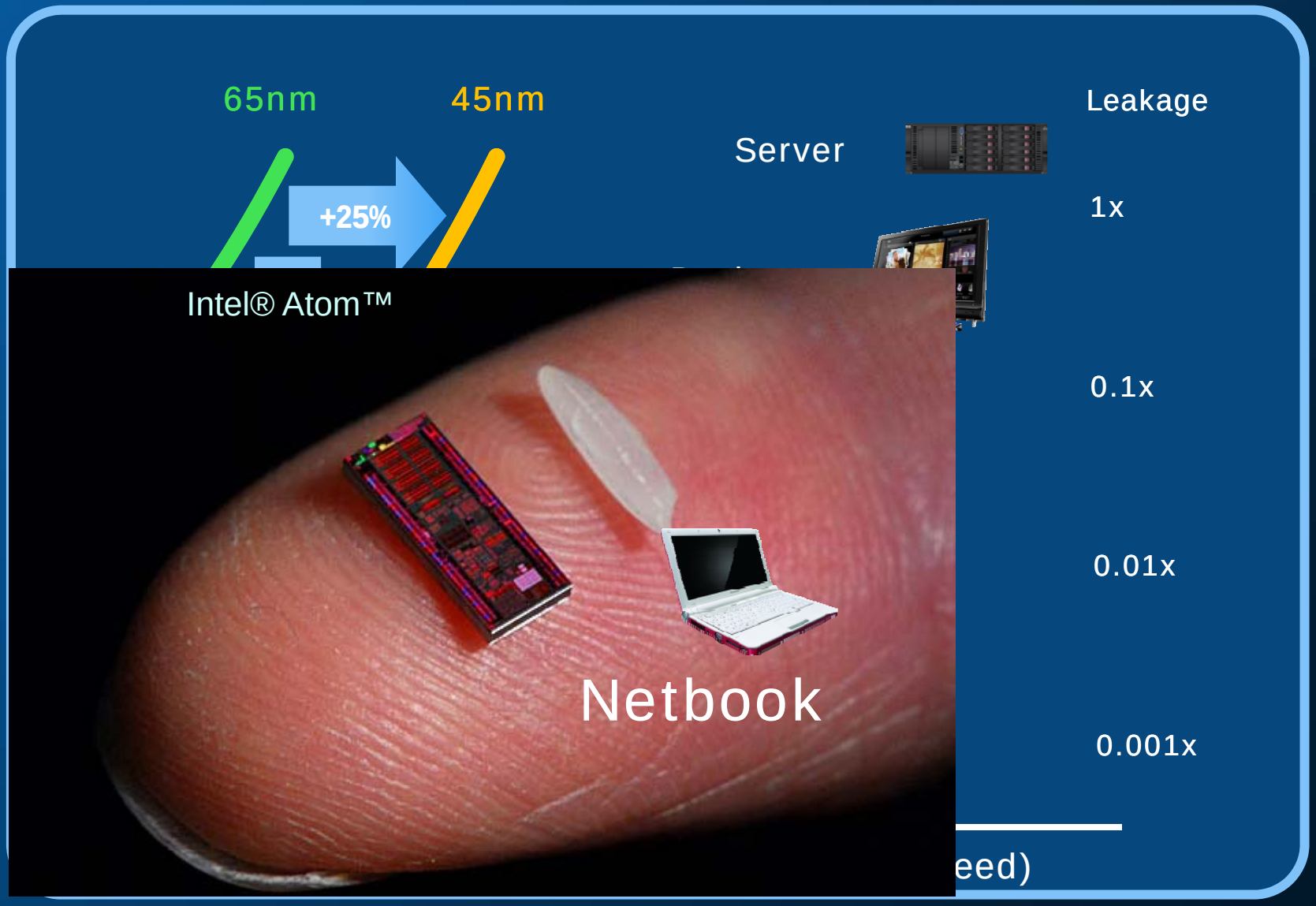
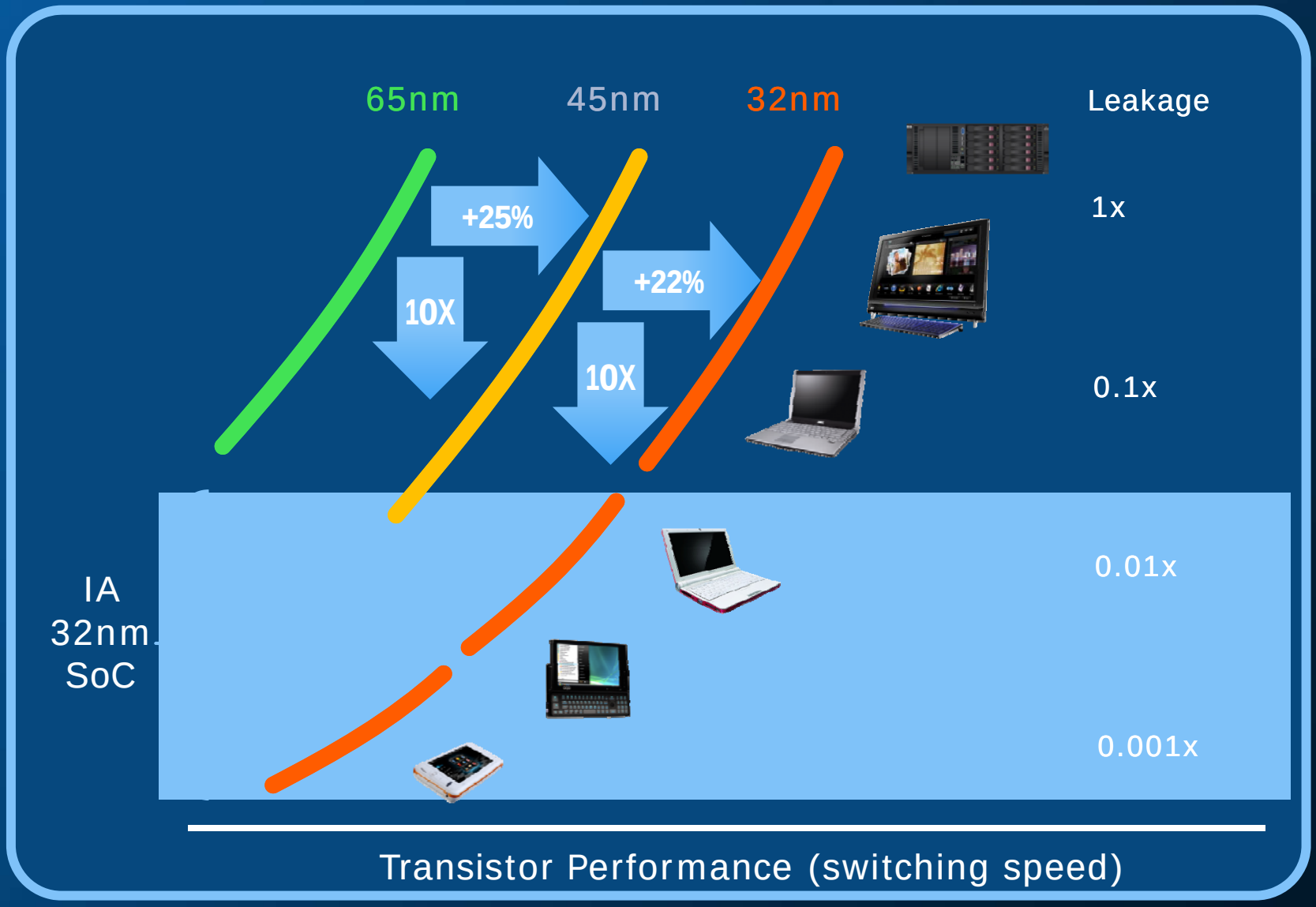
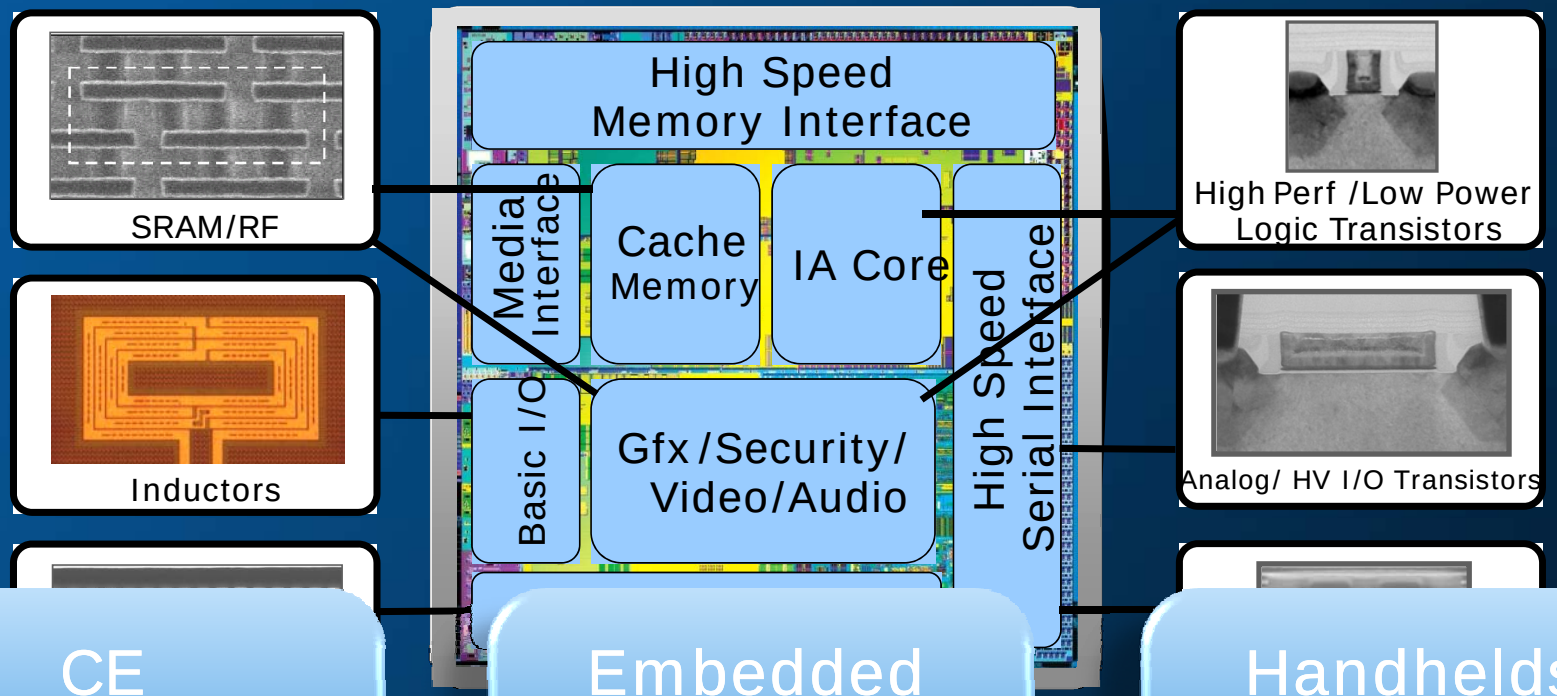


Extending Transistor Advantage to SoC's

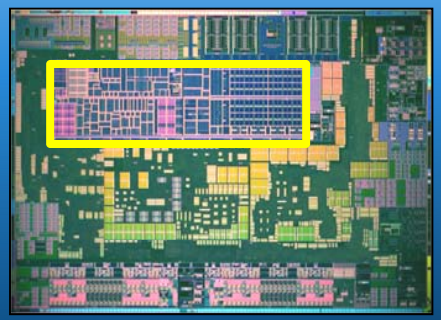
Faster Transistors and Better Power Performance



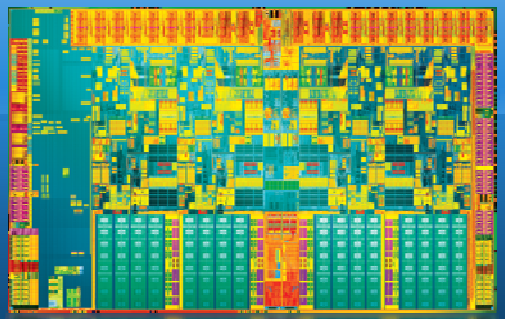
Implementing a Platform on a Chip



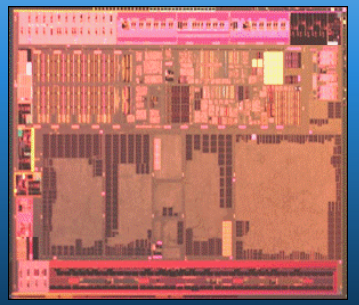
CE
Sodaville



Embedded
Jasper Forest



Handhelds
Lincroft



Economics, Technology, & Innovation

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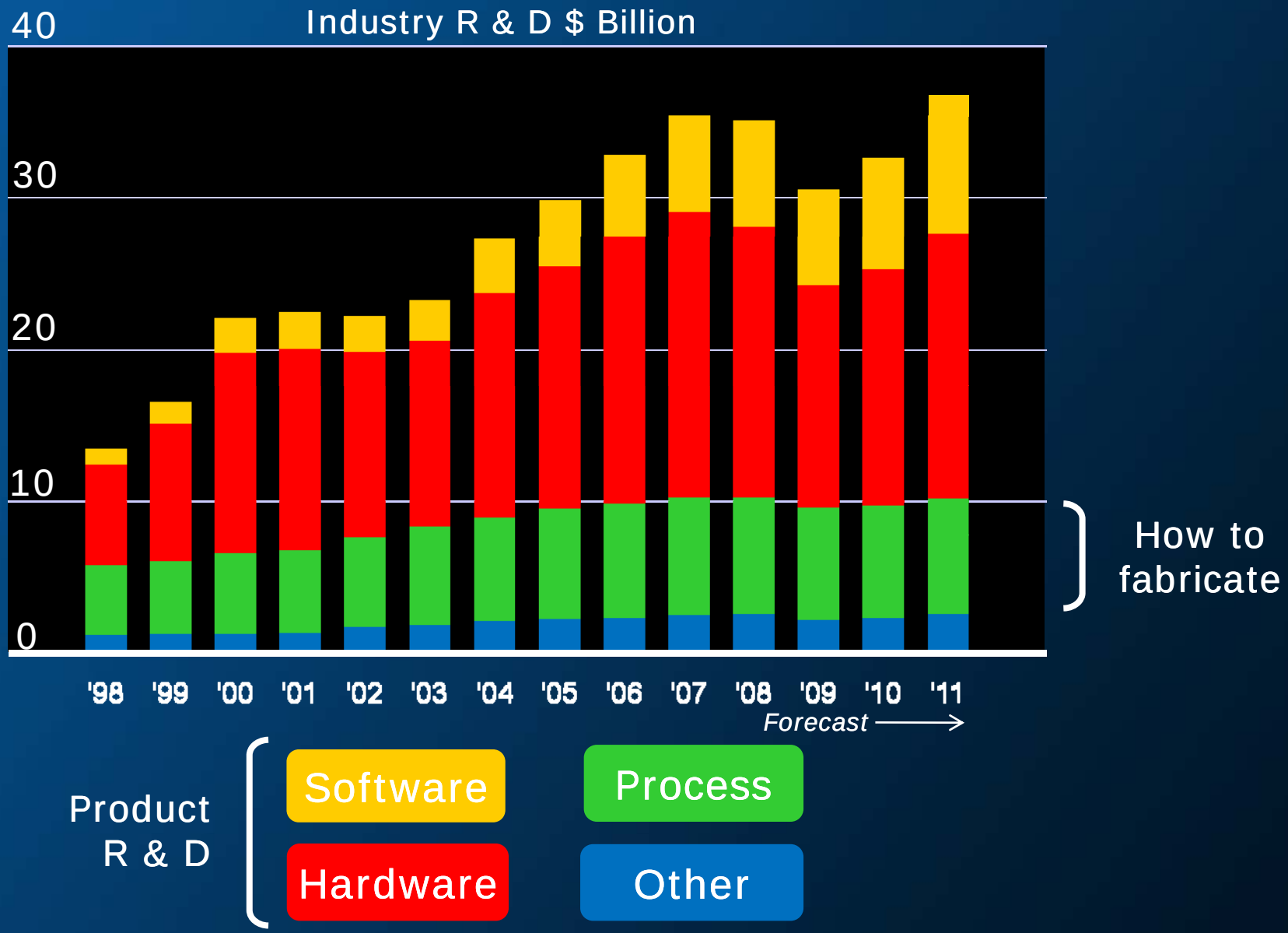
Technologies on Deck

Opportunities for Future Products

Visible Horizon and Beyond

Industry R & D is Increasing –
in dollars and as a percent of revenues



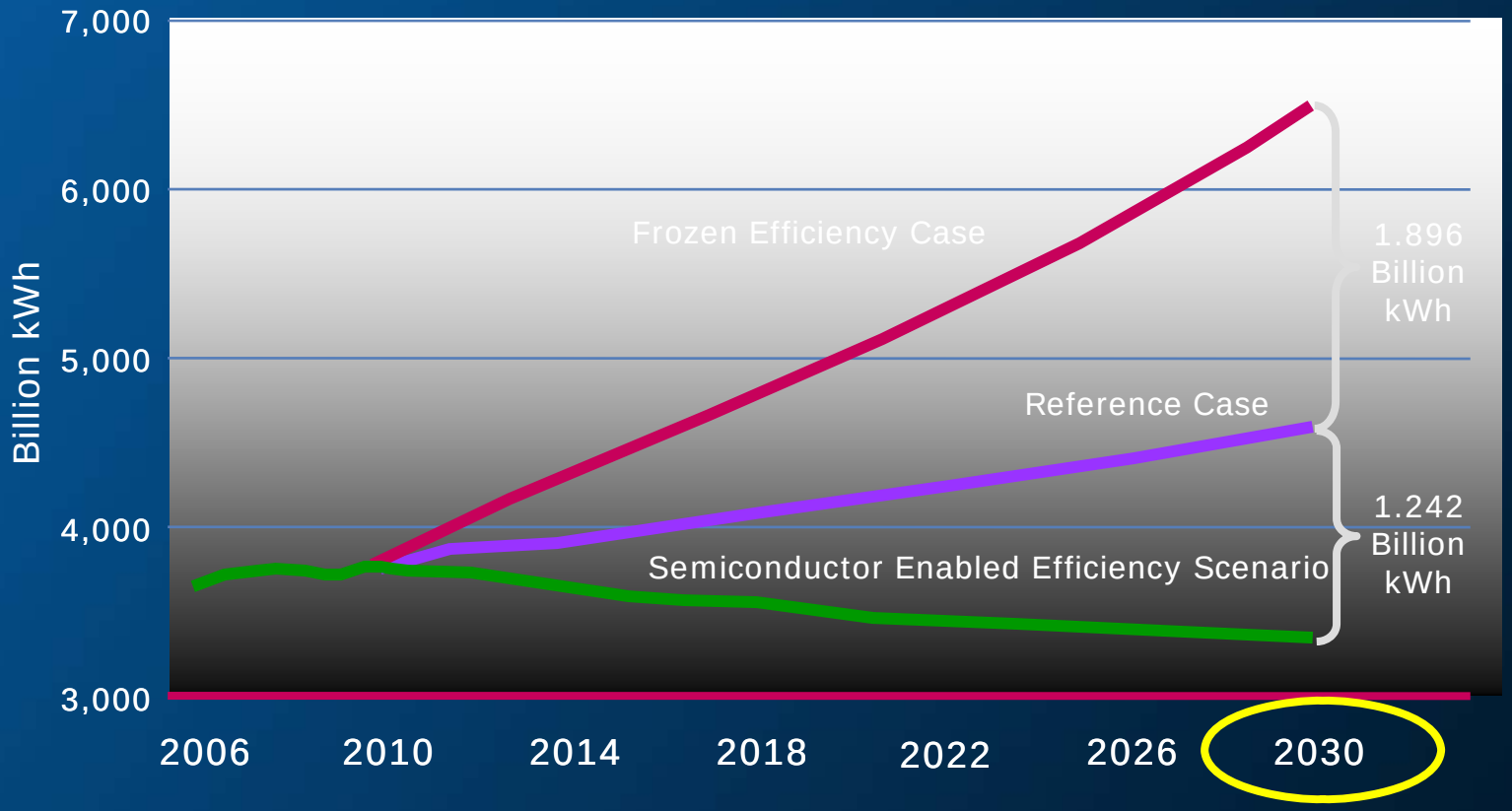
Source: IBS, Intel

Possible Product Possibilities

- Cloud computing
  - Solving grand challenge problems
  - Enable access anytime anywhere
- Life-like computing
  - Immersive experiences
  - Context aware
- Heterogenous networks
  - Computing in network
  - Integration with bio and sensors

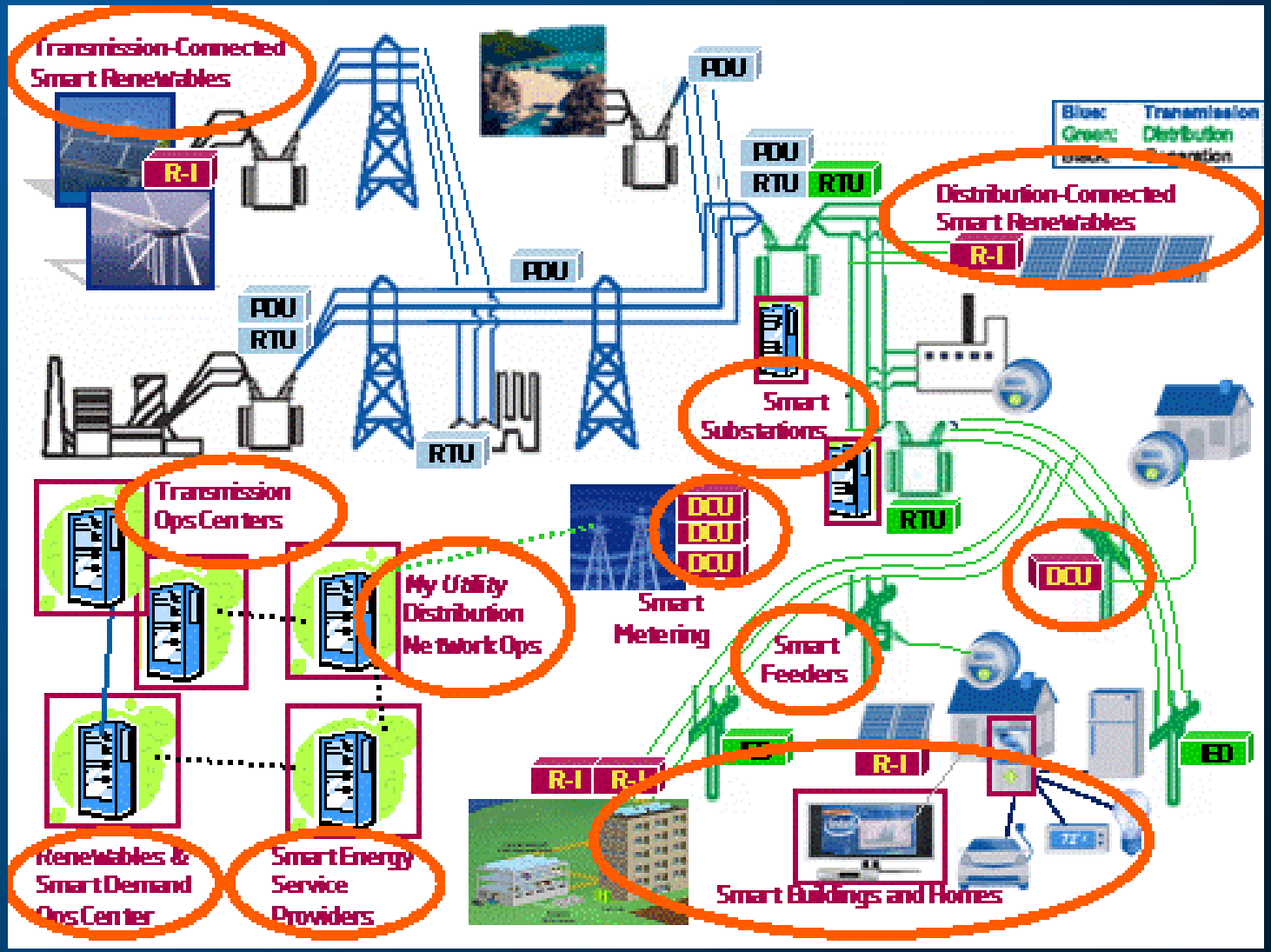
Potential Energy Savings Outside of Information and Communications Technology

Figure ES-1. Future Electricity Scenarios for the U.S.

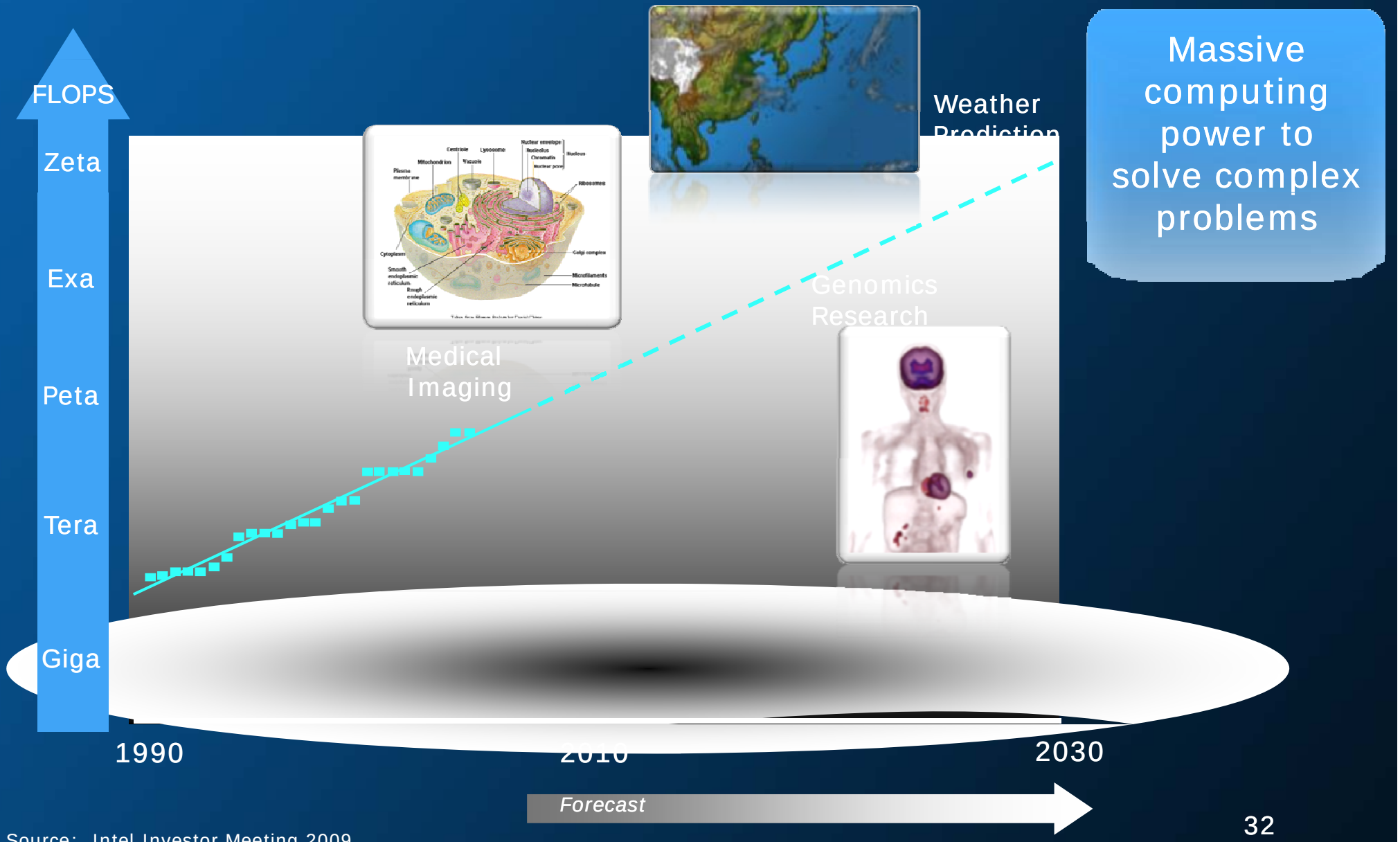


Source: ACEEE Report Number E094, May 2009
Semiconductor Technologies: The Potential to Revolutionize U.S. Energy Productivity

A truly Smart Grid Requires that Microprocessor intelligence be added throughout the network



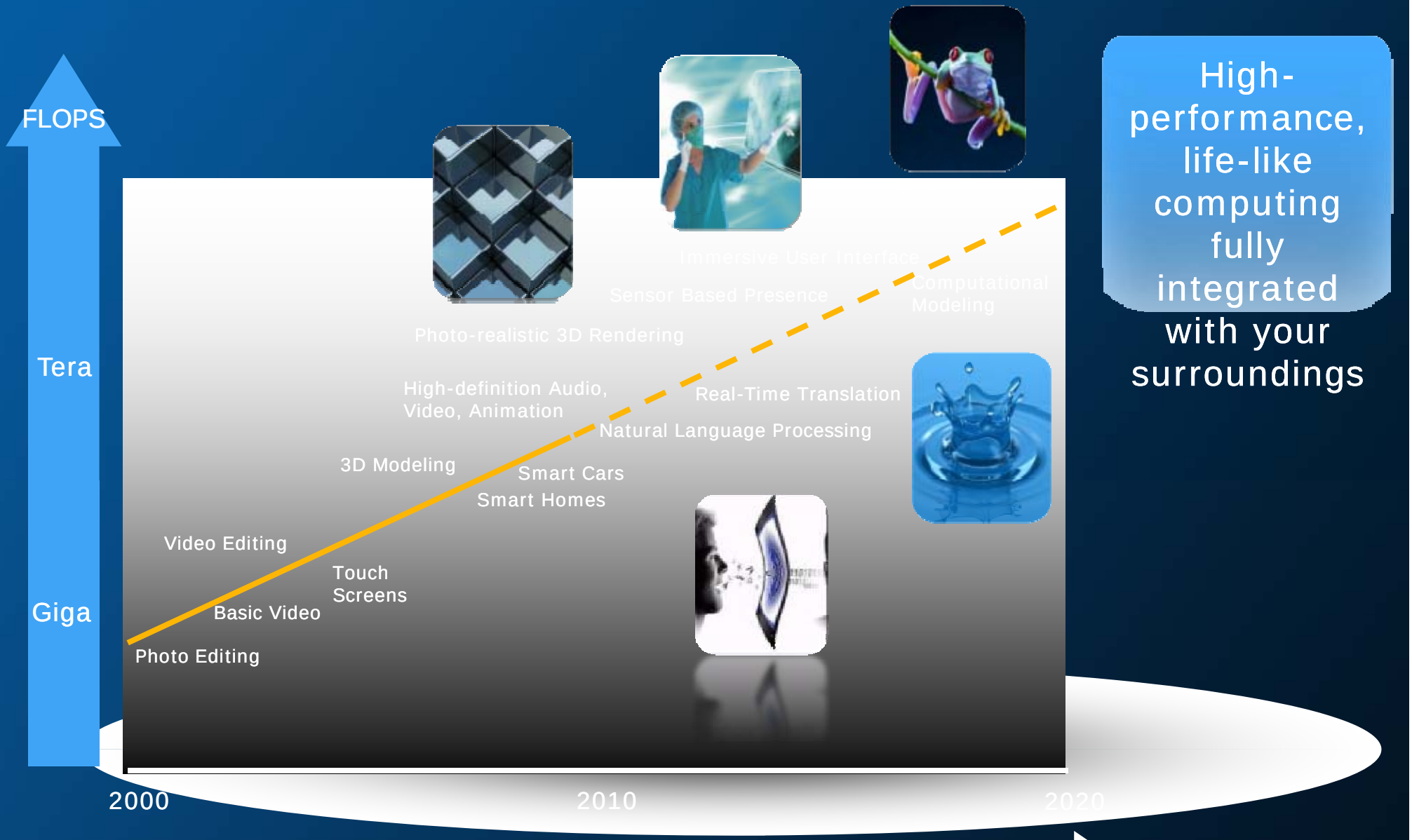
High Performance Computing Segment Needs Decades of Performance Increases



Massive computing power to solve complex problems

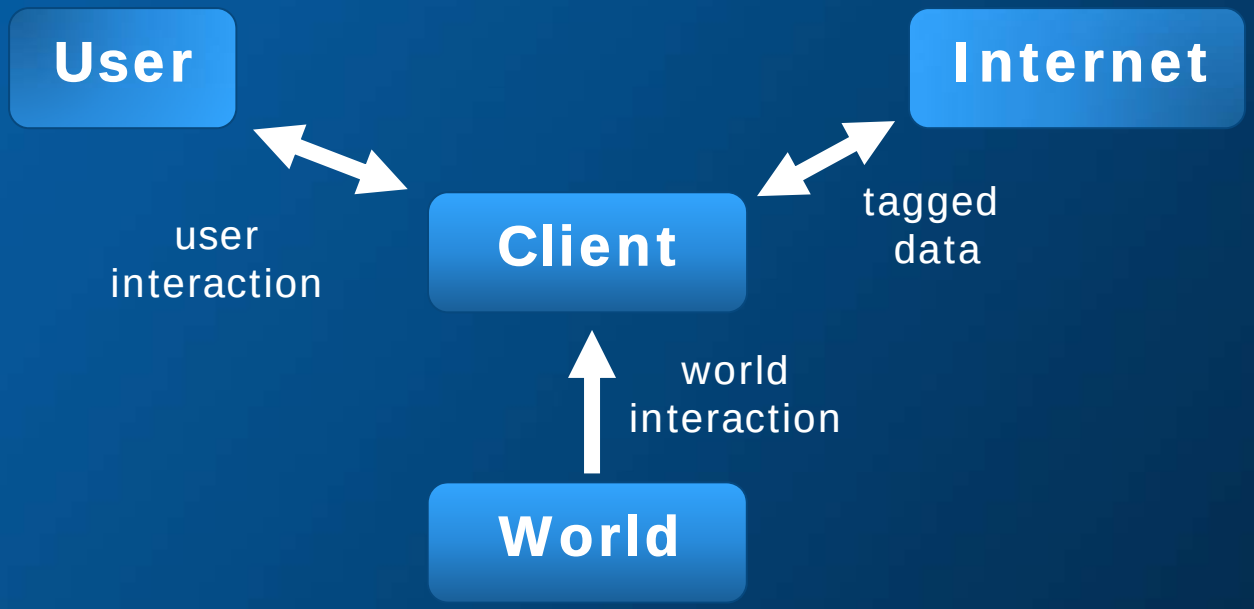
Source: Intel Investor Meeting 2009

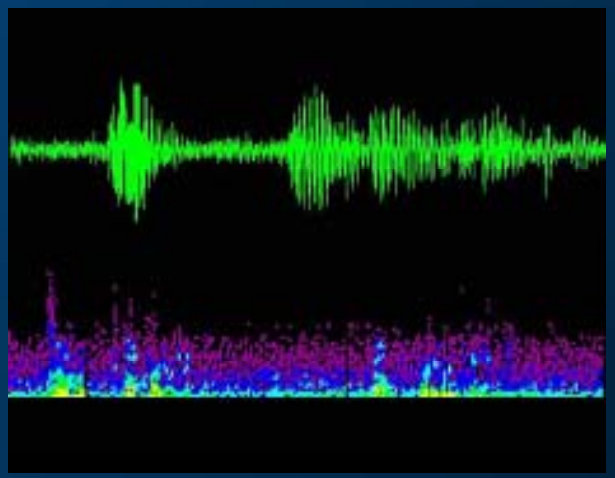
Core Computing Segment Will Need to Increase Performance to Support New Usages



Source: Intel Investor Meeting 2009

Perceiving the User to Make Interfaces Better





Small Computing Segment Needs
More and More Performance At Low Power

Real-time, 3D-Video
Augmented Reality

Anytime, anywhere, personalized, context-aware, environmental computing

FLOPS

Giga

Mega

Visual Search - Still Recognition

High-definition Audio, Video & Animation

Real-Time Language Translation

Natural Language Processing

Video Presence

Mobile TV
Video
Gaming
Camera
Touch screens
Web Browser
MMX
Music & Radio
E-mail
SMS
Voice

1995

2010

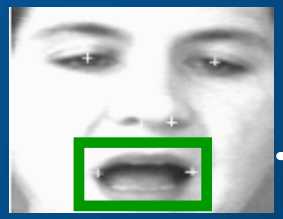
2025

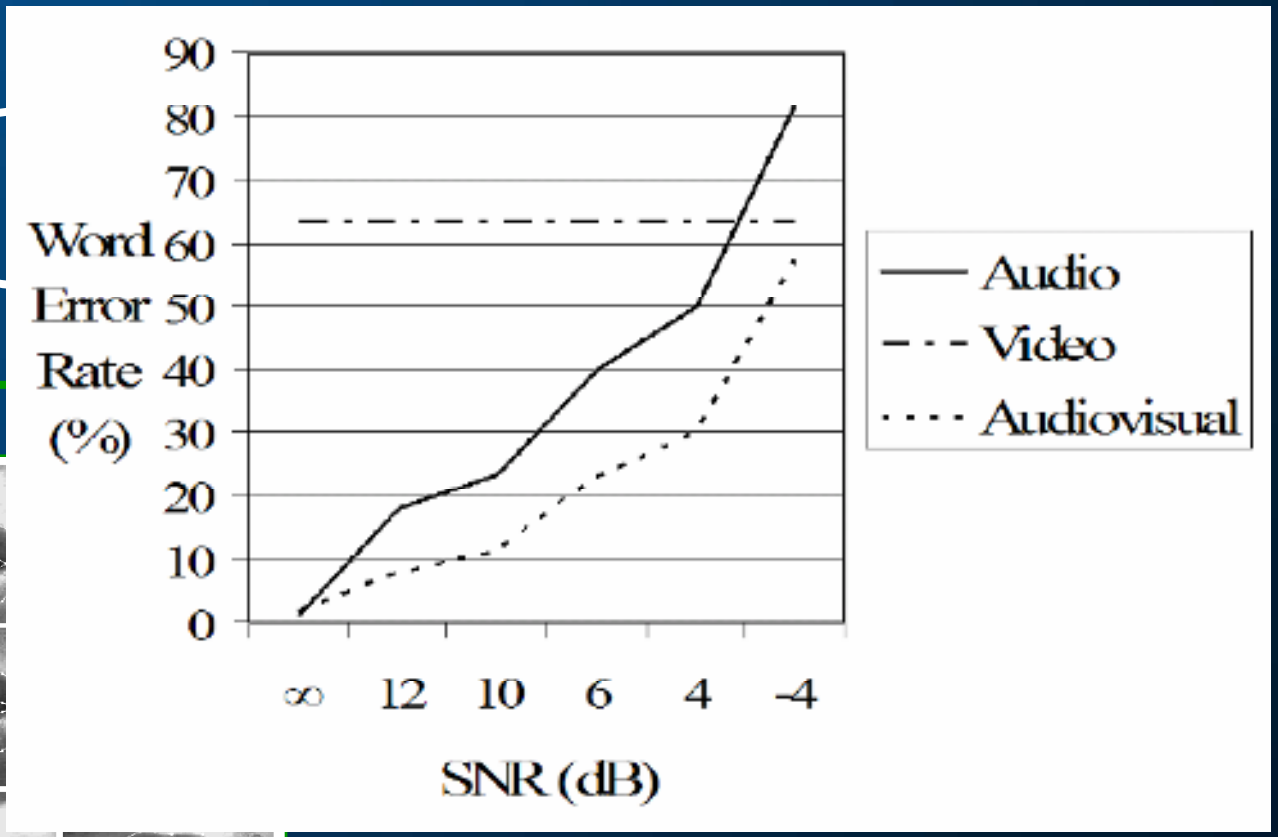
Forecast

Source: Intel Investor Meeting 2009

Speech Interfaces made Better with Audio-Visual Fusion

Speech recognition works, but
fails in noisy environments (mobile)





Source: Silsbee & Bovik, IEEE Speech & Audio

Economics, Technology, & Innovation

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Technologies on Deck

Opportunities for Future Products

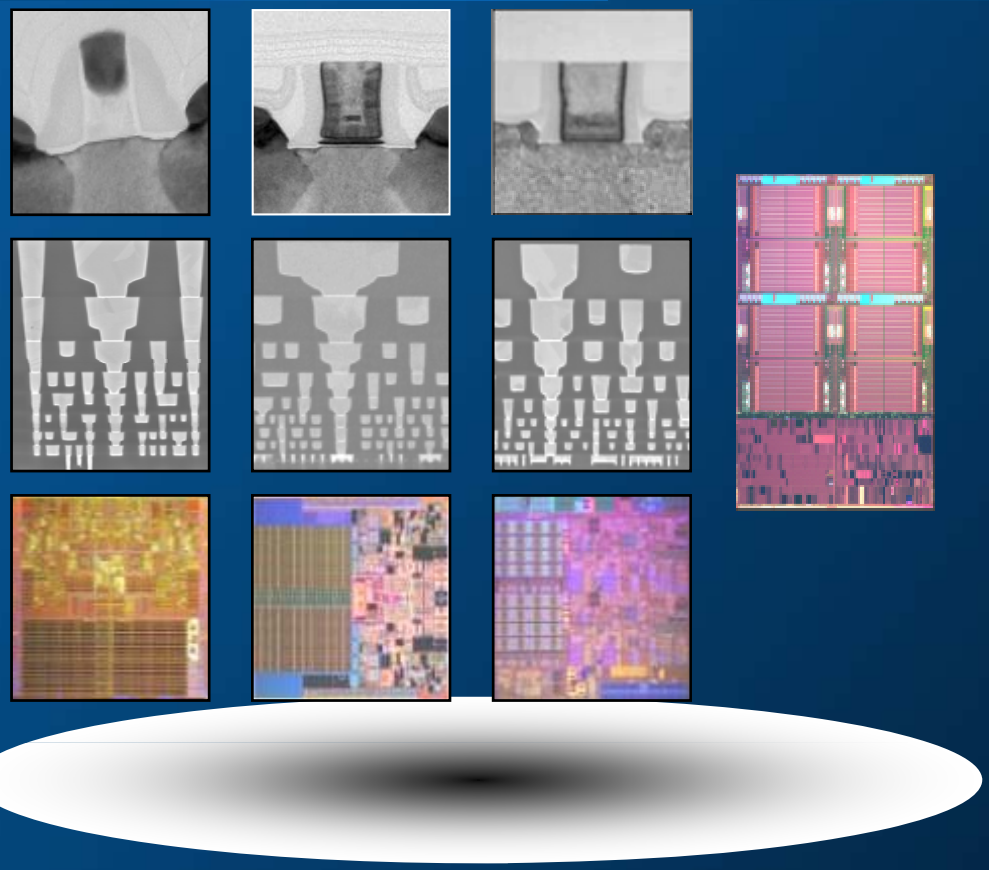
Visible Horizon and Beyond

Steady Technology Cadence

TECHNOLOGY GENERATION

65nm	45nm	32nm	22nm	15nm	11nm	8nm	Beyond
2005	2007	2009	2011	2013	2015	2017	2020

MANUFACTURING → DEVELOPMENT → RESEARCH

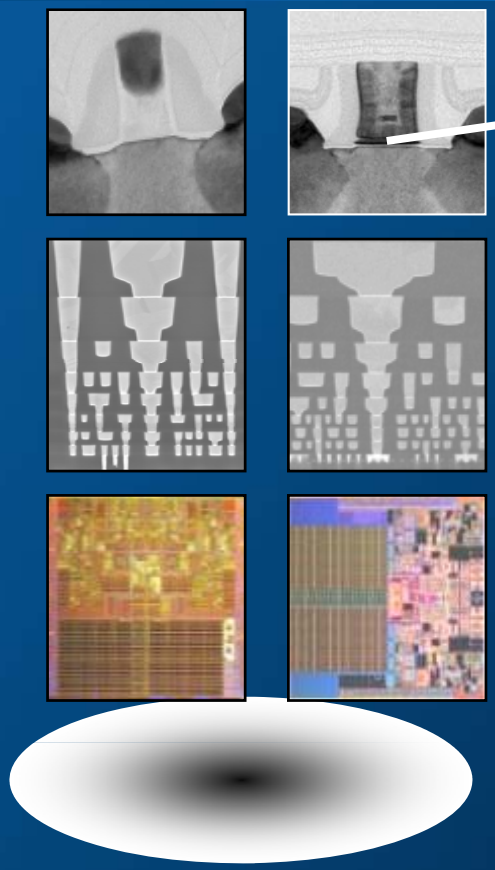


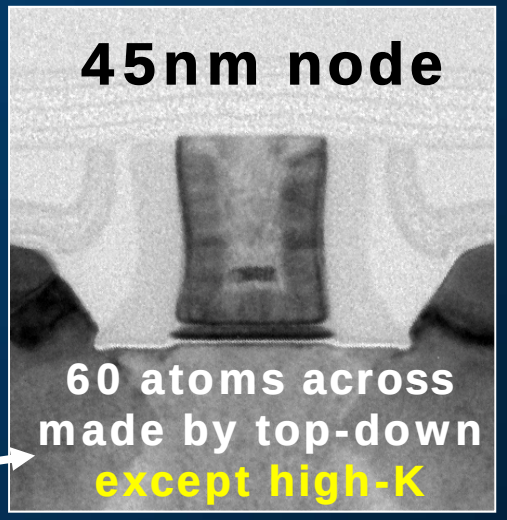
“We’re running out of atoms” Take 2

TECHNOLOGY GENERATION

65nm	45nm	32nm	22nm
2005	2007	2009	2011

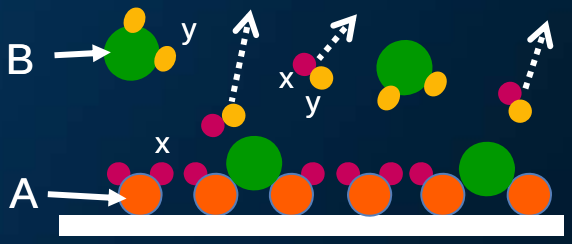
MANUFACTURING → DEVELOPMENT





Crafting Films with Atomic Layer Deposition

Step 1

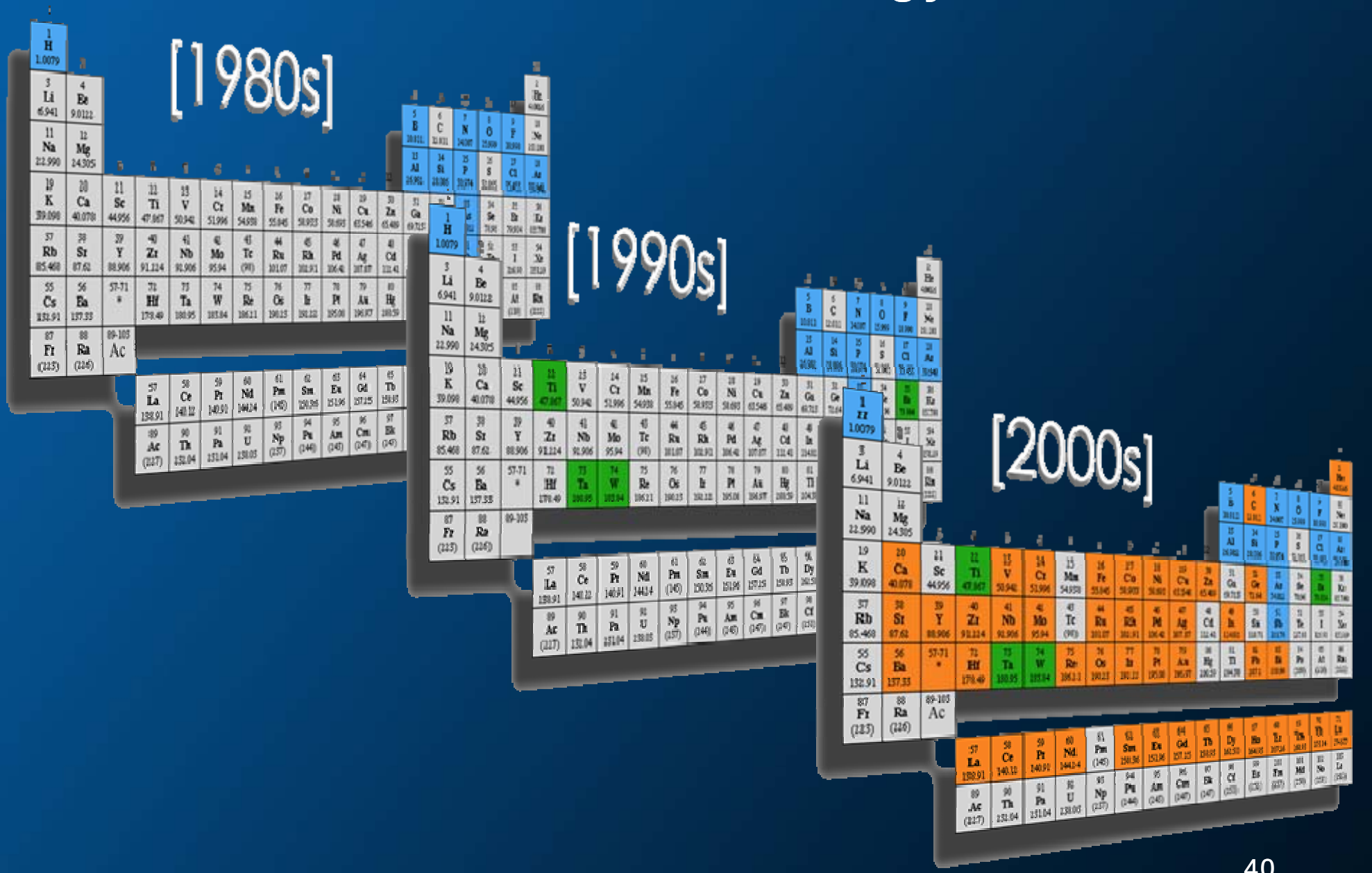


Step 3

Step 2

Step 4

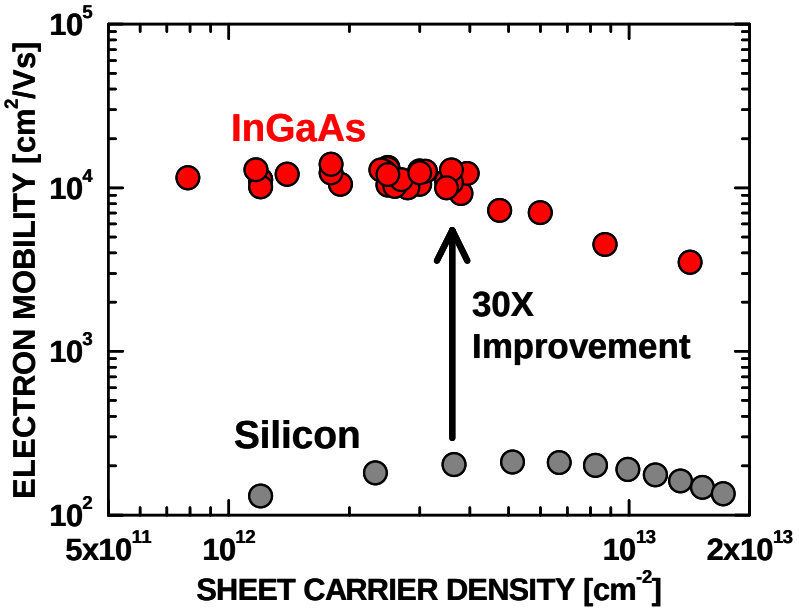
New Materials: Enabling the Future of Silicon Technology



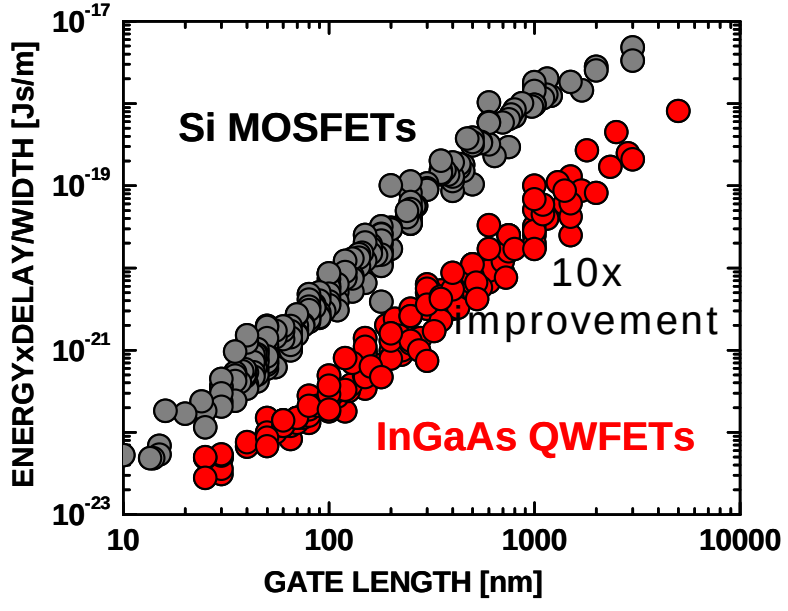
III-V Materials have Higher Mobility

Increased mobility in the transistor channel leads to higher performance and less energy consumption

Relative mobility

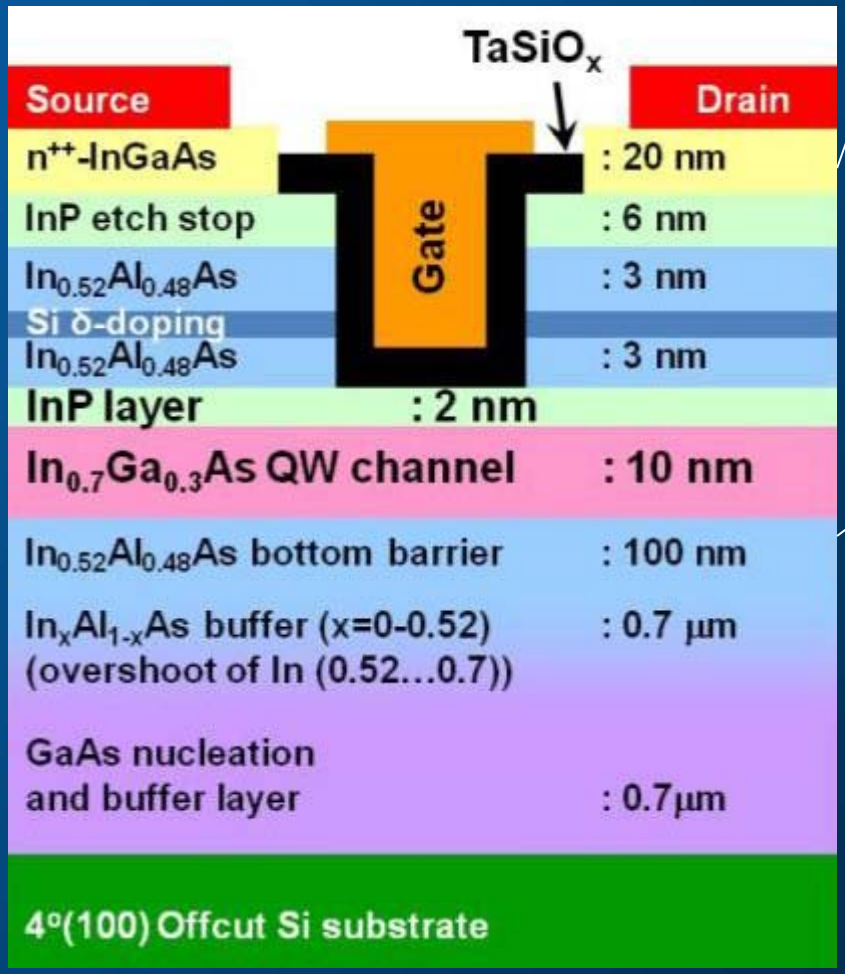


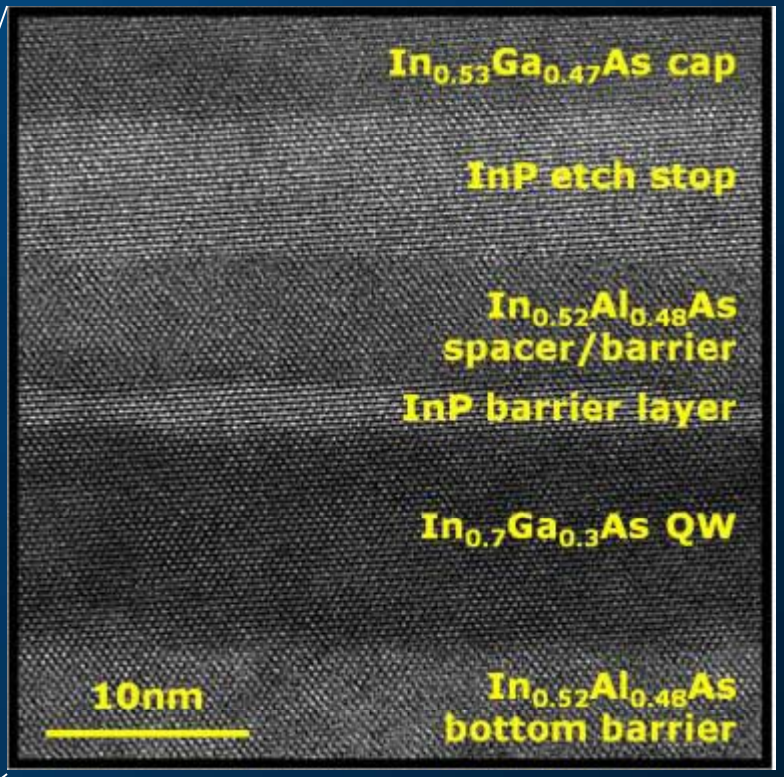
Relative power-performance



R. Chau et al, CSIC (2005)

Fabrication of QWFET with High-K





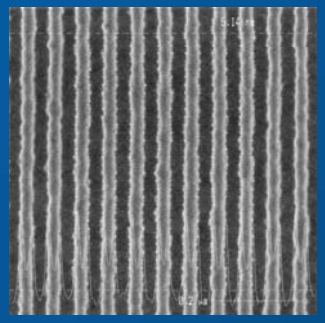
Fabrication challenges

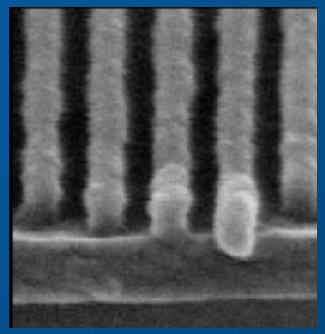
- Addition of two more unique materials to the stack (7 total)
- Molecular Beam Epitaxy & Atomic Layer Deposition used
- Atomic deposition precision needed across five critical layers

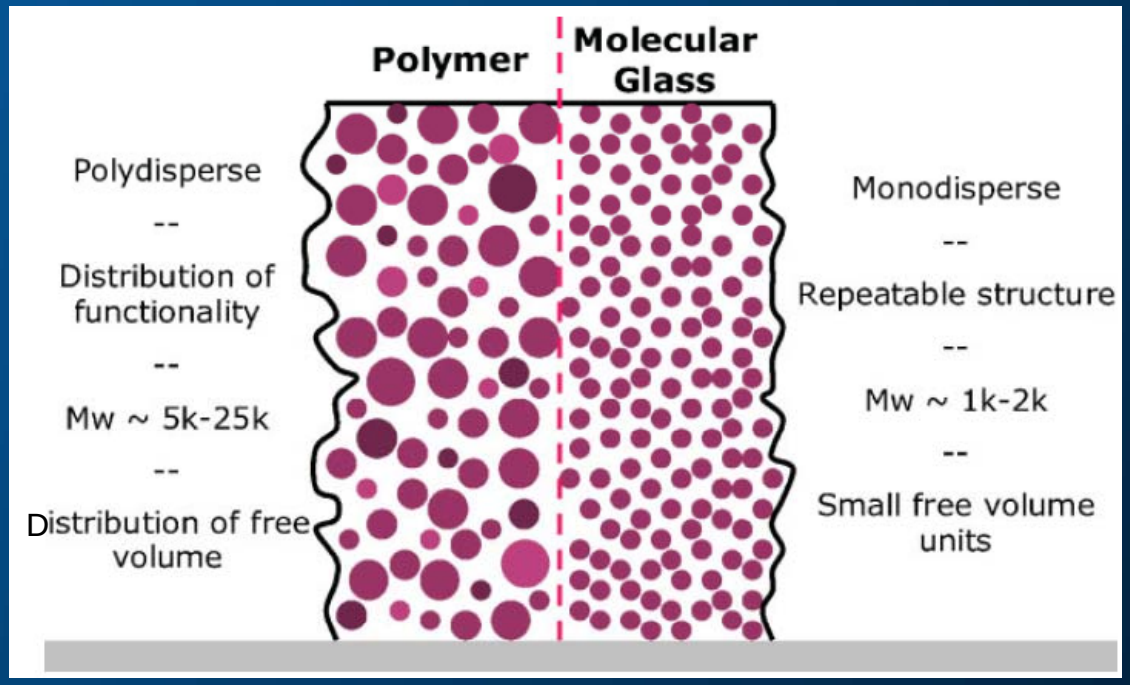
in partnership with IQE

Designing Materials with Smooth Grains

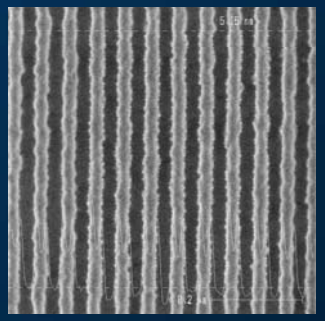
Polymer

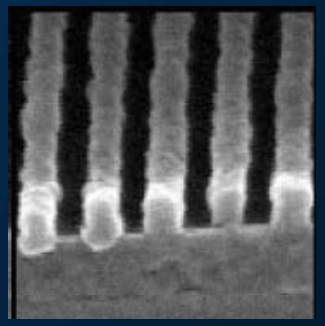






MG





Source: A. De Silva, et al. Adv. Mater. 2008

Polymer Blend
+ Mature materials platform
- Larger individual components

Molecular glass
+ Higher sensitivity at same resolution
- Lower mechanical strength (currently)

Need to engineer materials with components below 1nm

Our limit to visibility goes out ~10 years

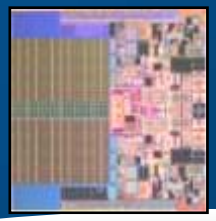
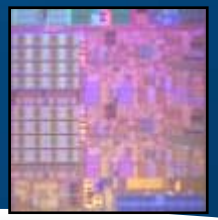
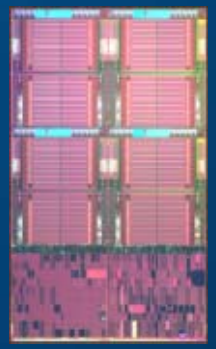
TECHNOLOGY GENERATION

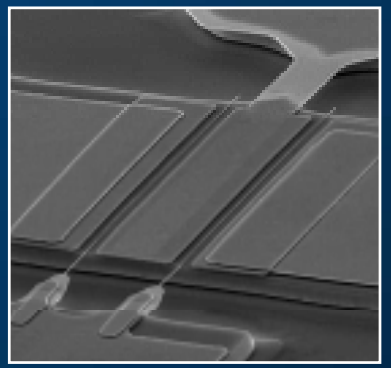
45nm	32nm	22nm	15nm	11nm	8nm	Beyond
2007	2009	2011	2013	2015	2017	2020

MANUFACTURING → DEVELOPMENT → RESEARCH

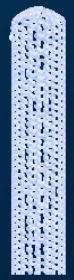




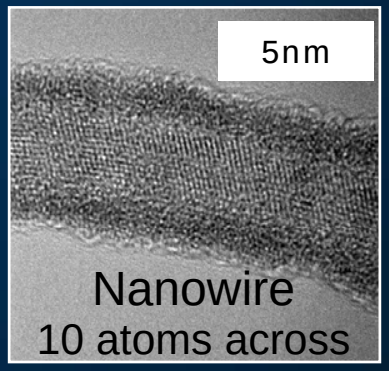





QW III-V Device

Carbon Nanotube
~1nm diameter



Graphene
1 atom thick

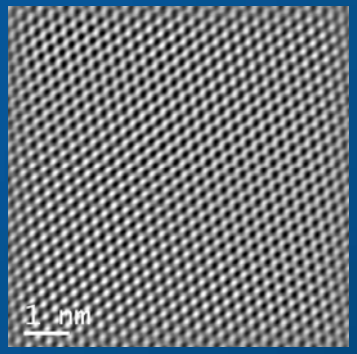


Nanowire
10 atoms across

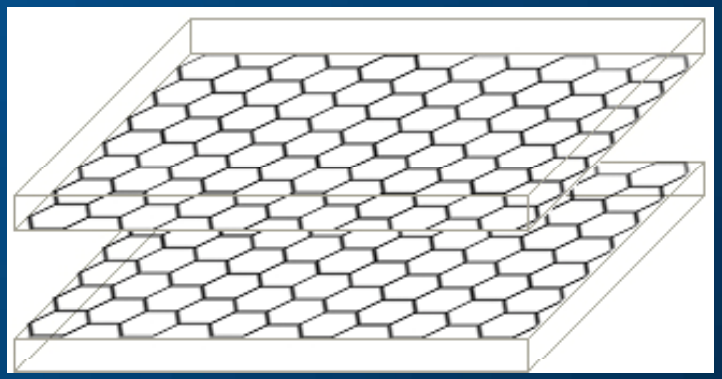
- Silicon lattice is ~ 0.5nm, hard to imagine good devices smaller than 10 lattices across – reached in 2020

Beyond 2020 and possible futures

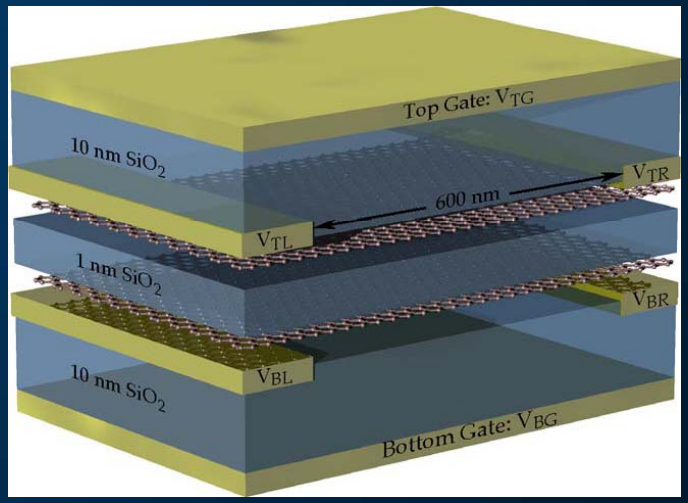
- Conventional fabrication architectures continue
  - Individual steps continue as 2D layers
  - More and more layers stacked to give increasing function



High resolution TEM of graphene



Graphene layers can couple together and create a quantum condensate



Bilayer graphene structure
Theoretically >10000x less power

Source: M. Gilbert et.al J Comput Electron (2009)

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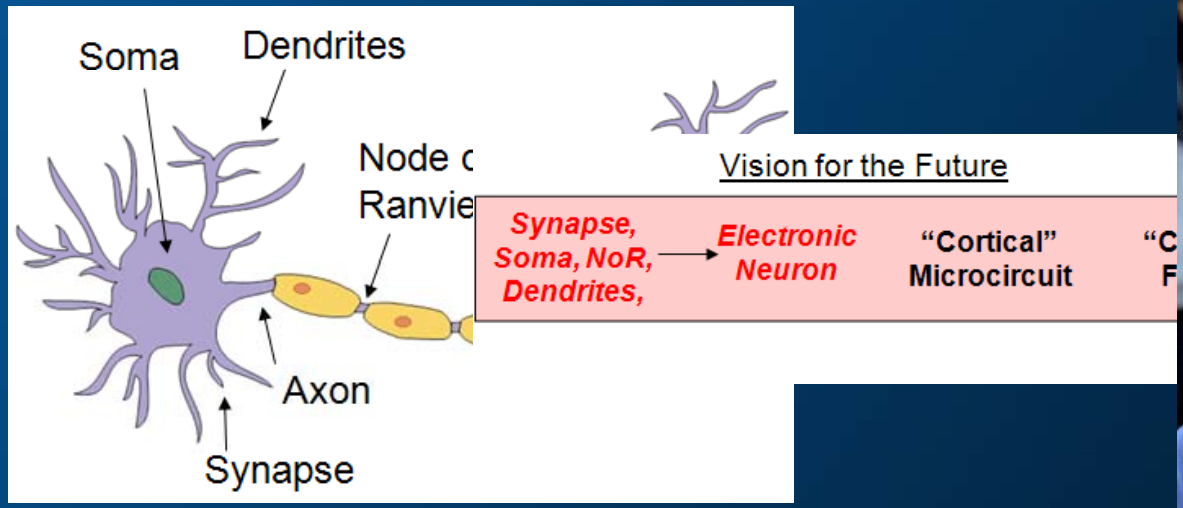
- Increasing use of heterogeneous technologies and novel ways to combine technologies
  - Electronics fabricated conventionally but combined with bio interface grown bottoms-up
  - Eliminating, reducing cost of interfaces



Source: NRI, SWAN review 2009

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  - Electronics fabricated conventionally but combined with bio interface grown bottoms-up
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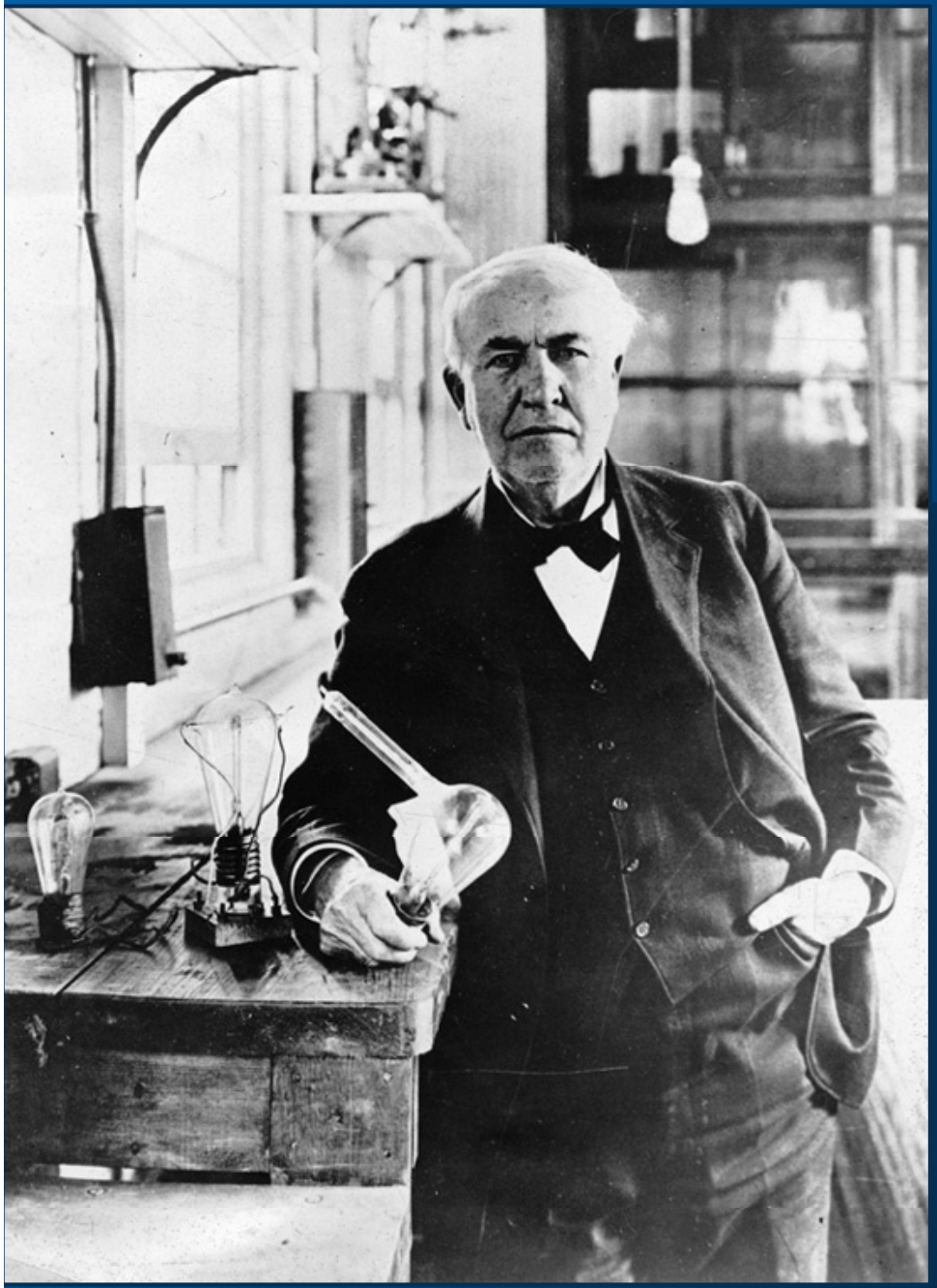
- Non-binary or alternate state computation
  - Same fabrication complexity, more value per function

Conclusions

- Moore's Law is not a law of nature, it is an expectation of continued innovation
- We expect to continue through focused research, rapid development, investment in production
- Scaling research is increasingly about materials research, solving problems brings opportunities
- New product opportunities will arise from continued advances in integration, connectivity



Closing Thought

Thomas Edison:

Opportunity is missed by most people because it is dressed in overalls and looks like work.

Source: National Archives and Records Administration

Thank You