# Pushing Past the Frontiers Of Technology

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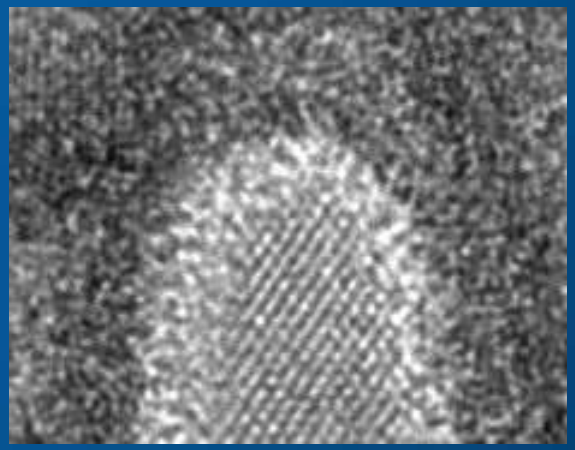
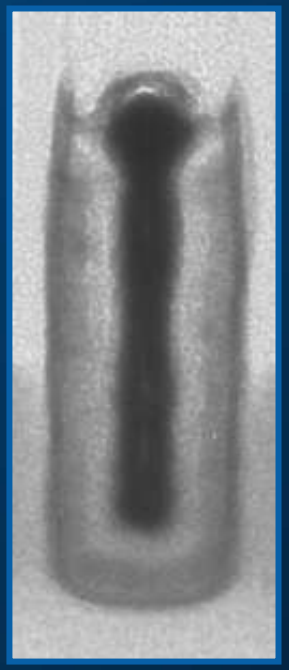
Director of Components Research
VP, Intel Corporation

March 2013

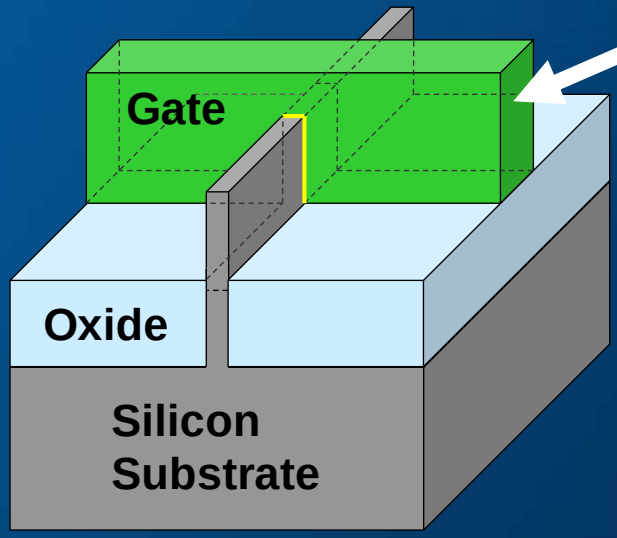
# You Are Here – 22nm node

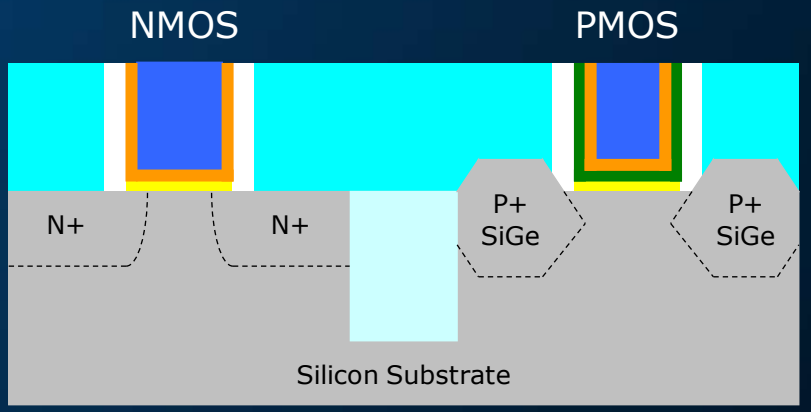
# Building a Complex 3D Structure





*Source: Auth et al. VLSI 2012*



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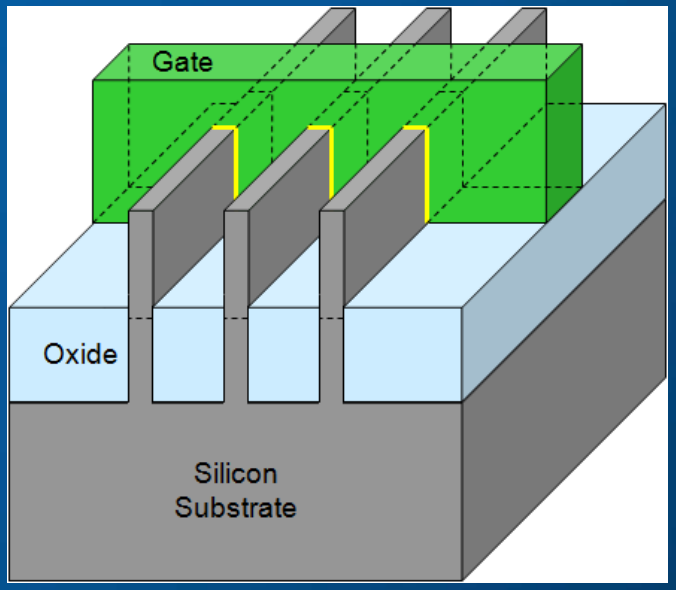
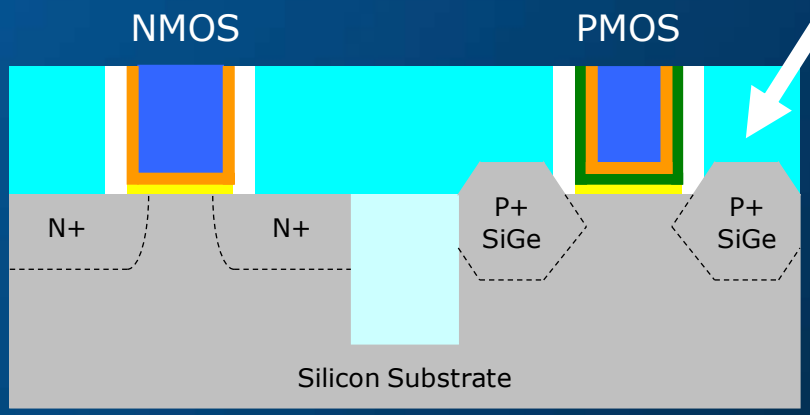
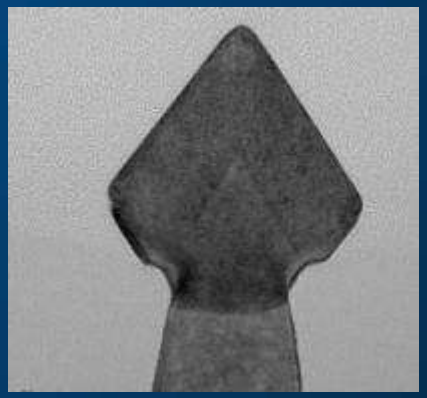
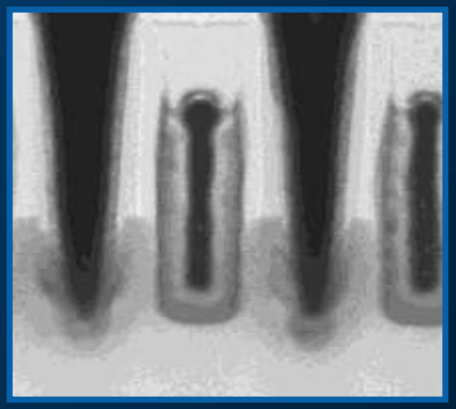


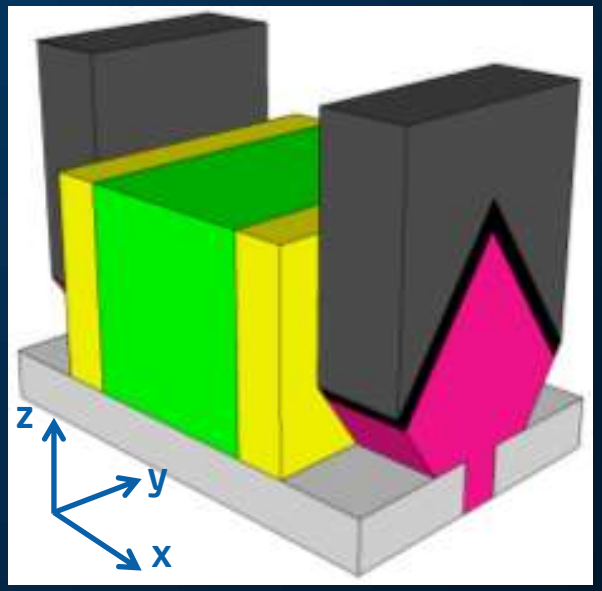

*Source: Auth et al. VLSI 2012*



PMOS Source/Drain



Self-Aligned Contacts



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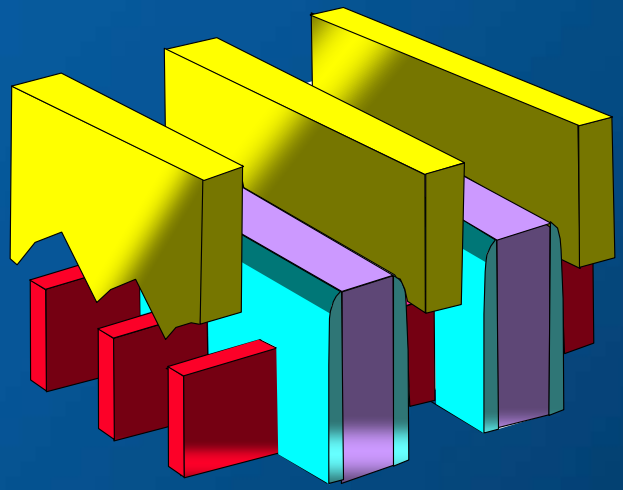
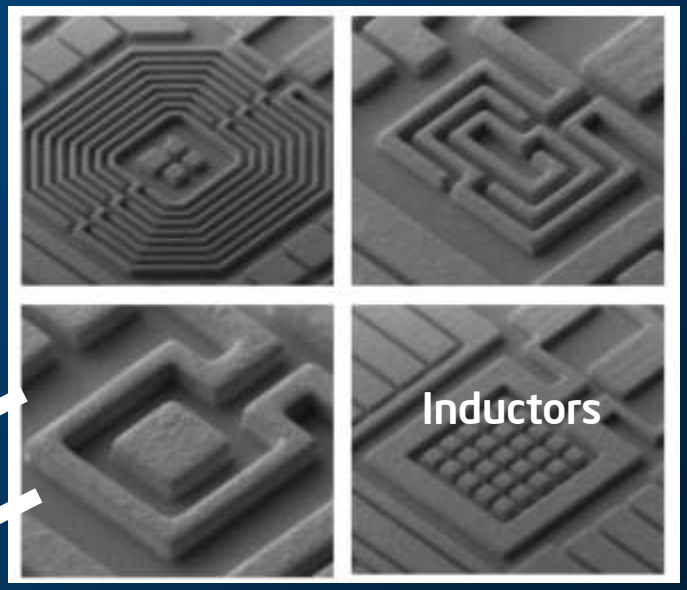
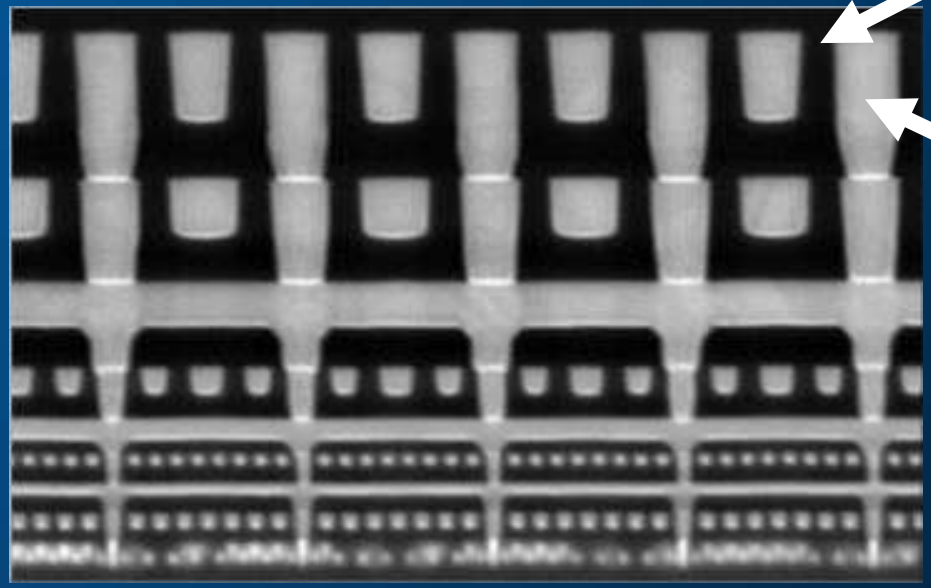
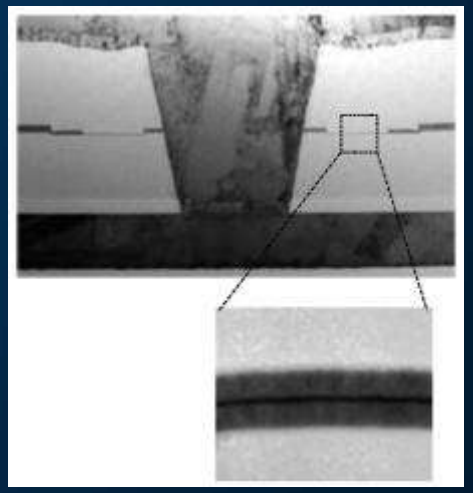






MIM cap

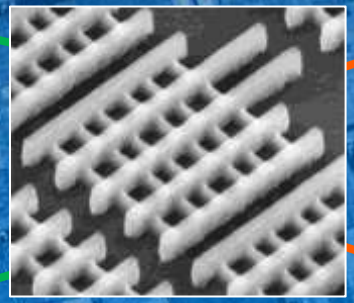
*Source: Auth et al. VLSI 2012*
*Jan et al. IEDM 2012*

# "Any sufficiently advanced technology is indistinguishable from magic"

– Arthur C. Clarke 1973

**1 x $10^9$**

1 billion transistors fit into an area of One square centimeter



**~1 x $10^{18}$**

Intel ships about one quintillion transistors per year

## Intel 2013

**Every 2 years**

Intel delivers a new manufacturing process

**2 x Better**

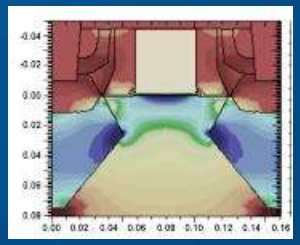
than the previous generation

## Intel in the Future

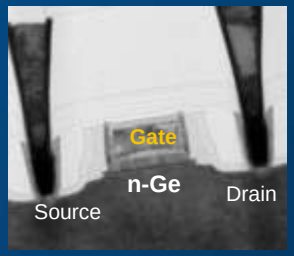
# The (likely) near future

# We Need Both New Materials & New Structures

Increasing Mobility

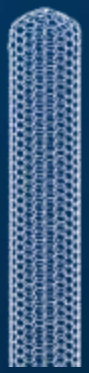


Strain



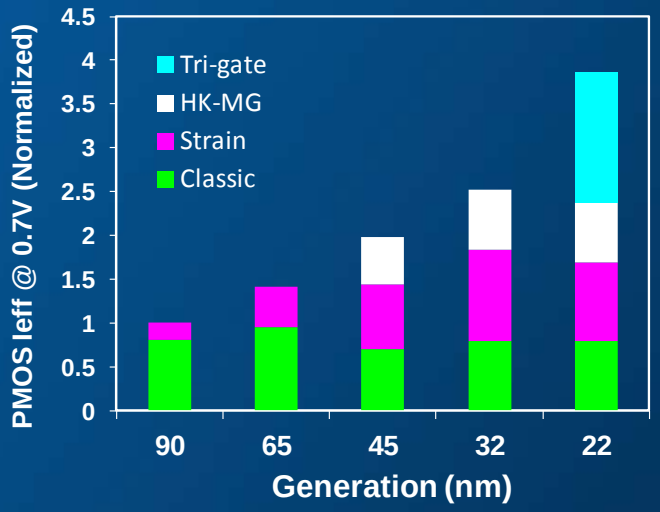

Ge

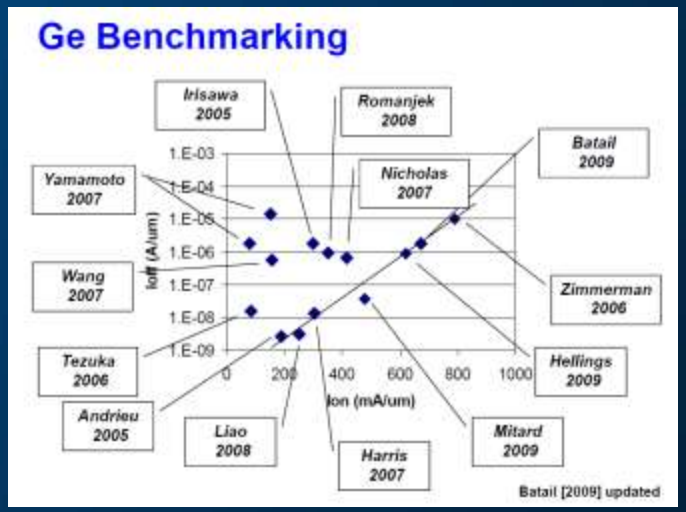

III-V

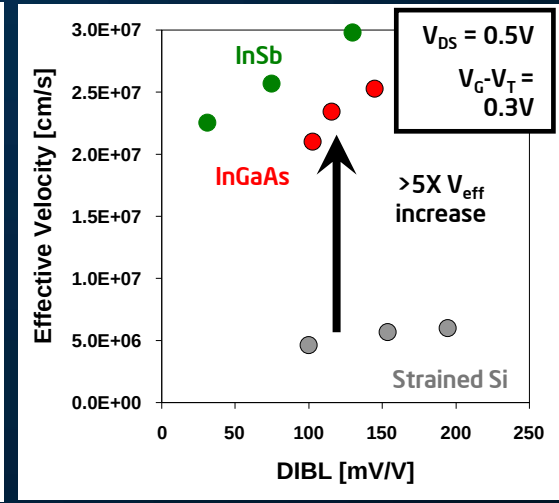


CNT

Graphene

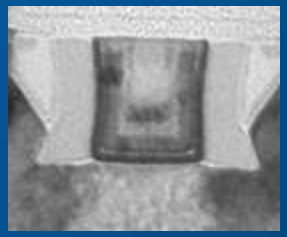


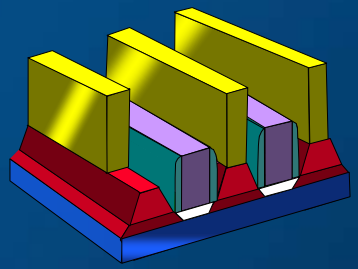




*Source: Intel*

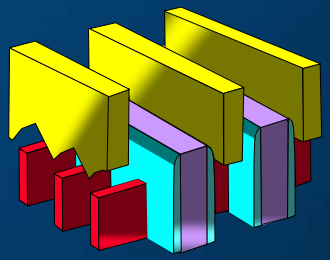
# We Need Both New Materials & New Structures



Planar
With High K



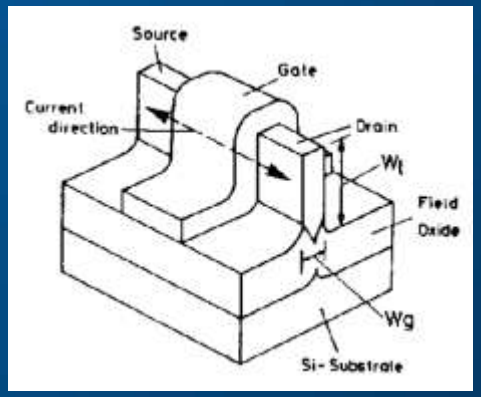
UTB SOI
(or QW)



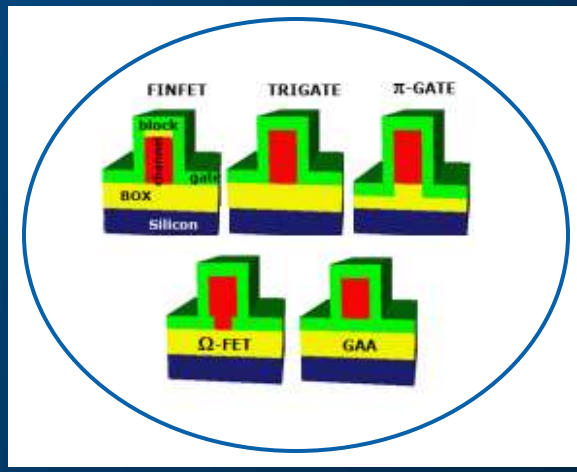
Fins &
Multigate


Wires/Dots

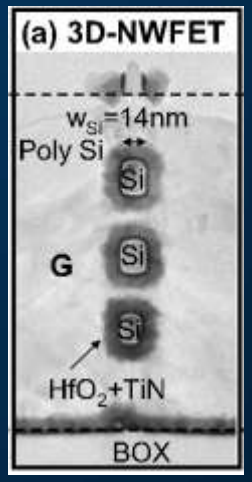
Increasing
Electrostatics



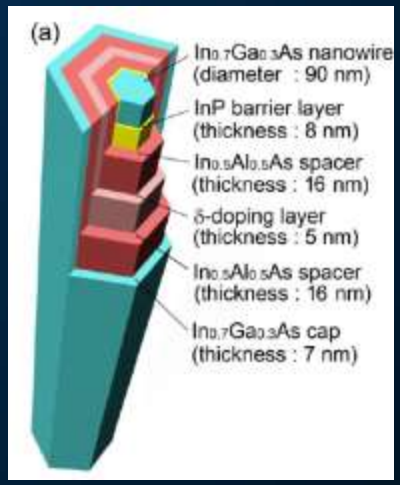

*Hisamoto – IEDM 1989*




*And many others*

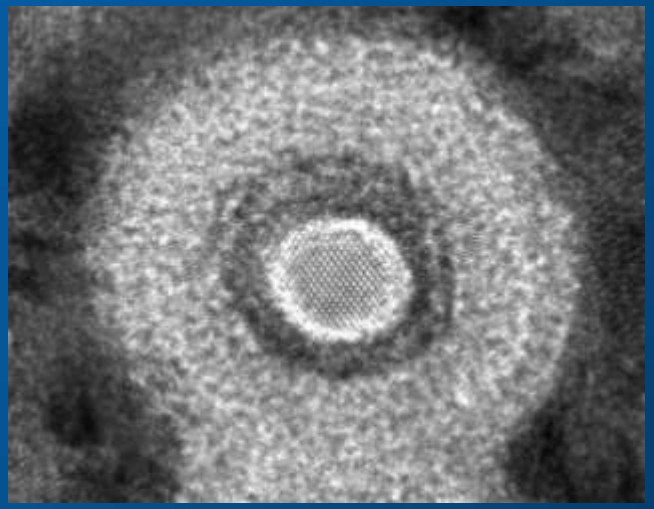


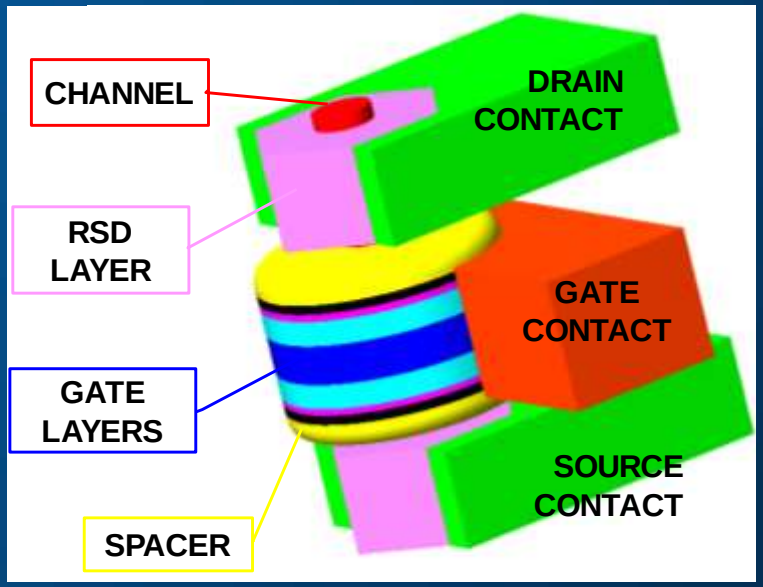

*Dupre*
*IEDM 2008*

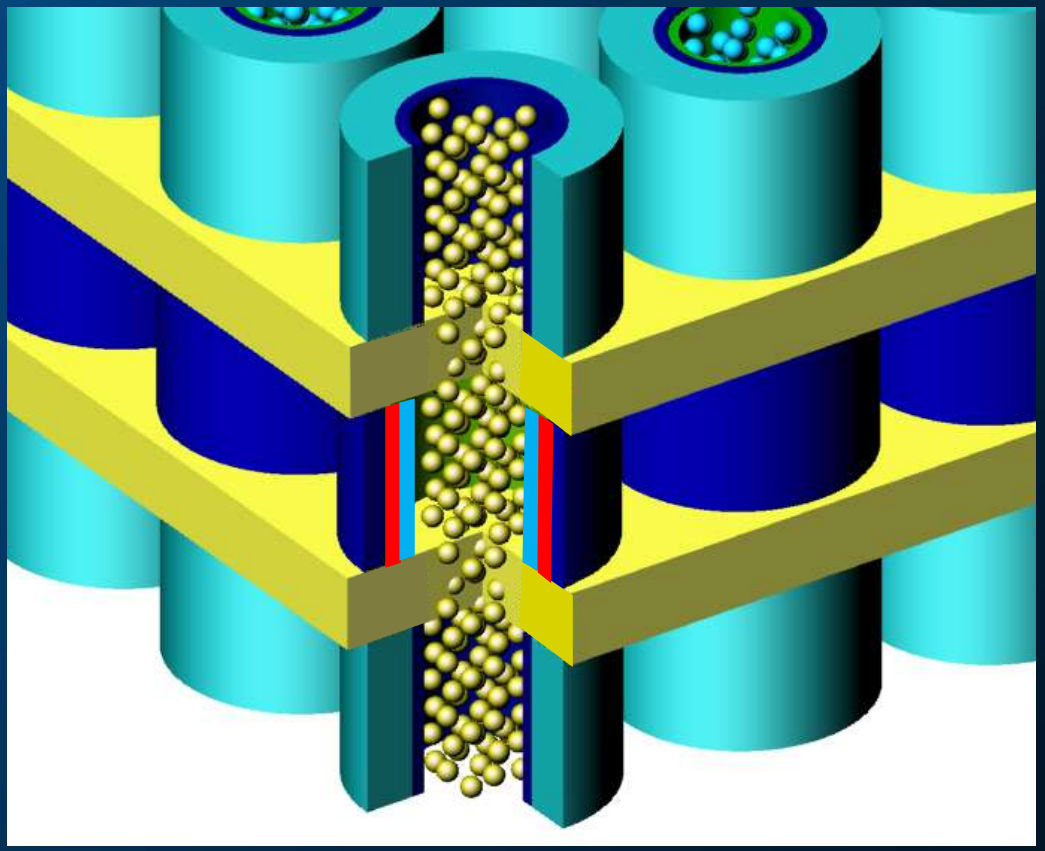



*Tomioka – IEDM 2011*

# The Gate All Around (GAA) Architecture is the Limit to Structural Electrostatic Control



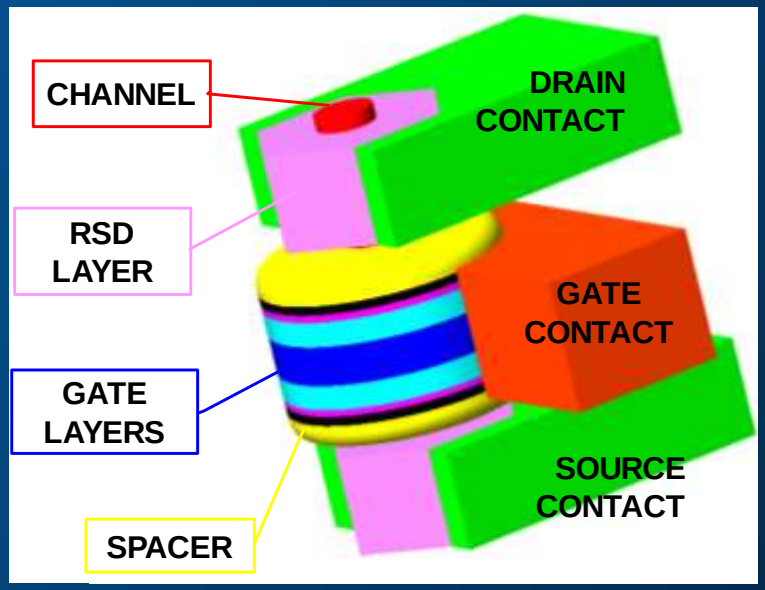


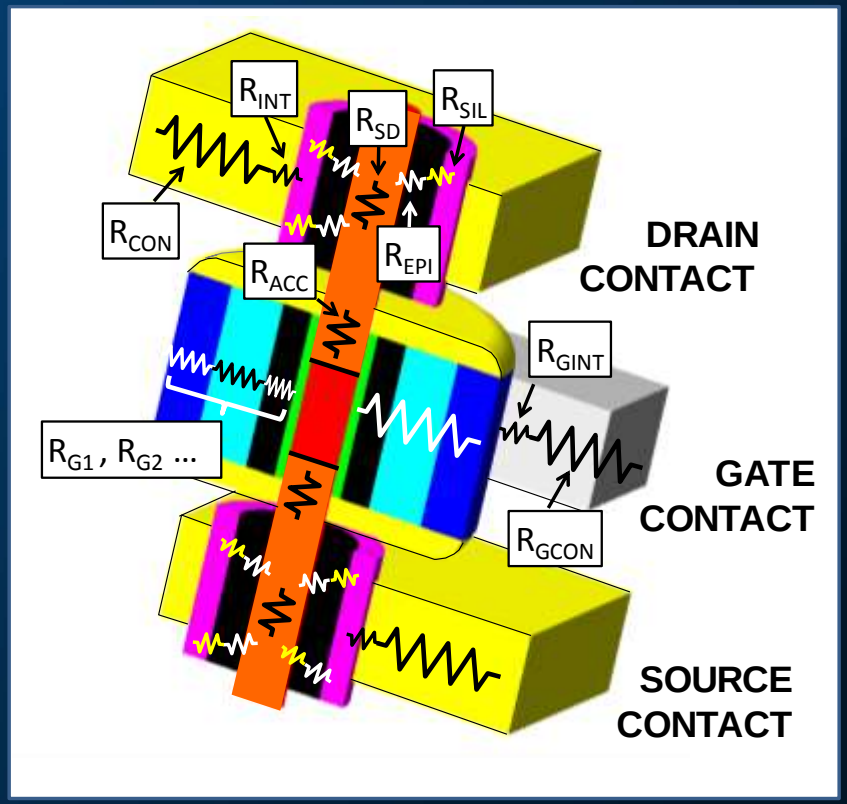



*Source: K. Kuhn et al. TED 59:7 2012*

# Modern Technologies are NOT Solely Limited by Transistors

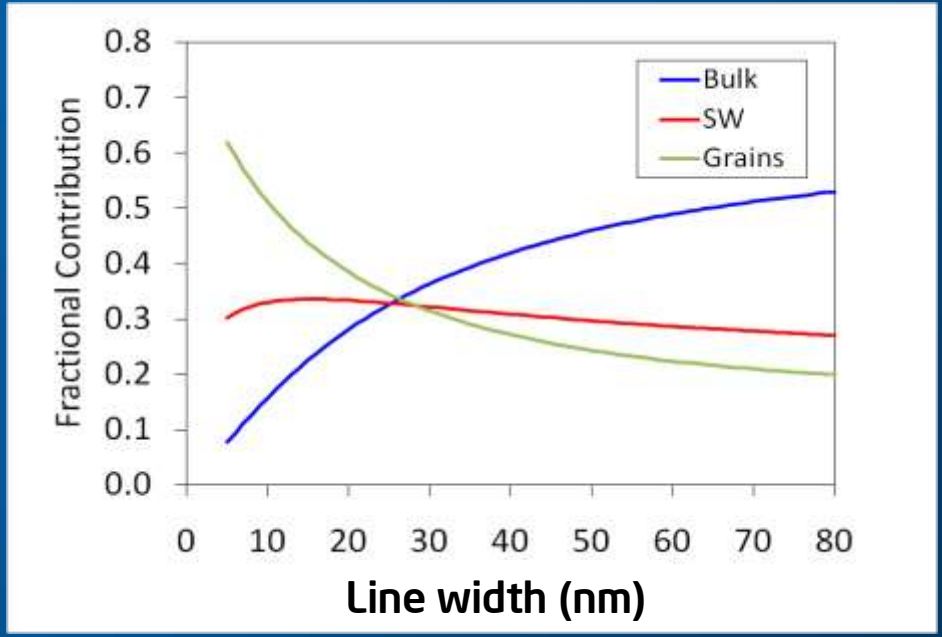
- Interconnections turn devices into useful functions
- 3D structures (finFET's, vertical FETs, etc.) make this considerably more challenging at 22nm and beyond
- Need thin conformal films for
  - Gate metals (NMOS and PMOS)
  - Contact metals

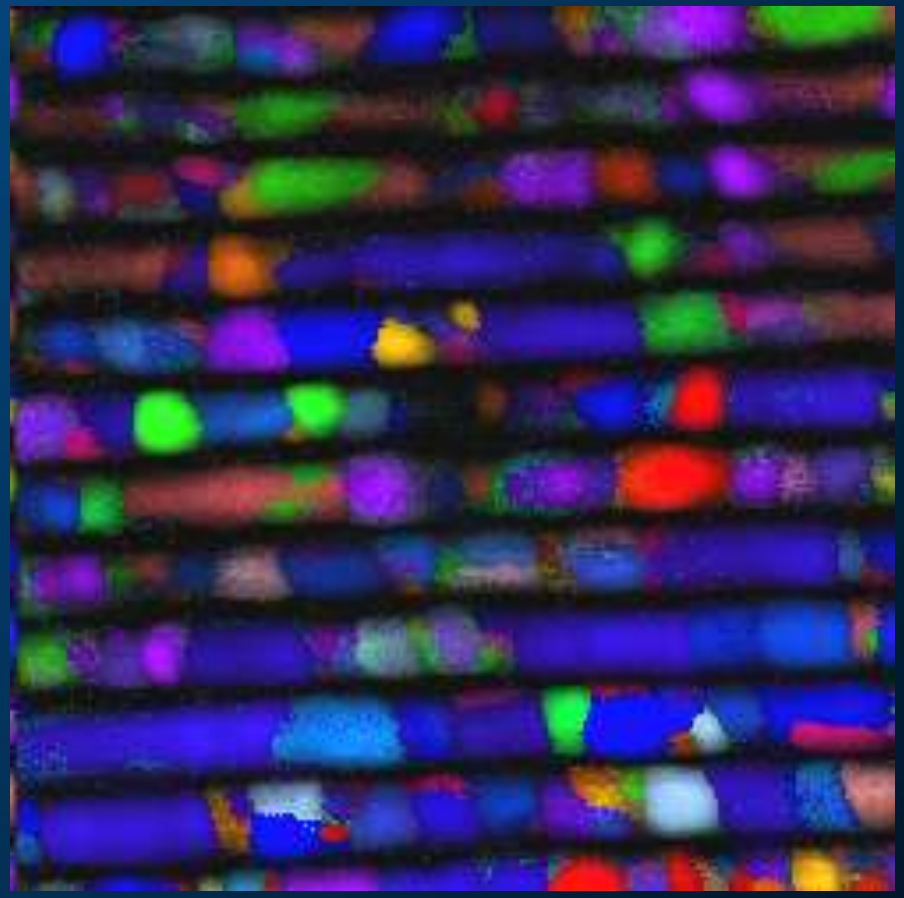



*Source: K. Kuhn et al. TED 59:7 2012*

# Key Issue: For Small Dimensions, Scattering from Grains & Sidewall becomes Dominant



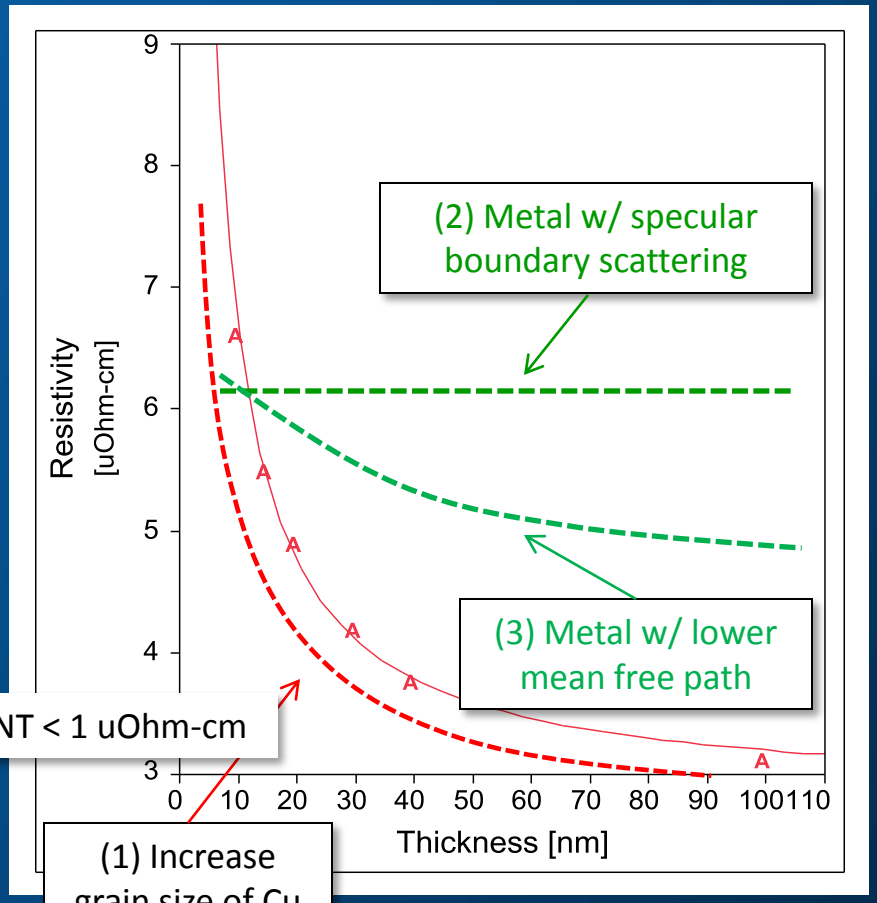



**What if We Could Eliminate Scattering ?**

Cu wires at 17nm drawn dimension
*(colors indicate crystal orientation measured with DSTEM)*

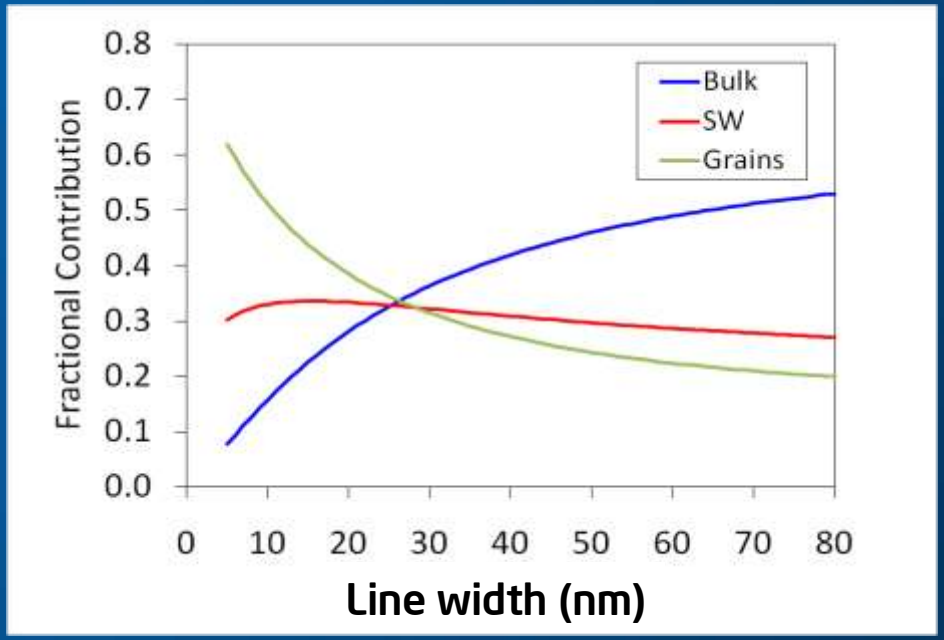
*Source: Intel*

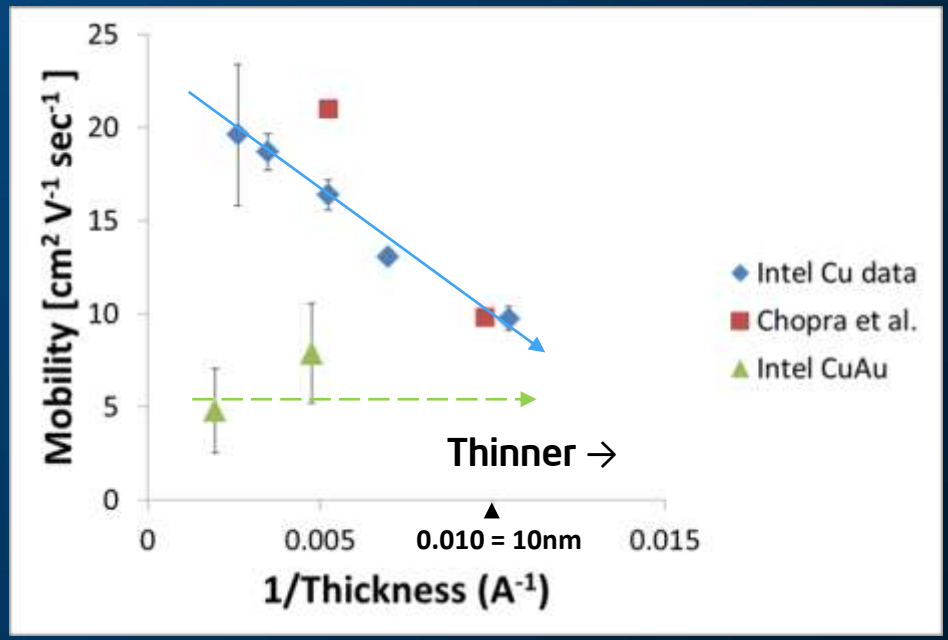
# Can We Make Better Materials?




1. Improve Cu – increase grain size
2. Alternative materials with specular boundary scattering
3. Alternative materials with lower mean free path
4. Disruptive technologies

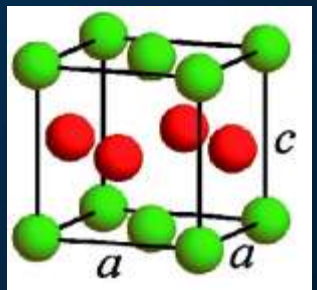
# Can We Make Better Materials?




**What if We Could Eliminate Scattering ?**

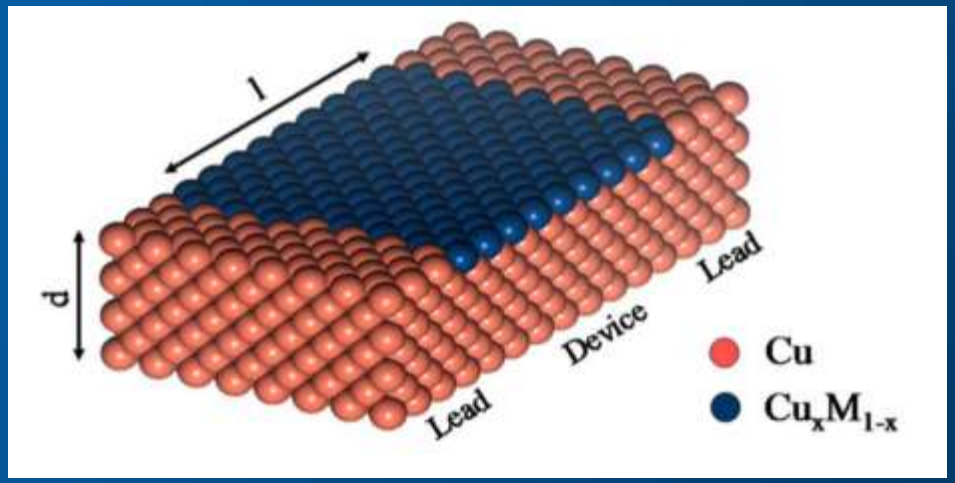
- Specular boundary scattering
- Small electron mean free path
- Potentially better at small dimensions



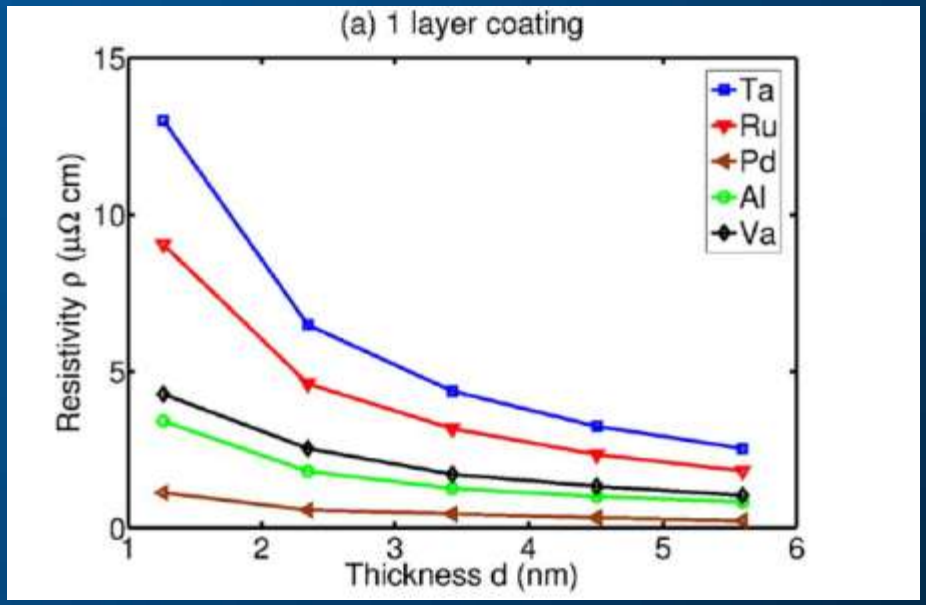

50 atomic% Au
CuAu I
CuAu $\alpha_l$”

*Source: Intel*

# Can We Make Better Materials?



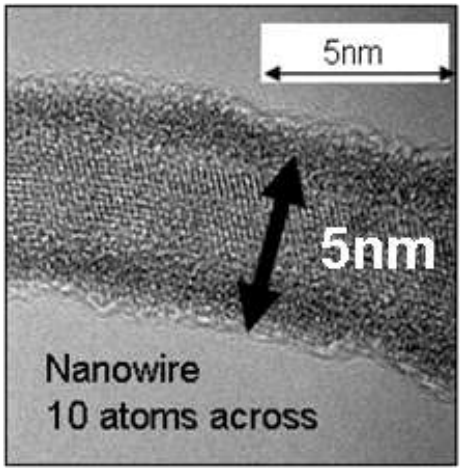

*Source: F. Zahid, Phys Rev. B. (2010) "Resistivity of thin Cu films coated with Ta, Ti, Ru, Al, and Pd barrier layers from first principles" (simulation)*



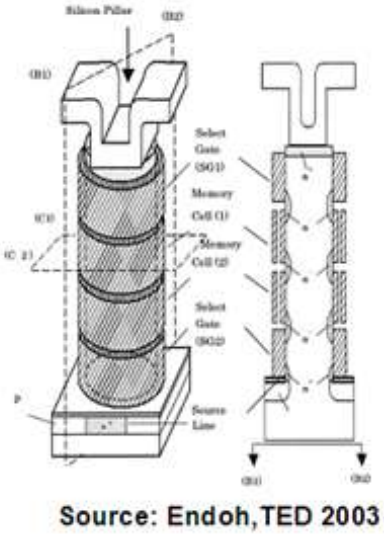

**Pd, Al better than Ta, Ru**

**?**

# Are there fundamental physical limits?

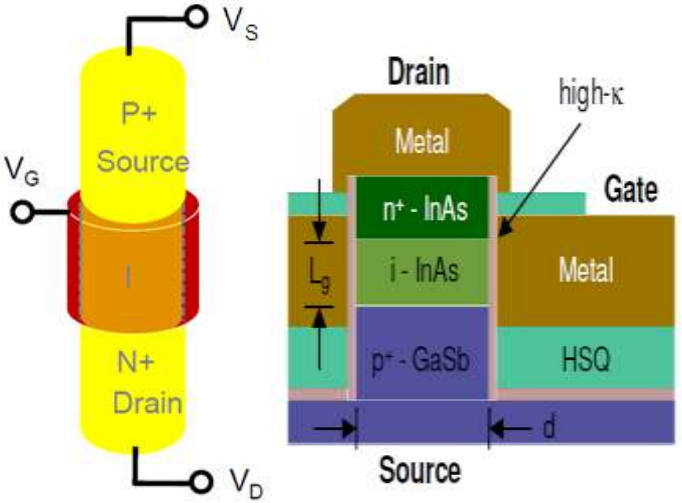



5nm device feature



Source: Endoh, TED 2003

Vertical devices




III-V Vertical Tunnel FETs

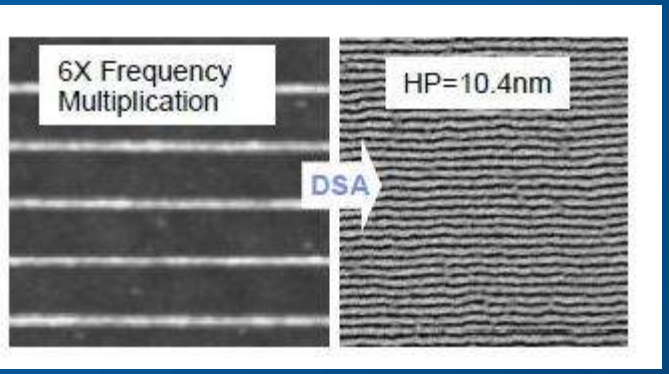
**Vertical device structures and new materials**

- 5nm device structures have been demonstrated in research labs
- New device architectures are under investigation

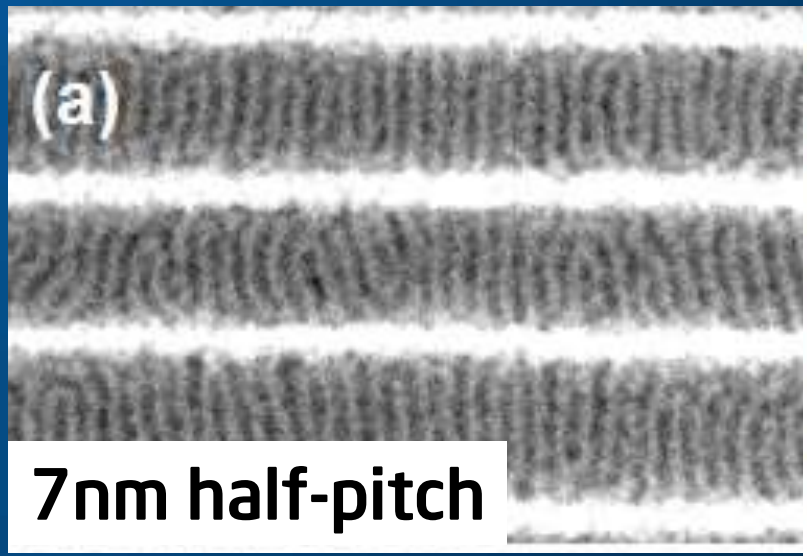
**Our ability to control is more a limitation than the physics**

**Control implies we can measure …**

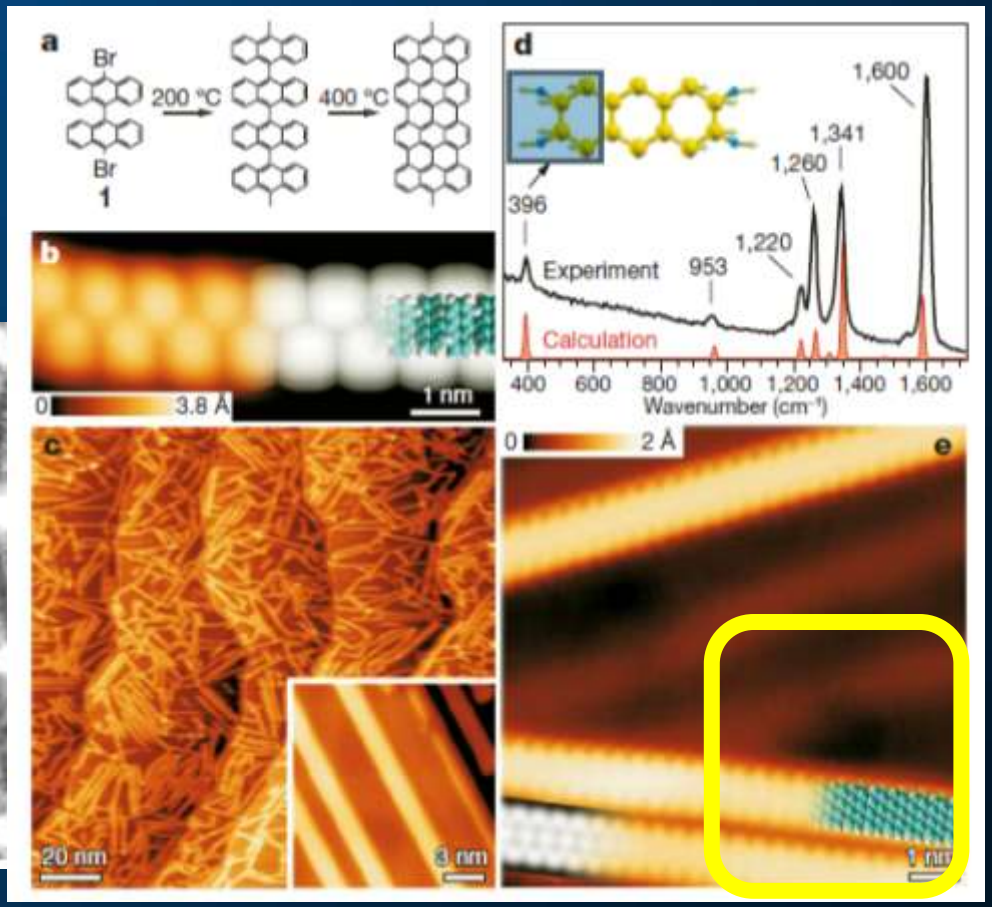
# How Small Can We Fabricate and Control?




**"Self-Assembling Materials for Lithographic Patterning"**
*Bill Hinsberg et al, IBM.SPIE 2010*

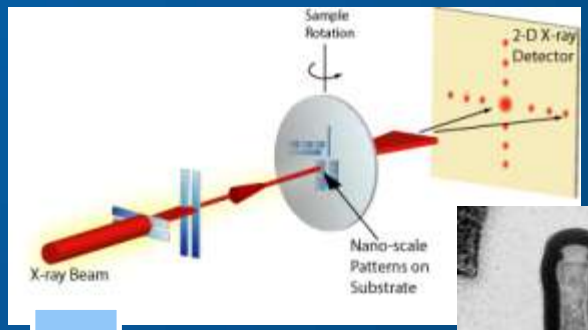



*IBM, Park et al, Nanotech 19 2008*



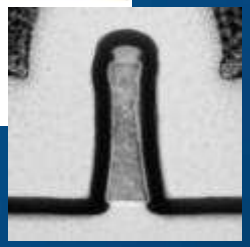

*Cai et al, Nature July 2010*

# How can we image a complex 3D structure and with Atomic Resolution of Interfaces and Chemistry?

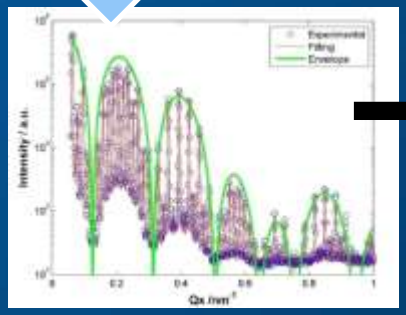


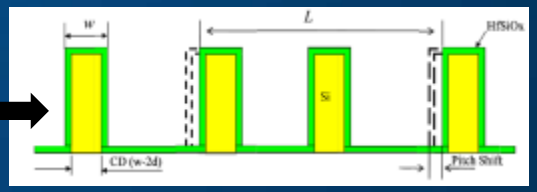

~ 100 images

±45°
1° steps

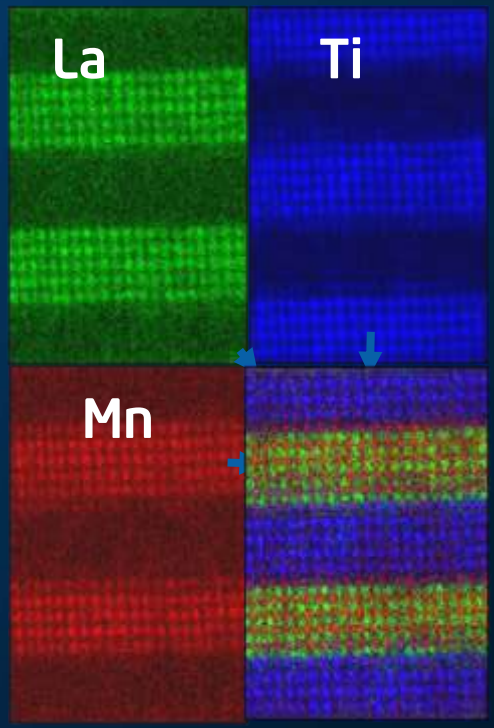


20 nm Hi k covered gate






Elastic Scattering
~ "Z contrast"




EELS: Chemical Imaging

## Small Angle X-ray Scattering?

*Bundy, SPIE 7272 M-5*

## STEM with electron energy loss spectroscopy?

*Muller, Science 319, 1073 (2008)*

# The End of Scaling is Near?

"Optical lithography can't do sub-micron"

"Optical lithography will reach its li[illegible]he range of 0.75-0.50 microns"

"Optical lithography should reach its l[illegible]s in the 1990-1994 period"

"X-ray lithography will be [illegible]ded below 1 micron"

"Minimum geometries will saturat[illegible] the range of 0.3 to 0.5 microns"

"Channel lengths can be reduce[illegible] approximately 0.2 microns"

"Minimum gate oxide thickness is limited to ~2 nm"

"Oxide reliability may limit oxide scaling to 2.2 nm"

"Plasma etched aluminum will not happen in our lifetime"

"Copper interconnects will never work"

"Scaling will end in ~10 years"

Source: ISSCC 2009, *The New Era of Scaling in an SoC World*, M. Bohr

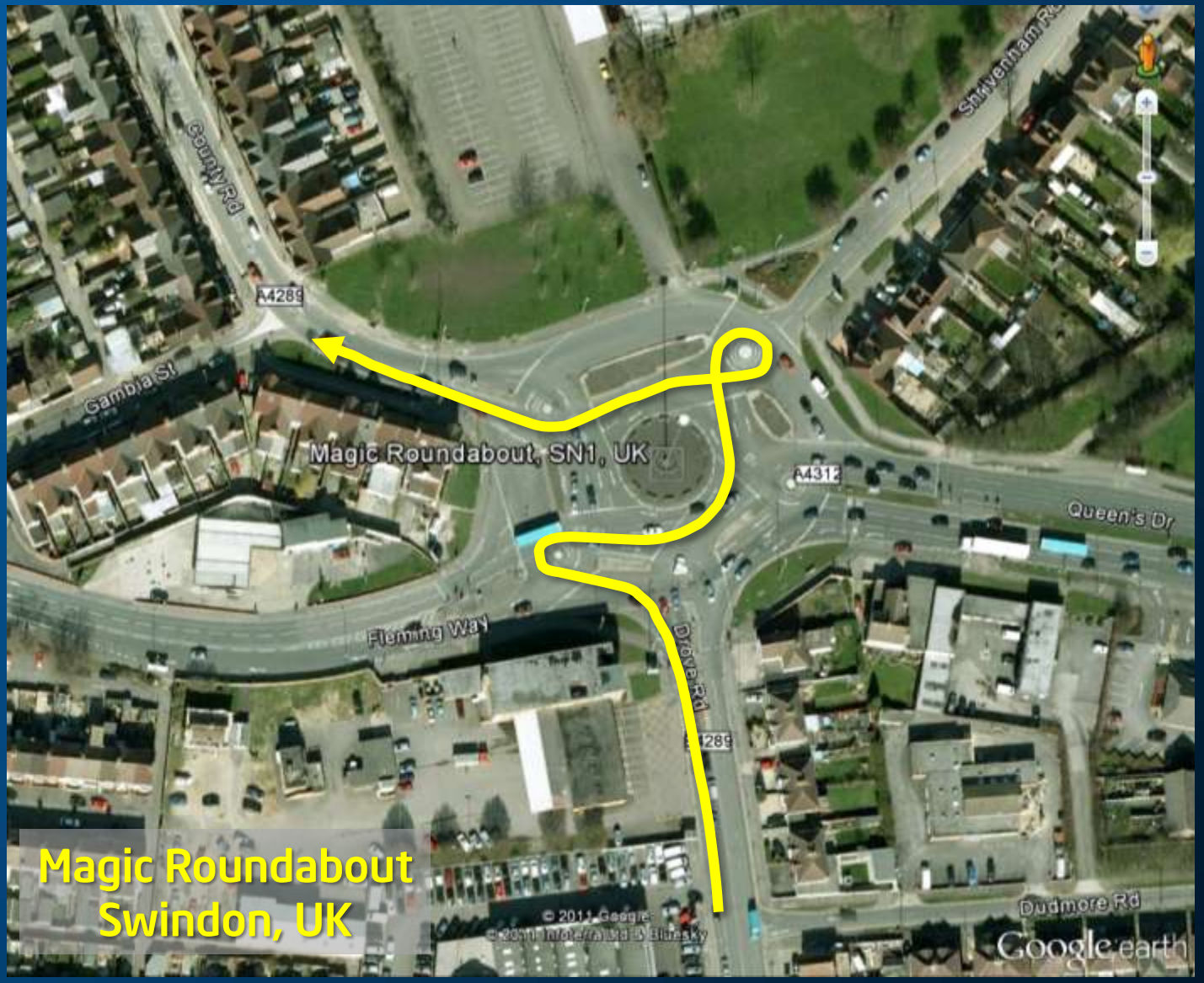
# Inflection Points

- Size Limited by Granularity, Process Control
- Size limited by Electrical behavior (tunneling)
- Voltage scaling limited by Mobility
- Interconnects and transport limit performance
- We don't know how to measure or control
- …

"The only way of discovering the limits of the possible is to venture a little way past them into the impossible"

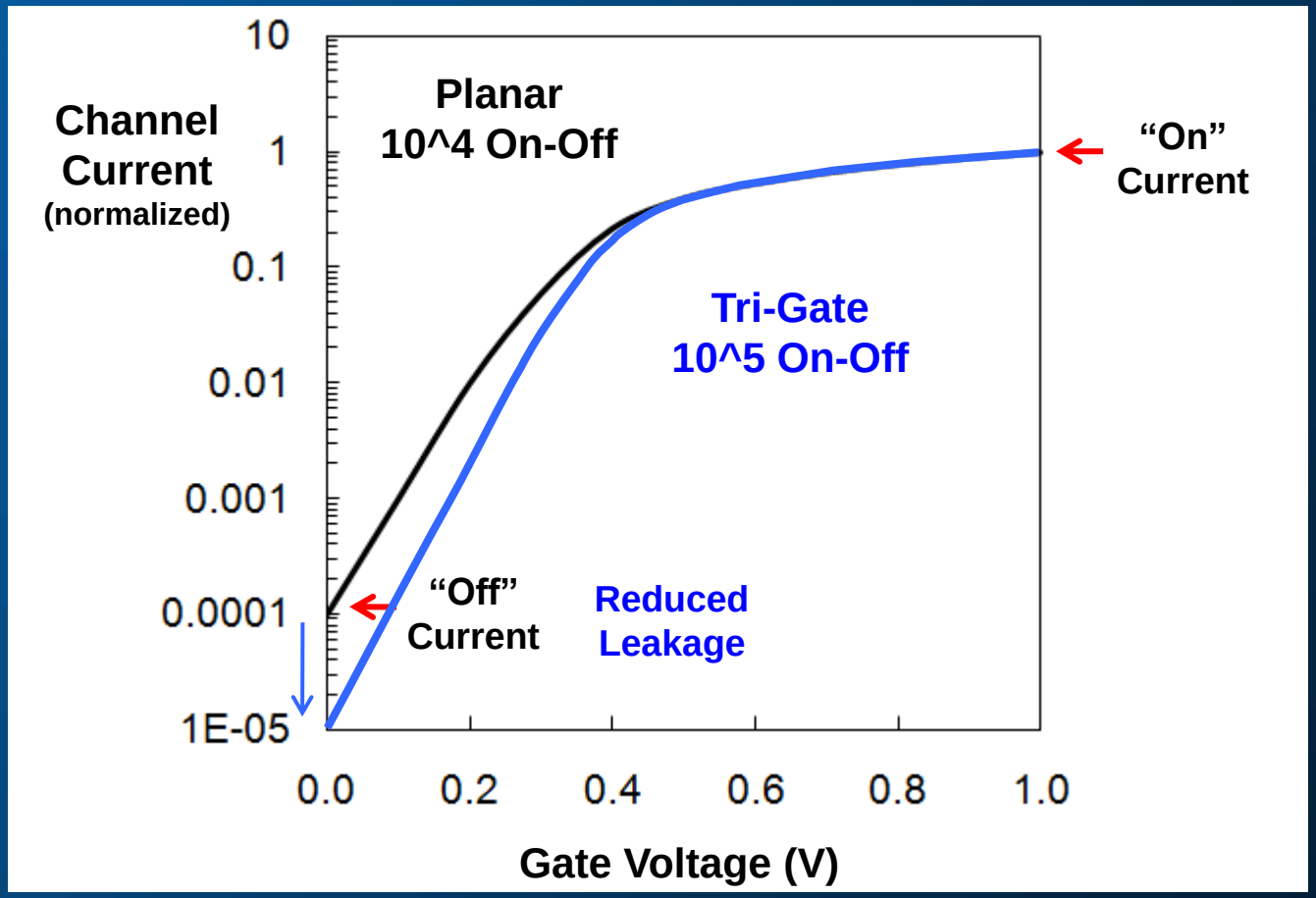
– Arthur C. Clarke 1962

# Alternative paths



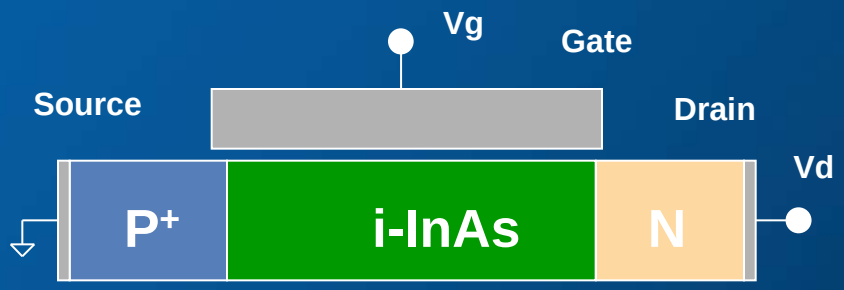

Source: Google Earth

# The Quest for a Better Switch

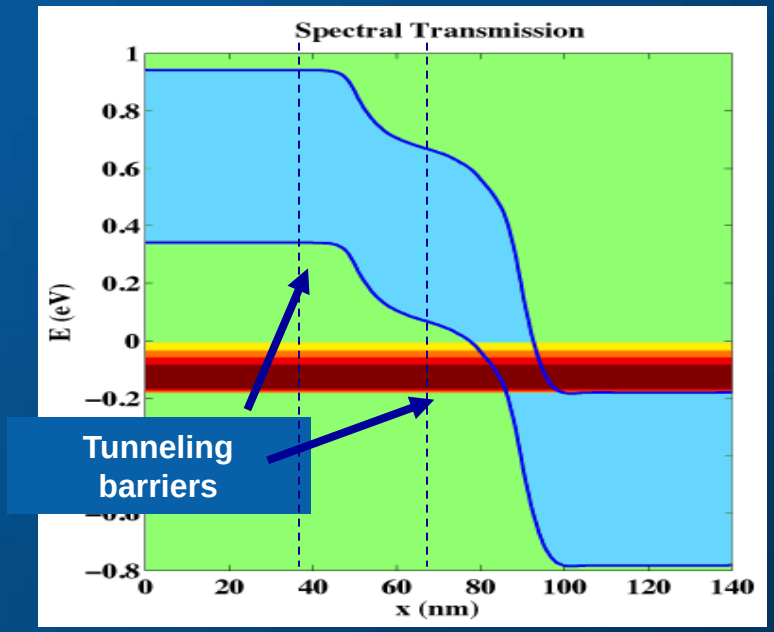



*Source: Intel*

# TFET (Tunneling Field-Effect Transistor)




Tunnel FETs operate by tunneling through the S/D barrier rather than diffusion over the barrier

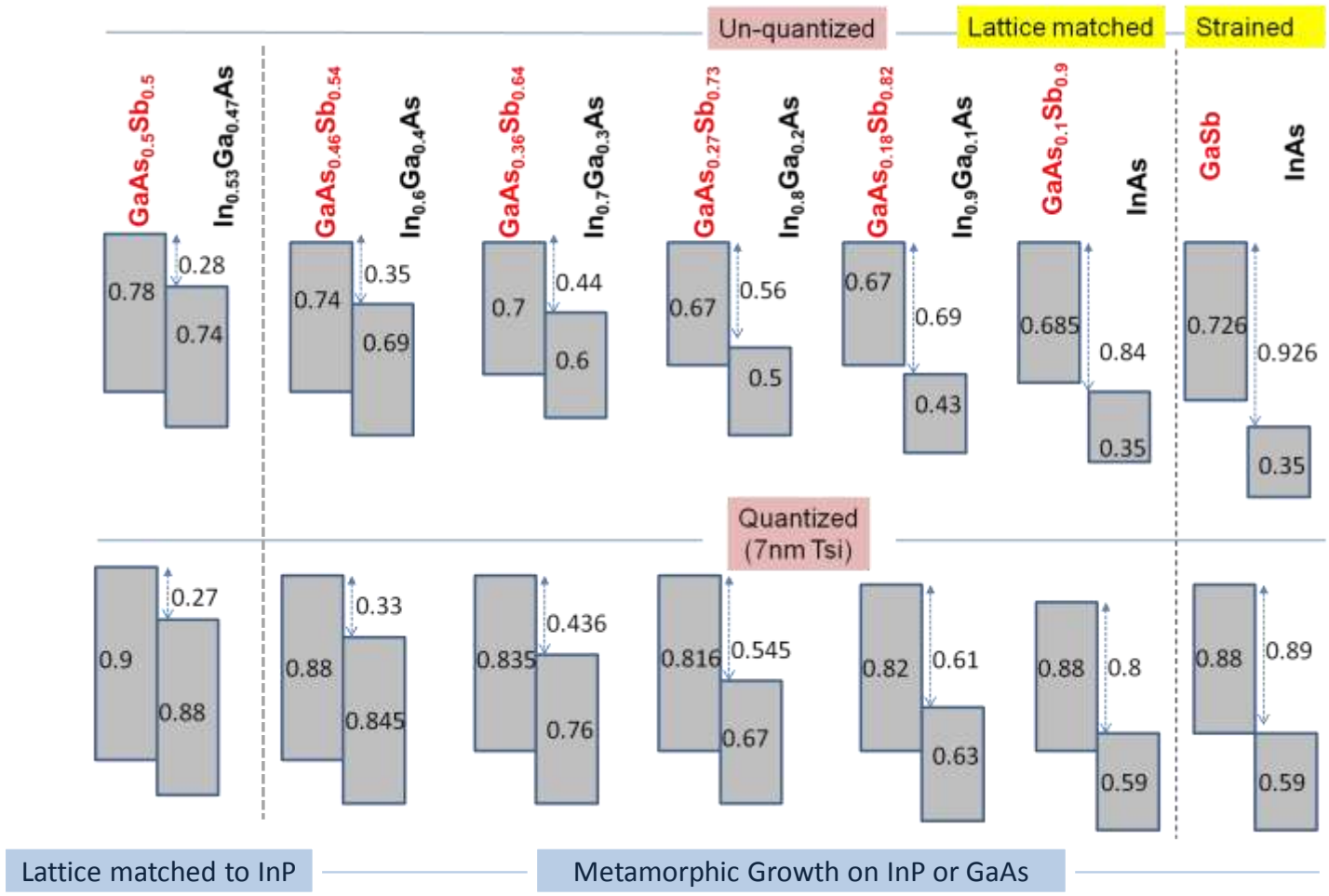



*Animation courtsey M. Luisier (Purdue)*

Two required conditions:

- Thin enough barrier over a large enough area for effective tunneling
- Sufficient density of states on both sides to provide for the carriers

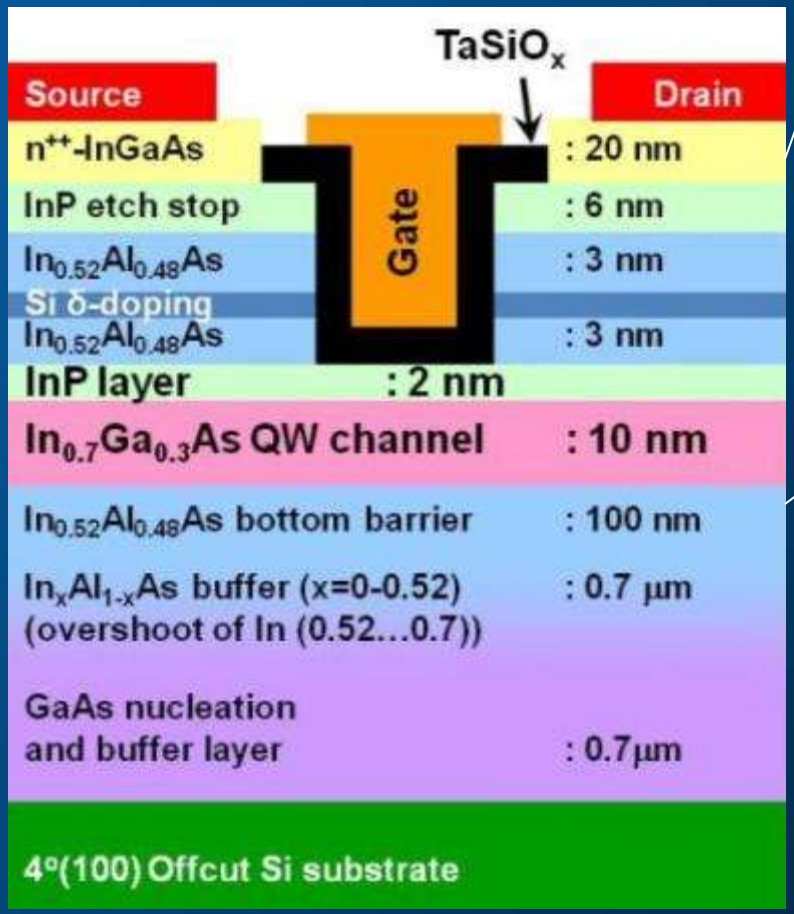
# HTFET Material Considerations

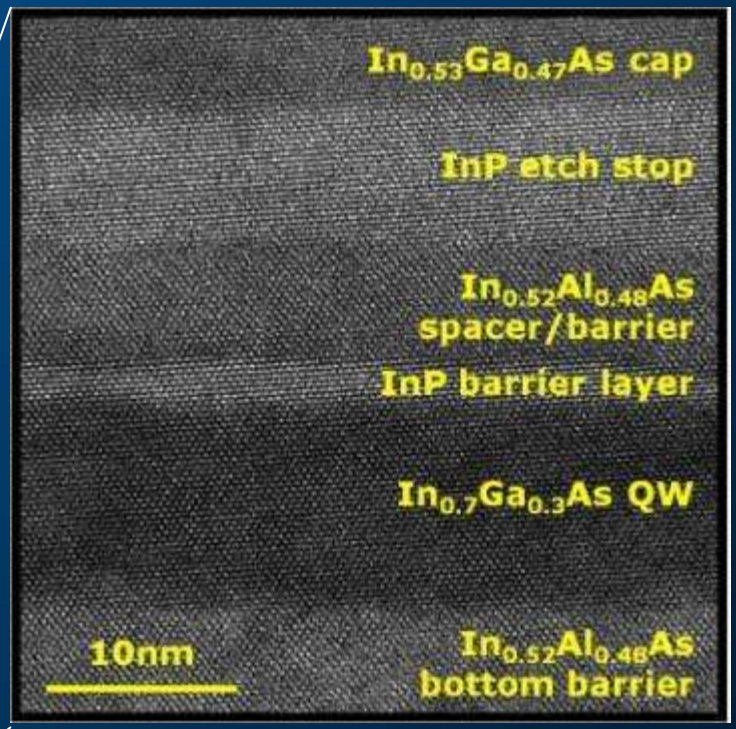



Staggered and broken gap systems have higher tunneling probability.

*Courtesy of Theresa Mayer and Suman Datta, Penn State*

# Fabrication of QWFET with High-K



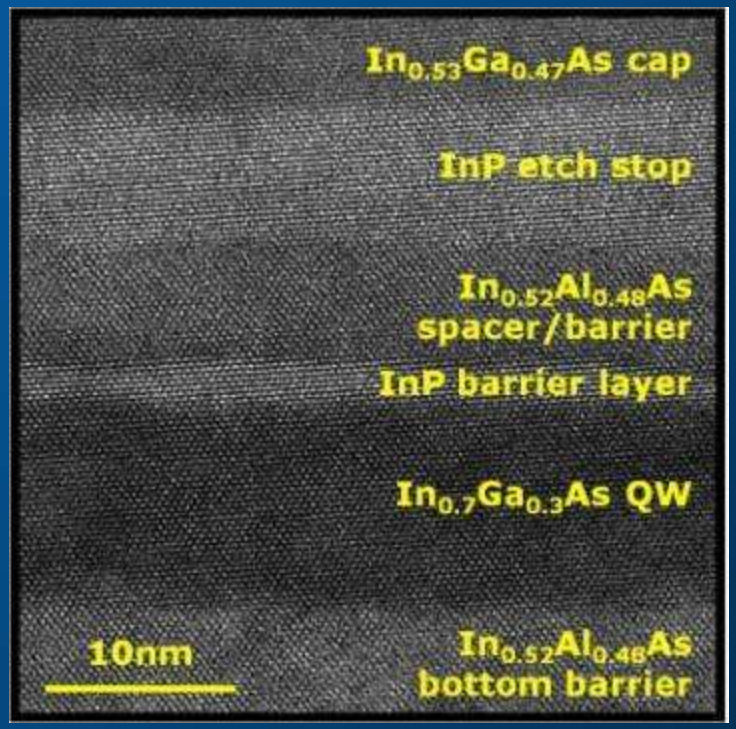




**Fabrication challenges**

- Multiple unique materials
- Molecular Beam Epitaxy & Atomic Layer Deposition used
- **Atomic deposition precision needed across five critical layers**

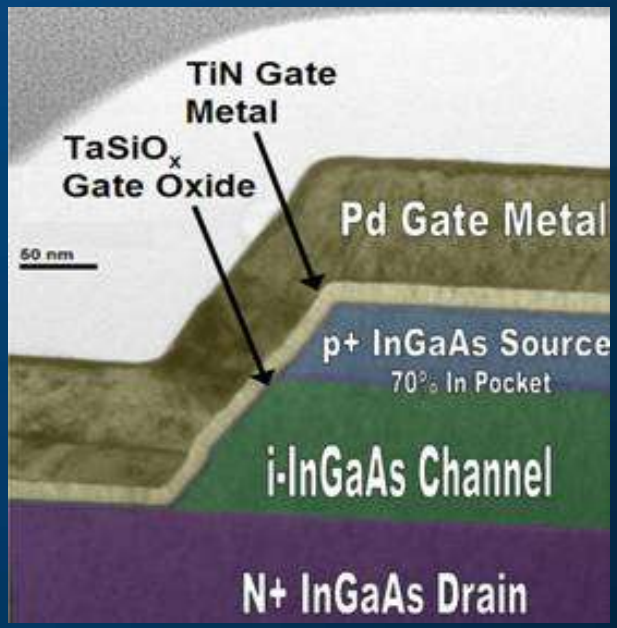
*Radosavljevic et al. IEDM 2009*

# Fabrication of TFET

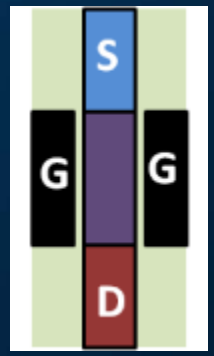



*Radosavljevic et al. IEDM 2009*
*Dewey et al. IEDM 2011*

## What we can make




## What we need to make

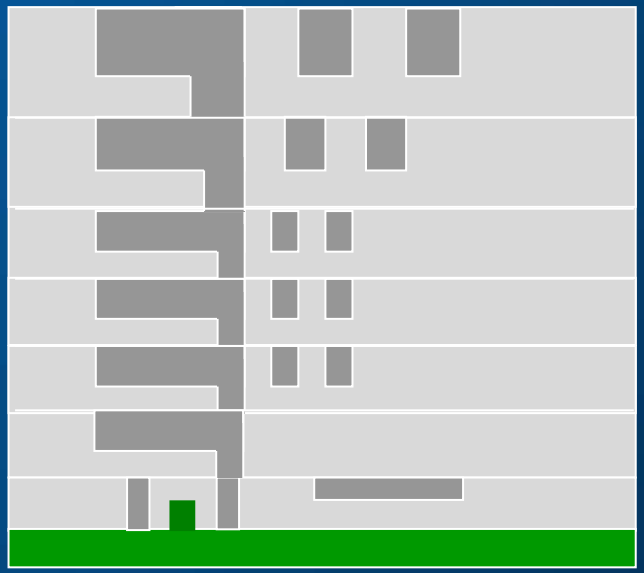



**Fabrication challenges**

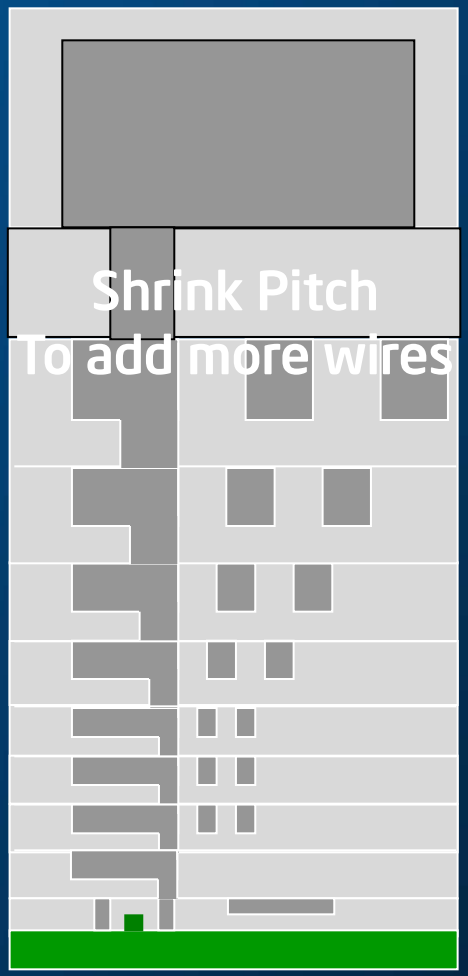
- Multiple unique materials
- Molecular Beam Epitaxy & Atomic Layer Deposition used
- Atomic deposition precision needed across multiple critical layers
- Complex band edge engineering in 3D

# Rethinking Interconnects

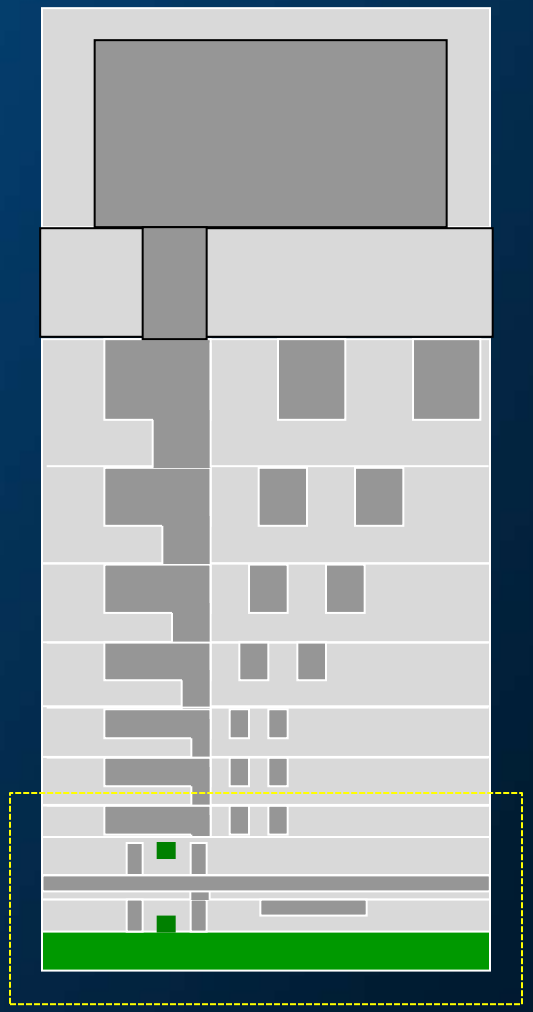
Stack Layers
To add more wires



Shrink Pitch
To add more wires

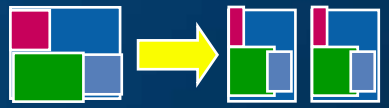


Tinker with
materials

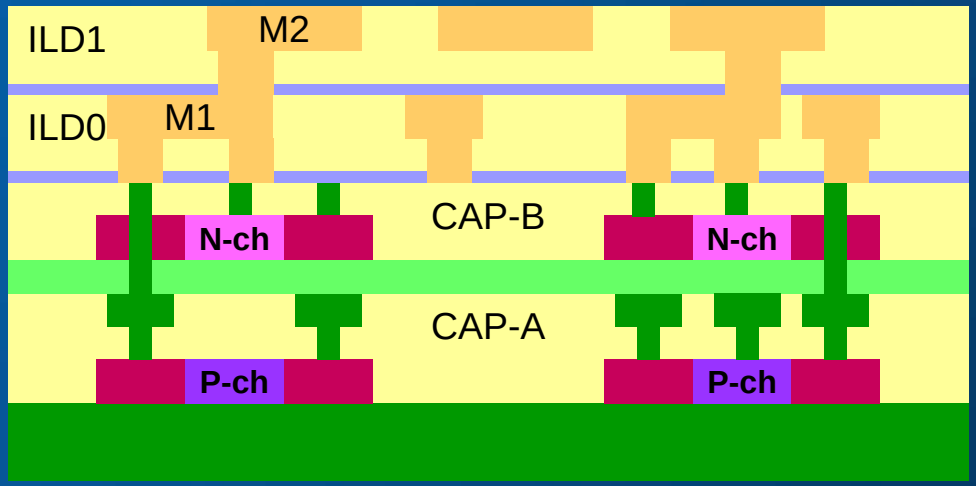


Stack Layers
Above and below
To add more wires
And more devices

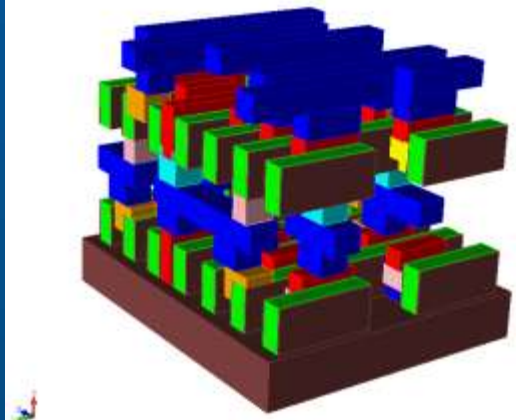
# 3D Technology Progression

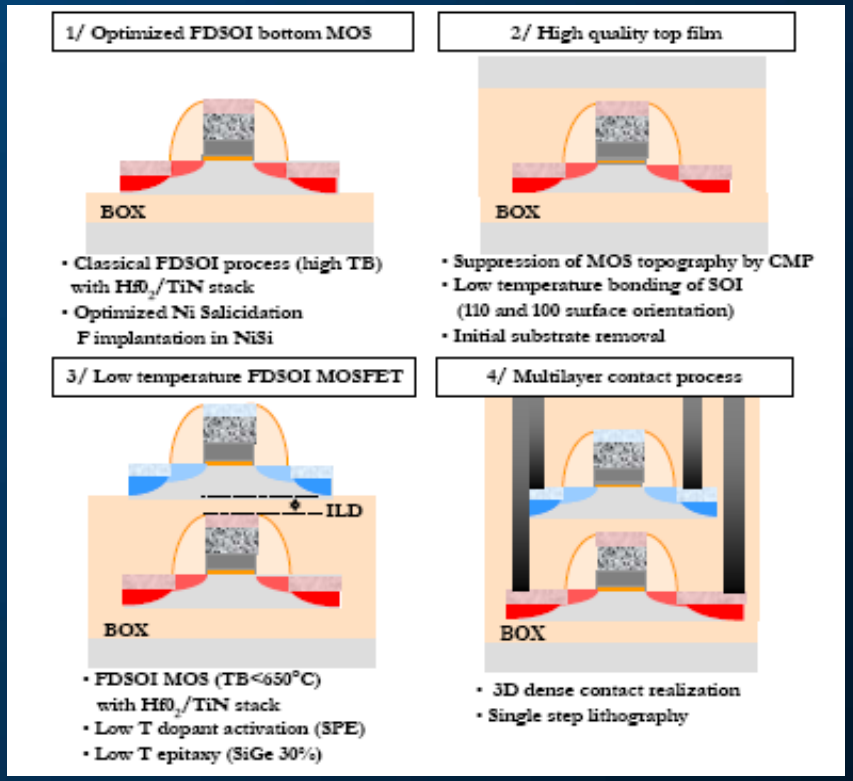
| Possible Application | Bonding/ Fabrication Method | Die-die pitch/ μbump dia/ #connections |
|---|---|---|
| Memory + Logic |  Face to back/DtD | 50μm/20μm<br>~1000s |
| Multiple die stacking |  Face to back/DtD | 40μm/20μm<br>~1000s |
| Smart unit repartitioning (logic+logic) | Face to face/ WtW or DtD   | 5μm/2μm<br>~1M+ |
| Within unit repartitioning (logic+logic) |  Face to face/ WtW or DtD | 1μm/0.5μm<br>~10M-100M |
| Circuit /device repartitioning | Sequential processing  NOT TSV | 5-10nm<br>~10B+ |

# Layer Stack Density Benefit: 30-50%




## Stacked Latch

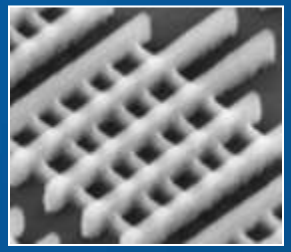


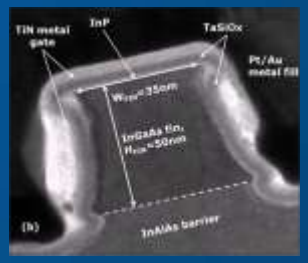


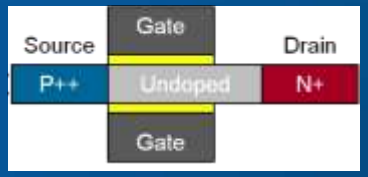

*Source: STM/Leti, 2009 IEDM*

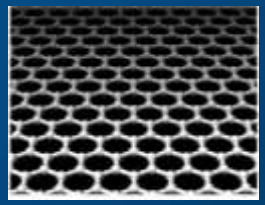
**Widespread use requires new design methods … and some new metrology**

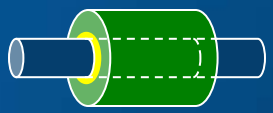
# Heterogeneous System Integration

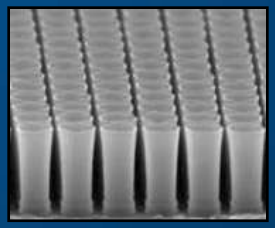


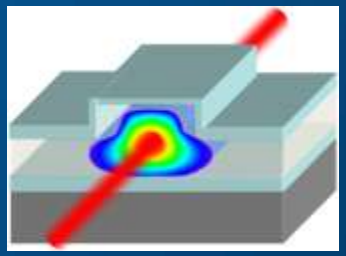


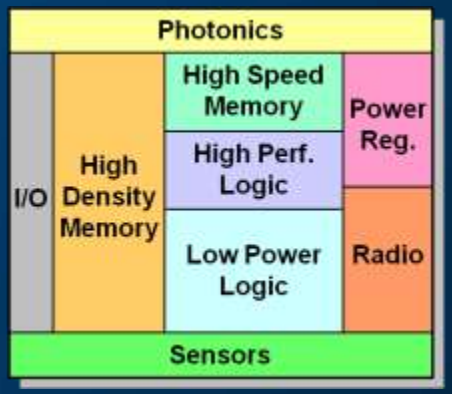





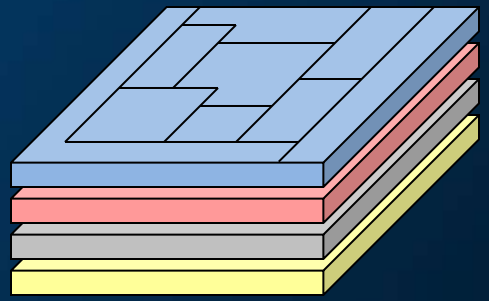




2-D Integration (SoC)




3-D Integration (SiP)

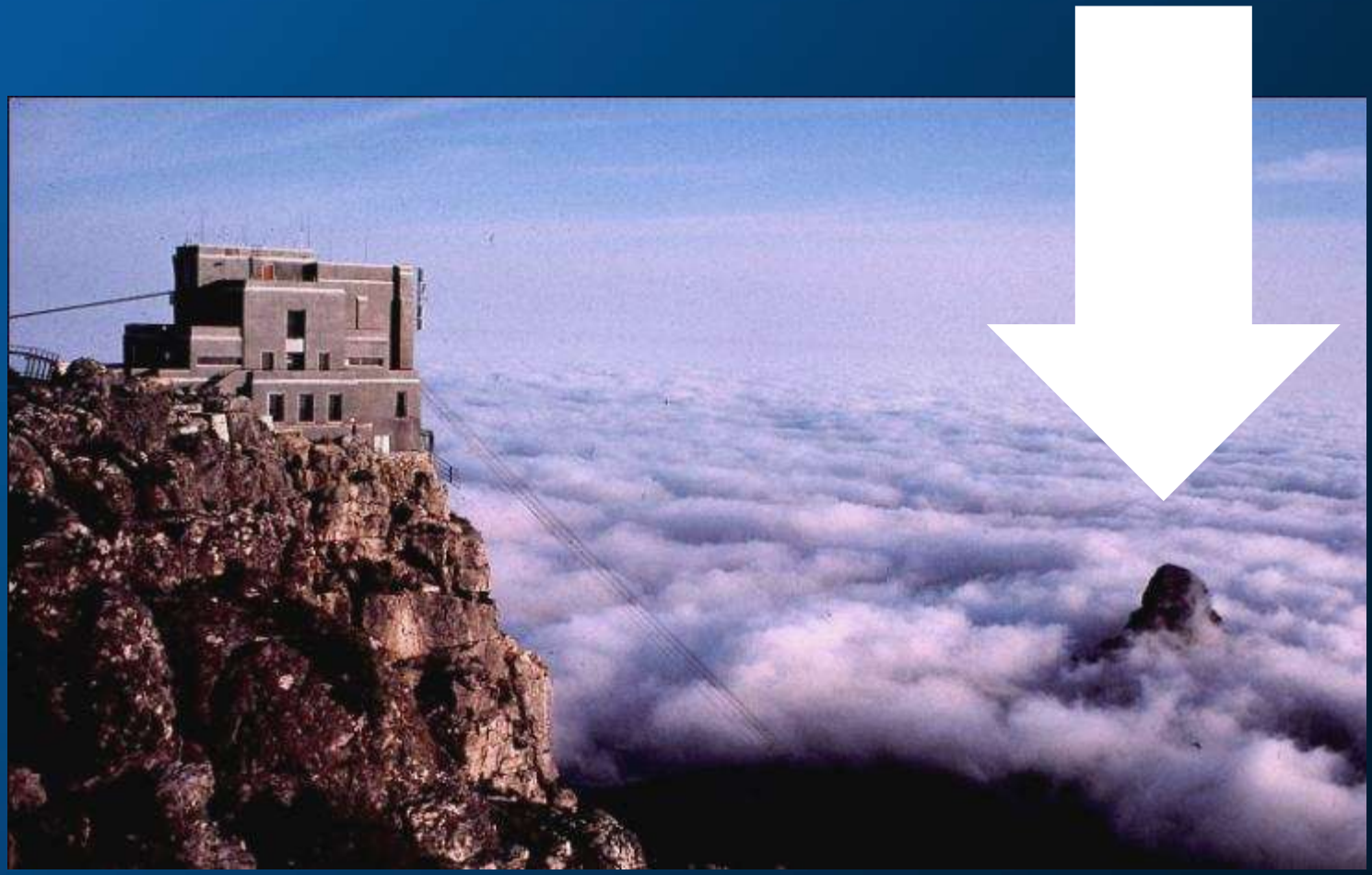


Logic
Memory
Power Reg.
Radio
Sensors
Photonics

Future systems will integrate a much wider variety of materials and device structures

Source: IEDM 2011: *The Evolution of Scaling from the Homogeneous Era to the Heterogeneous Era*, **M. Bohr**

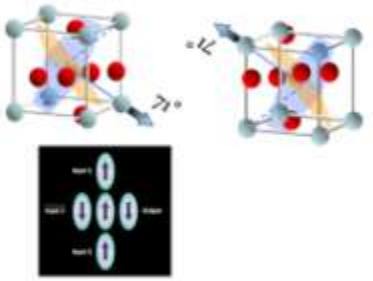
# Pushing beyond the frontier



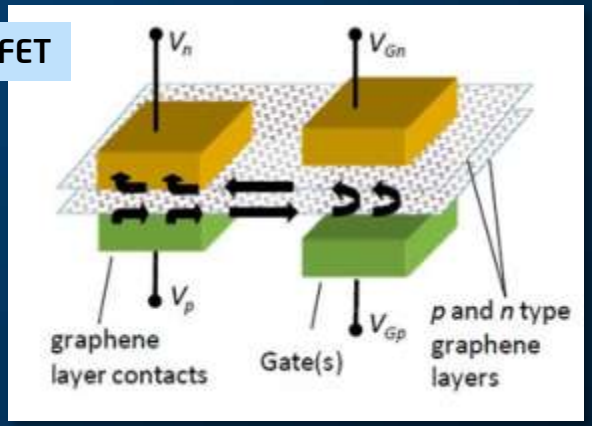
*Source: M. Mayberry*

# Nanoelectronics Research Initiative
## *The Search for Next Switch*

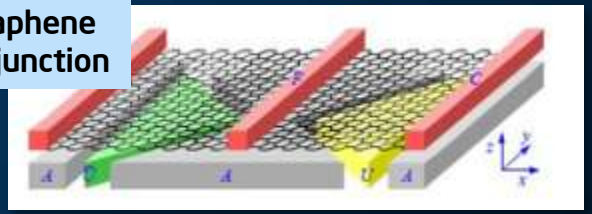
1. Charge, current, voltage (Q,I,V)
2. Electric dipole (P)
3. Magnetic dipole = spin (M)
4. Orbital state (Orb) in e.g. quantum well, molecule, crystal, also excitons, esp. Bose condensate (Cond)



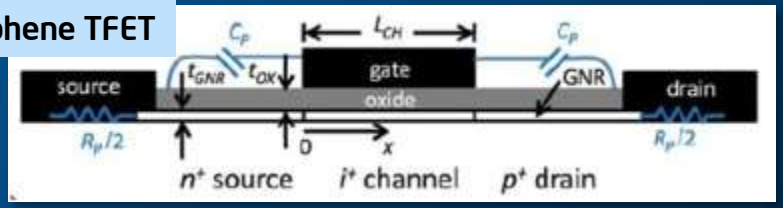

**BiSFET**



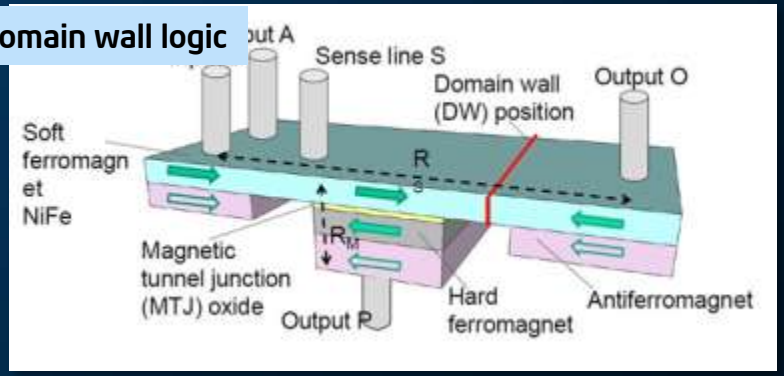

**Graphene PN junction**



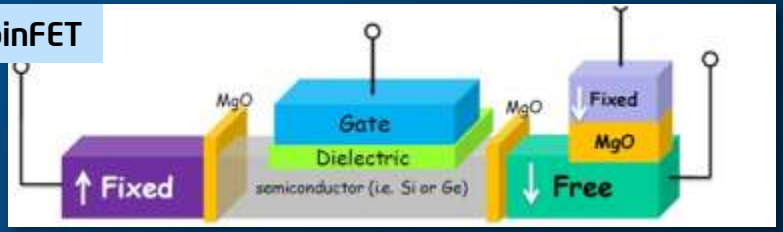
**Graphene TFET**




**Domain wall logic**

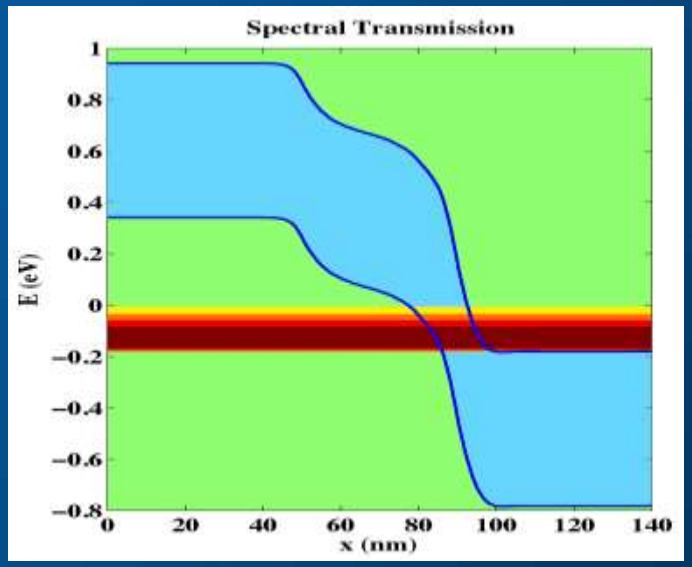



**SpinFET**



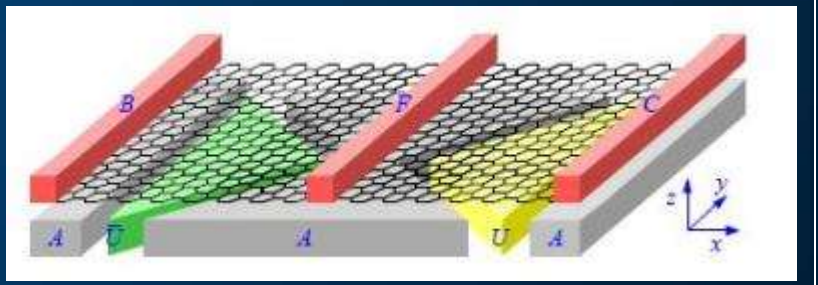

Source: NRI, Intel

# Beyond CMOS Devices - Electronic




Tunneling FET

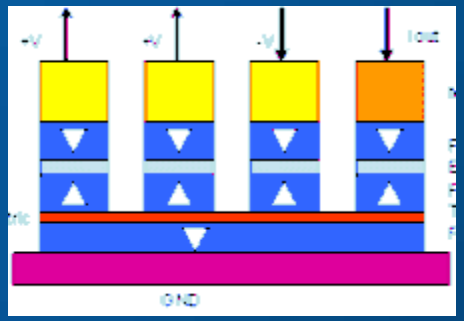
III-V TFET (IIIV TFET)
Heterojunction TFET (HJ TFET)
Graphene Nanoribbon TFET (Gnr TFET)



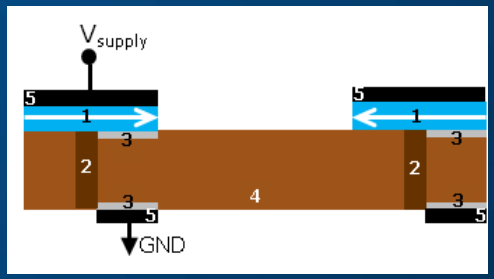

Graphene pn Junction (GpnJ)

*Source: D. Nikonov and I. Young, 2012 IEDM*

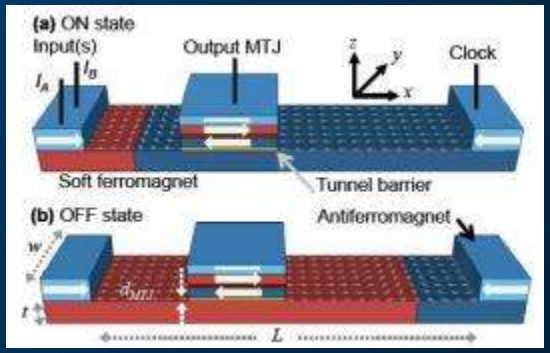
# Beyond CMOS Devices - Noncharge



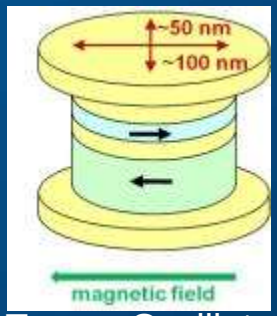
Spin Torque Majority Gate (STMG)



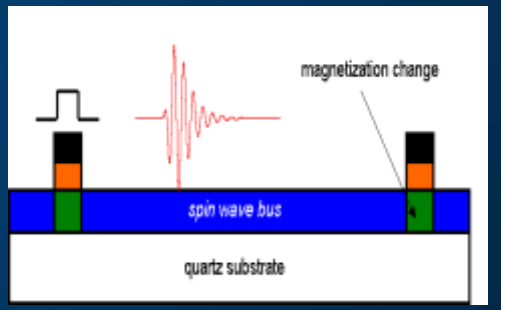

All Spin Logic (ASLD)



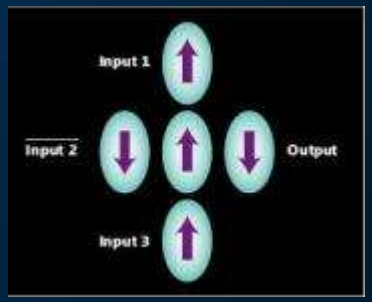

Spin Torque Domain Wall (STT/DW)




Spin Torque Oscillator (STO)




Spin Wave Device (SWD)




Nanomagnetic Logic (NML)

*Source: D. Nikonov and I. Young, 2012 IEDM*

# Rethinking Computational Density

## Compact Full Adder: Non-Boolean Logic

- **Option1:** conventional ASL (44 magnets)
- **Option2:** functionality enhanced ASL (5 magnets)

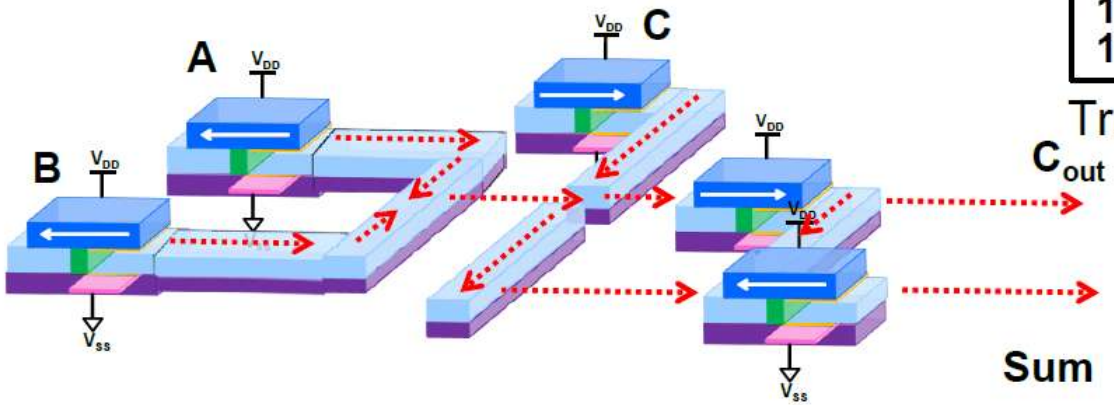
Inputs: A, B and C
Outputs: Sum and Cout

$$Sum = A \oplus B \oplus C$$

$C_{out}$=AB+AC+BC=M (A,B,C)

| A | B | C | C'out | | Sum |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 1 | 1 | 0 |
| 0 | 0 | 1 | 1 | 1 | 1 |
| 0 | 1 | 0 | 1 | 1 | 1 |
| 0 | 1 | 1 | 0 | 0 | 0 |
| 1 | 0 | 0 | 1 | 1 | 1 |
| 1 | 0 | 1 | 0 | 0 | 0 |
| 1 | 1 | 0 | 0 | 0 | 0 |
| 1 | 1 | 1 | 0 | 0 | 1 |

Truth Table for SUM

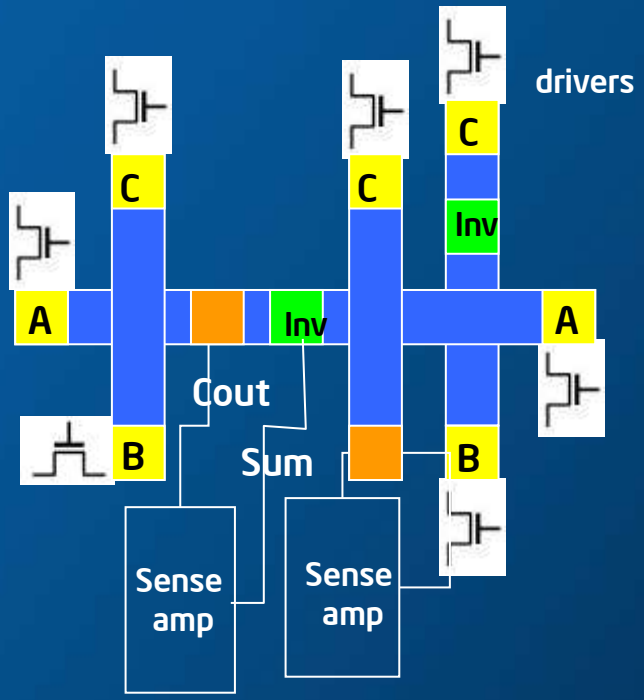


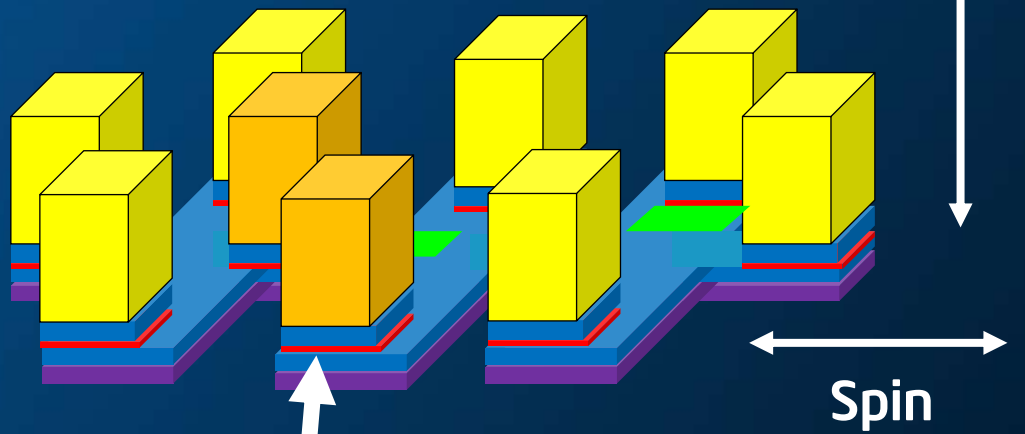

Functionality Enhanced ASL (FEASL)

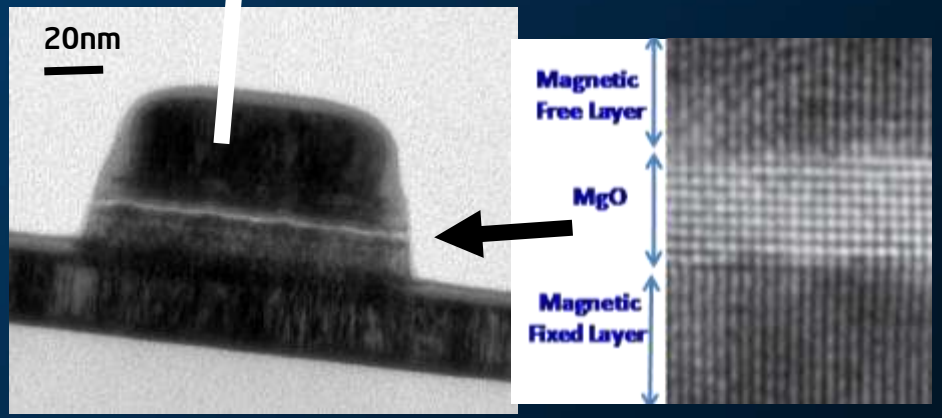
*C. Augustine et al., NanoArch, 2011*

15

# Spintronic Circuit uses Mixed Domains



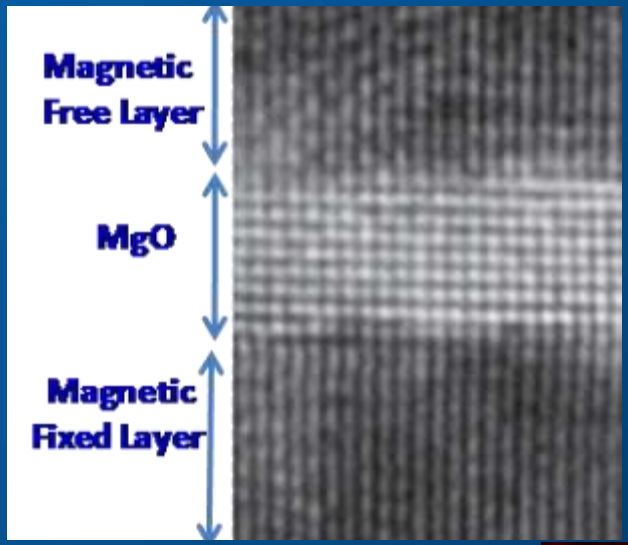




Spin Filter

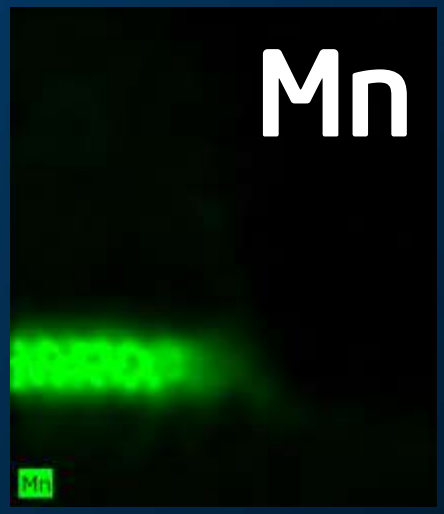
*Source: Intel*

# Fabricating a Spintronic Circuit Requires Precise Metrology & New Ways to Measure State





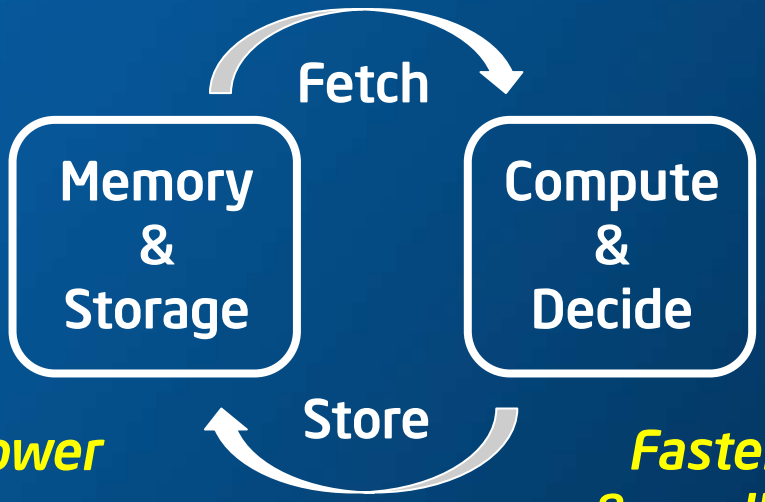






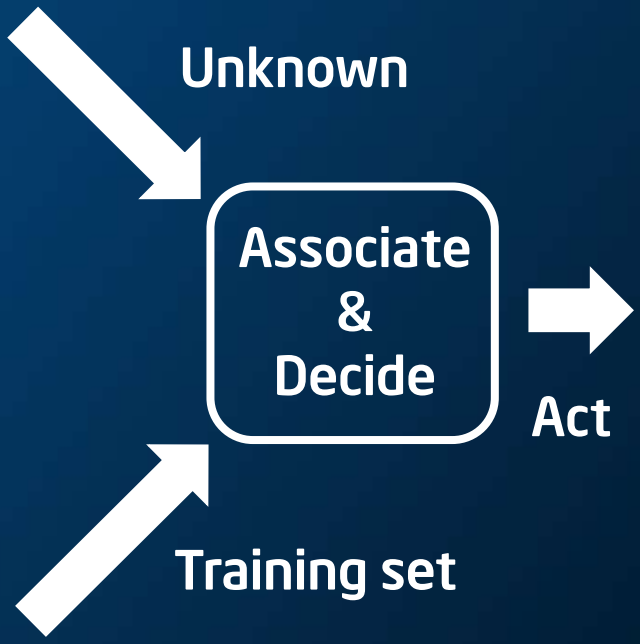
*Source: Intel*

# Exploring Other Ways to Compute




"Von Neumann"

*Bottleneck = memory/storage*
*Transport limited devices make it worse*

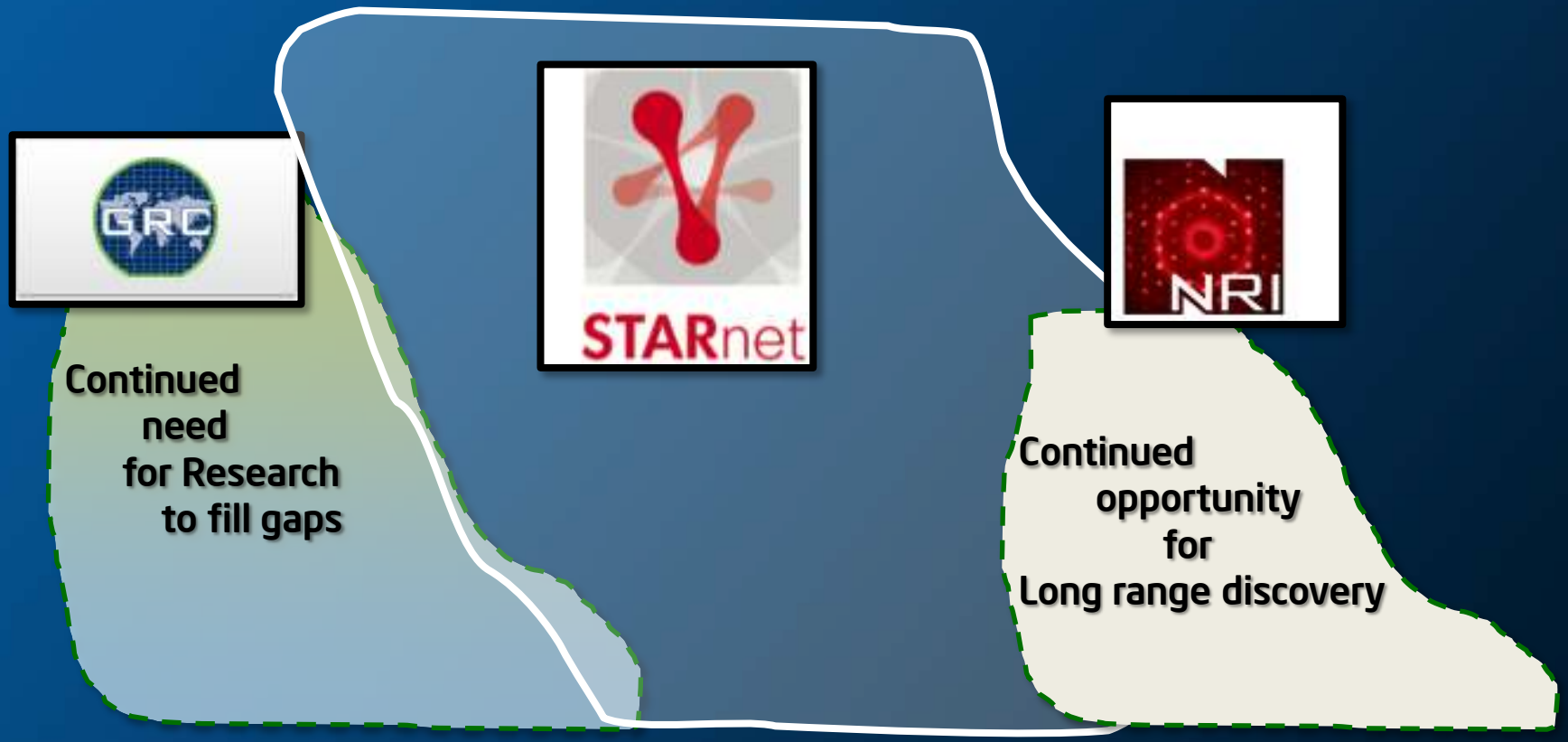



*Bottleneck = training*
*Potentially favorable for novel devices*

# As We Recognize Inflection Points Coming We Start the Needed Research


*Source: SRC*

# Planned Research Landscape




| GRC-Industry | Industry-DARPA | Industry-NIST-NSF |
|---|---|---|
| Ongoing selections | 2012 selections | 2013 selections |

*Source: SRC*

# Key Points

- Novel materials in complex 3D structures are here now and will be increasingly prevalent going into the future
- Metrology and characterization are vital to develop, improve, and control advanced manufacturing processes
- New methods are needed to image in three dimensions and to measure new material properties such as spin
- New metrology research is needed now in order to be ready as these process challenges unfold

# Thank You


intel

# Risk Factors

The above statements and any others in this document that refer to plans and expectations for the first quarter, the year and the future are forward-looking statements that involve a number of risks and uncertainties. Words such as “anticipates,” “expects,” “intends,” “plans,” “believes,” “seeks,” “estimates,” “may,” “will,” “should” and their variations identify forward-looking statements. Statements that refer to or are based on projections, uncertain events or assumptions also identify forward-looking statements. Many factors could affect Intel’s actual results, and variances from Intel’s current expectations regarding such factors could cause actual results to differ materially from those expressed in these forward-looking statements. Intel presently considers the following to be the important factors that could cause actual results to differ materially from the company’s expectations. Demand could be different from Intel's expectations due to factors including changes in business and economic conditions, including supply constraints and other disruptions affecting customers; customer acceptance of Intel’s and competitors’ products; changes in customer order patterns including order cancellations; and changes in the level of inventory at customers. Uncertainty in global economic and financial conditions poses a risk that consumers and businesses may defer purchases in response to negative financial events, which could negatively affect product demand and other related matters. Intel operates in intensely competitive industries that are characterized by a high percentage of costs that are fixed or difficult to reduce in the short term and product demand that is highly variable and difficult to forecast. Revenue and the gross margin percentage are affected by the timing of Intel product introductions and the demand for and market acceptance of Intel's products; actions taken by Intel's competitors, including product offerings and introductions, marketing programs and pricing pressures and Intel’s response to such actions; and Intel’s ability to respond quickly to technological developments and to incorporate new features into its products. Intel is in the process of transitioning to its next generation of products on 22nm process technology, and there could be execution and timing issues associated with these changes, including products defects and errata and lower than anticipated manufacturing yields. The gross margin percentage could vary significantly from expectations based on capacity utilization; variations in inventory valuation, including variations related to the timing of qualifying products for sale; changes in revenue levels; product mix and pricing; the timing and execution of the manufacturing ramp and associated costs; start-up costs; excess or obsolete inventory; changes in unit costs; defects or disruptions in the supply of materials or resources; product manufacturing quality/yields; and impairments of long-lived assets, including manufacturing, assembly/test and intangible assets. The majority of Intel’s non-marketable equity investment portfolio balance is concentrated in companies in the flash memory market segment, and declines in this market segment or changes in management’s plans with respect to Intel’s investments in this market segment could result in significant impairment charges, impacting restructuring charges as well as gains/losses on equity investments and interest and other. Intel's results could be affected by adverse economic, social, political and physical/infrastructure conditions in countries where Intel, its customers or its suppliers operate, including military conflict and other security risks, natural disasters, infrastructure disruptions, health concerns and fluctuations in currency exchange rates. Expenses, particularly certain marketing and compensation expenses, as well as restructuring and asset impairment charges, vary depending on the level of demand for Intel's products and the level of revenue and profits. Intel’s results could be affected by the timing of closing of acquisitions and divestitures. Intel's results could be affected by adverse effects associated with product defects and errata (deviations from published specifications), and by litigation or regulatory matters involving intellectual property, stockholder, consumer, antitrust and other issues, such as the litigation and regulatory matters described in Intel's SEC reports. An unfavorable ruling could include monetary damages or an injunction prohibiting us from manufacturing or selling one or more products, precluding particular business practices, impacting Intel’s ability to design its products, or requiring other remedies such as compulsory licensing of intellectual property. A detailed discussion of these and other factors that could affect Intel’s results is included in Intel’s SEC filings, including the annual report on Form 10-K for the fiscal year ended December 31, 2012.