Crolles2 Alliance

2005 International Conference on
Characterization and Metrology for ULSI Technology, Dallas, USA

Launched by Motorola
freescale™
semiconductor

PHILIPS

The Role of a Physical Analysis Laboratory in a 300 mm IC Development & Manufacturing Centre

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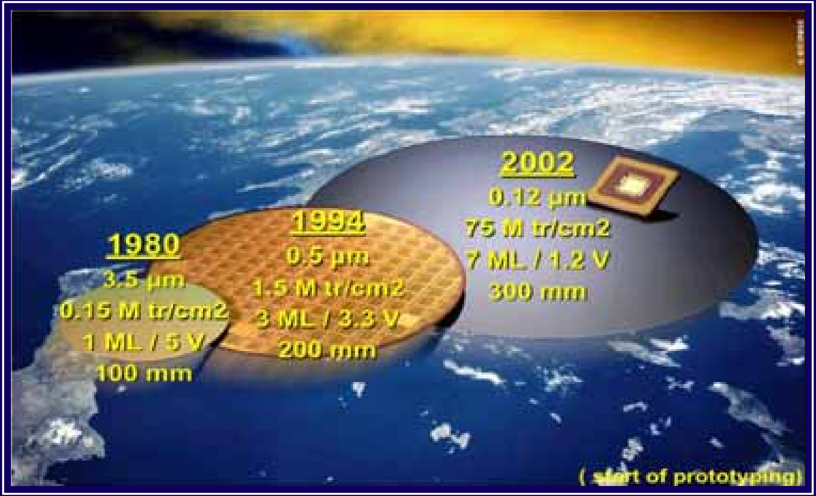
Outline

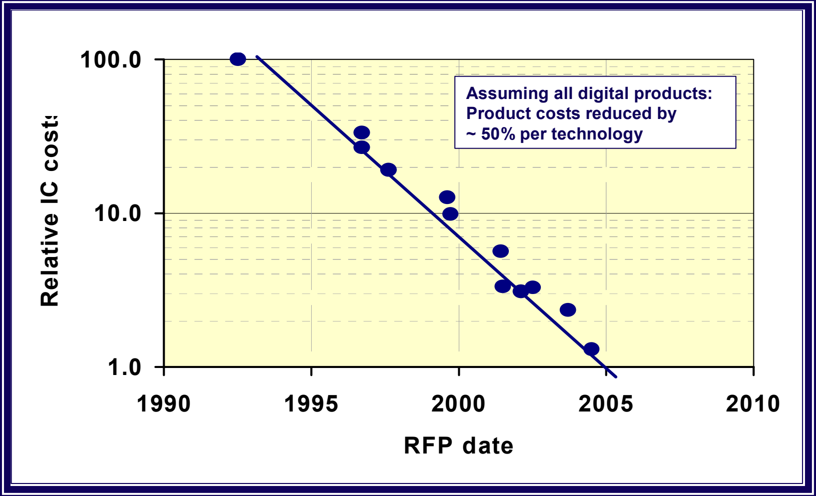
- **Business challenges**
- **Crolles 2 Alliance**
- **Characterization and Metrology strategy**
  - Microscopy, Materials Analysis
  - Full wafer systems, benefits & economics
  - Failure Analysis, the need for better precision & resolution
- **Conclusions & Perspectives**

IC Manufacturing Trends

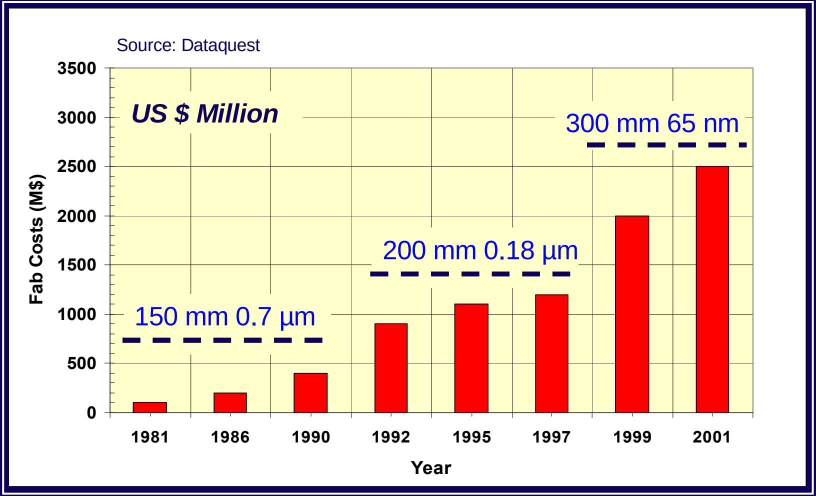
Complexity increase…



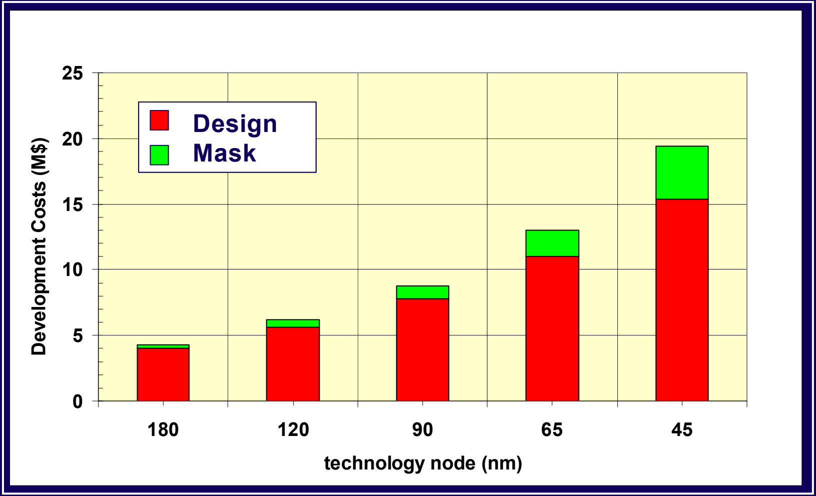
Price erosion…



Fab Costs explosion…

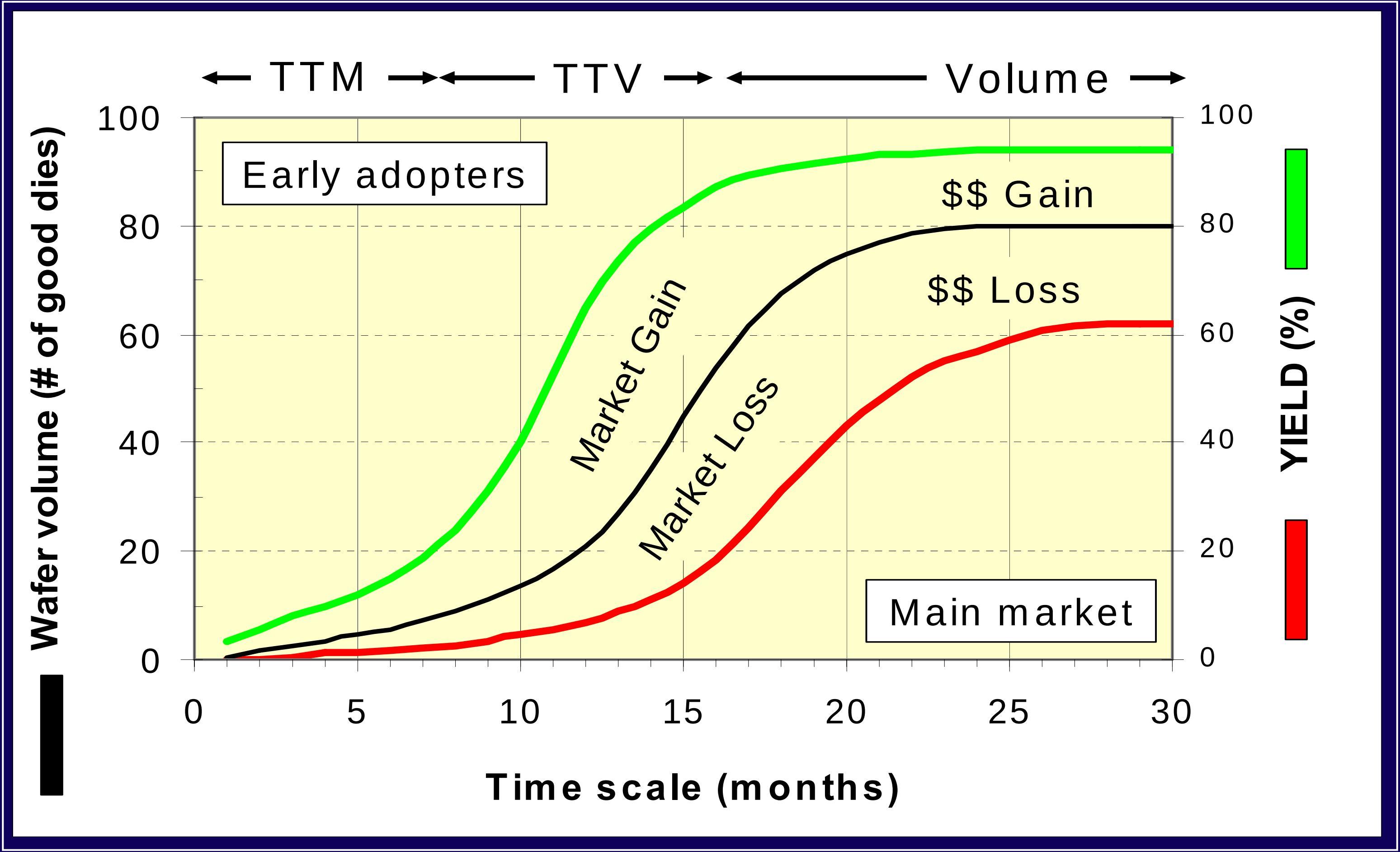


Design Costs explosion…



Semiconductor Business Challenges

The Dollar Gap…



The Winner takes it all…

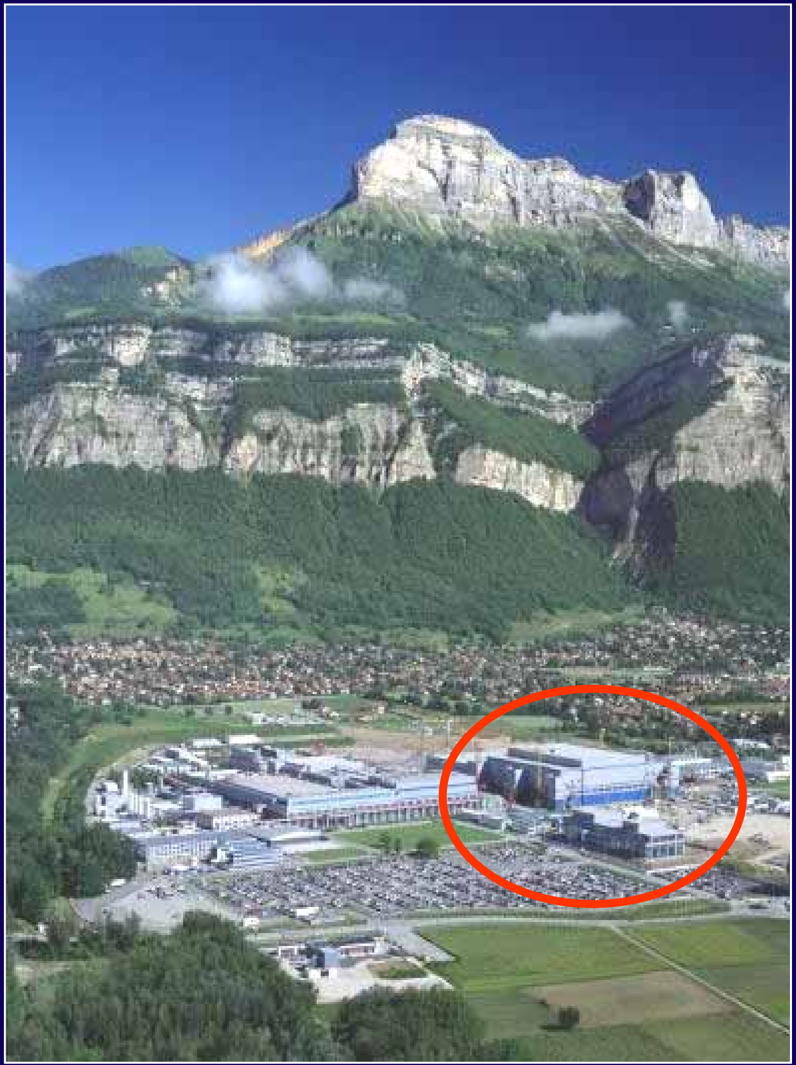
Crolles 2 Alliance Strategy

to capture market our priorities are :

- **First time right**
- **Time to Market (TTM)**
  - **Technology development, prototyping**
- **Time to Volume (TTV)**
  - **Process control & Yield ramp**

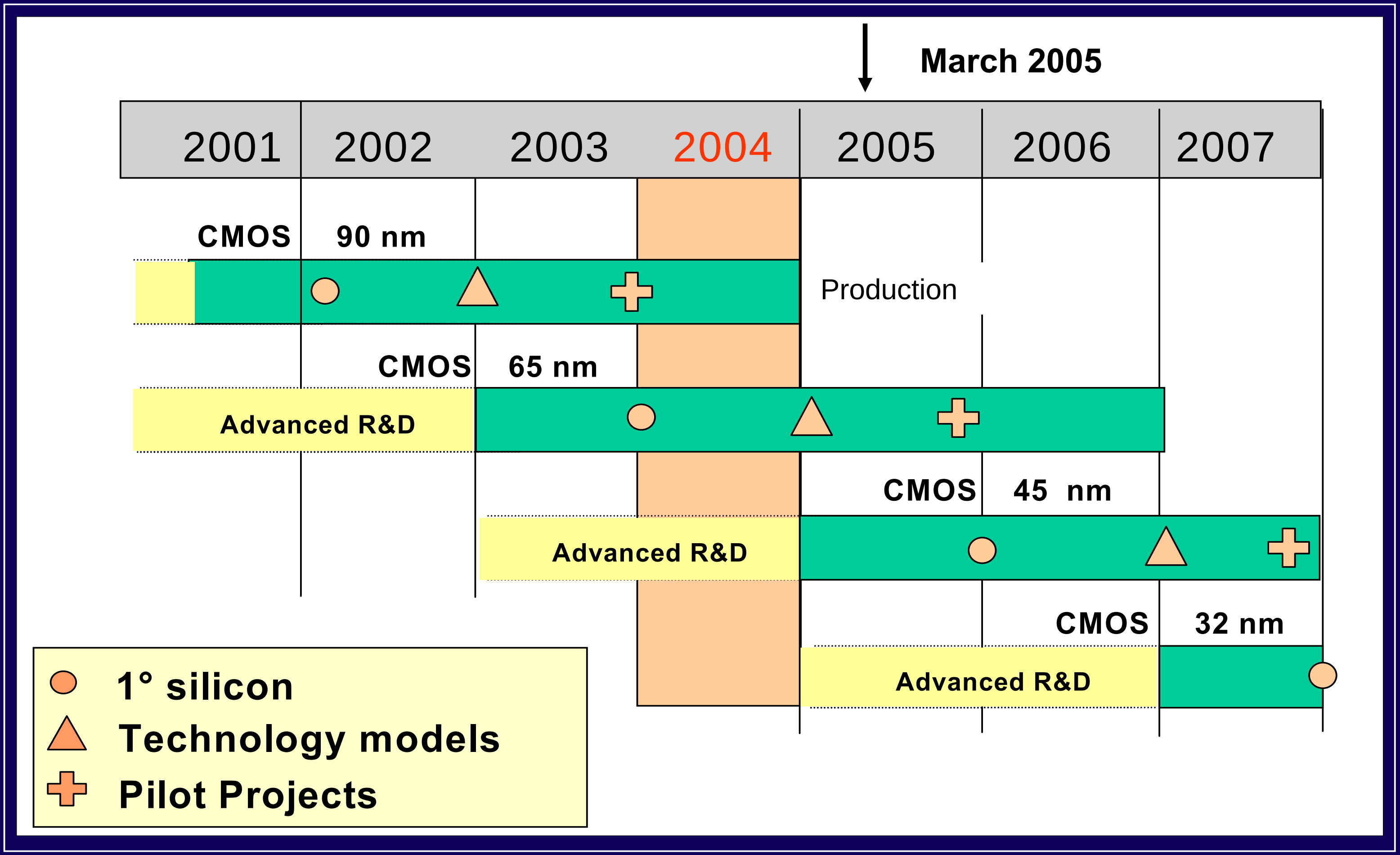
→ ***Cycle time and Yield are key!***

Crolles 2: The Joint R&D and Pilot Fab

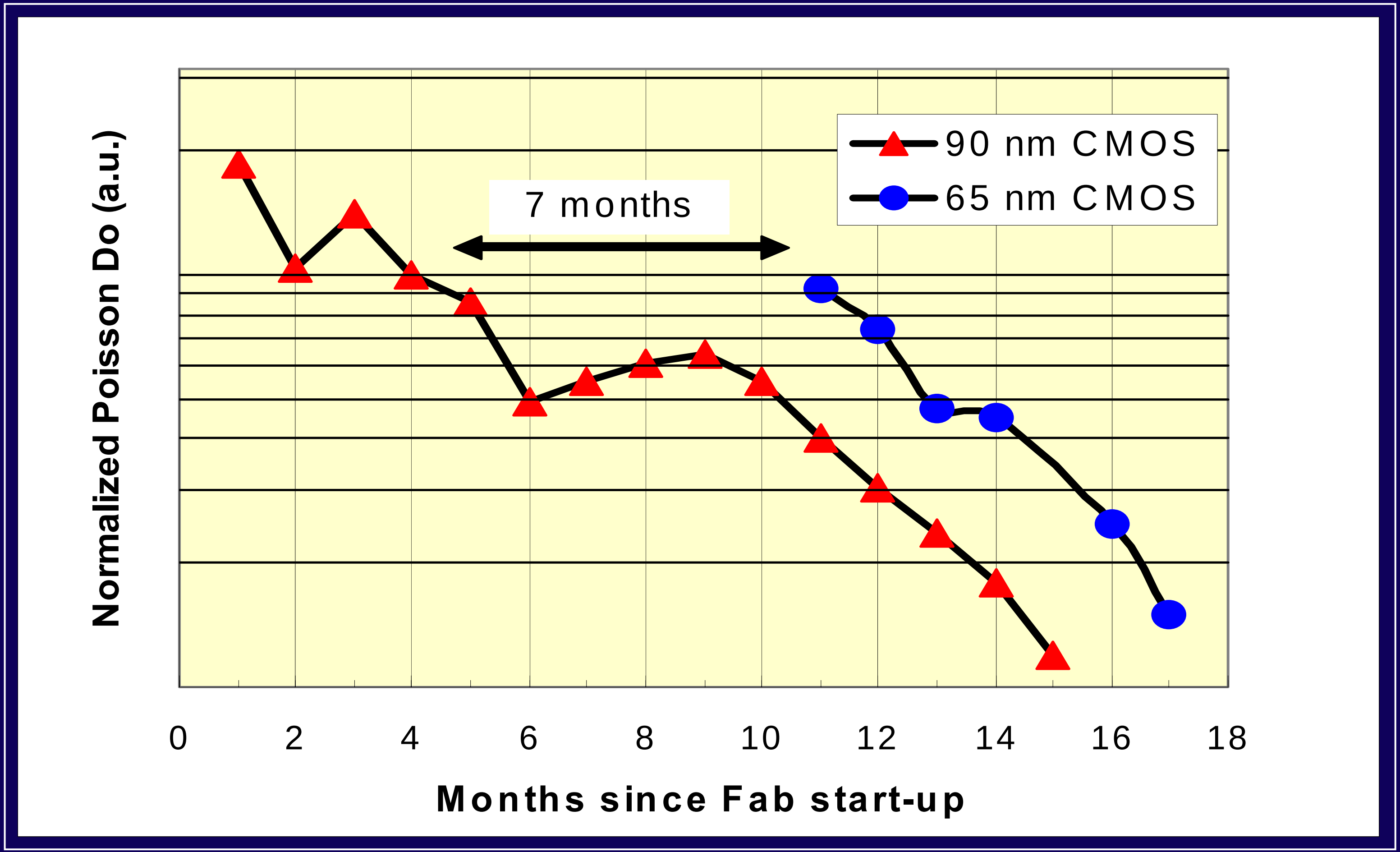


- **Partnership between ST Philips and Freescale**
  - R&D & pilot fab Crolles 2
  - 120, 90, 65, 45nm processes
  - Bulk CMOS, SOI, EDRAM
  - Std Libraries shared
  - First products in 2003
- **300 mm Pilot line**
  - Clean room: 5000 m^2
  - 1.4 B$ investment
  - 1200 people

Crolles 2 : CMOS Technology Roadmap



Crolles 2 : Yield and Learning cycles



Off-line Characterization support

Without fault isolation
R&D support
Process development

With fault isolation
Yield loss analysis

Voltage Contrast
Test structure

OBIRCH
Test structure
Product

Bitmap
Memories

Physical characterization
FIB, SEM, TEM, EELS, AES, TOF-SIMS, XRR, XRD…

Off-line Characterization support

Without fault isolation

R&D support

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OBIRCH

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Bitmap

Memories

Physical characterization

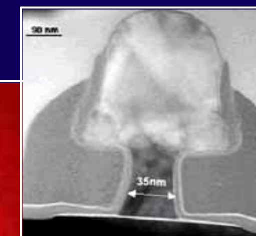
FIB, SEM, TEM, EELS, AES, TOF-SIMS, XRR, XRD…

MICROSCOPY

Physical Characterization: Microscopy

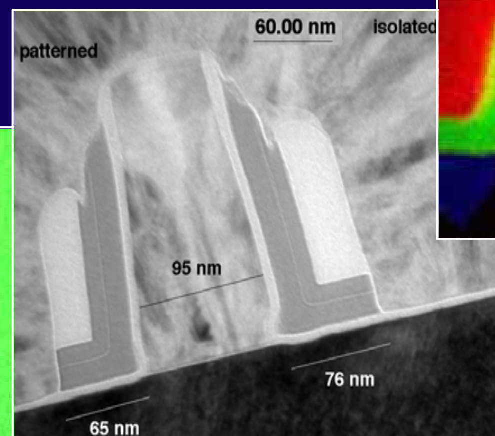
Transistor scaling…

32 nm transistor

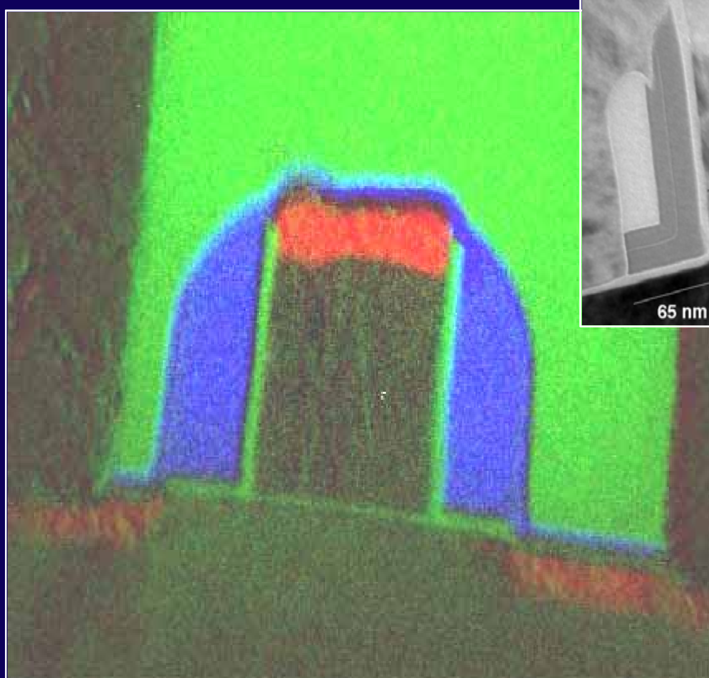


65 nm transistor

90 nm transistor

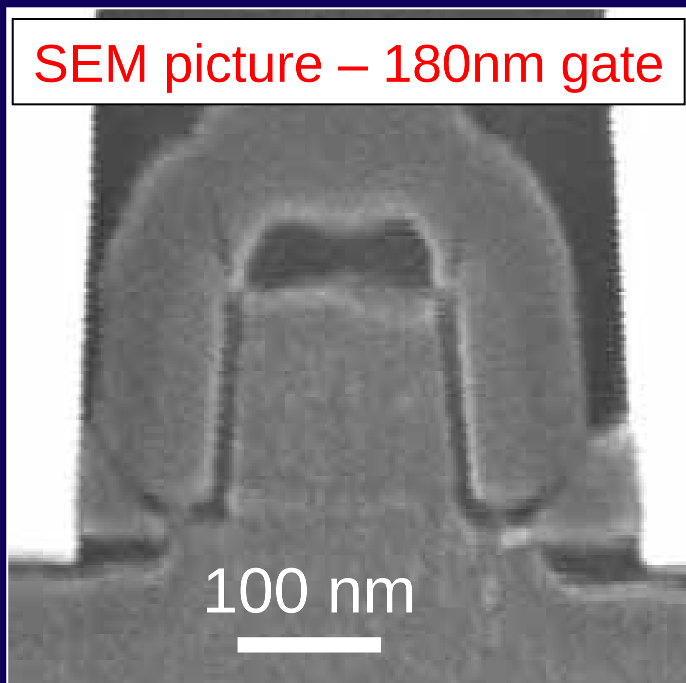


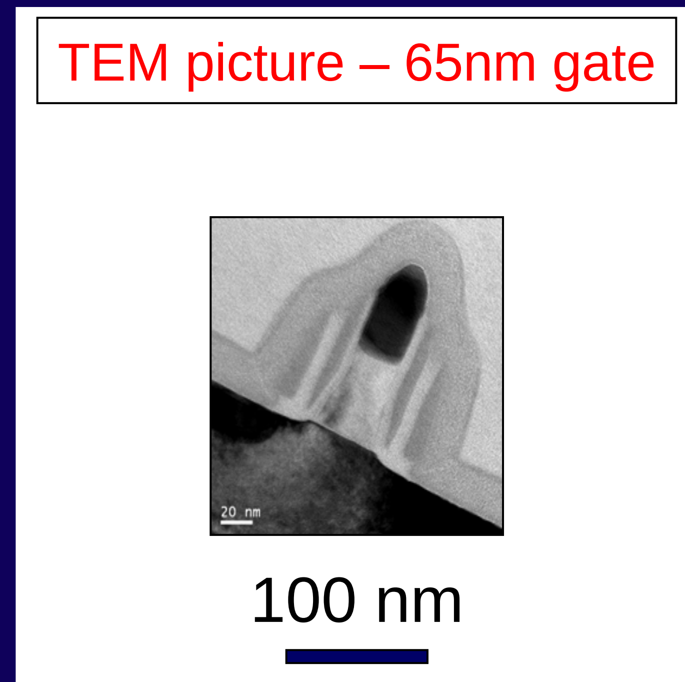
180 nm transistor



Physical Characterization: Microscopy

Structural analysis: SEM / TEM



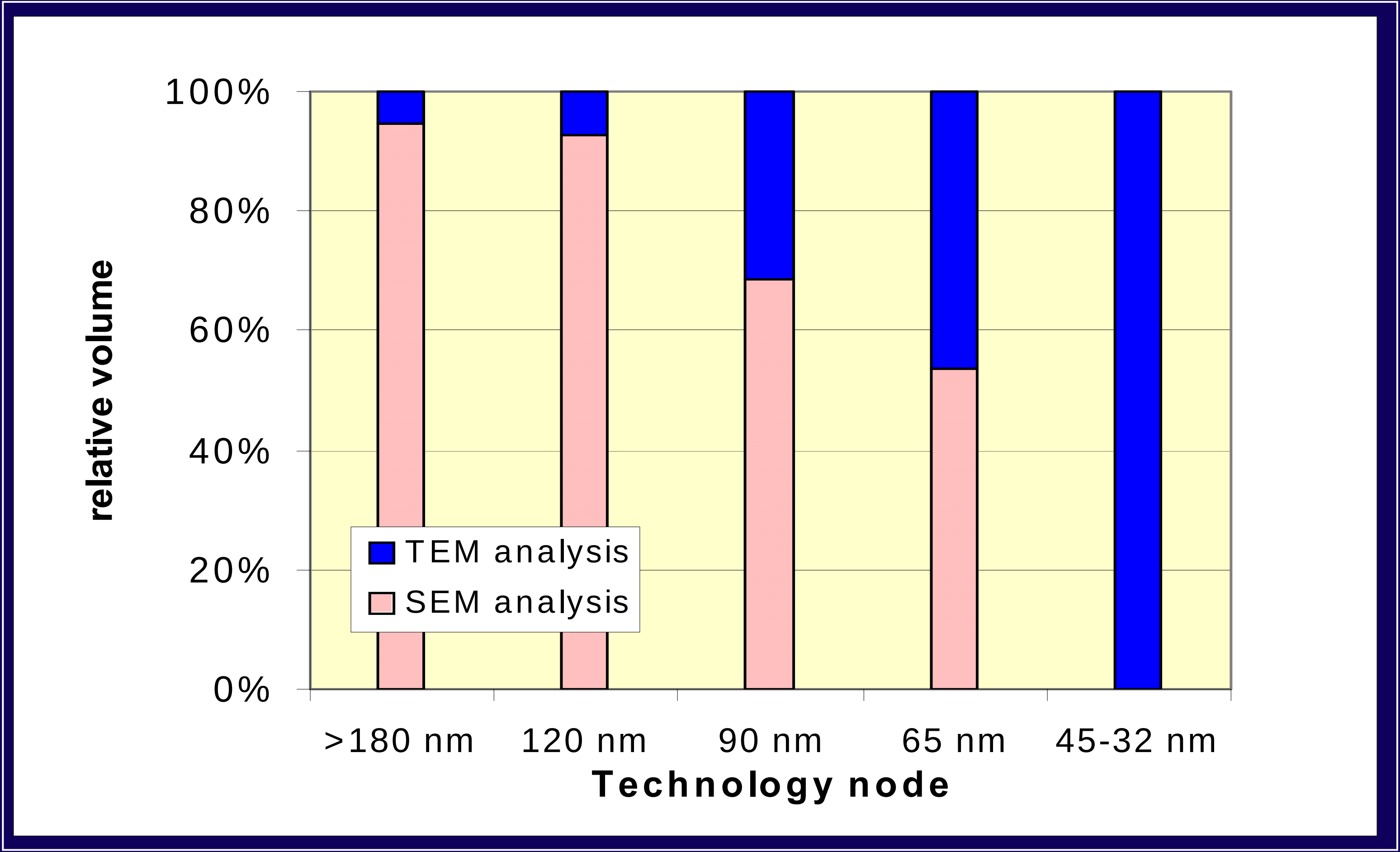


Details difficult to detect with SEM

- 180 nm Technology: 90% SEM – 10% TEM
- 65 nm Technology: 55% SEM – 45% TEM

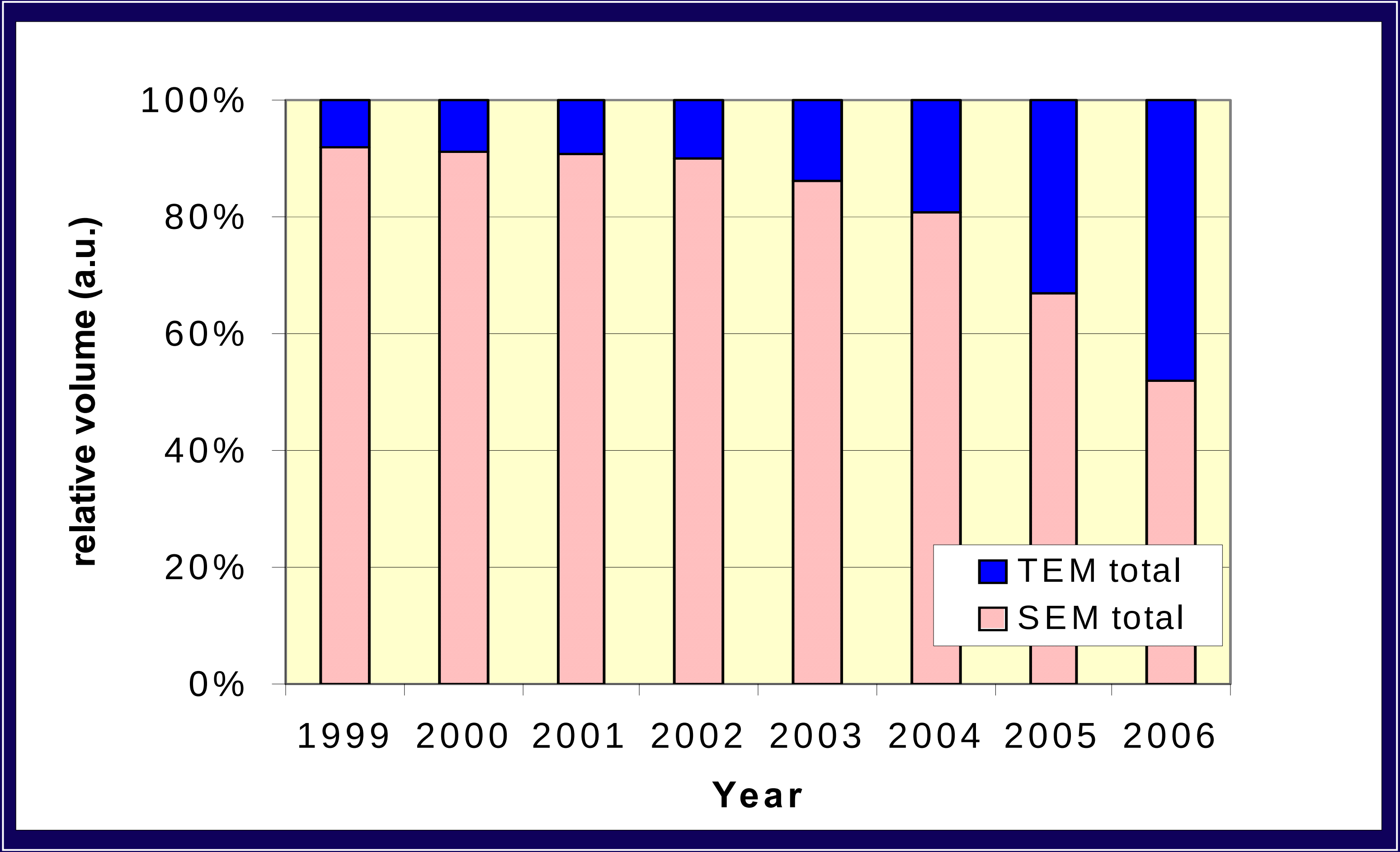
Microscopy: SEM is out…!

65 and 45 nm CMOS developments require TEM…



Microscopy: TEM is in… but we need more!

SEM volume stagnates, TEM volume increases…



But TEM is not a volume technique yet…

Microscopy: Economics of SEM vs. TEM

- **SEM activity until now**
  - Volume: 3000 – 5000 samples / year
  - Cycle time: 1 – 5 days
  - Equipment: 3 SEM's, 2 FIB's, ~ 4 M$ Capex
  - ➔ ~ 200 – 300 $ / sample
- **TEM activity until now**
  - Volume: 400 – 800 samples / year
  - Cycletime: 2 – 10 days
  - Equipment: 2 FIB/SEM's, 2 TEM's, ~ 7 M$ Capex
  - ~ 2000 – 4000 $ / sample

➔ ***Costs / sample is rather prohibitive….***

Microscopy: an Industrial TEM line

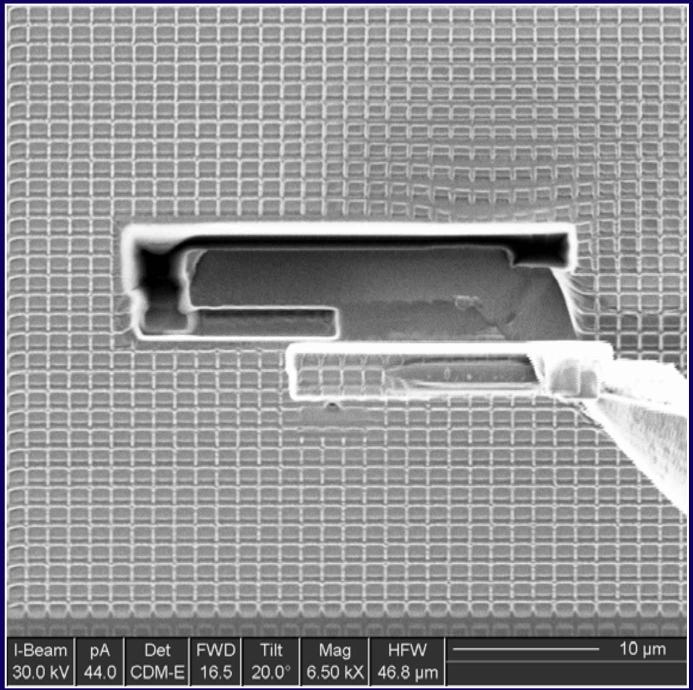
- **Boost TEM volume, improve cycle times**
  - Volume: 1500 – 3000 samples / year
  - Cycle time: 1 – 5 days
  - Equipment: 3 FIB/SEM's, 2 TEM's, ~ 9 M$ Capex
  - ~ 600 – 1200 $ / sample

  ➔ *Focus on high value added TEM data!*

- **Strategy:**
  - 300 mm FIB/SEM for non - destructive sample pluck
  - 300 mm Wafer Return into process flow
  - Small chamber FIB/SEM for final sample preparation
  - Fully equipped (EELS/EDX) TEM systems for analysis

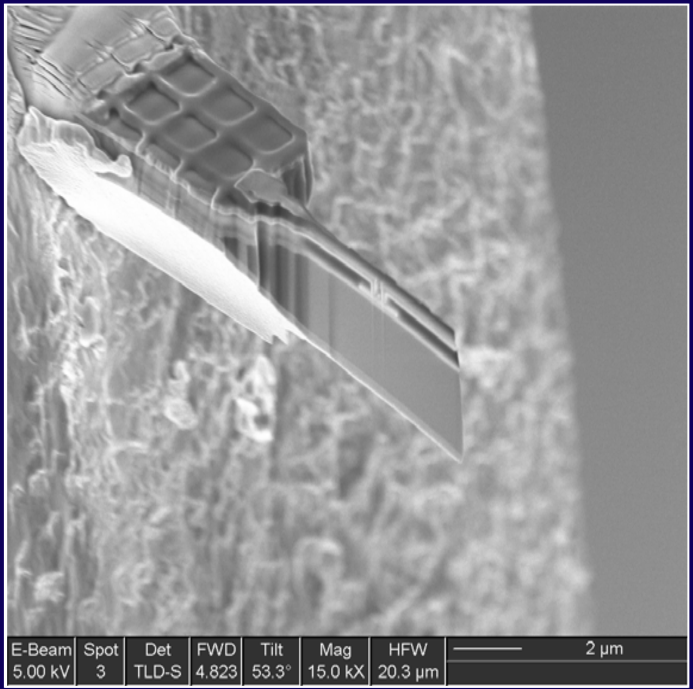
TEM Microscopy: TEM lamella preparation

TEM lamella creation process



90 % yield

Chunk milling process and In-situ extraction in 300 mm FIB/SEM system

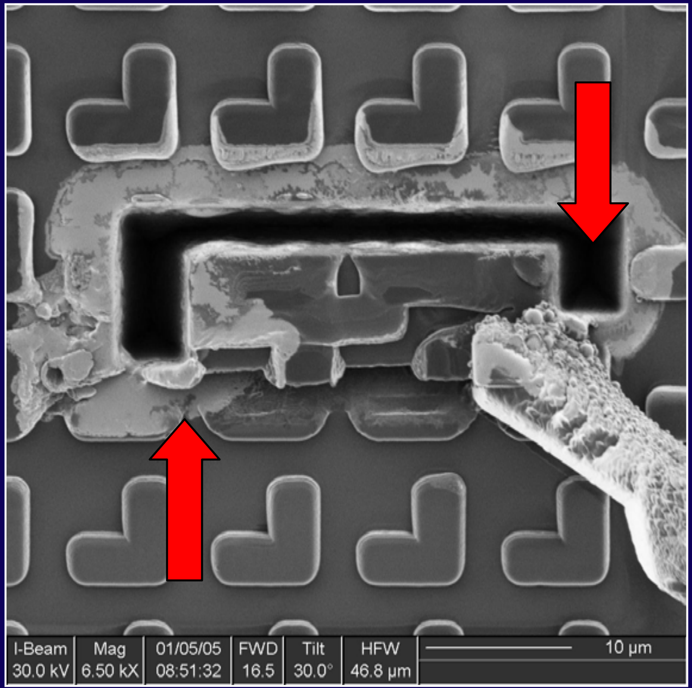


80 % yield

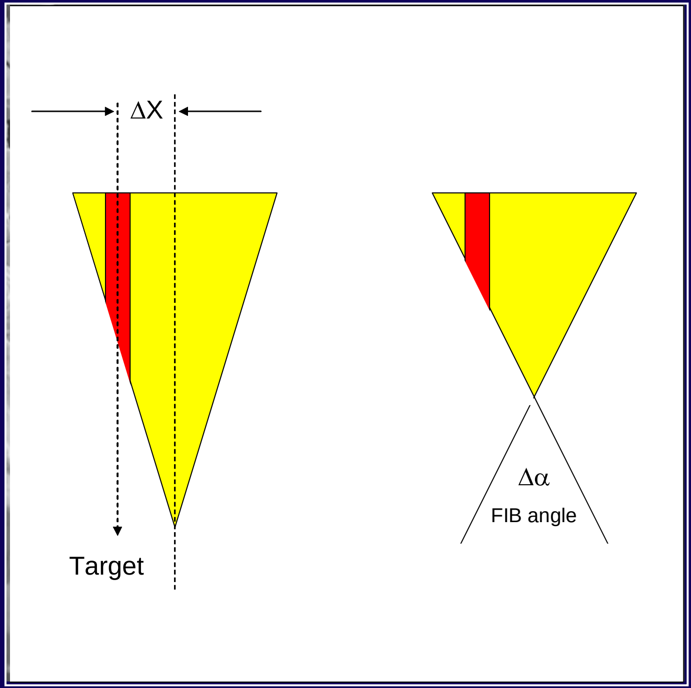
Final lamella thinning in small chamber FIB/SEM system

TEM Microscopy: Practical Issues to resolve

Imperfections in the process



Material re-deposition

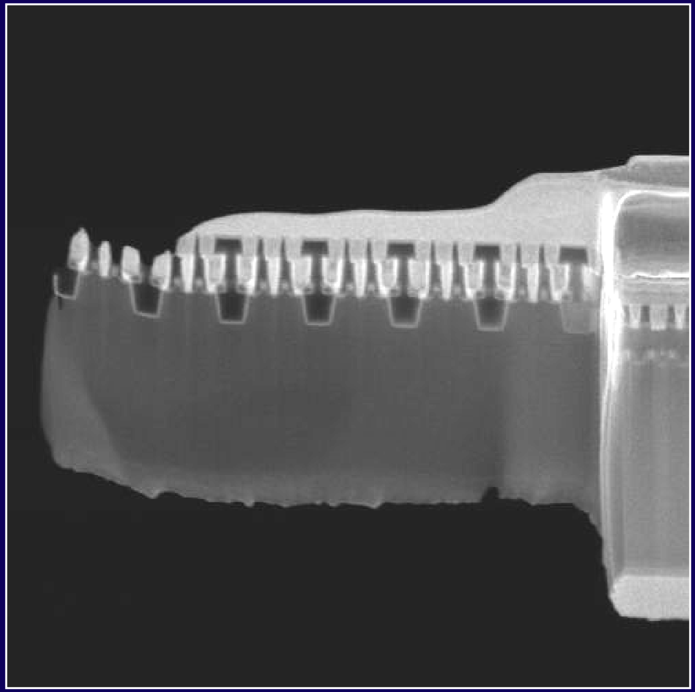


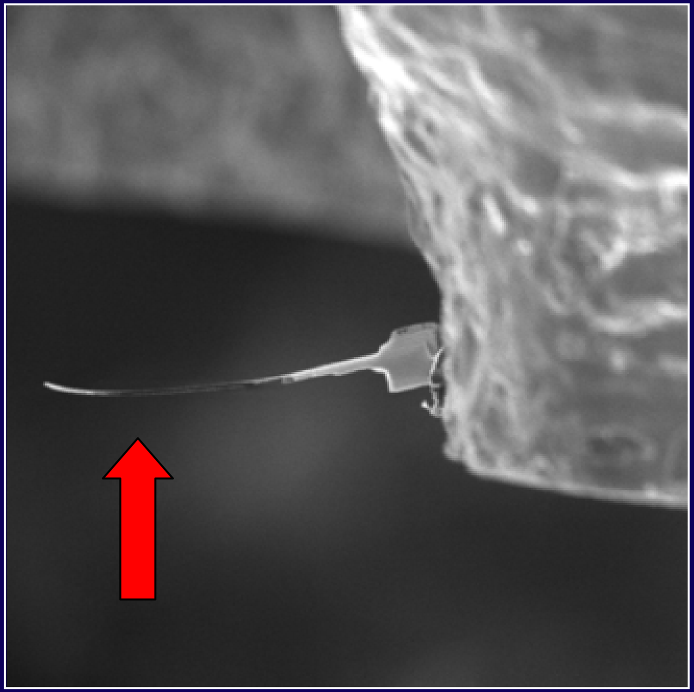
Insufficient sample heigth

Needs further optimization of chunking process recipe

TEM Microscopy: Practical Issues to resolve

Bending of thin lamella



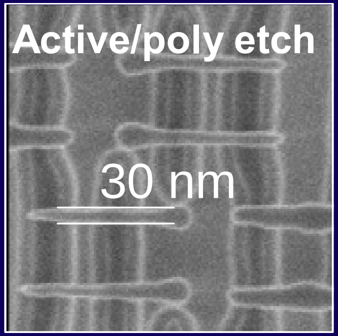


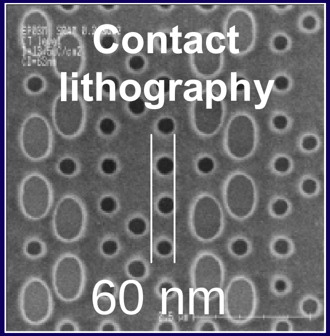
Difficulties with TEM alignment!

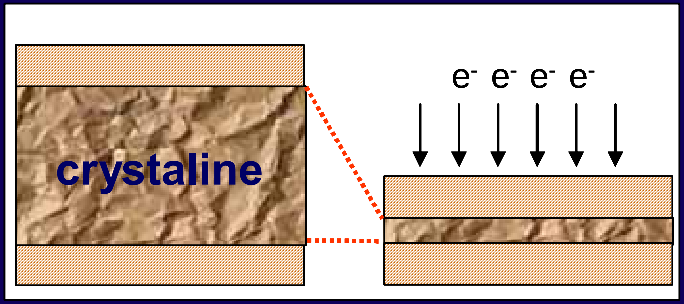
- FIB milling process induced (Ga implant, heating,…)
- Needs adapted procedures (lamella shape/process)

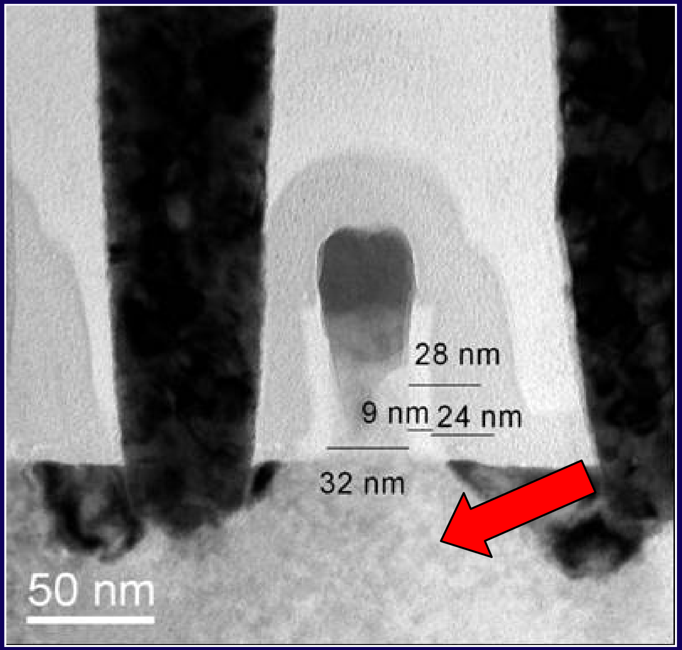
TEM Microscopy: Practical Issues to resolve

Amorphisation of very thin (< 40 nm) lamella







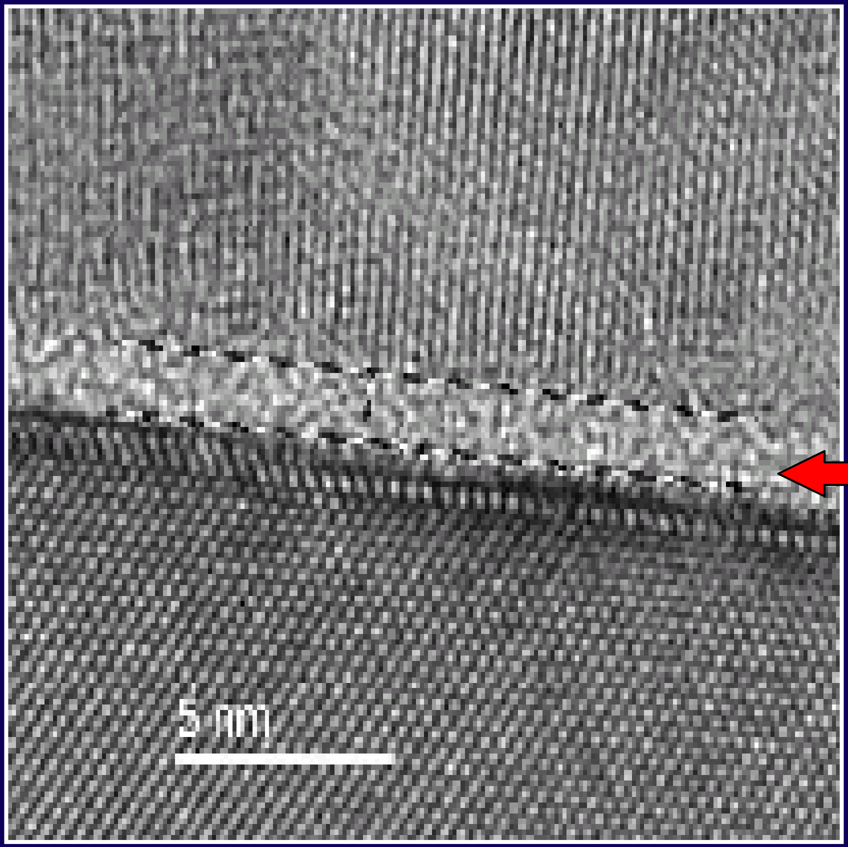


Amorphous Silicon!

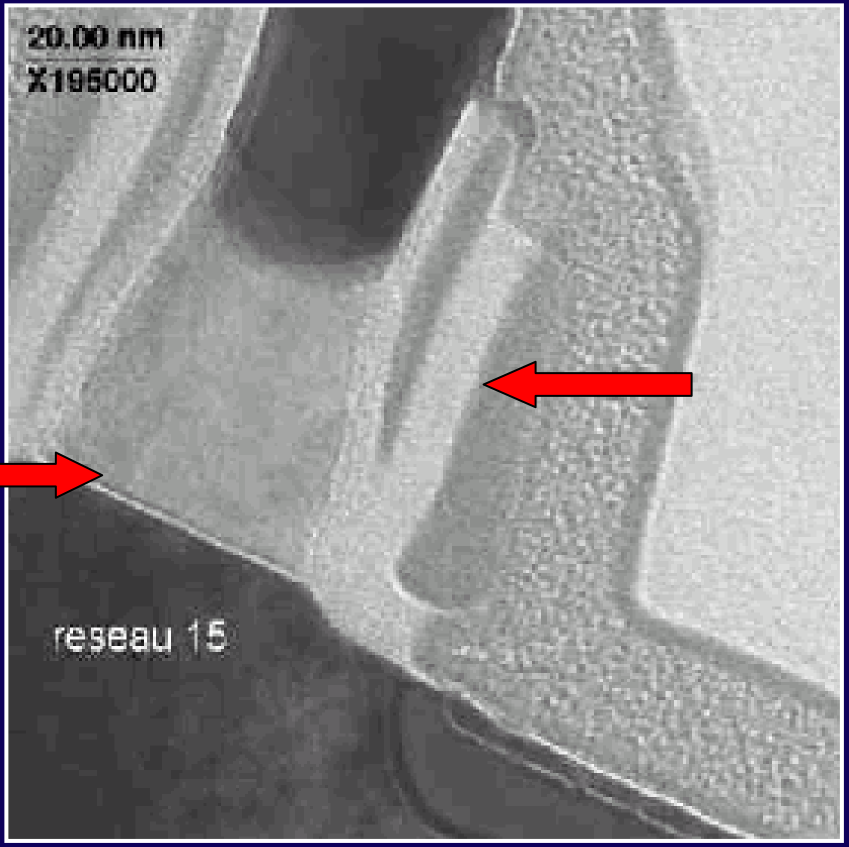
- FIB induced @ 15 KeV ~ 15 - 20 nm each side
- Low energy (< 2KeV) FIB milling process needed

TEM Microscopy: High Value Added data

45 nm Transistor engineering



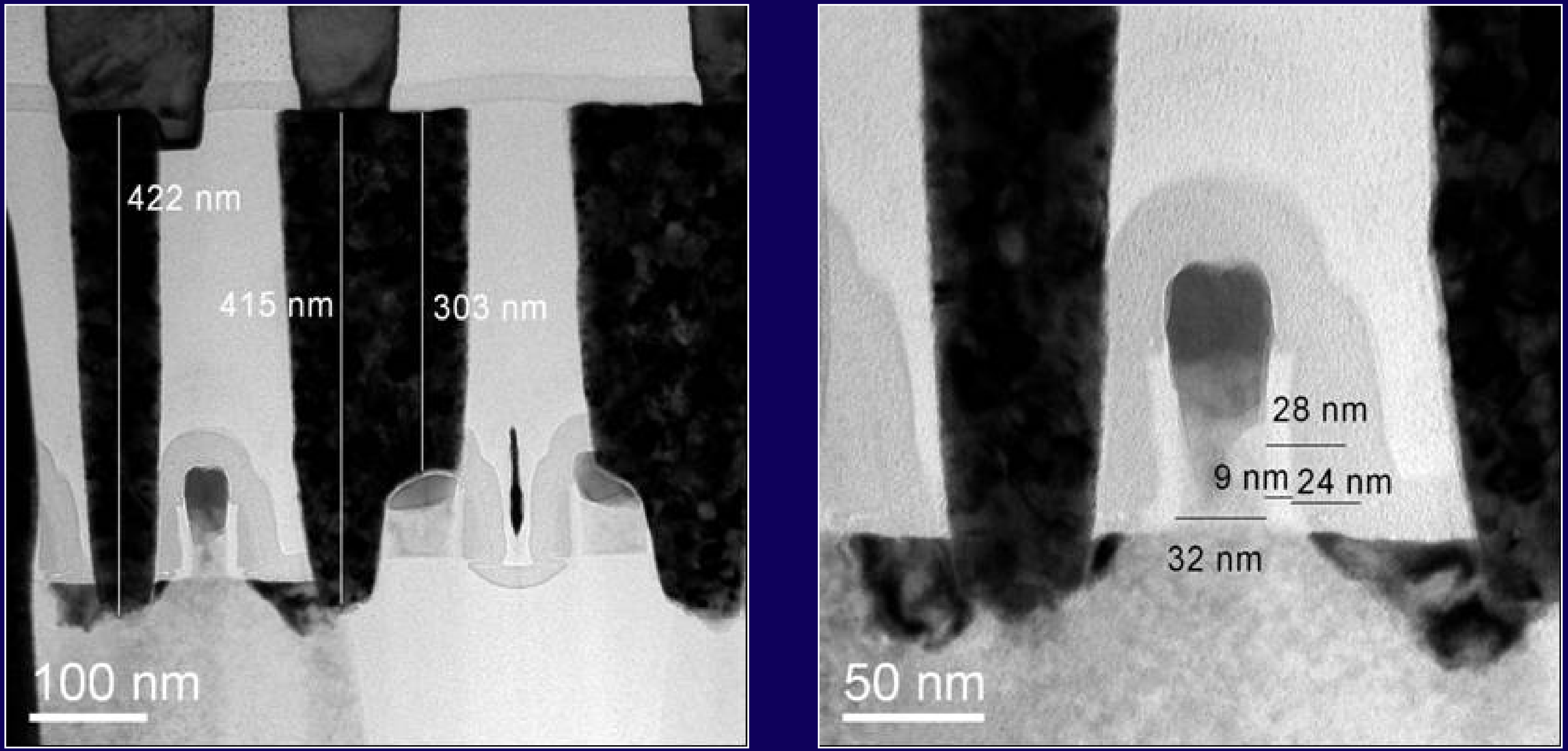
Process control at atomic level!



2-D spacer shape affects transistor characteristics !

TEM Microscopy: High Value Added data

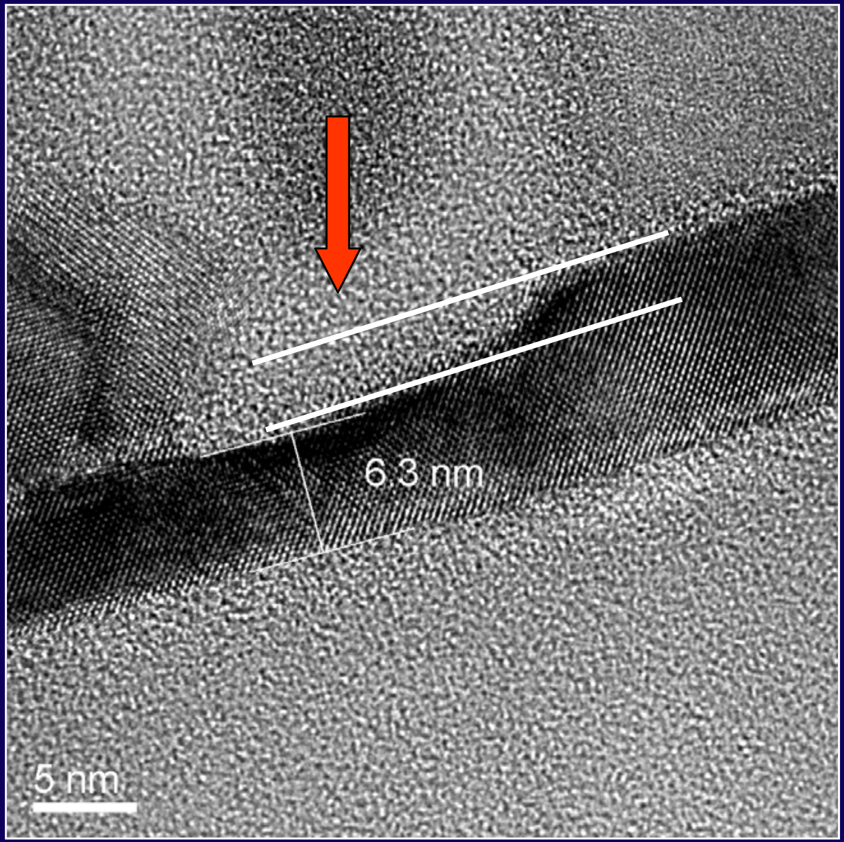
45 nm SRAM Cell construction analysis

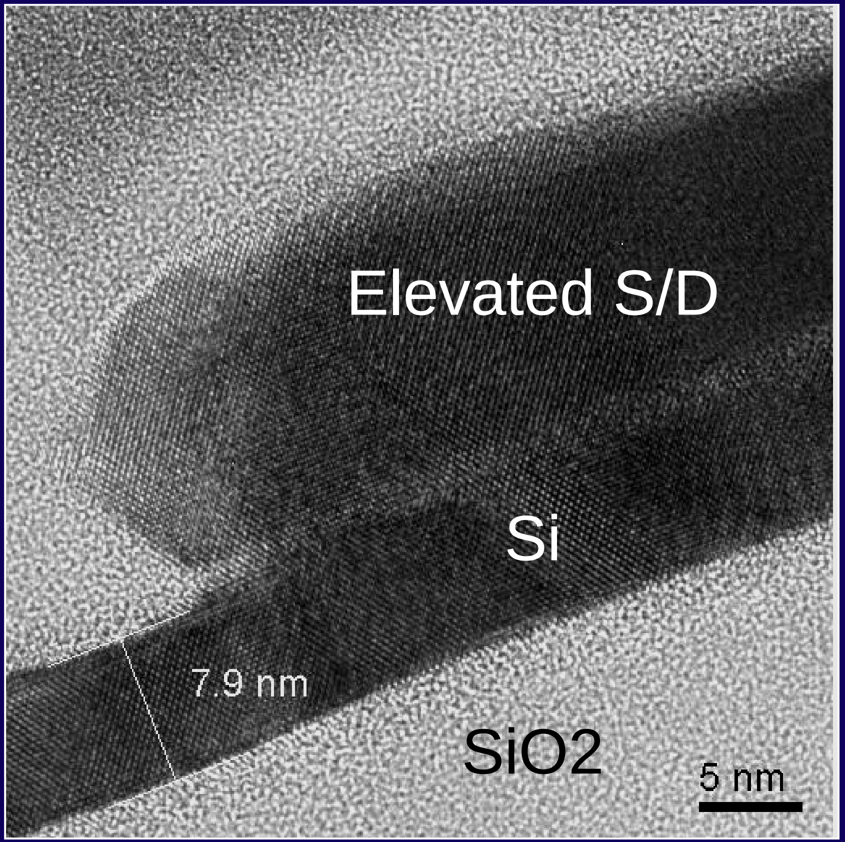


Dimensional control, process anomalies, alignment accuracy etc…

TEM Microscopy: High Value Added data

Elevated Source/Drain on SOI substrates

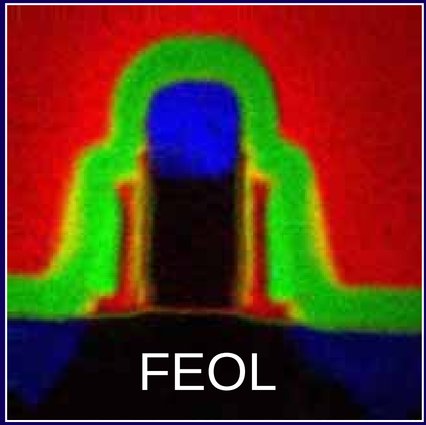


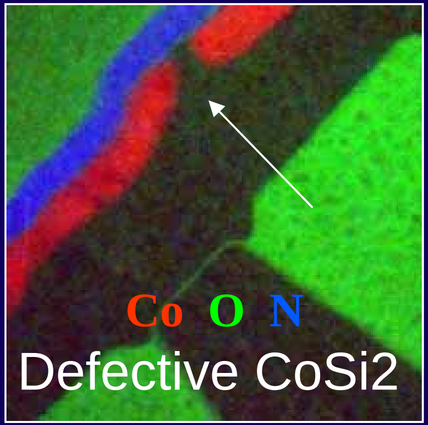


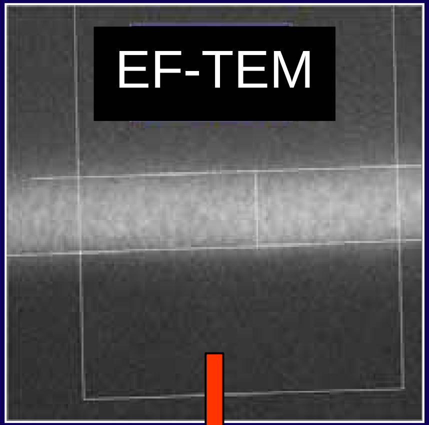
Excessive Silicon etching during surface cleaning steps may influence channel characteristics

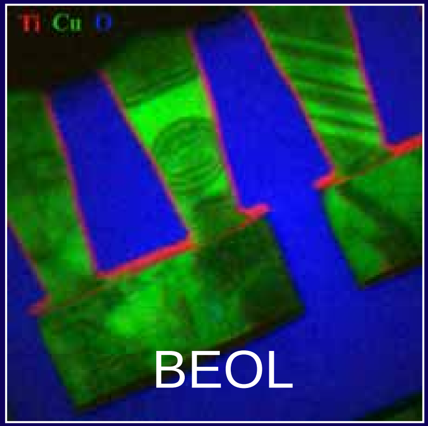
TEM Microscopy: High Value Added data

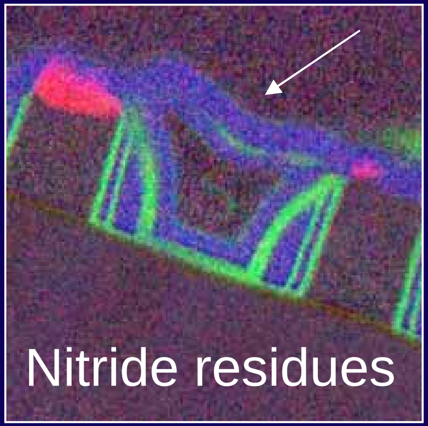
Chemical Analysis via EFTEM, EELS

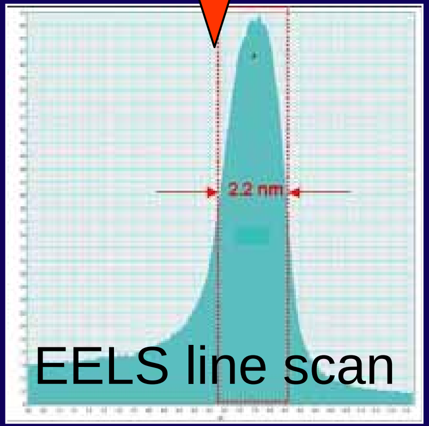












Microscopy: Conclusions

- **Development of latest technology requires a *high quality*, *fast* and *volume* TEM service.**
- **Efficient TEM sample preparation is key to success!**
- **Non-destructive Full wafer sample extraction offers significant advantages for fast learning cycles.**
- **The overall process still needs to be improved and become more automated in order to arrive at correct TEM volumes**

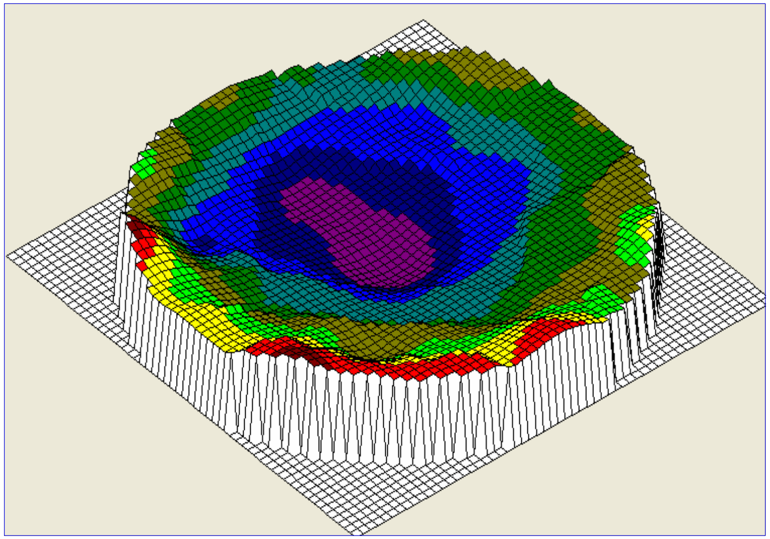
MATERIALS ANALYSIS

Materials Analysis

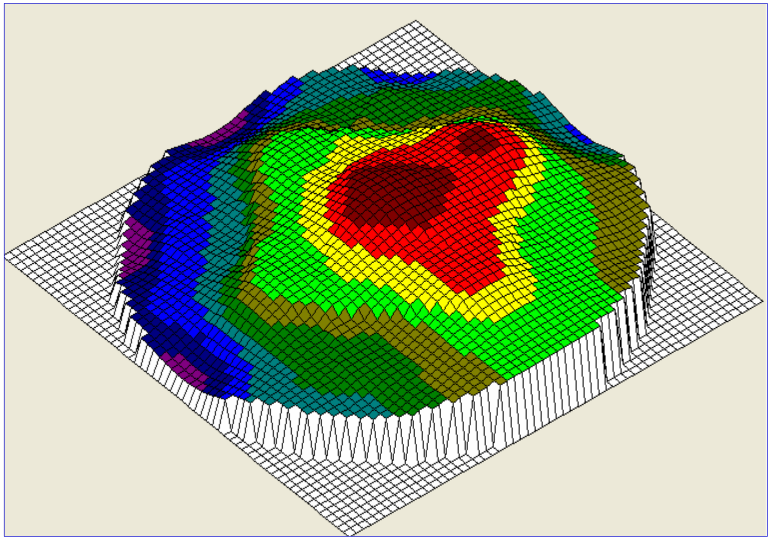
- The Materials Analysis group activities:
  - Chemical Analysis (SIMS, µ-AES, ToF-SIMS, XRF)
  - Structural Analysis (XRD, EBSD)
  - Mechanical Analysis (TEM-CBED, µ-Raman spectr.)
  - Metrology Applications development (XRR/XRF, IRSE, µ-XRD, …)
- Full Wafer analysis strategy
  - Easy to operate, Fab compatible, high throughput
  - Non-destructive, several complementary techniques can be used to characterize one wafer/die
  - Easy navigation facilitates Failure Analysis

Materials Analysis: 300 mm Wafer Tools

Full wafer SIMS : allows full wafer process mapping



ALD TiN process A
Chlorine variation = +/-19.6%
25 points analysis, 3.5h

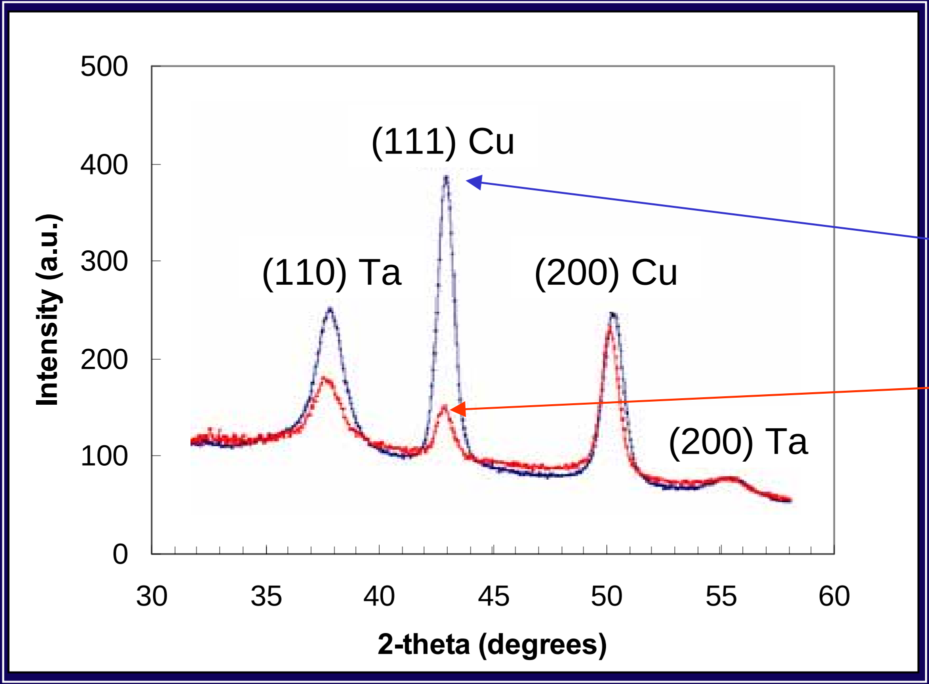


ALD TiN process B
Chlorine variation = +/- 9.1%
17 points analysis, 2.5h

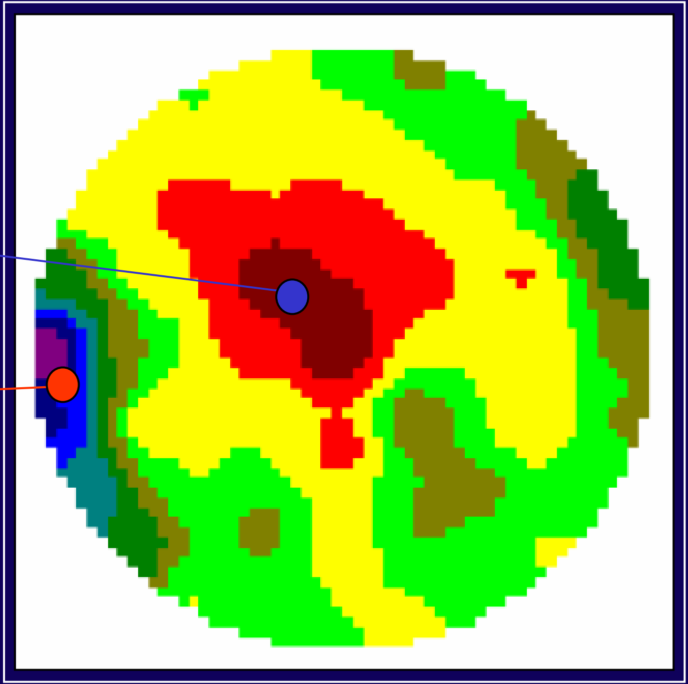
Fast and relevant feedback allows rapid Process development cycles

Materials Analysis: 300 mm Wafer Tools

Full wafer µ-XRD : TaN/Ta/Cu seed wafer



XRD at two locations

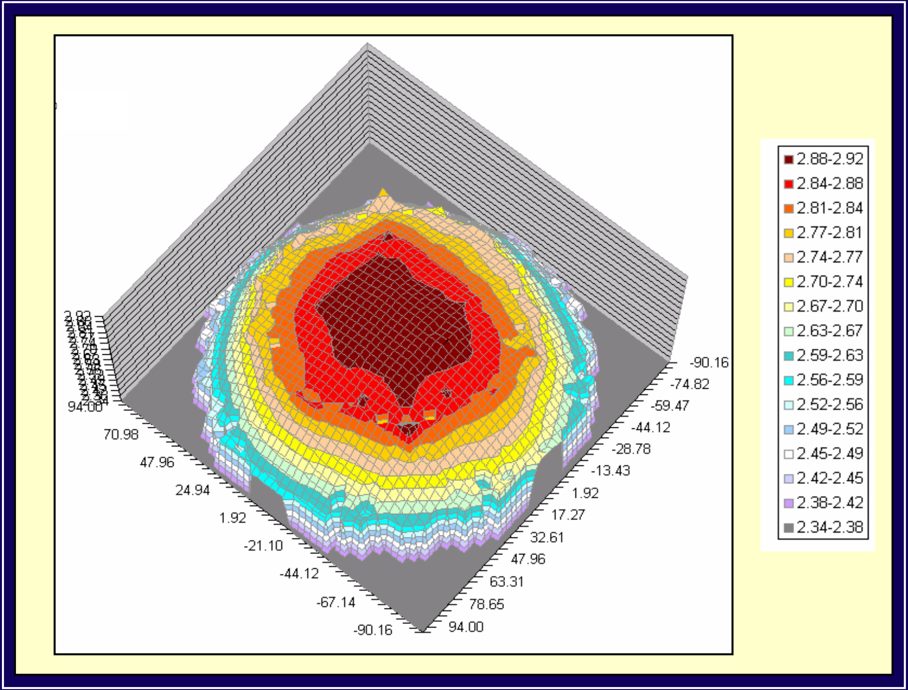


Ta Thickness Map

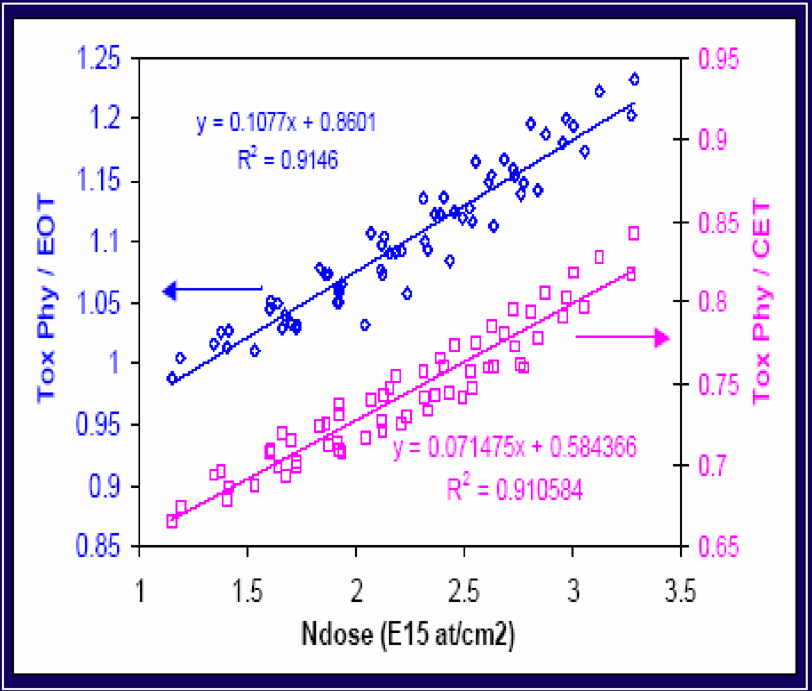
- XRD Diffraction patterns of thin and thick regions on Ta/Cu wafer.
- Thick Ta with (110) texture seems to induce a strong (111) Cu texture.

Materials Analysis: 300 mm Wafer Tools

Full wafer XPS : Nitrided Gate Oxide monitoring



XPS Nitrogen dose Map (E15 at/cm²)

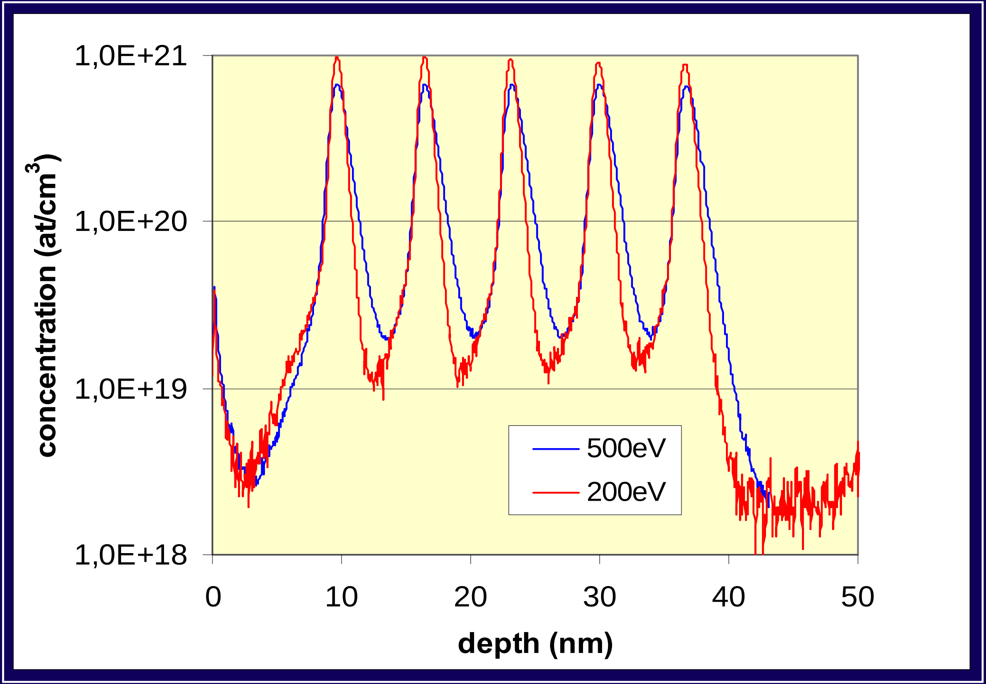


Nitrogen dose vs. Thickness

- XPS does provide both thickness and dose information
- It is possible to predict EOT/CET from in line XPS measurements

Materials Analysis: Application Development

Full wafer SIMS : USJ analysis, Boron

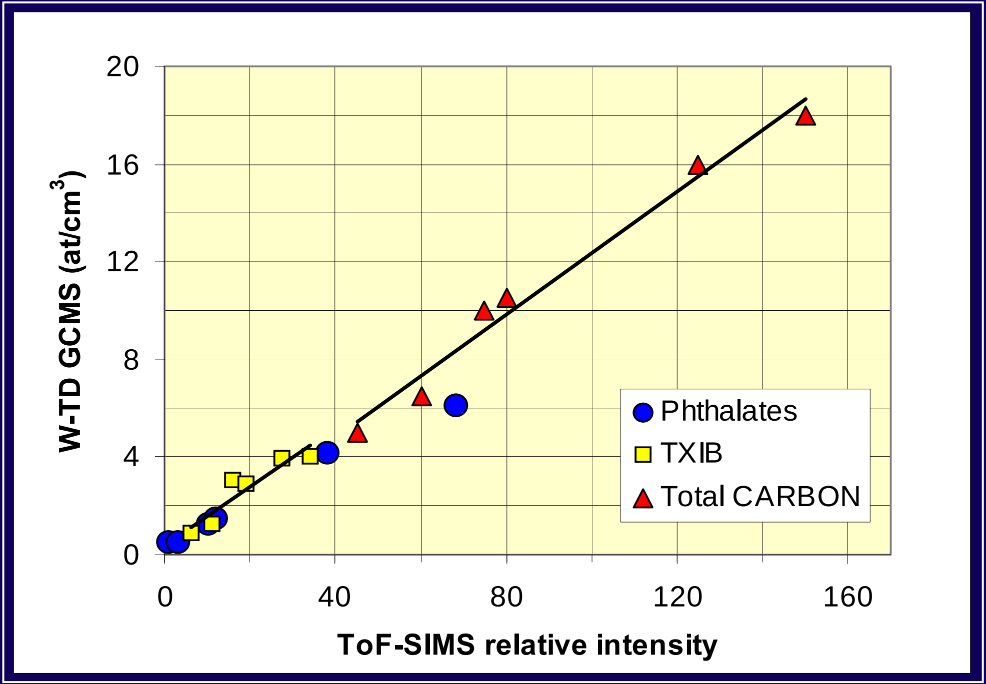


Reduction of SIMS etching energy from 500eV down to 200eV:

depth resolution improves from 1.5nm/decade down to 0.9nm/decade

Materials Analysis: Application Development

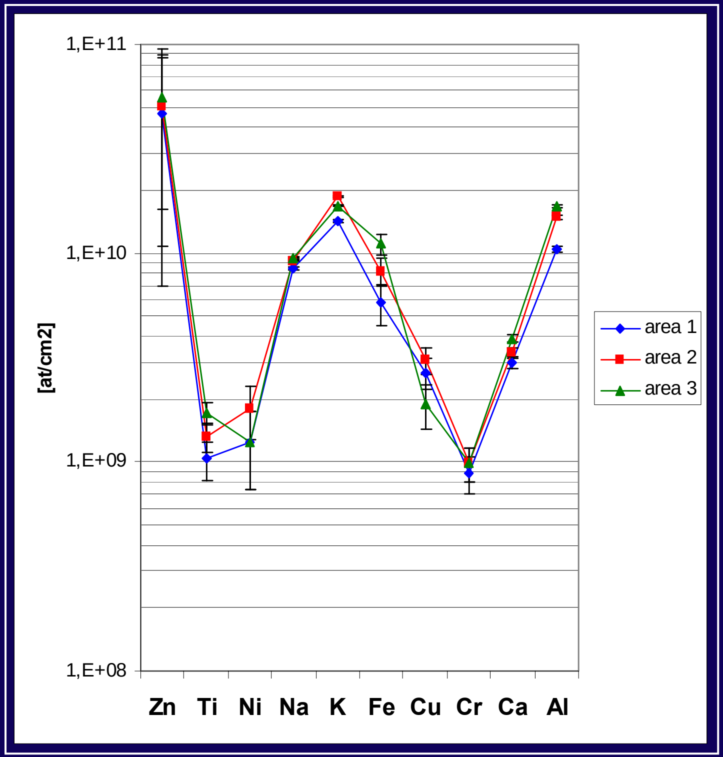
ToF- SIMS: Clean Room AMC Monitoring

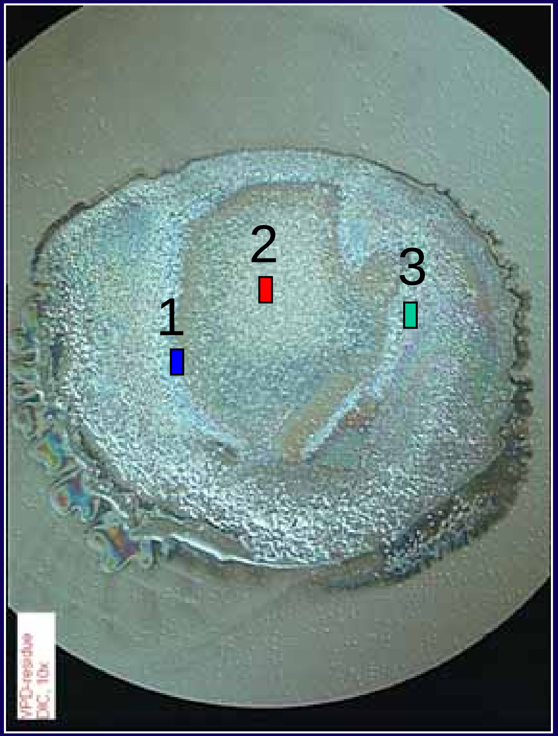


At Room Temperature ~ 30 – 70 % of the volatile species desorb from the wafer surface and remain undetected by ToF-SIMS!

With a LN_2 sample cooling protocol, desorption is avoided and quantitative monitoring can be achieved (via W-TD-GCMS calibration)

ToF- SIMS analysis of VPD residues

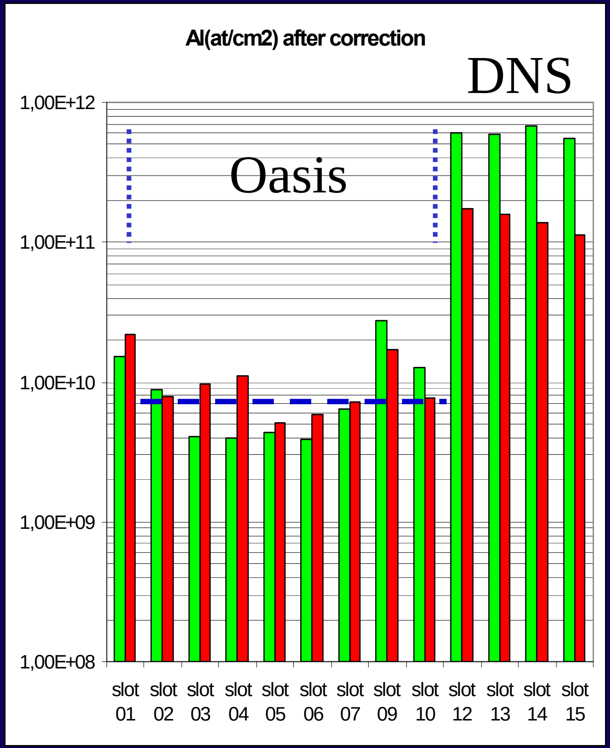




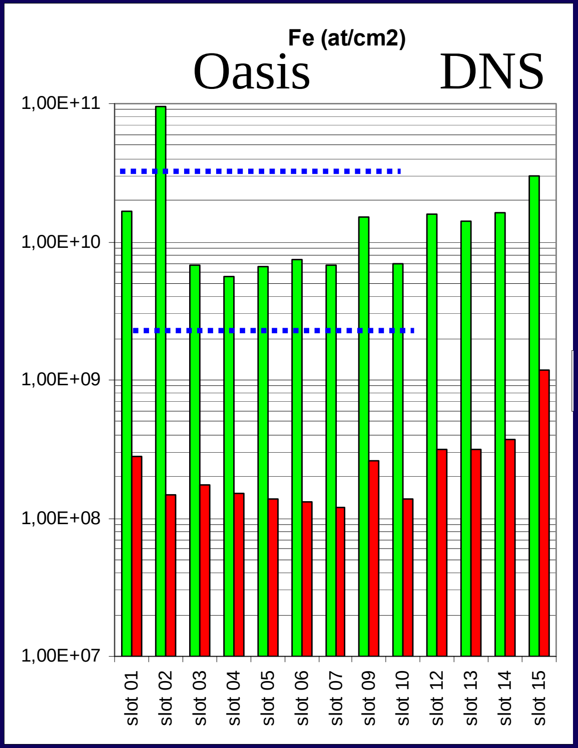
ToF-SIMS analysis (left) at different locations within the droplet (right) shows its constant chemical composition

Materials Analysis: Application Development

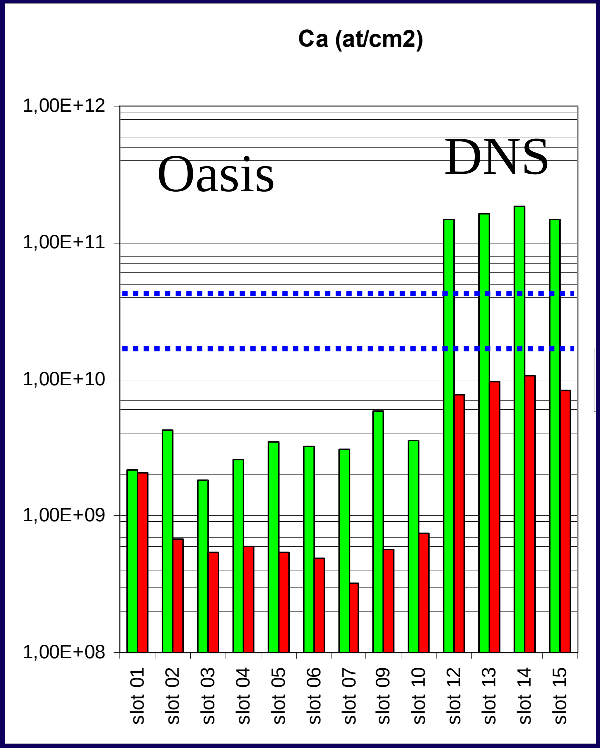
VPD -ToF- SIMS ■ vs. VPD-TXRF ■ vs. VPD-ICPMS ■



Aluminum (Calibration)



Iron

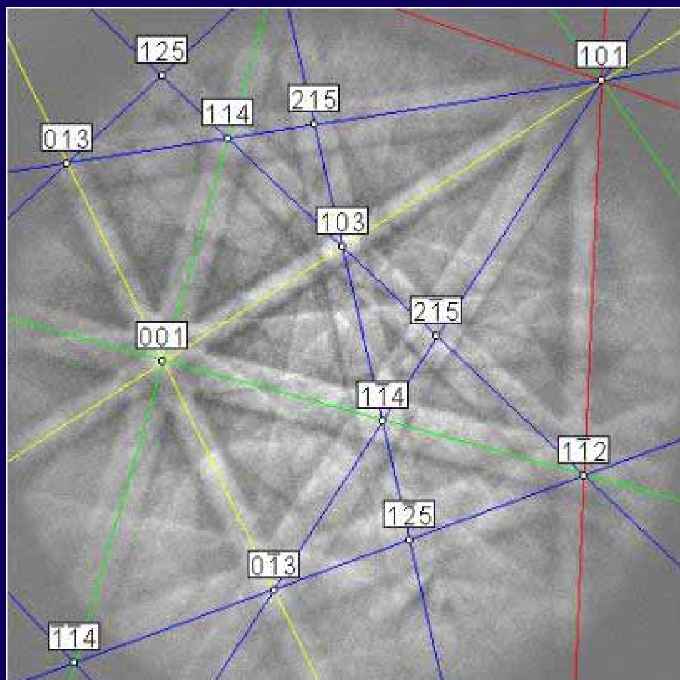


Calcium

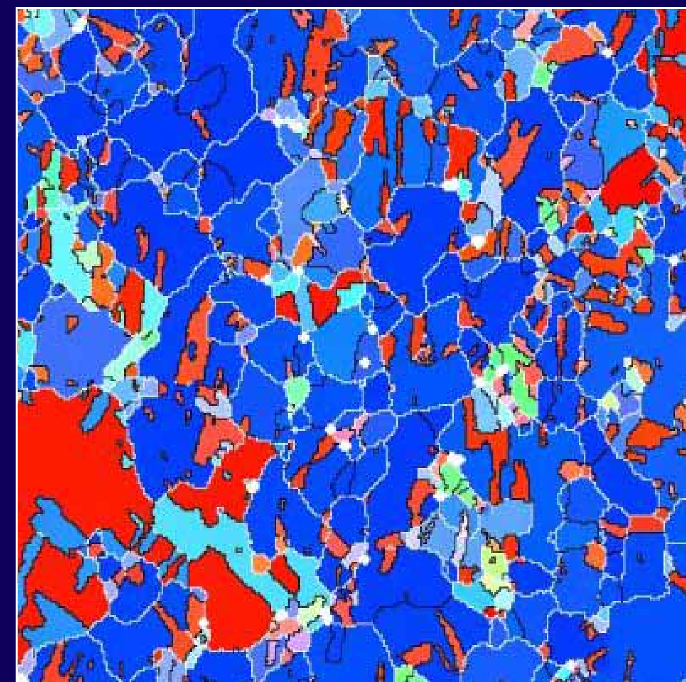
VPD-TXRF results in lower values due to X-ray absorption in residue (0.2 – 1.0 µm thick)

Materials Analysis: Application Development

Copper grainsize analysis with EBSD



EBSD diffraction pattern



Cu grainsize & orientation

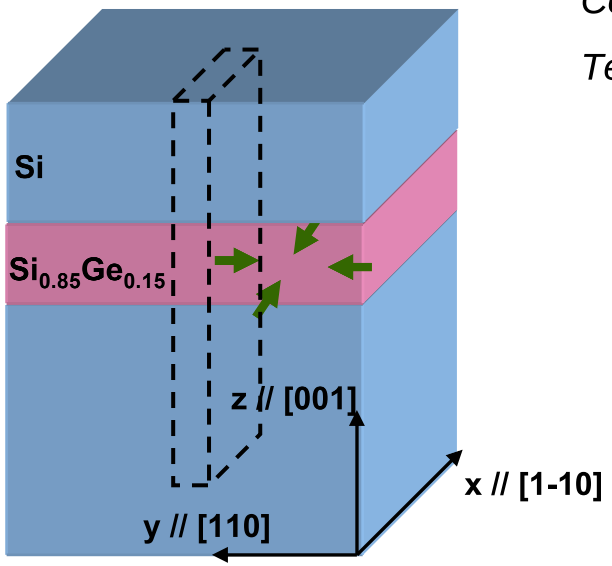
blue is {111} , red = {100}

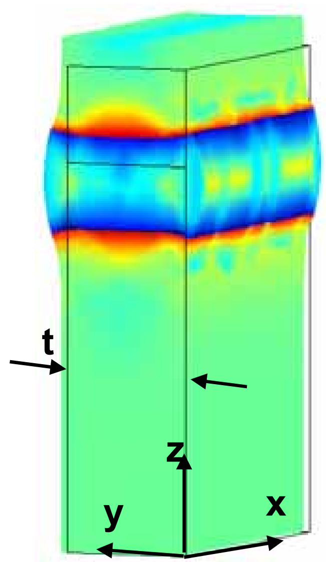
Strain Analysis with nm resolution: TEM-CBED

Si/Si(1-x)Gex/Si Epitaxial growth x=15%

Compressive biaxial stress : $\sigma_{xx}=\sigma_{yy}=\sigma_0=-1.1GPa$

Tetragonal distortion along z direction



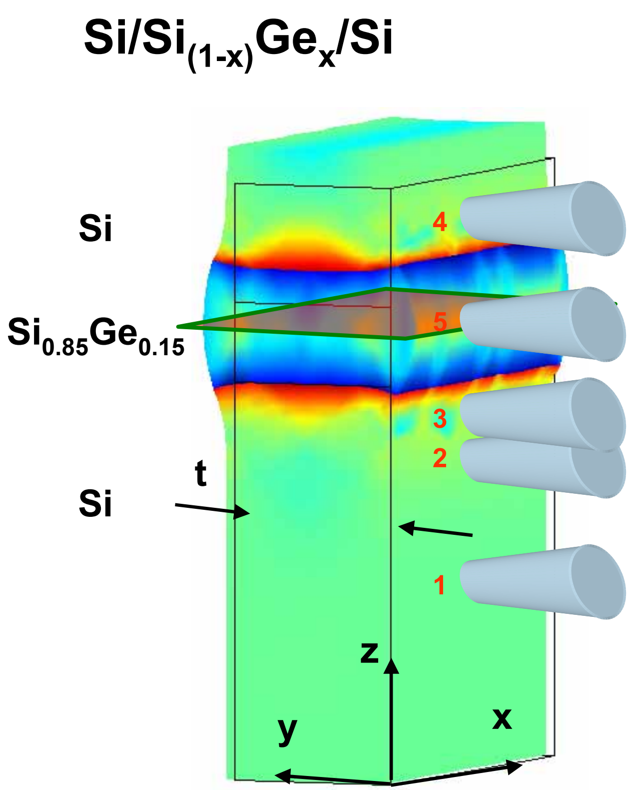


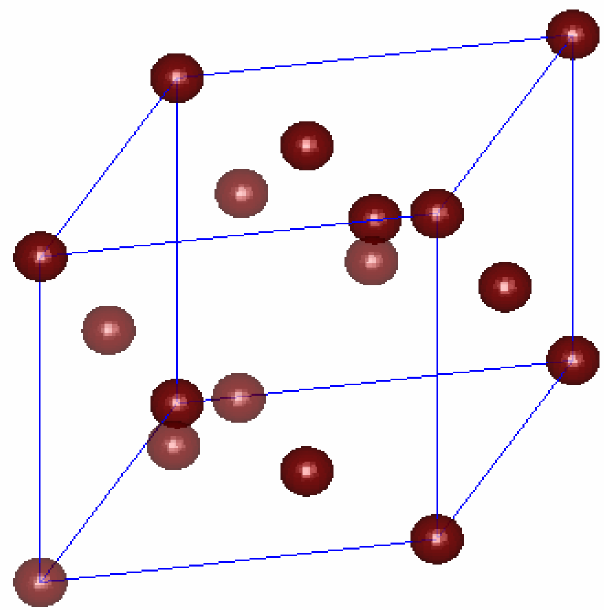
FIB sample preparation

relaxation along [110] direction

Materials Analysis: Application Development

Strain Analysis with nm resolution: TEM-CBED





Holz Line broadening

+

Finite element Modelling

$\sigma_{xx} = \sigma_0 = -1.1$ GPa $\sigma_{yy} = -0.2$ GPa

Materials Analysis: Conclusions

- Materials analysis in latest technologies requires that more and more techniques become available (XRD, XRR, EBSD, Raman….) and that existing ones are more refined (SIMS, ToF-SIMS).

- Full wafer tools offer appreciable advantages but have its price!

- The materials analysis team provides analytical services but also actively develops a wide variety of applications and evaluates new metrology tools.

ELECTRICAL FAILURE ANALYSIS

Off-line Characterization

Without fault isolation

R&D support

Process development

With fault isolation

Yield loss analysis

Voltage Contrast

Test structure

OBIRCH

Test structure

Product

Bitmap

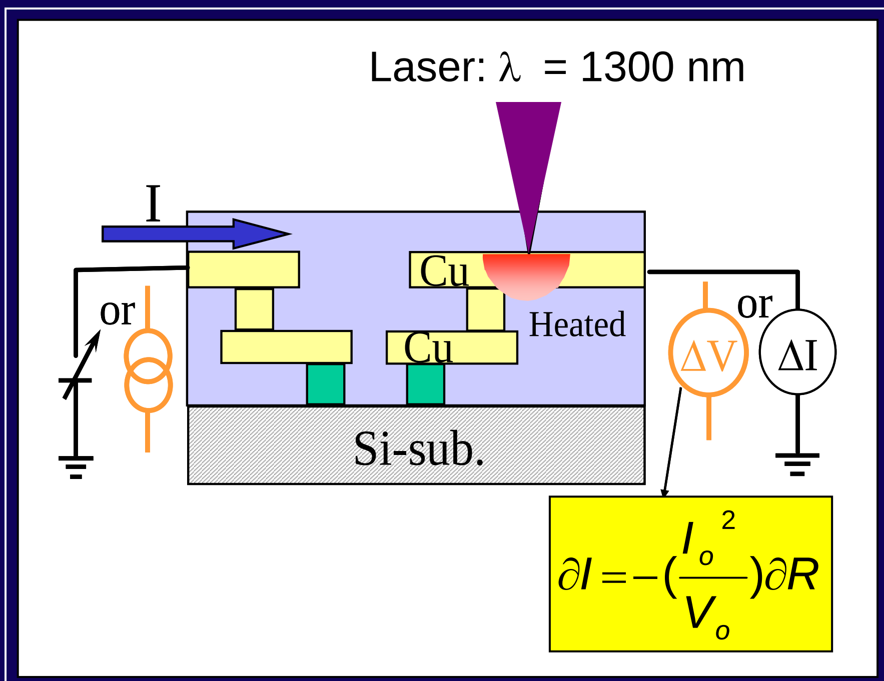
Memories

Physical characterization

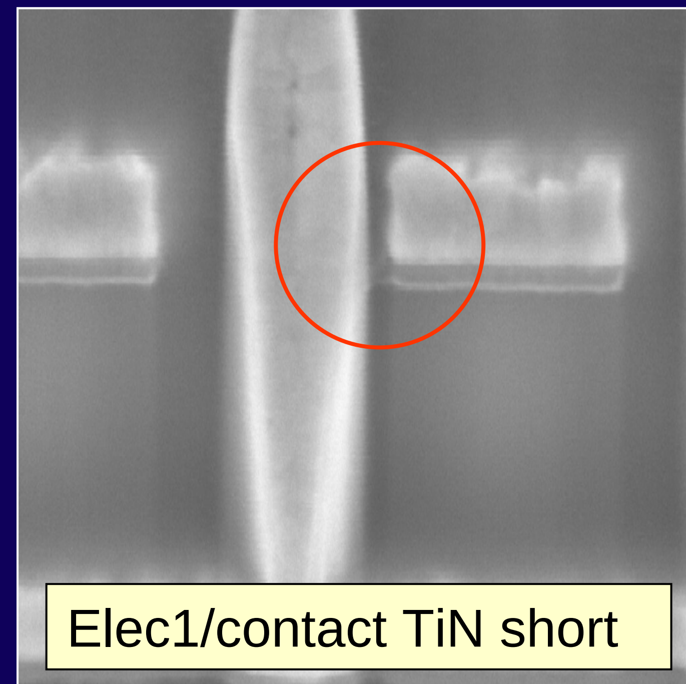
FIB, SEM, TEM, EELS, AES, TOF-SIMS, XRR, XRD…

OBIRCH based analyses

Detection of resistive paths based on current changes



Detection sensitivity improves with higher laser power and higher current

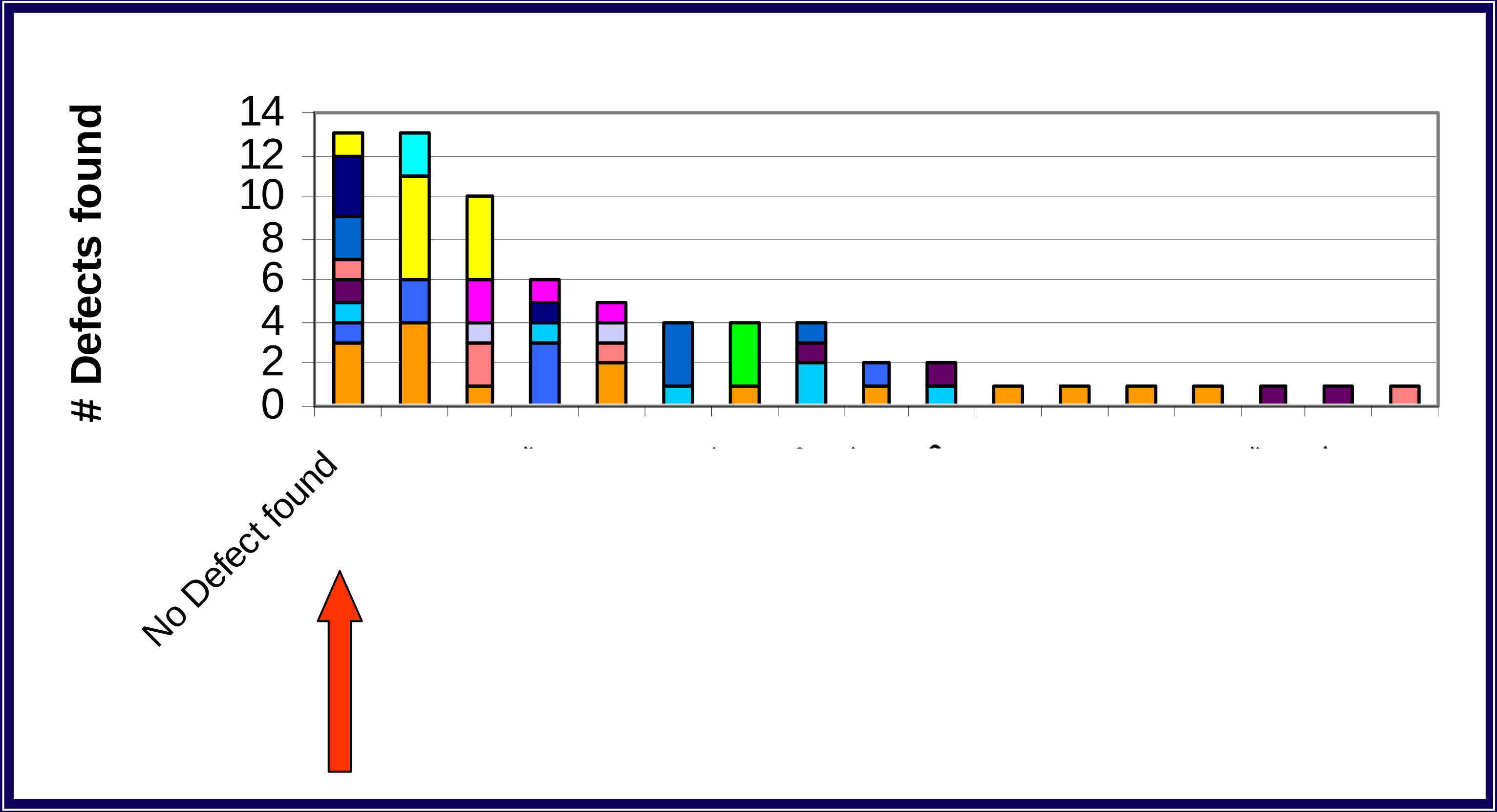


DRAM parametric test structure

But latest technology operates at lower V (lower I_o) and is more sensitive to laser induced damage…

YIELD Learning in 90 nm CMOS Technology

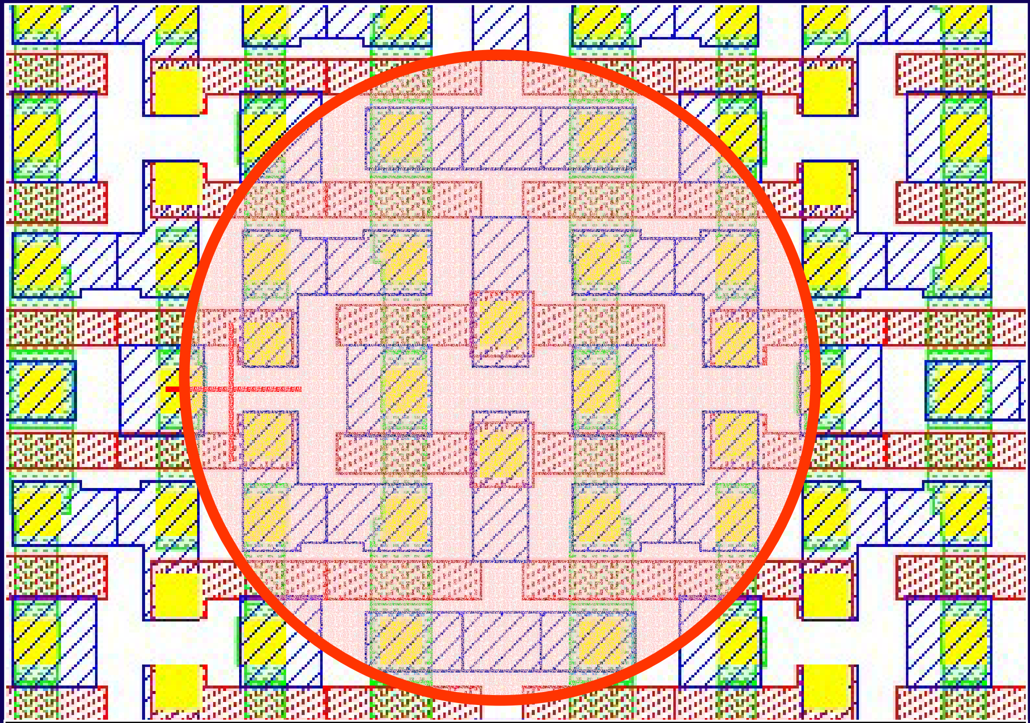
Physical Failure Pareto …



~ 20% : No defect found…

For 65 nm technology: > 30 % of defects not found

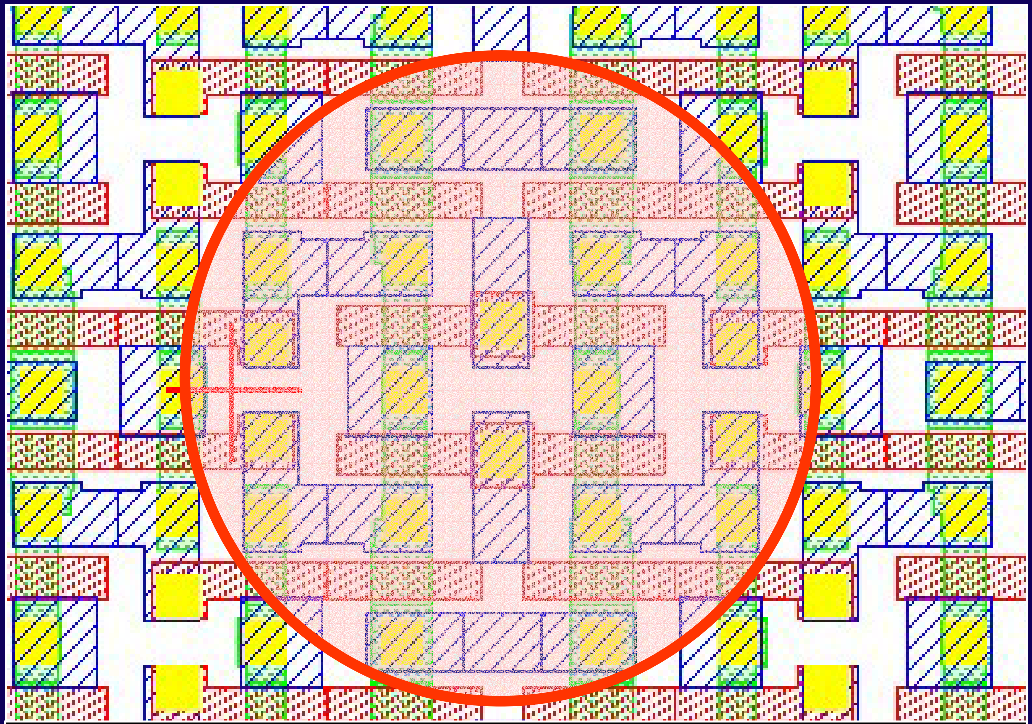
OBIRCH Limitations: Spatial Resolution



OBIRCH point superimposed on SRAM layout

- OBIRCH spot surface ~ 1 µm²
- 65 nm elementary SRAM cell ~ 0.5 µm²
- In one OBIRCH spot: 12 transistors, 20 contacts,…

OBIRCH Limitations: Spatial resolution



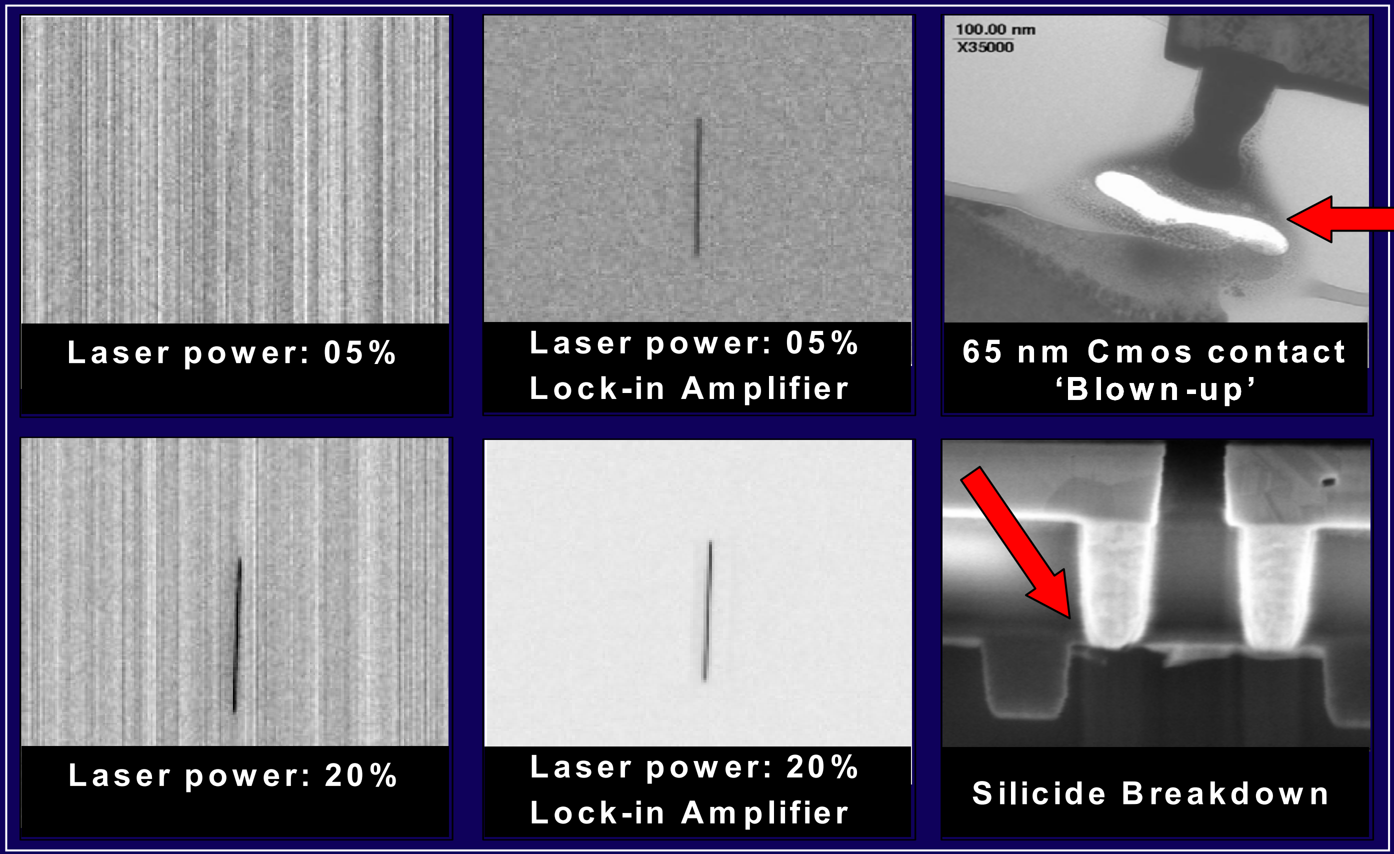
OBIRCH point superimposed on SRAM layout

"Looking for a Needle in a Hay stack!"

→ *Spatial resolution has to be improved*

OBIRCH limitations: S/N ratio & laser power

Latest technologies require low laser power…

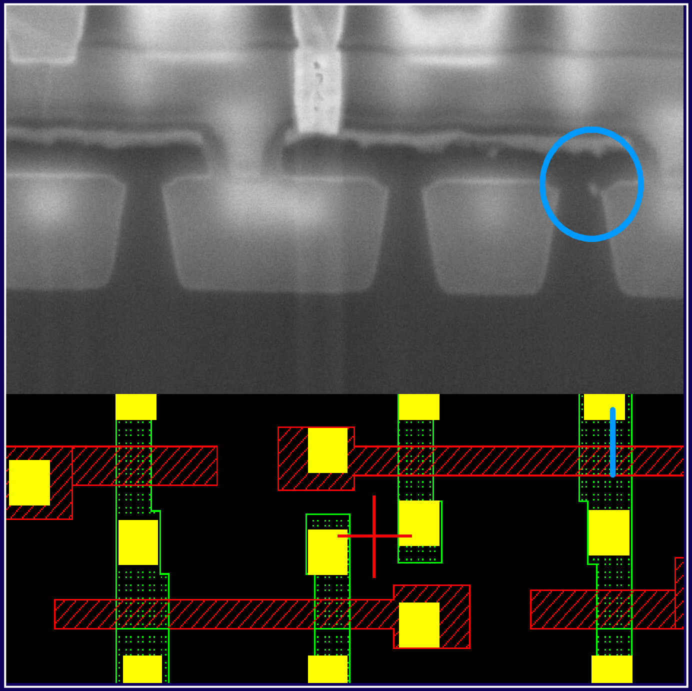


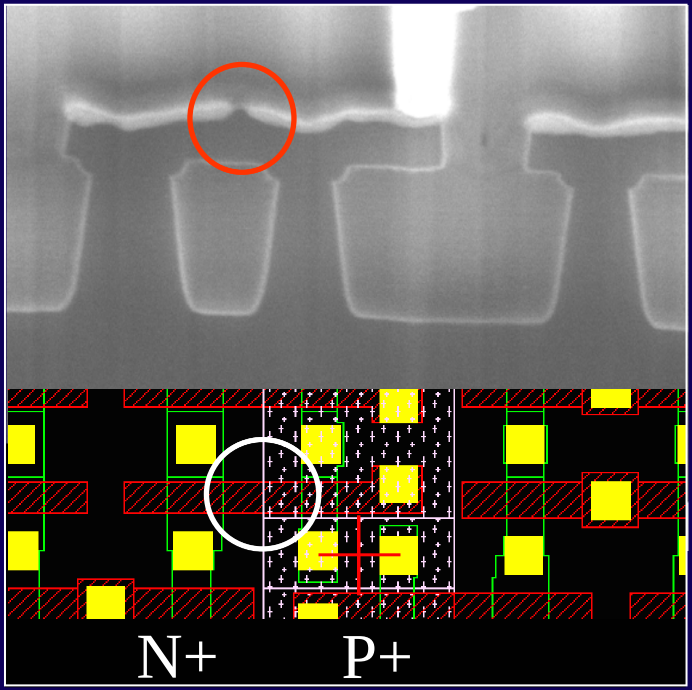
$$\partial I = -\left(\frac{I_o^{\,2}}{V_o}\right)\partial R$$

Lock-in amplifier is needed to improve sensitivity

FA Limitations: SEM Spatial Resolution

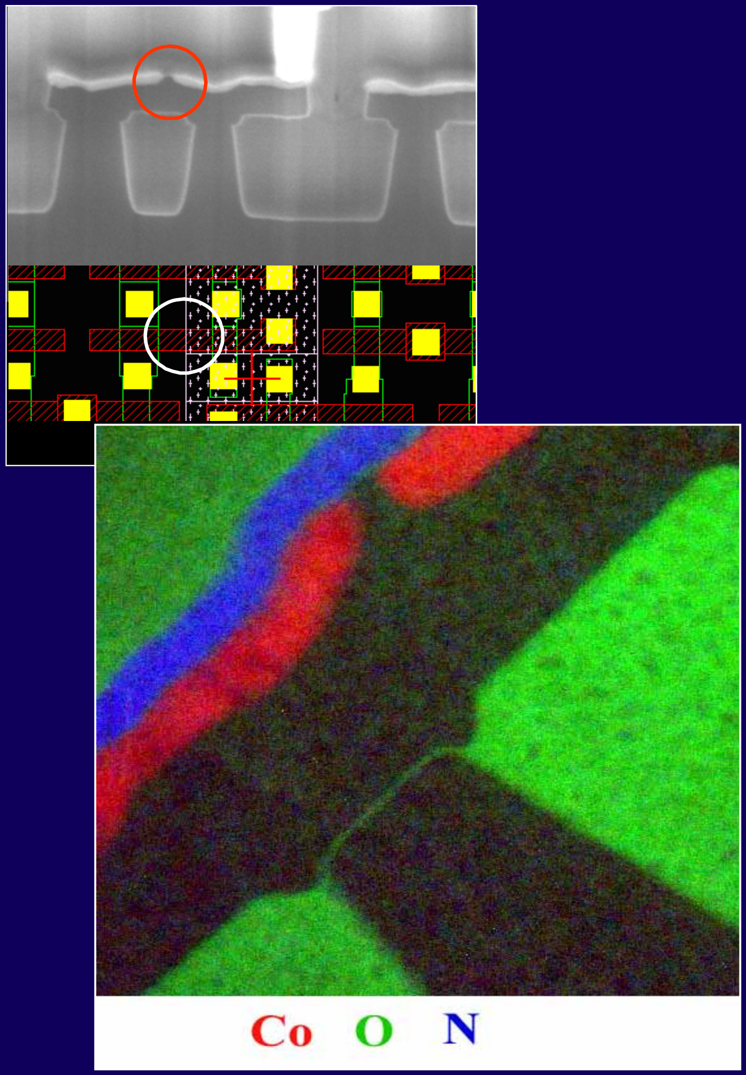
FIB-SEM based BITMAP analysis

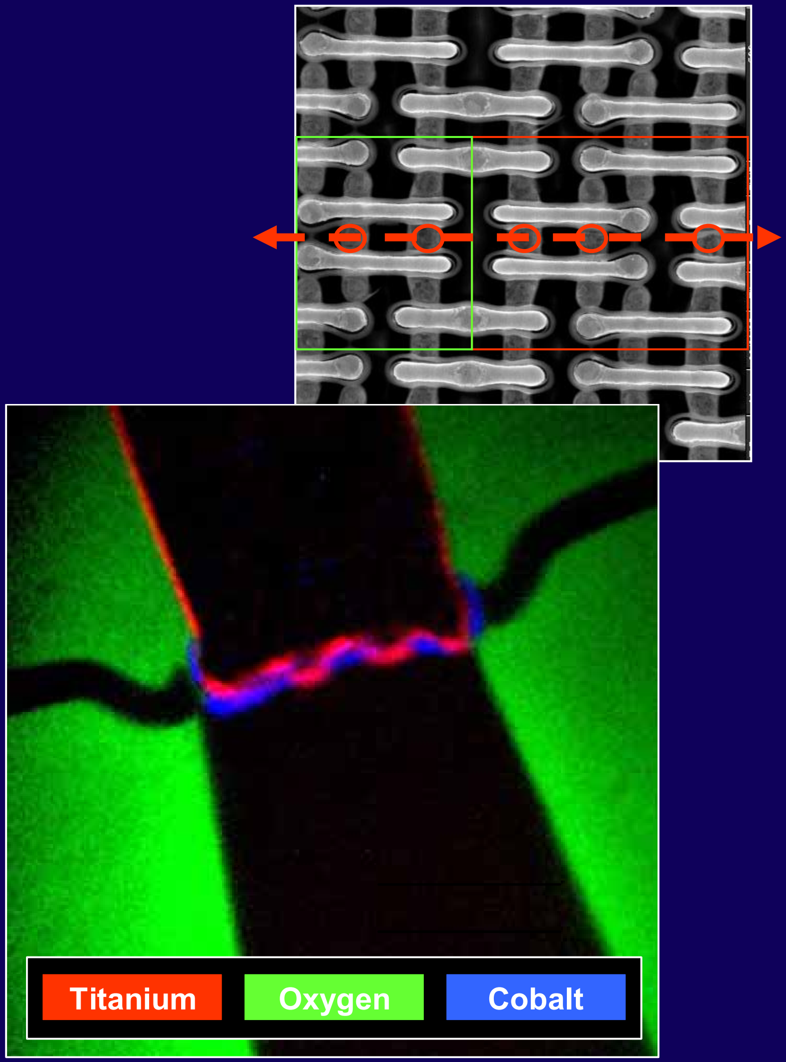




SEM Observation becomes delicate…!

FA Limitations: TEM Resolution is needed!





Electrical Failure Analysis: Conclusions

- **Failure Analysis has been effective for 120 and 90 nm technologies but is less effective for 65 nm technology.**
- **The two main limitations are**
  - Fault isolation inaccuracy
  - limited SEM imaging resolution
- **New developments are definitely required**
  - Improved OBIRCH, or complementary techniques
  - Software based Fault Diagnosis methods to identify faulty nets or cells
  - 3-D Tomography, TEM based EFA

CONCLUSIONS & PERSPECTIVES

- With the increase of technology complexity, also the need for adequate physical characterization support increases.

  Many challenging development tasks are ahead of us!

- TEM microscopy and appropriate sample preparation techniques will be a focal point for the years to come.

- Several ‘Lab’ techniques will have to transform into ‘Fab’ techniques for in-line defectivity monitoring and metrology.

- The FA community needs to re-think strategy and to come up with new or smarter techniques and methodologies to narrow the gap that starts to exist between what is *needed* and what is *available* for effective failure analysis on most advanced technologies.

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