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Metrology Challenges for the Ultra-thin SOI

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Outline

- Introduction
- Layer Thickness Measurements for FD SOI
- Electrical characterization of SOI layers
- LPD inspection challenge
- Preferential Chemical Etching of Structural Defects
- Conclusions

SOI wafer metrology

BULK	SOI METROLOGY ADJUSTMENT	SOI SPECIFIC	SSOI SPECIFIC
Crystal parameters	**Defectivity**	**Defectivity**	**Defectivity**
Crystal orientation	Front side surface	HF	Structural defects
Notch characteristics		**Electrical**	**Stress**
Oxygen		DIT	
Carbon		Qbox	
Metal		**Geometry**	
BMD		Thickness	
Oisf			
Slip Lines			
Etch pits			
Geometry parameters			
Diameter			
Flatness			
Nanotopology			
Edge			
Thickness			
Roughness			
Electrical			
Resistivity			
Minority carrier lifetime			
Defectivity			
Front side surface			
Back side surface			
Edge			

Most characterizations identical to bulk

Metrology adjustment for surface inspection

SOI specific characterizations

(Defectivity, DIT, mobility, Qbox, layer thickness)

sSOI: stress measurements, Ge%, structural defects

Overview of SOI metrology to address development of new SOI products: FDSOI, sSOI

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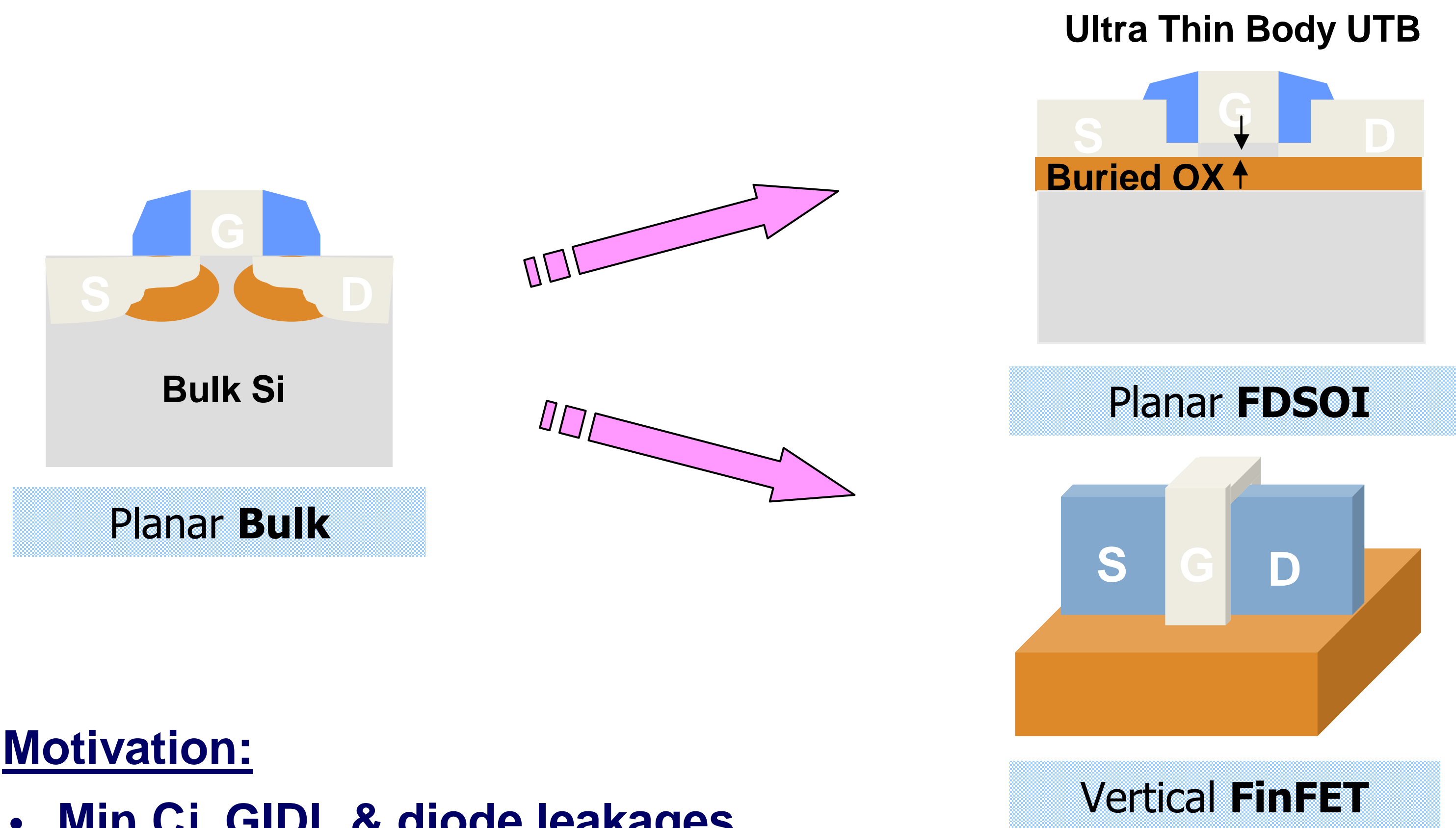
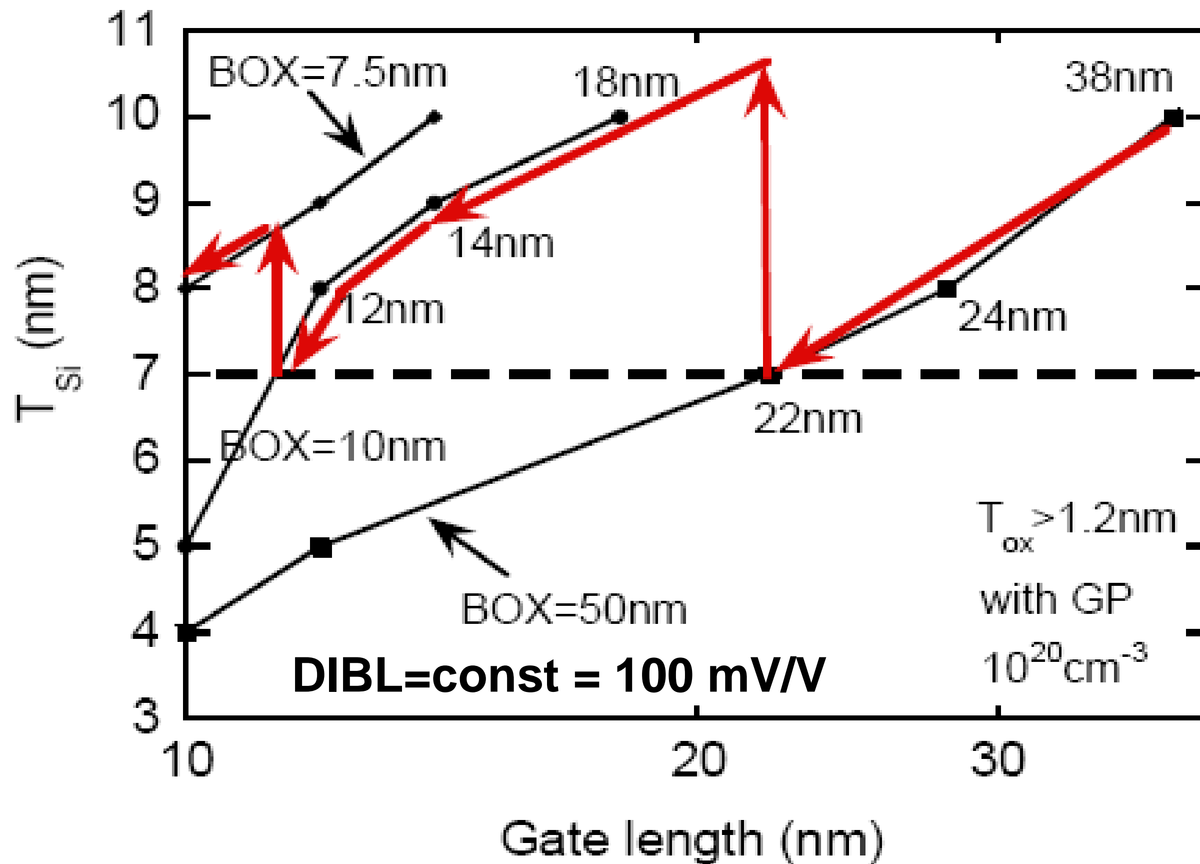
Fully Depleted Devices – next generation of CMOS



Motivation:

- Min Cj, GIDL & diode leakages
- Undoped channel: min RDF & V_T mismatch
- Improved SCE & back bias option
- Improved mobility
- Low-noise with least sensitivity to soft-error upsets

Top Si and BOX scaling for FDSOI

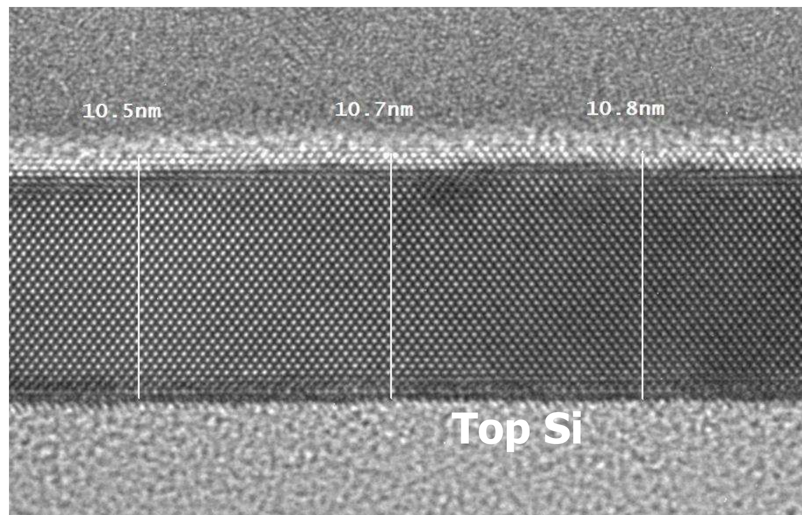


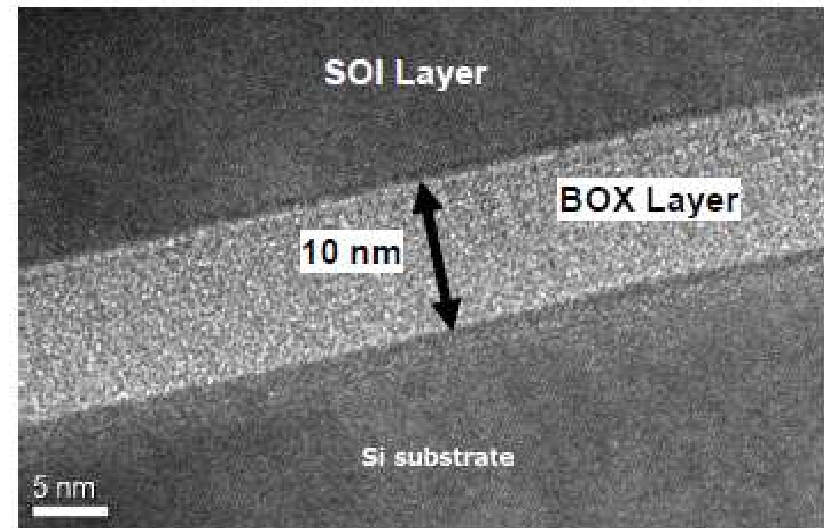
- TCAD extrapolation for channel Si thickness
- Model is calibrated with Si data

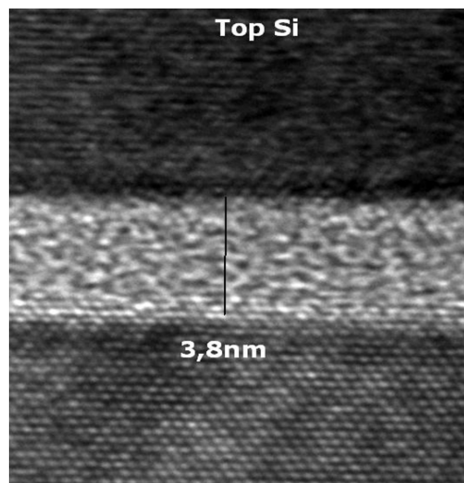
O. Faynot et. al. FDSOI Workshop Oct. 15, 2009; Courtesy of CEA-LETI

1. FDSOI is scalable down to L_G=10nm with **T_{Si}~7nm**
2. BOX scaling **below 10 nm** enables FDSOI scalability beyond node 11nm
3. No dominance of quantum effects for ≥5nm

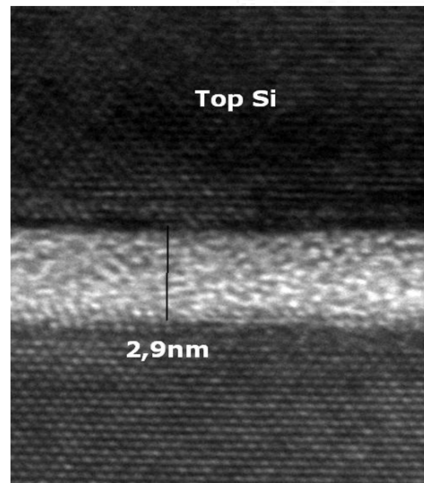
Top Si and BOX scaling for FDSOI



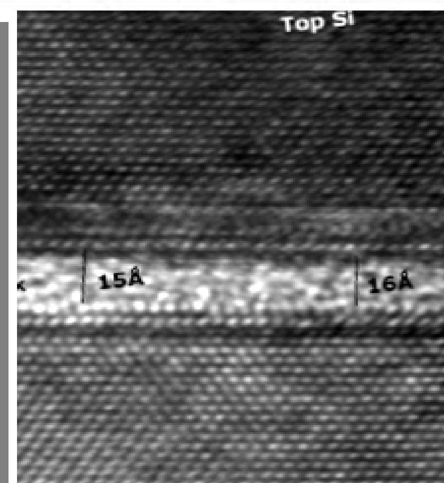




UTBOX
4nm



UTBOX
3nm

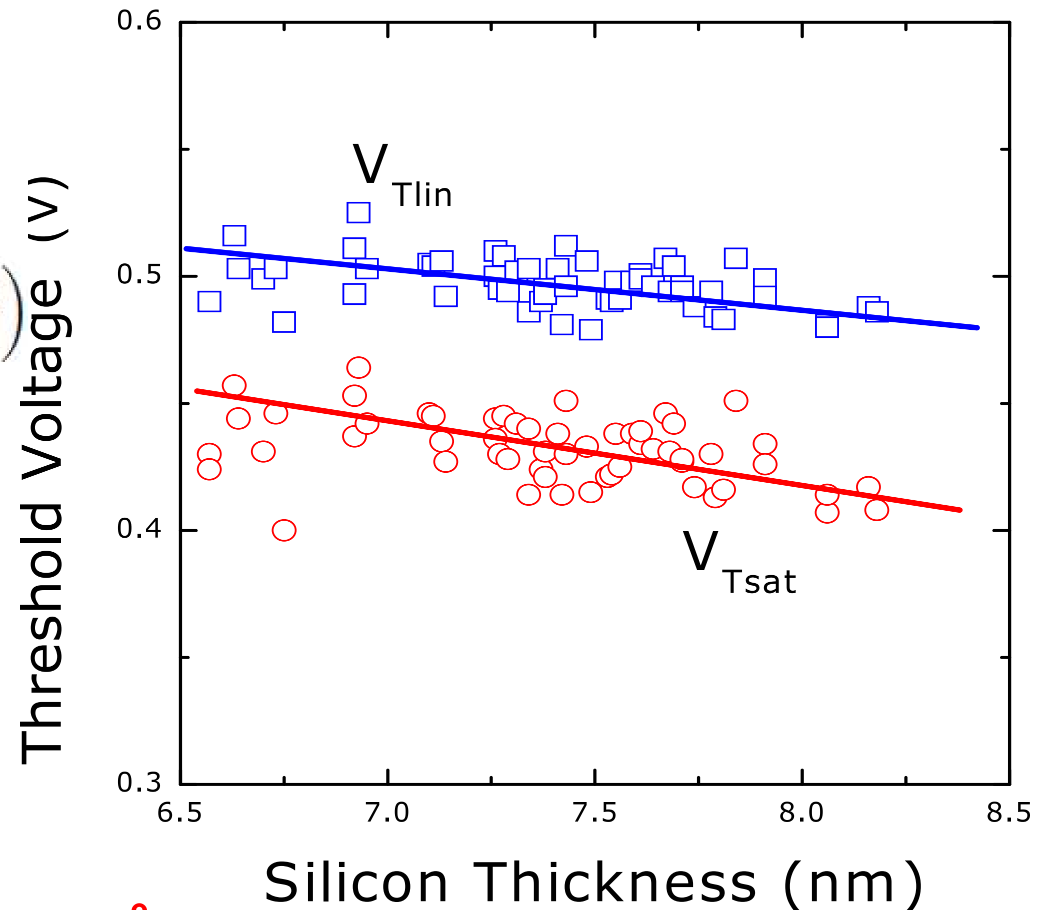


UTBOX
1.5nm

Global V_T Variation vs. FDSOI Thickness Variation

$$V_{Th}^{A} = \psi_{sf} + \frac{C_{Si}}{C_{OXf}}\psi_{sf} + \frac{qN_A t_{Si}}{2C_{OXf}}$$

$$V_{Th}^{D} = \psi_{sf}\left(1 + \frac{C_{Si}}{C_{OXf}}\right) + \frac{qN_A t_{Si}}{2C_{OXf}} + \frac{C_S C_{OXb}}{C_{OXf}(C_{OXb} + C_{Si})}\left(\frac{C_{Si}\psi_{sf}}{C_{OXb}} - \frac{qN_A t_{Si}}{2\epsilon_{Si}}\right)$$



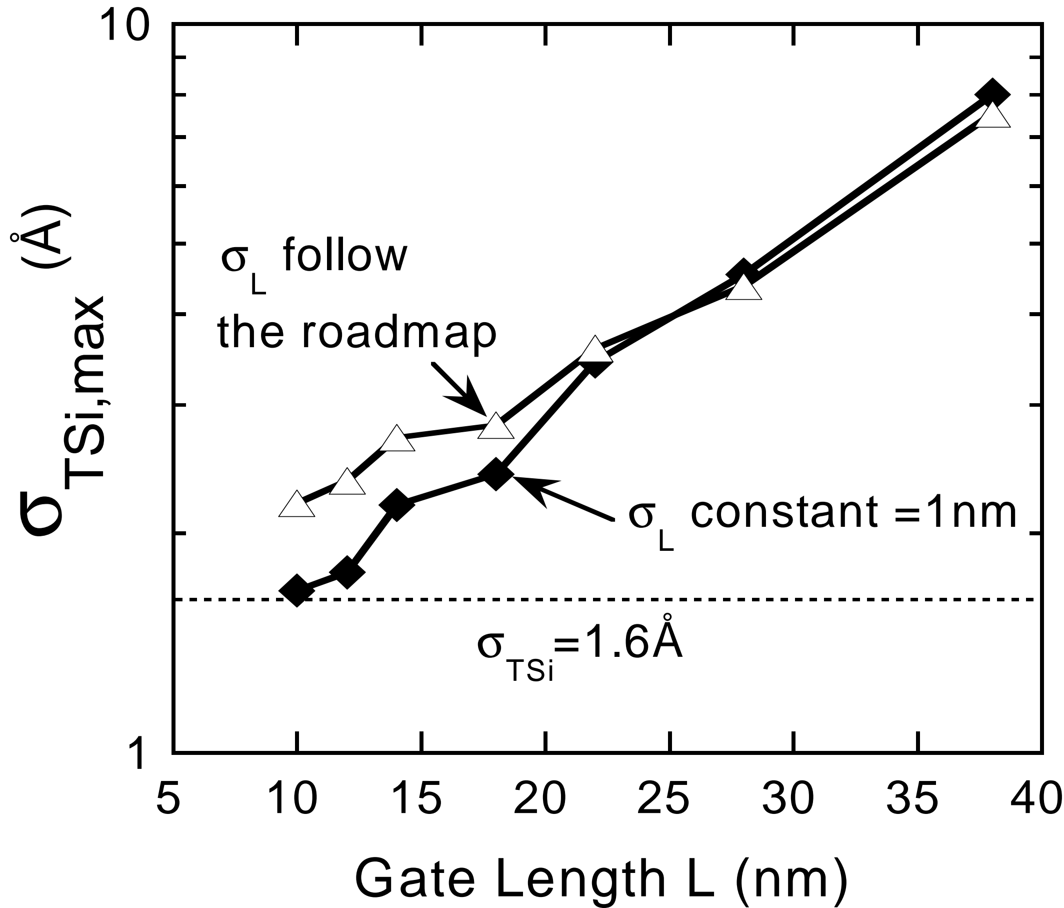
- V_T sensitivity ~ 25mV/nm
- L_G=25nm - multiple sources contributing to V_T variation

"All transistors should have Tsi within +/-5Å"

B. Doris et. al. FDSOI Workshop Dec. 9, 2009

σ_{TSi} roadmap for FDSOI

BOX scaling allows relaxation T_{Si} and T_{ox} and σ_{TSi} !



σ_{TSi} should be below 2Å for 22 – 11 nm nodes

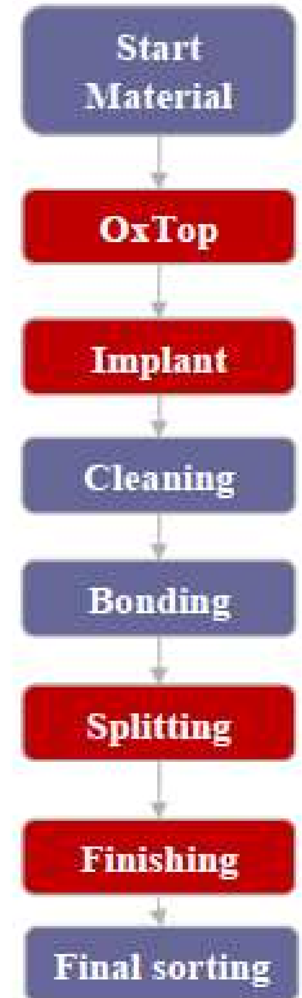
In the (10nm – 100mm)$^{-1}$ spatial frequency range

Courtesy of O.Weber, CEA-LETI

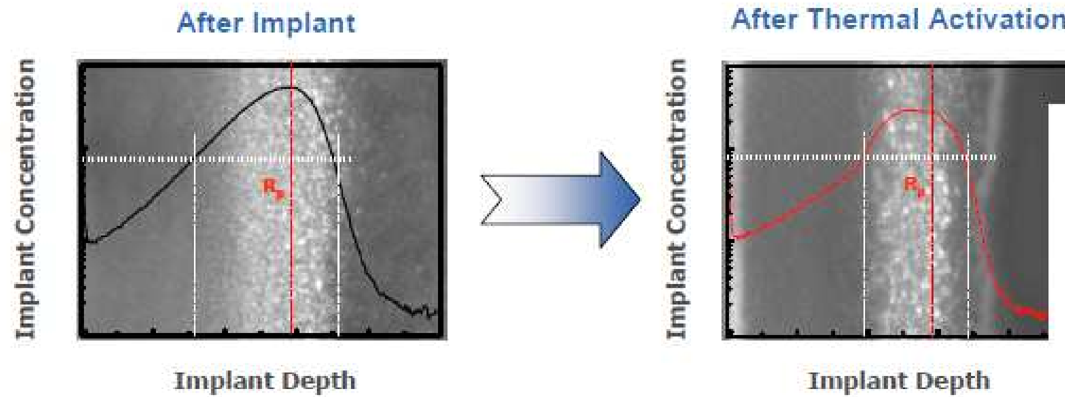
SmartCut process flow

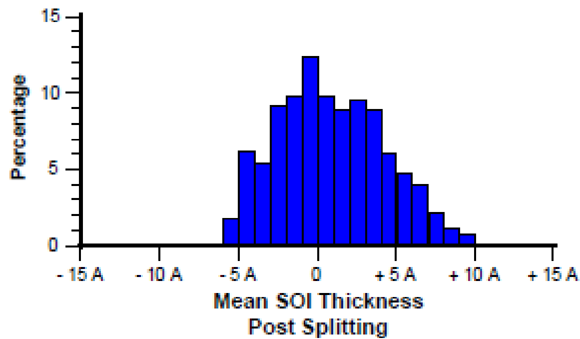
A
1_Initial silicon
B
A
2_Oxidation
A
3_Implantation
4_Cleaning and bonding
A
B
A
5_Splitting
6_Finishing
7_Donor wafer becomes new wafer A
SOI wafer

Thickness Uniformity Driver

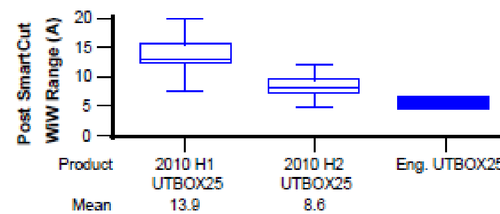


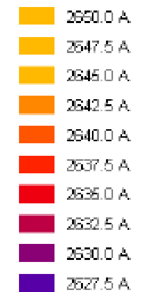
SmartCut thickness uniformity after splitting



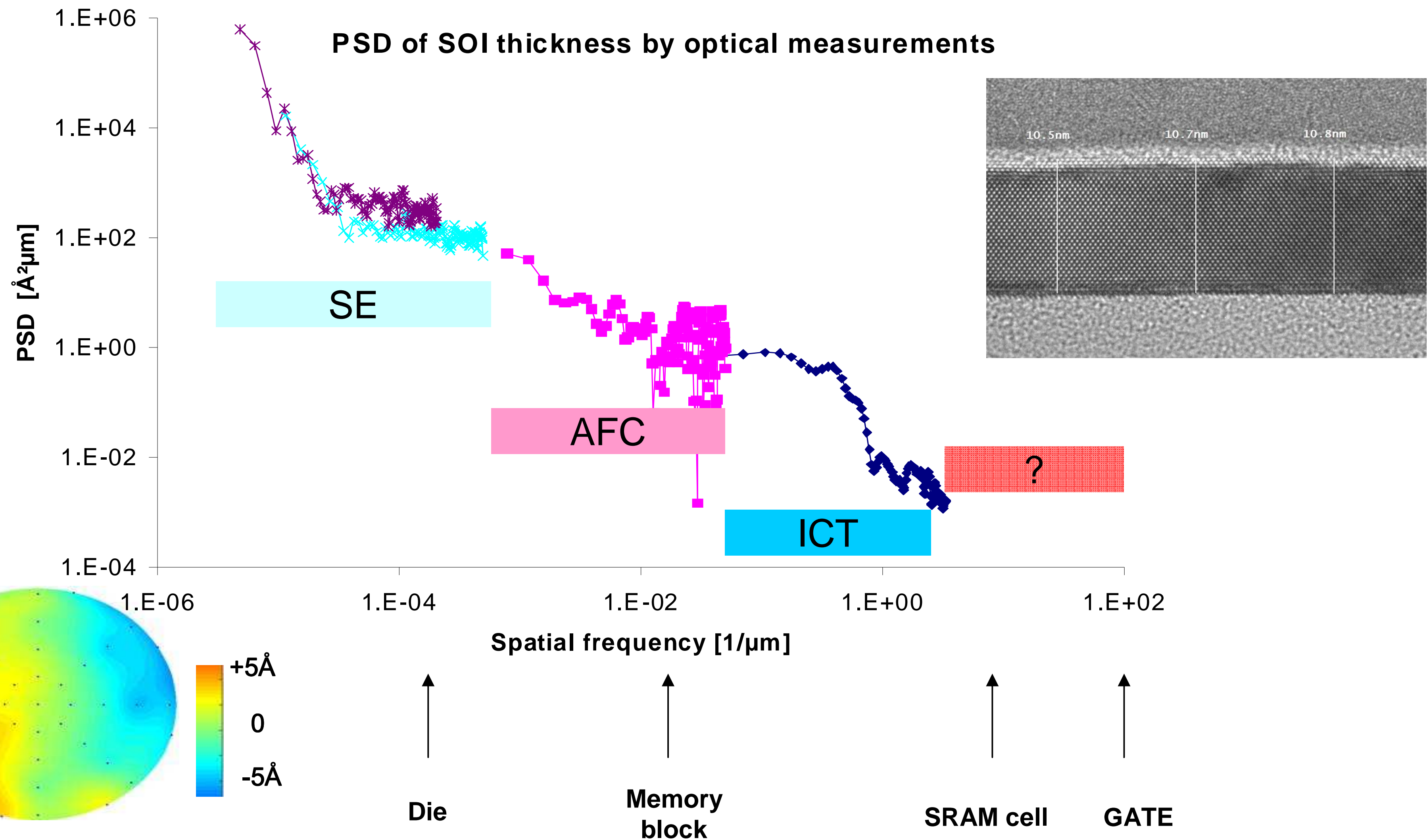


SmartCut enhancement demonstrated
Post splitting range ≤ oxide range





Spatial frequency spectrum of SOI thickness variation



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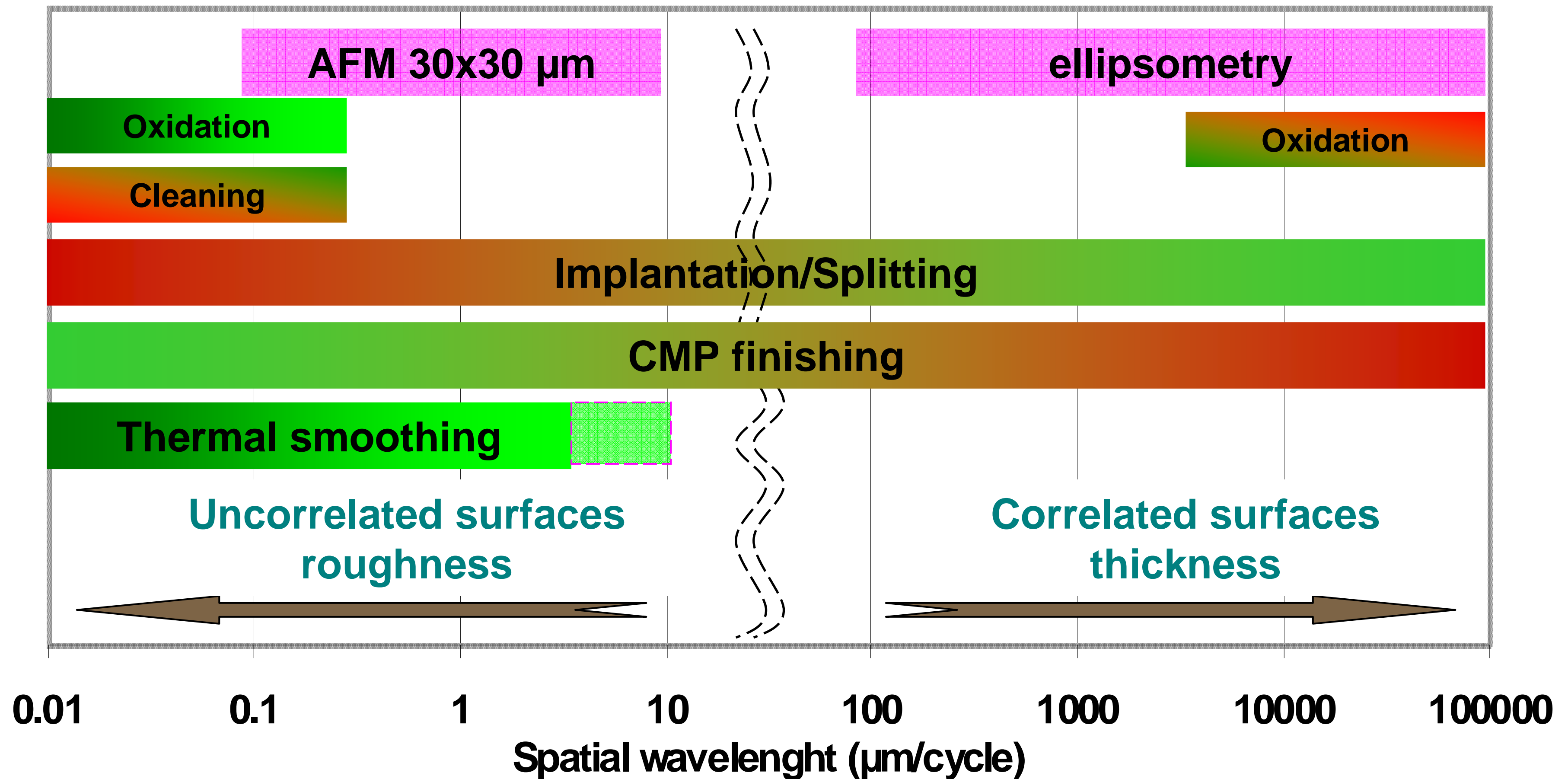
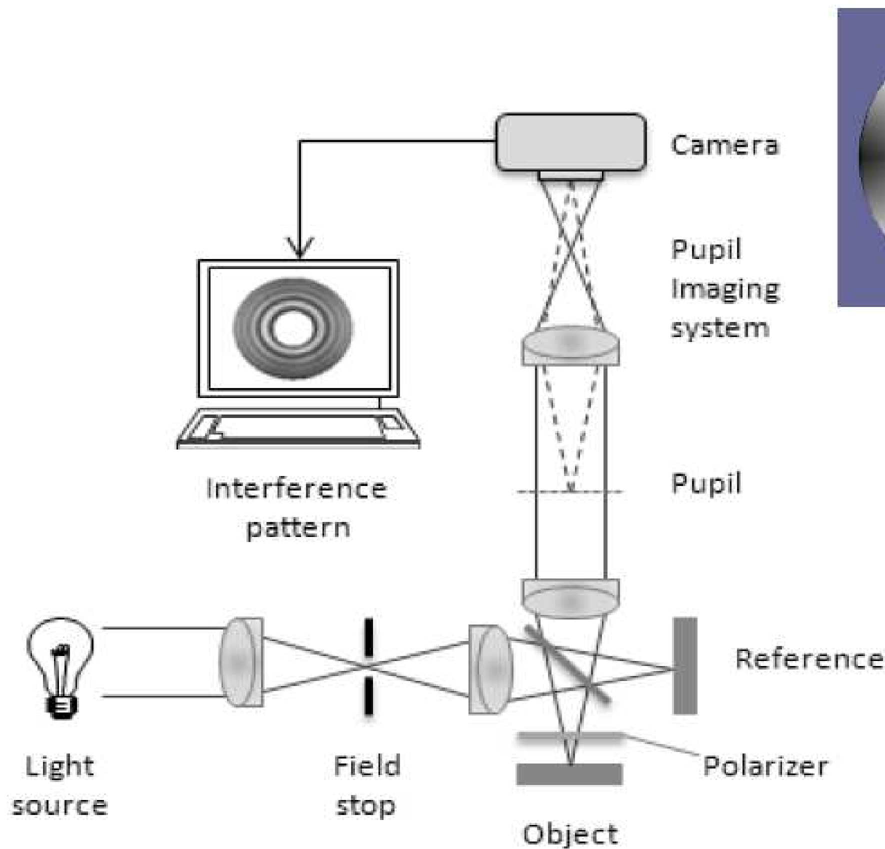
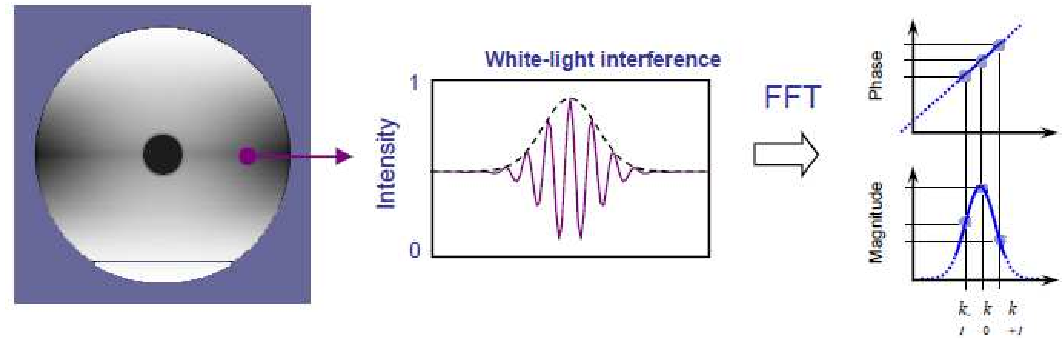
Effect of SOI processes on thickness variation



- Optimization of implantation/splitting
- Replacement of CMP by annealing in inert ambient

White Light Pupil Plane Interference Microscopy (Advanced Film Capability)





Standard SWILI setup with additional lens which images objective pupil into the camera

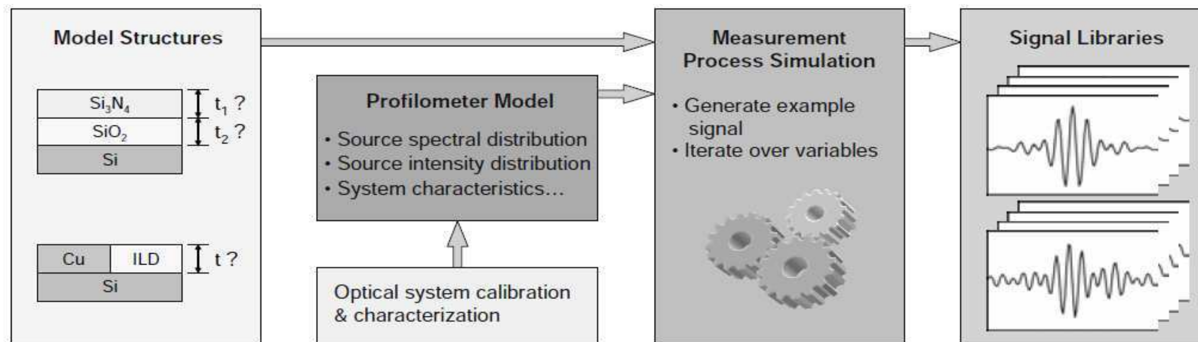
Each pupil point gives information about electric field:

- **azimuth – polarization**
- **radial position – angle of incidence**
- **swili – wavelength**

Spatial resolution is defined by field stop = 10µm

X. Colonna de Lega and P. de Groot, Proc. of SPIE 6995; pp. 1-9, 2008

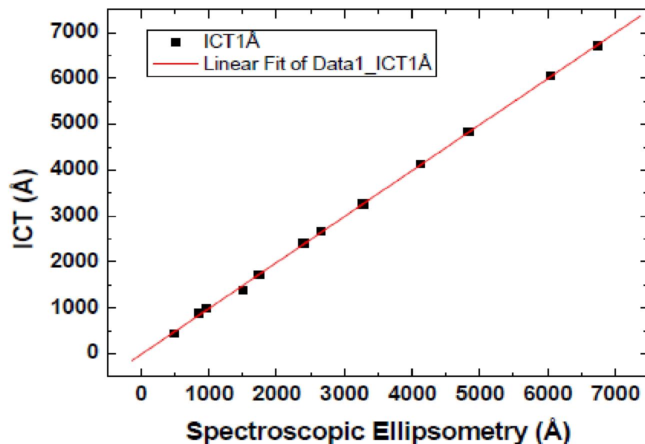
Scanning White Light Interference Microscopy
ICT – index corrected topography



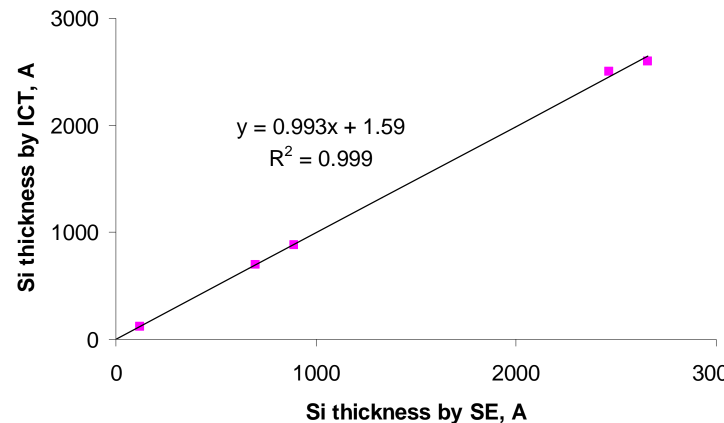
For each pixel for 10x10µm field an interferogramm is collected and compared with the library of signals. Thickness, height is determined by the best fit.

P. de Groot and X. Colonna de Lega, Proc. of SPIE 7064, pp. 1-6, 2008

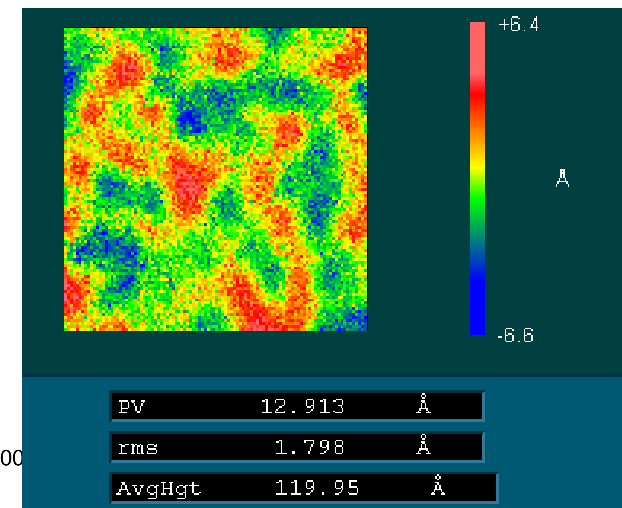
Calibration on oxide film



Calibration on SOI



SOI thickness map

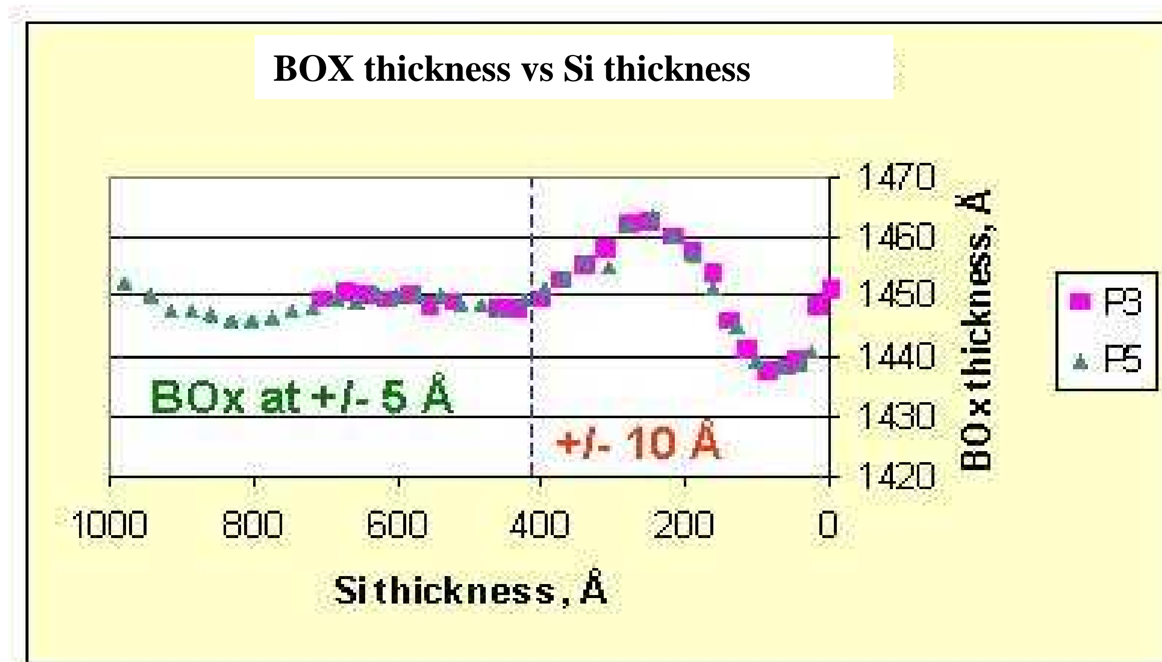


Thickness measurement open questions

Lack of metrology in 10nm – 1µm spatial domain

Lack of traceable SOI thickness standards

Accuracy of ellipsometric models



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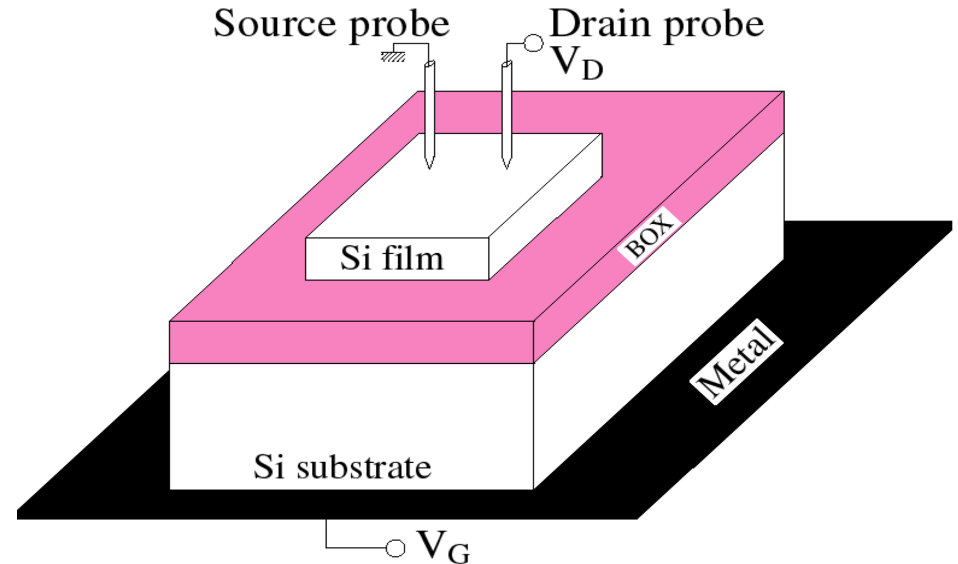
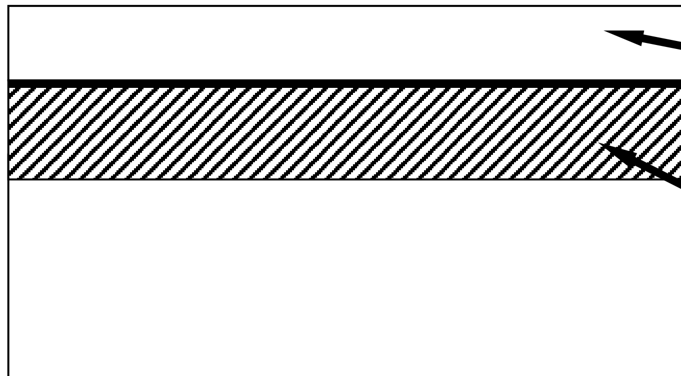
Introduction to the Pseudo-MOSFET : Ψ-MOS

Raw material analysis with little sample processing.
⇒ Characterization of material and **not processing technology** (contrary to device processing). Much **faster** turn-around.

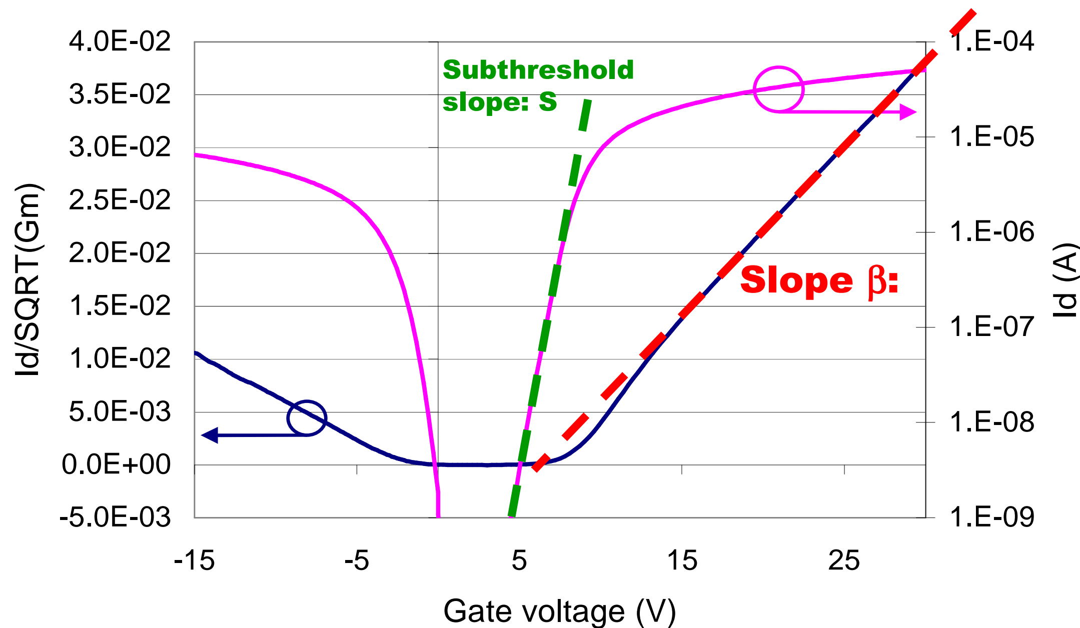




Characterization of:

- **Si film** (electron μ_e et hole μ_p mobility) **!!!** **close to the interface !!!**
- **Si / BOX interface** (Dit)
- **BOX** (Q_{BOX})

The Pseudo-MOSFET Measurement



Pink : $I_D(V_G)$ Blue : $F = \frac{I_D}{\sqrt{\partial I_D / \partial V_G}}(V_G)$

Input parameters:

- Film thickness T_{Si}
- BOX thickness T_{BOX}
- Physical constants (ε_{Si}, ε_{ox} …)
- Applied drain/gate bias
- Geometrical factor (f_g)

Measured data:

- Drain current
- Source current
- Gate current

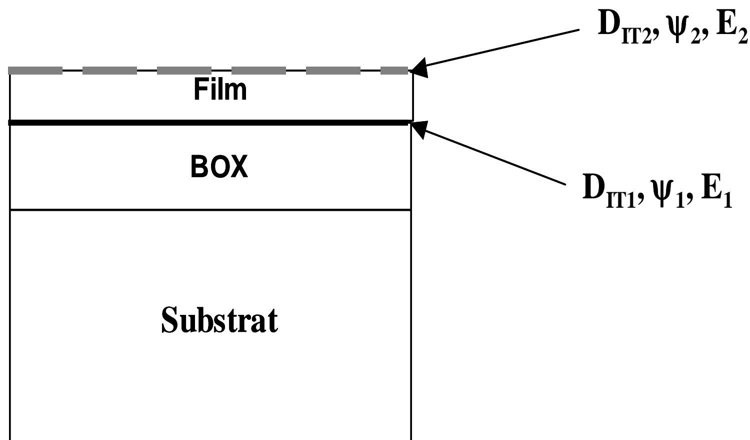
$$\mu_0 = \frac{\beta^2}{f_g C_{BOX} V_D}$$

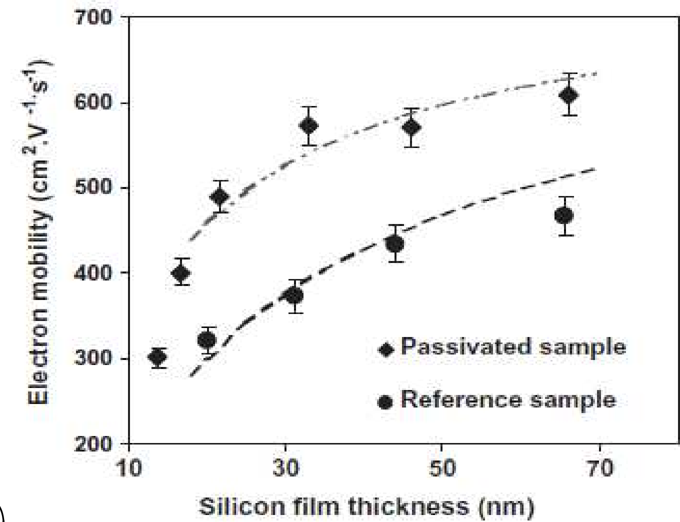
$$D_{it} = \frac{C_{BOX}}{q}\left[\frac{S}{60} - \left(1 + \frac{C_{Si}}{C_{BOX}}\right)\right]$$

Output parameters : Mobility (μ); Dit; Flat-band (V_{FB}) & Threshold (V_T) voltages; Oxide charge (Q_{BOX})

Quantitative Ψ-MOS. Two interface model.

All extracted parameters can be influenced by top surface (strong Dit), which gets closer when the film gets thinner !





G.Hamaide et al. 2010

$$S \cong \frac{\ln 10}{C_{BOX}} \left(\beta - \frac{1}{E_1 T_{Si}} \frac{C_{IT2}}{(C_{IT2} + C_{Si})} \right)^{-1} \left(C_{BOX} + C_{IT1} + \frac{C_{Si} C_{IT2}}{C_{Si} + C_{IT2}} \right)$$

$$E_1 = \frac{1}{T_{Si}} \left(\psi_1 - \psi_2 + \frac{qN_A}{2\varepsilon_{Si}} T_{Si}^2 \right)$$

Thin films require models which take into account top surface Dit (fitting parameter):

- **Threshold : N.Bresson's model [N. Bresson & al., ECS Proc Vol. 2005-03, pp. 317-324]**
- **Dit : H.Hovel's model *[H.J. Hovel; SSE vol.47; pp. 1311-1333; 2003]***

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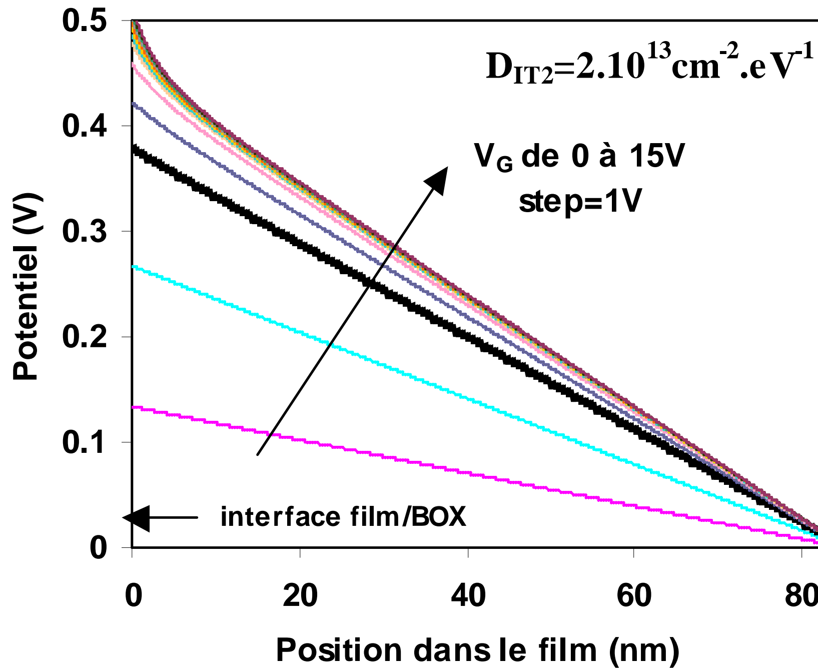
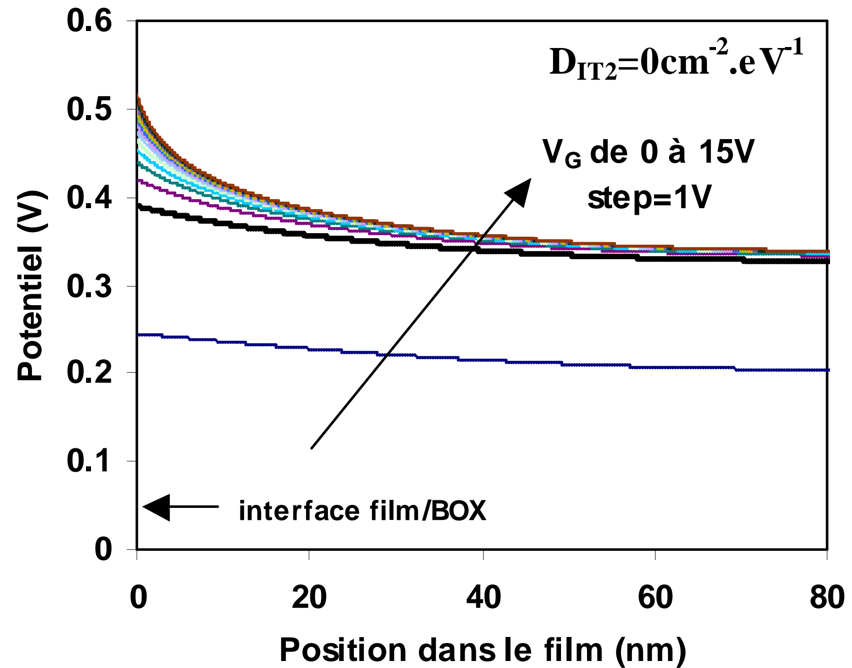
Quantitative Ψ-MOS. Two interface model.





Free-surface

(standard configuration)

Passivated surface

(ideal case)

$$S \cong \frac{\ln 10}{C_{BOX}} \left(\beta - \frac{1}{E_1 T_{Si}} \frac{C_{IT2}}{(C_{IT2} + C_{Si})} \right)^{-1} \left(C_{BOX} + C_{IT1} + \frac{C_{Si} C_{IT2}}{C_{Si} + C_{IT2}} \right) \qquad E_1 = \frac{1}{T_{Si}} \left(\psi_1 - \psi_2 + \frac{q N_A}{2 \varepsilon_{Si}} T_{Si}^2 \right)$$

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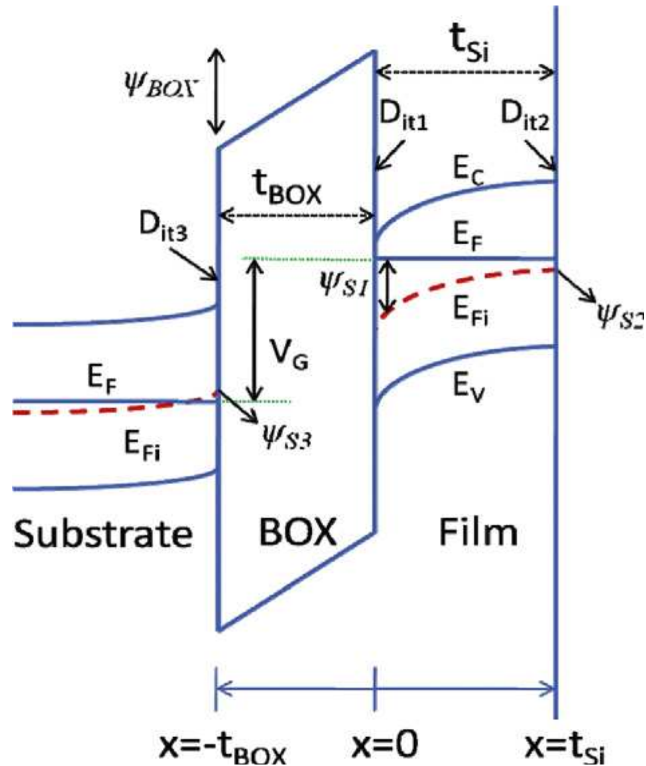
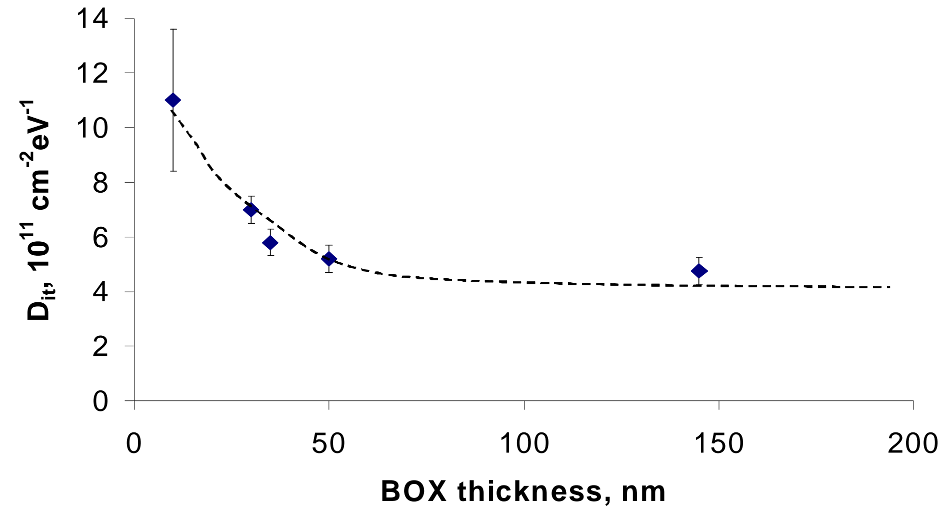
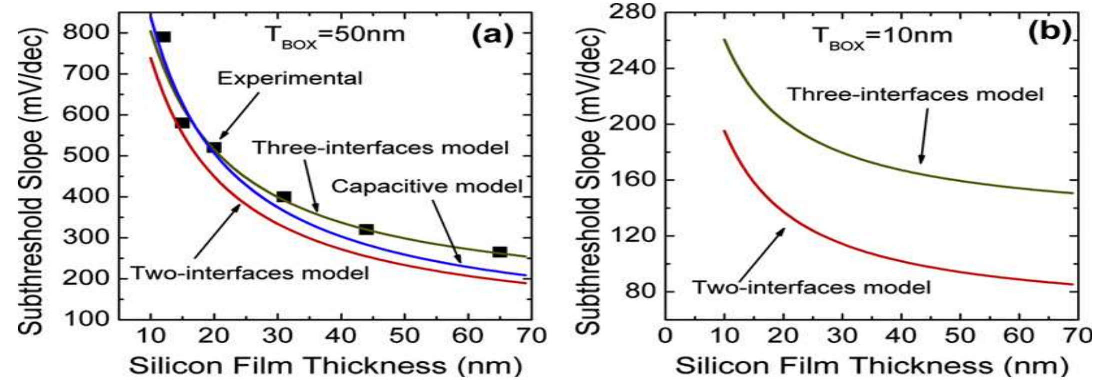
Three interface model. Effect of BOX thickness.



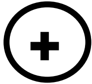




N.Rodriguez, Microel.Eng., 2011

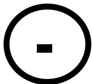
Three interface model predicts quite well effect of BOX thickness

Advantages & limits of the technique



- Very inexpensive technique compared to device processing
- Very fast mobility / Dit measurement technique
- Good screening technique (sensitive to defects)
- Acceptable R&r (<10%)

But :



- Sensitivit limit of Dit ~ few e11 $cm^{-2}eV^{-1}$
- Thin layer measurements require surface passivation
- Complex modeling with fitting parameter to account for thickness effects
- Gives effective mobility, which is difficult to compare with “device” mobility

- **Technique is very powerful tool if used for comparative studies or SPC, but difficult to obtain quantitative parameters**

Mobility Enhancement by Material and Strain Engineering

SiGe20%
SiGe30%
SiGe40%
SiGe50%
SiGe60%
SiGe80%
Ge

XsSOI 30%
SiGe40%/sSOI
SiGe50%/sSOI
SiGe60%/XsSOI
SiGe20%/sSOI
SiGe40%/sSOI
SiGe30%/sSOI
XsSOI 30%
sSOI 20%
SiGe40%/SOI
SiGe30%/SOI
SiGe80%/SOI
SiGe20%/SOI
SiGe60%OI
SiGe40%OI

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SOI defectivity according to ITRS

Table FEP10 Starting Materials Technology Requirements											
Year of Production	*2009*	*2010*	*2011*	*2012*	*2013*	*2014*	*2015*	*2016*	*2017*	*2018*	*2019*
DRAM ½ Pitch (nm) (contacted)	52	45	40	36	32	28	25	23	20	18	16
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	54	45	38	32	27	24	21	19	17	15	13
MPU Physical Gate Length (nm)	29	27	24	22	20	18	17	15	14	13	12
DRAM Total Chip Area (mm^2)	61	47	49	39	31	49	39	31	49	39	31
DRAM Active Transistor Area (mm^2)	19.2	14.5	21.2	16.8	13.3	21.2	16.8	13.3	21.2	16.8	13.3
MPU High-Performance Total Chip Area (mm^2)	260	184	260	184	260	206	164	260	206	164	260
MPU High-Performance Active Transistor Area (mm^2)	34.7	25.4	37.2	27.3	40.2	32.3	25.9	41.7	33.5	26.9	43.2
*General Characteristics * (99% Chip Yield)*											
Maximum Substrate Diameter (mm)—High-volume Production**	300	300	300	300	300	450	450	450	450	450	450
Edge exclusion (mm)	2	2	2	2	2	2	2	2	2	2	2
Front surface particle size (nm), latex sphere equivalent (A)	≥65	≥45	≥45	≥45	≥32	≥32	≥32	≥22	≥22	≥22	≥16
Particles (cm^{-2})***	≤0.18	≤0.18	≤0.18	≤0.18	≤0.18	≤0.18	≤0.18	≤0.18	≤0.18	≤0.18	≤0.18
Particles (#/wf)****	≤126	≤126	≤126	≤126	≤126	≤286	≤286	≤286	≤286	≤286	≤286
Site flatness (nm), SFQR 26mm x 8 mm Site Size	≤52	≤45	≤40	≤36	≤32	≤28	≤25	≤23	≤20	≤18	≤16
Nanotopography, p-v (nm), 2 mm dia. analysis area (I)	≤13	≤11	≤10	≤9	≤8	≤7	≤6	≤6	≤5	≤4	≤4
*Epitaxial Wafer * (99% Chip Yield)*											
Large structural epi defects (DRAM) (cm^{-2}) (B)***	≤0.016	≤0.016	≤0.016	≤0.016	≤0.016	≤0.016	≤0.016	≤0.016	≤0.016	≤0.016	≤0.016
Large structural epi defects (MPU) (cm^{-2}) (B)***	≤0.004	≤0.004	≤0.004	≤0.004	≤0.004	≤0.004	≤0.004	≤0.004	≤0.004	≤0.004	≤0.004
Small structural epi defects (DRAM) (cm^{-2}) (C)***	≤0.033	≤0.033	≤0.033	≤0.033	≤0.033	≤0.033	≤0.033	≤0.033	≤0.033	≤0.033	≤0.033
Small structural epi defects (MPU) (cm^{-2}) (C)***	≤0.008	≤0.008	≤0.008	≤0.008	≤0.008	≤0.008	≤0.008	≤0.008	≤0.008	≤0.008	≤0.008
*Silicon-On-Insulator (SOI) Wafer * (99% Chip Yield)*											
Edge exclusion (mm)*****	2	2	2	2	2	2	2	2	2	2	2
Starting silicon layer thickness (Partially Depleted) (tolerance ± 5%, 3σ) (nm) (D)	54-83	50-76	46-71	43-65	40-60	38-56	35-52	33-48	31-45	Note: Table entries may be	
Starting silicon layer thickness (Fully Depleted) (tolerance ± 5%, 3σ) (nm) (E)		17-32	16-21	16-20	15-19	14-17	14-16	13-16	13-15	13-15	13-14
Buried oxide (BOX) thickness (Fully Depleted) (tolerance ± 5%, 3σ) (nm) (F)		40-66	36-60	34-56	30-50	28-46	26-42	24-38	22-36	20-32	18-30
D_{LASOI} Large area SOI wafer defects (DRAM) (cm^{-2}) (G)***	≤0.016	≤0.016	≤0.016	≤0.016	≤0.016	≤0.016	≤0.016	≤0.016	≤0.016	≤0.016	≤0.016
D_{LASOI} Large area SOI wafer defects (MPU) (cm^{-2}) (G)***	≤0.004	≤0.004	≤0.004	≤0.004	≤0.004	≤0.004	≤0.004	≤0.004	≤0.004	≤0.004	≤0.004
D_{SASOI} Small area SOI wafer defects (DRAM) (cm^{-2}) (H)***	≤0.262	≤0.262	≤0.238	≤0.238	≤0.238	≤0.238	≤0.238	≤0.238	≤0.238	≤0.238	≤0.238
D_{SASOI} Small area SOI wafer defects (MPU) (cm^{-2}) (H)***	≤0.145	≤0.145	≤0.135	≤0.135	≤0.125	≤0.125	≤0.125	≤0.121	≤0.121	≤0.121	≤0.116

- **LLS minimum detection size**
- **Definition of large vs small area defects in FDSOI**

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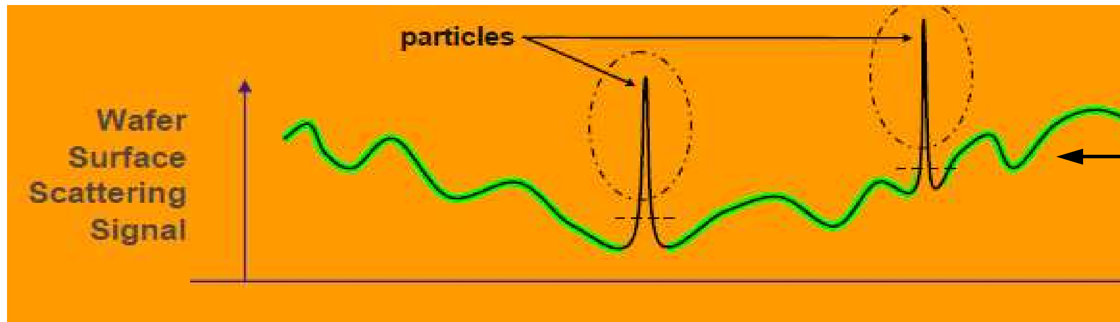
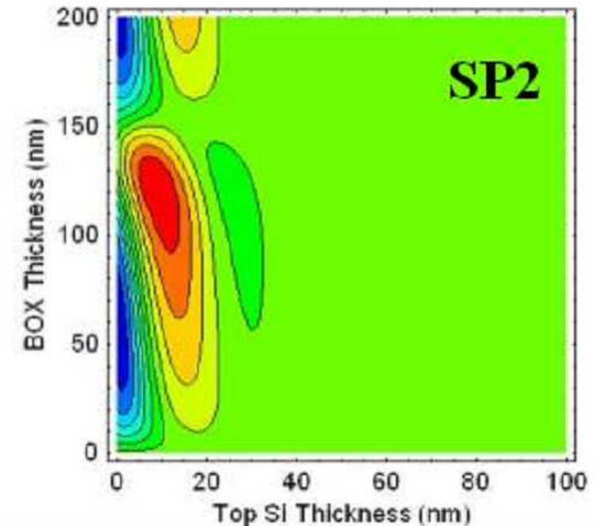
LPD size detection limit



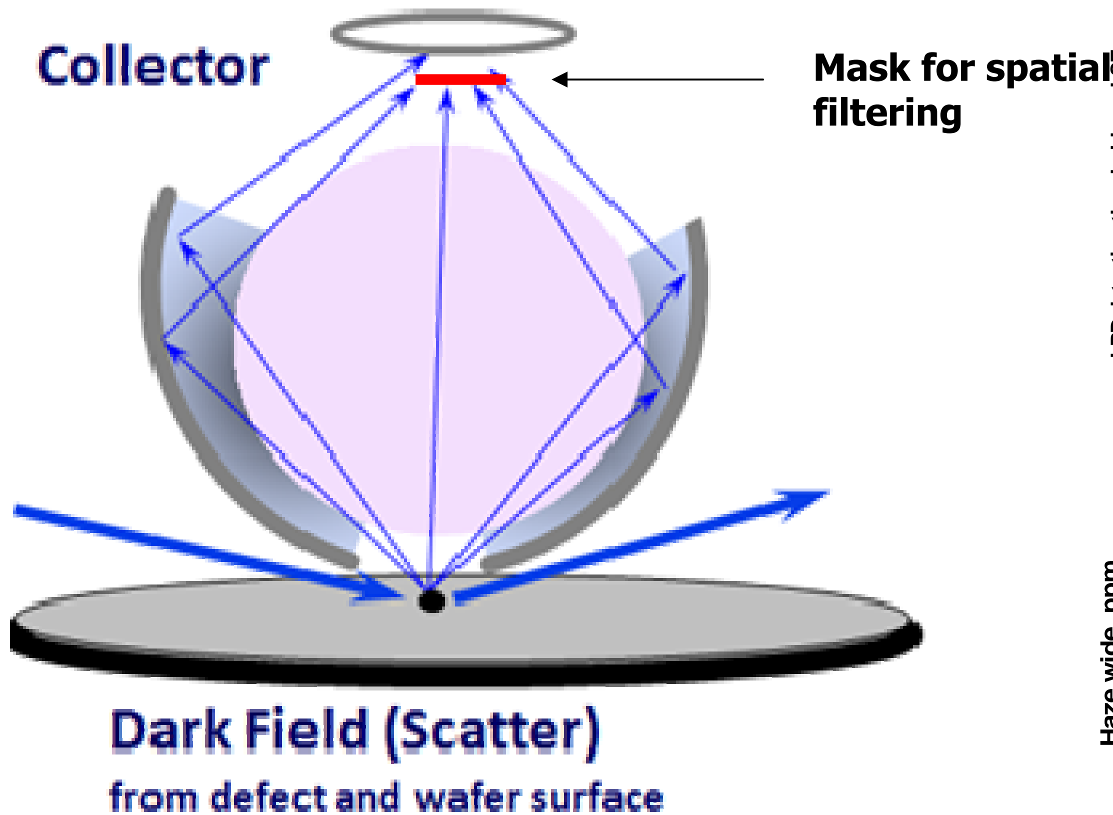
$$I_s = \left(\frac{4\pi \cos(\theta_i)}{\lambda} \right)^2 R \sigma^2$$

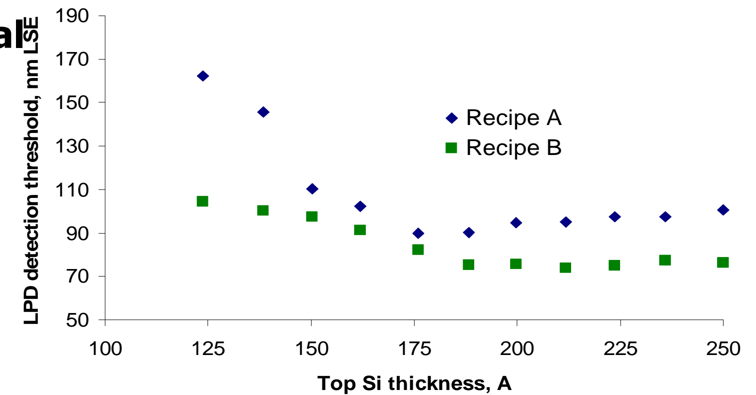
λ =355nm (SP2)

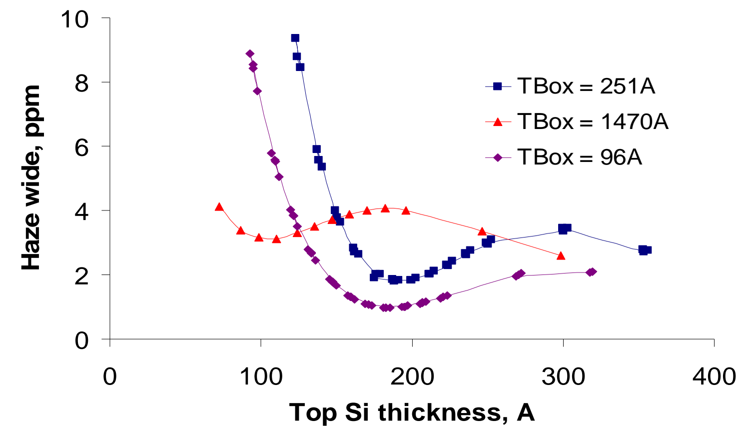


Interference in film stack changes SOI reflectivity
Additional scattering from BOX/Si interfaces

LPD detection limit improvement



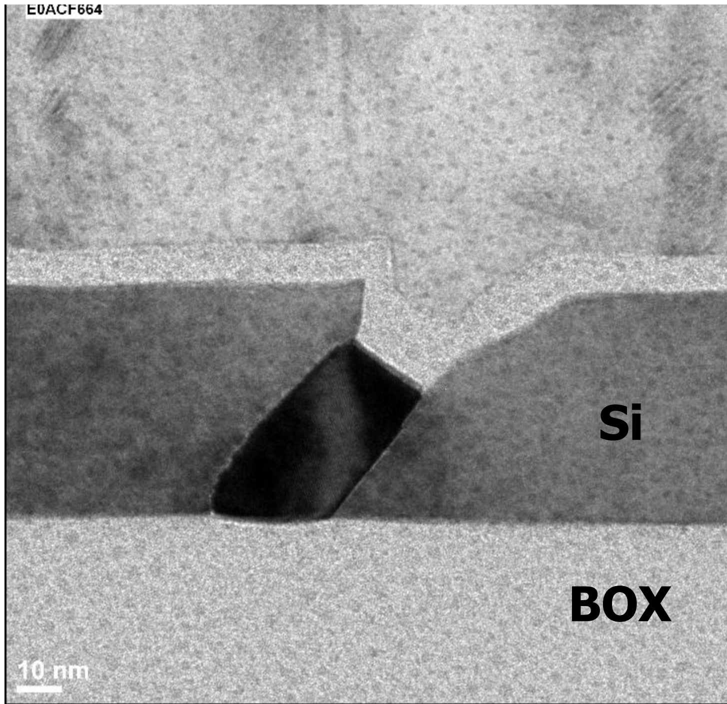




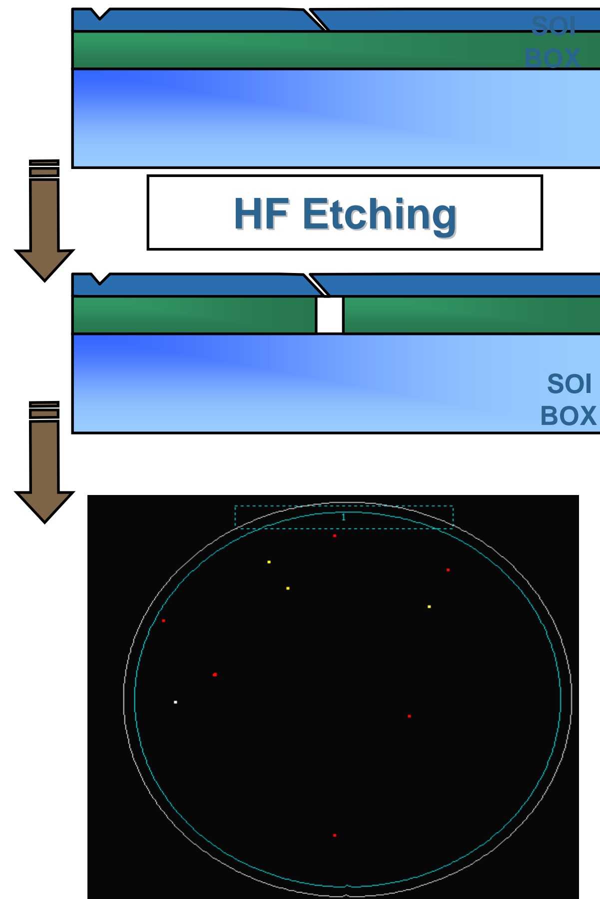
Introducing spatial frequency signal filtering in SP2 can improve detection limit on SOI upto 60%

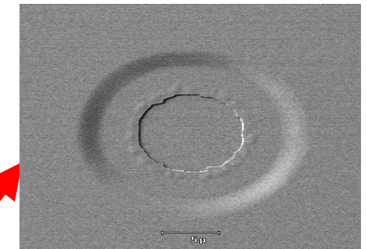
To satisfy requirements of ITRS new generation of LPD inspection tools needs to be developed

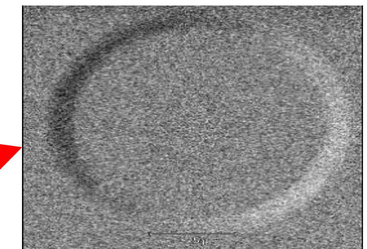
HF decoration technique for Large Area defects

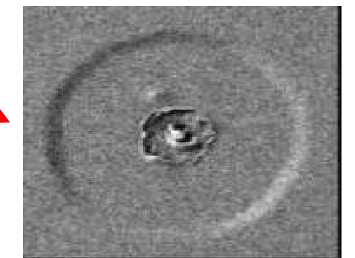


$FeSi_2$ precipitate in SOI





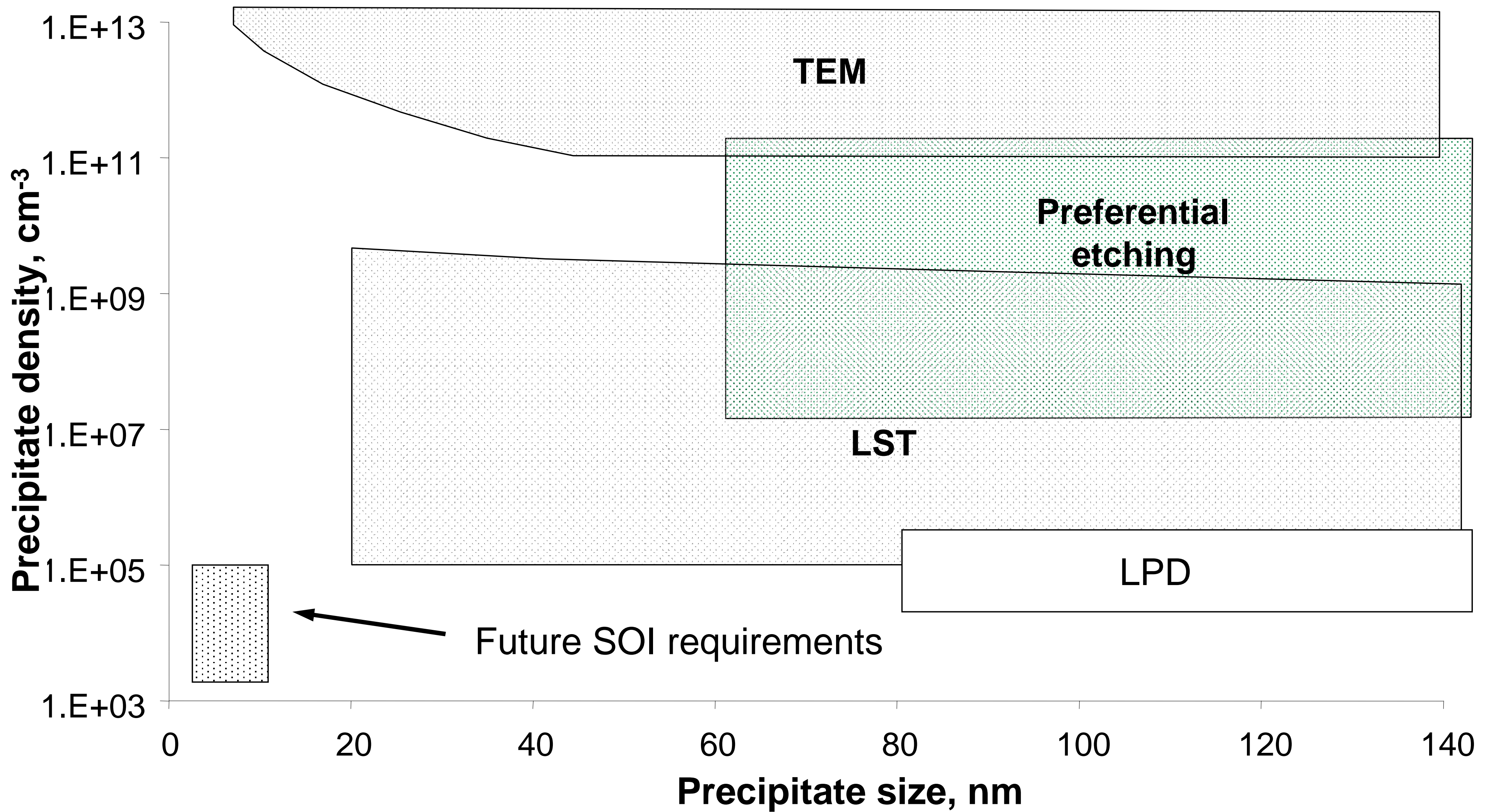




Physical size of large area defects (precipitates, holes in Si layer) will decrease according to Si layer thickness scaling

There is no nondestructive technique which is capable of detection sub 10nm inclusions

Precipitate metrology options



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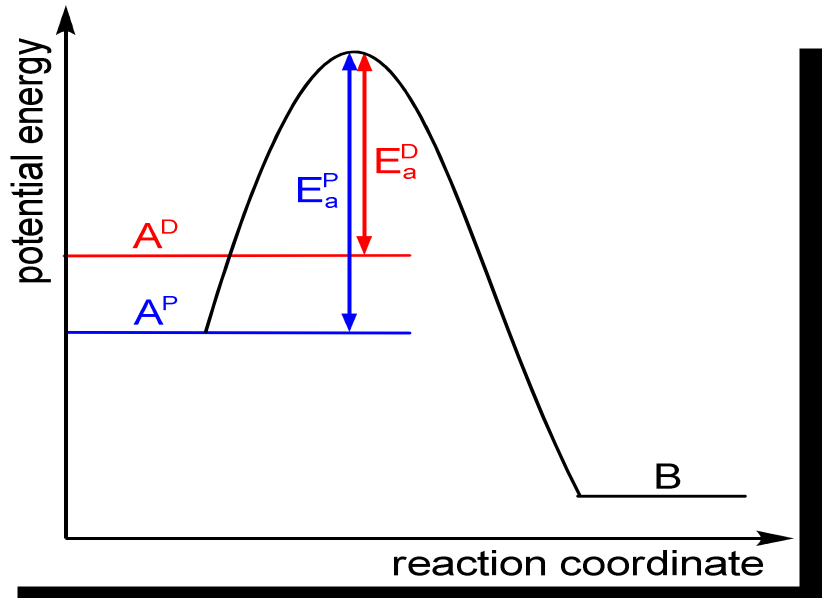
Outline

- Introduction
- Layer Thickness Measurements for FD SOI
- Electrical characterization of SOI layers
- LPD inspection challenge
- **Preferential Chemical Etching of Structural Defects**
- Conclusions

Preferential chemical etching



(A_P) = perfect crystal (A_D) = defect
$E^D{}_a$ = act. energy for reaction at defect

- **Different etch rate at defect site and crystal caused by surface potential**

- **Simplified reactions:**

  - reaction initiation (oxidizing agents..)
  - reaction propagation : (complexing agents..)

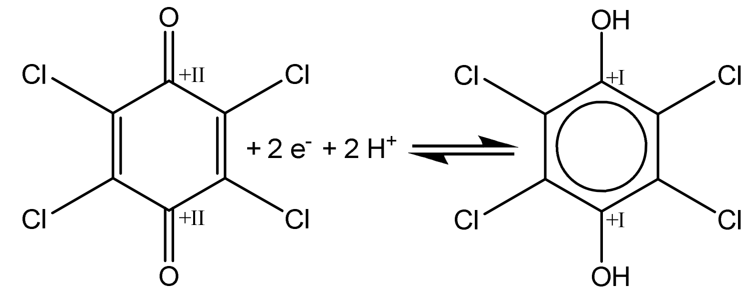
For thin layers needs second "highlight" step:

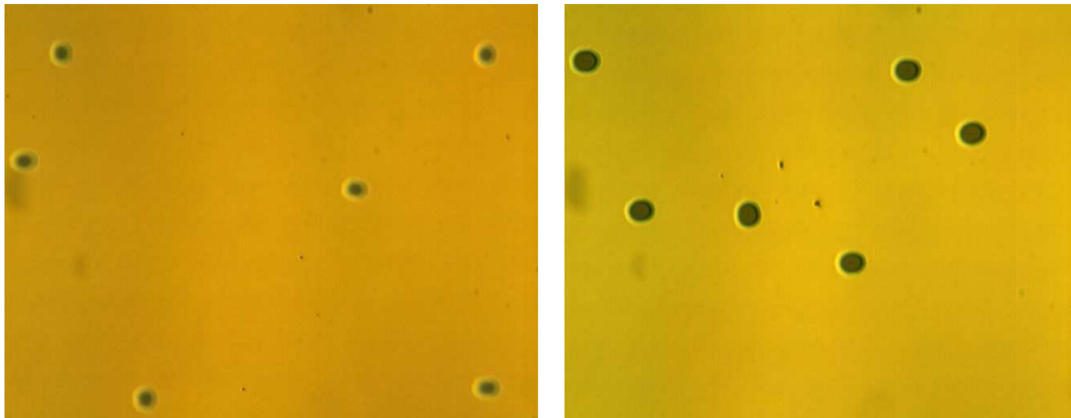
Secco/HF for SOI/sSOI ⇒ L.Giles et al. (1993), S.Bedell et al. (2005)
Secco/H_2O_2 for sSi/SiGe ⇒ G.Rozgonyi et al. (2005)

All best preferential etchants for Si are based on Cr^{6+} - toxic

Preferential chemical etching Cr-free solution

2,3,5,6-tetrachloro-1,4-benzoquinone (p-chloranil) solution in acetonitrile





p-CA in acetonitrile + HF | Secco (0.04 M)

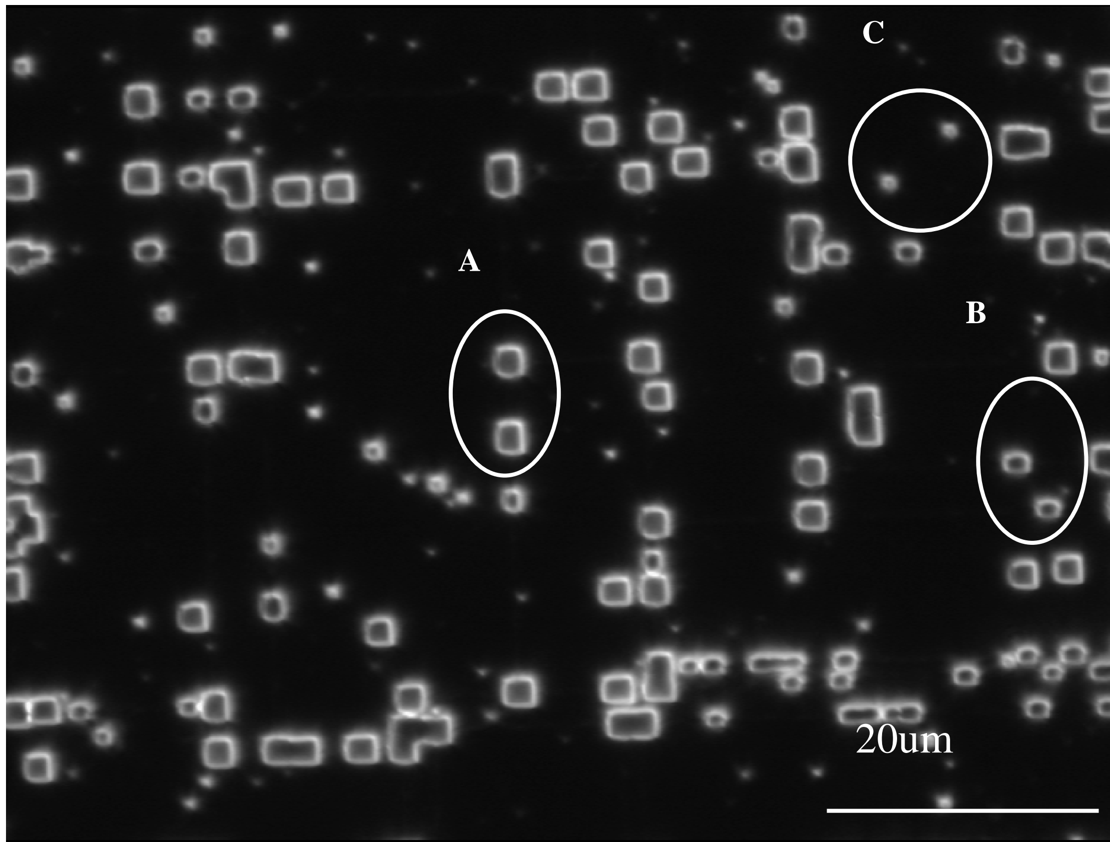
E_a = 32.5±1.1 kJ/mol | E_a = 34.1±1.2 kJ/mol

ΔEa = -1.4 kJ/mol (= -4.3 %) | ΔEa = -1.2 kJ/mol (= -3.5 %)

Non-toxic preferential etching of structural defects in SOI with same selectivity

J. Mähliß et al, ECS Journal 2011

Gas phase HCl etching of sSOI



sSOI (20%)
600A/1450A

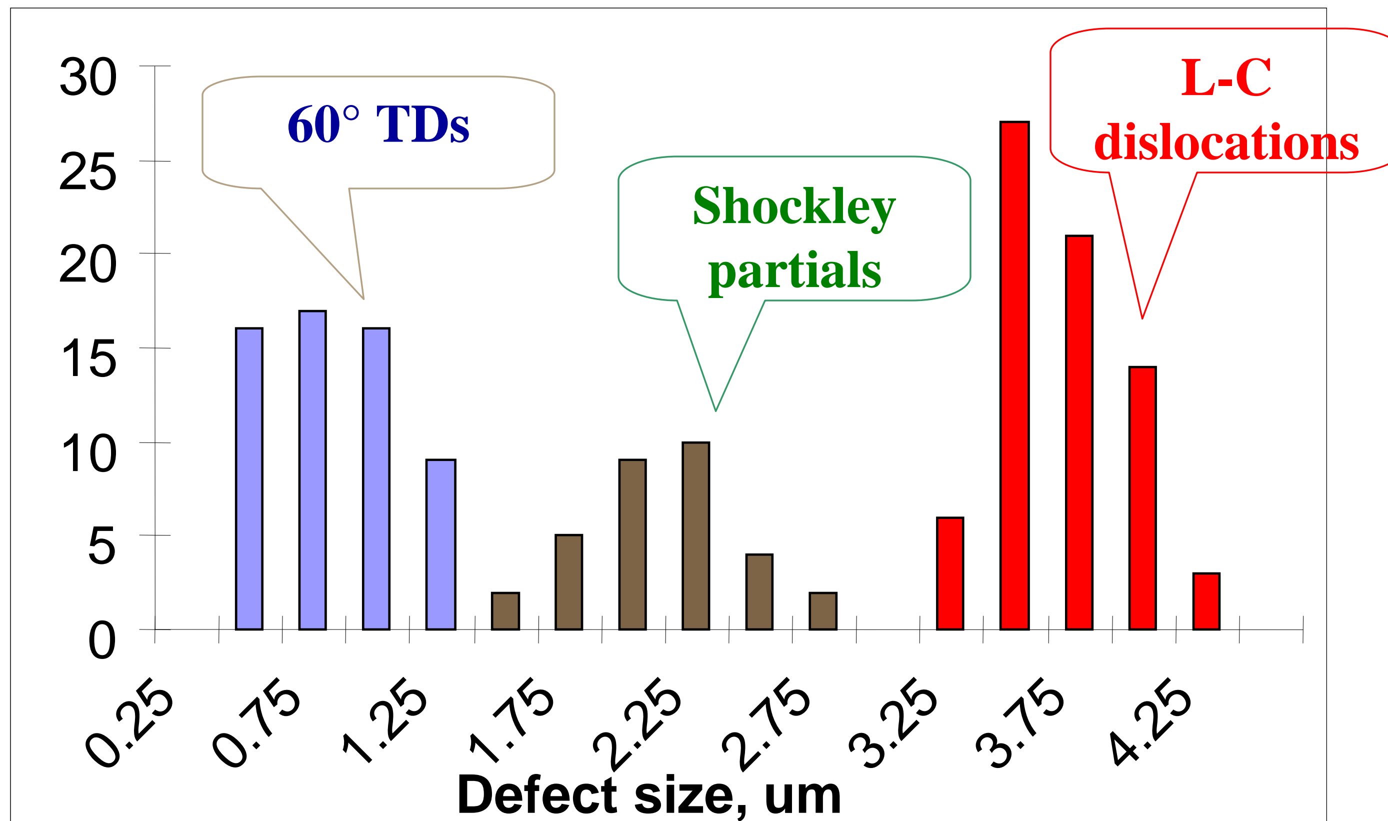
TDD ~ 10^6cm^{-2}

Three characteristic sizes of the defects

Optical microscope (x500) Nomarski contrast, 430 A of Si removed

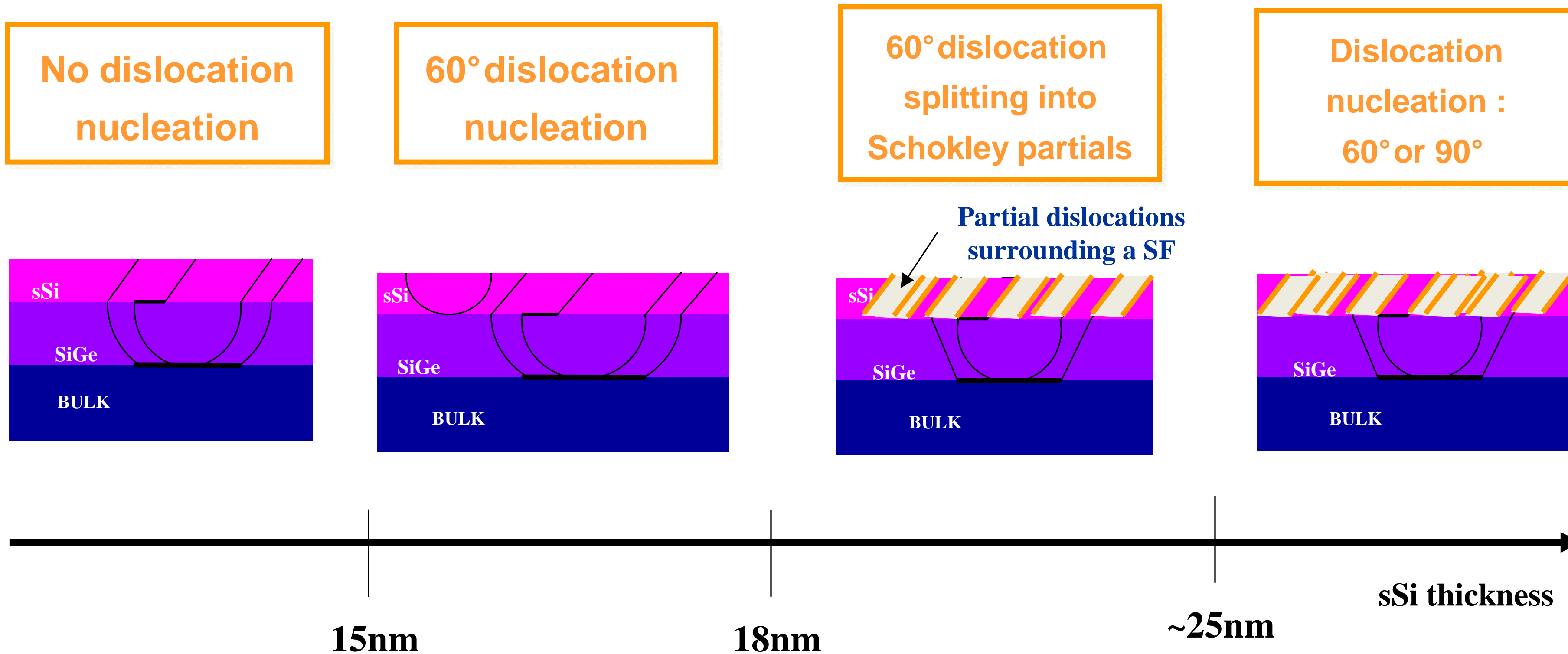
A.Abbadie et al, *J. Electrochem. Soc., 2007*

Dislocation type descrimination by etching



Statistical sample > 200 defects

Mechanism of sSi relaxation in low TDD films



- sSi relaxation proceed, above 18nm, by 60° dislocation splitting into Shockley partial surrounding a Stacking Fault

Conclusions

Development of FD MOSFET technology requires SOI wafers with ultra thin layers. SOI characterization techniques should be adapted to address specific requirements of FDSOI future products:

- **Layer thickness measurement techniques have to be expanded in higher spatial frequency domain**
- **New generation of LPD inspection tools has to be introduced to avoid interference effects**
- **Sensitivity of electrical characterization of BOX interfaces has to be improved**
- **New nondestructive techniques for structural characterization of defects in Si with sizes below 10nm have to be developed**