Short Papers

An Electronic Ratio Error Set for Current Transformer Calibrations

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Abstract—**A direct-reading electronic ratio error set for current transformer calibrations is described. It is capable of generating direct and quadrature error currents from 1 ppm to 5 percent of transformer secondary currents up to 10 A. The uncertainty is less than one percent of the generated current. The set features electronic display of the direct and quadrature components with three digits each and is direct reading at 50, 60, and 400 Hz.**

I. Introduction

Current transformers are generally calibrated by comparison against another ratio standard, either a current transformer or current comparator, as shown in Fig. 1. This technique has been described in previous literature [1], [2], [3]. It requires the injection of a small amount of current to balance the transformer error. The injection device must be able to generate a current having direct and quadrature components which are known proportions of the secondary current. The burden imposed by the circuit on the transformers must be small and the output impedance of the circuit must be large enough to avoid shunting current around the transformers. Because the device generates only the relatively small error current, and not the total secondary current, its accuracy need not be extremely high. It is called direct reading because it gives a readout of the injected current as a fraction of the secondary current at selected frequencies. This paper describes an electronic realization of the specified device based upon the circuit found in [1].

II. Description of Circuit

A block diagram of the circuit is shown in Fig. 2. The secondary current I_s is converted to a proportional voltage. The signal path then splits into two channels, direct and quadrature. The direct channel is scaled by a factor of α and the quadrature channel by β. The quadrature channel then receives a $\pi/2$ rad phase shift after which the channels are summed. Finally, the combined voltages are converted to a current.

Fig. 3 diagrams the current-to-voltage conversion. The secondary current flows through a four-terminal resistor of 0.1 Ω. The potential connections are attached to the input of an instrumentation amplifier. This is constructed from an operational amplifier with well-matched feedback and input resistors to give accurate gain and high common mode rejection. The input impedance is high enough to present negligible loading of the shunt. The gain can be switch-selected to be 5 or 10 depending upon the range of secondary current. The output voltage is connected both to a front panel jack for current monitoring and to the next stage for scaling of the direct and quadrature voltages.

This scaling is accomplished through the circuit indicated schematically in Fig. 4. Each channel uses the same circuit so only one is shown. A digital panel meter is used to generate a binary code which is applied to the digital inputs of a multiplying digital-to-analog converter. The voltage from the previous stage is applied to the analog input of the converter whose output is the the analog voltage scaled by the binary code. The panel meter display value, which is the decimal representation of the binary, is set by adjusting a 10 turn potentiometer to select the appropriate

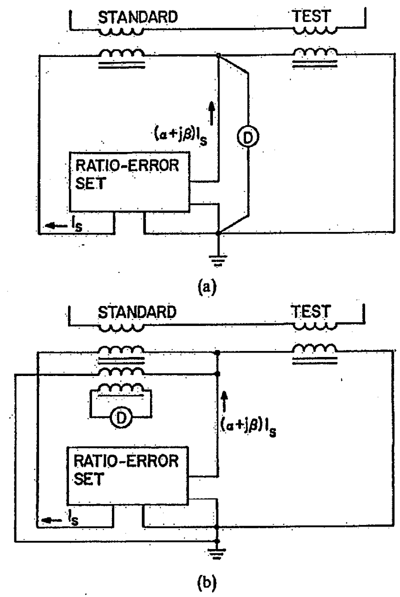

Fig. 1. Current transformer calibration circuits using current injection. (a) With standard current transformer as reference. (b) With compensated current comparator as reference.

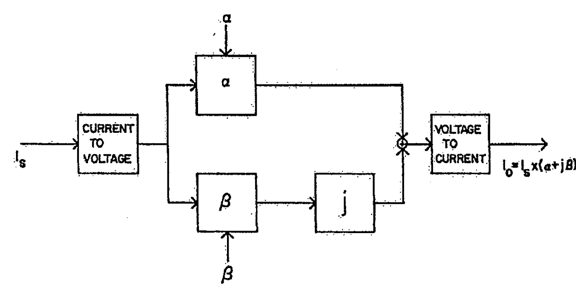

Fig. 2. Block diagram of ratio error set.

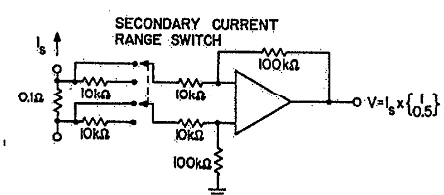

Fig. 3. Current-to-voltage conversion.

Manuscript received May 23, 1978.
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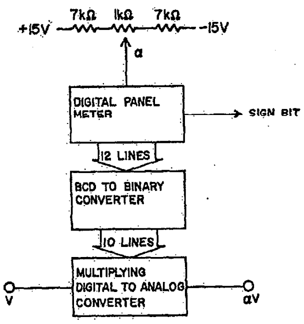

Fig. 4. Digital scaling of error signal.

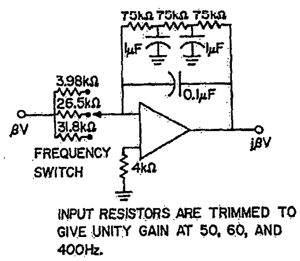

Fig. 5. Quadrature channel phase shift circuit.

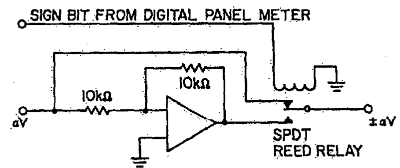

Fig. 6. Establishment of sign of error.

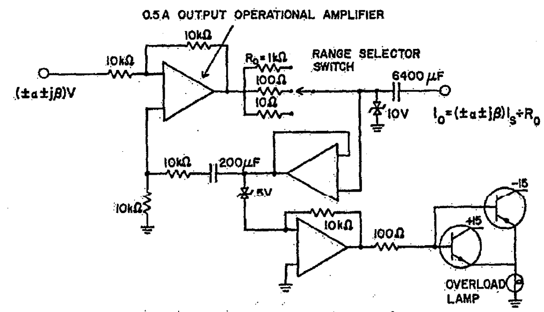

Fig. 7. Voltage-to-current conversion.

meter input voltage. In this fashion the scaling of direct and quadrature voltages is controlled by two knobs, one for each channel, as opposed to one for each digit of the scaling factor, and the scaling factor is displayed on the panel meter. The only critical specifications are the linearity and gain of the converter so the scaling accuracy is localized to a single component.

The quadrature channel receives a $\pi/2$ rad phase shift through a single integrator, as shown in Fig. 5. The operational amplifier has low offset voltage and current to facilitate dc stabilization. The feedback capacitor has a low dissipation factor to minimize phase error. The ladder network in the feedback provides a dc path for offsets while having high transfer impedance at operating frequencies to avoid phase error.

In this way, the phase shift is correct at any operating frequency without retuning. This is in contrast to the circuit of [1] which uses two phase shifting circuits, each adjusted to $\pi/4$ rad and having large frequency dependence of phase shift. The switch-selectable input resistors establish the integrator at unity gain for frequencies of 50, 60, and 400 Hz.

Each channel is then connected to a noninverting amplifier with an independently selectable gain of 1 or 10. This feature allows independent multiplication of one error component to make possible 3 digit display of each component, even if, as is sometimes the case, one is an order of magnitude smaller than the other.

After adjusting the magnitude of each component, it is necessary to establish the sign. This is accomplished as shown in Fig. 6 for one channel. The error voltage is supplied to the input of an inverting amplifier. A relay selects either the inverted or noninverted signal for transmission to later stages. The relay in turn is controlled by the sign bit produced by the digital panel meter previously mentioned.

Both components are then summed and applied to the input of a voltage-to-current converter, represented in Fig. 7. It is similar to that of [1] with two additions. The divider in the positive feedback loop is preceded by a high input impedance buffer thus reducing the systematic error due to leakage current through the divider. A second improvement is the overload detection and protection. If the output voltage becomes greater than 5 V there exists the possibility of exceeding the linear range of the operational amplifier. When this condition exists, Zener diodes on the output of the buffer amplifier conduct and a miniature incandescent lamp is driven. A semiconductor transient absorption device on the output clamps it at 10 V in order to prevent damage to the electronics in the event of an extreme voltage surge as might occur if a test transformer became open circuited.

The instrument was constructed using 0.01 percent ratio matching of critical input and feedback resistors where possible. The digital-to-analog (D/A) converters required trimming to obtain an accuracy of 0.1 percent; their linearity was found to be better than 0.1 percent by tests on the final instrument. The feedback capacitor used in the integrator was of polystyrene dielectric and had a dissipation factor of 0.01 percent. Combined with the phase error due to the *RC* ladder this gives 1-mrad phase error. The input resistors of the integrator were trimmed to give unity gain within 0.1 percent tolerance. Output impedance of the voltage-to-current circuit is about 250 kΩ producing negligible error in a current transformer calibration. The output resistors are all 0.1-percent tolerance. From consideration of the above sources of error, the total uncertainty is estimated to be less than 0.5 percent of the indicated error current.

III. Calibration

Two techniques were used for the calibration of the set. The first method requires only a stable power supply and a voltmeter having uncertainty of less than 0.1 percent. Current is passed through the four-terminal resistor and its value is measured at the output of the instrumentation amplifier, Fig. 3. This assumes the amplifier is accurate to better than 0.1 percent; in the present case, the gain resistors were matched to give an uncertainty of 0.01 percent. The power supply is adjusted to produce a convenient voltage, about 5 V. The output current is then determined by measuring the voltage across the output resistor R_0, Fig. 7. With the output grounded, the only significant error in this measurement will be the leakage through the voltmeter input impedance.

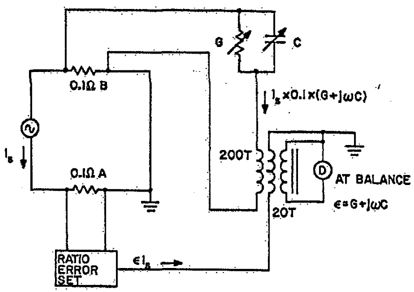

Fig. 8. Calibration of ratio error set.

R_0 is 1 kΩ at maximum so that a 1 mΩ input impedance enables the measurement to be made with a 0.1 percent uncertainty. The ratio between the input and output currents as determined by the voltage measurements is adjusted by means of the D/A trimming resistors and the quadrature trimming resistors until the ratio corresponds to the front panel readout. This is done at 50, 60, and 400 Hz after which the calibration is checked using the second method.

Fig. 8 diagrams the circuit used for the second calibration. Current passes through the reference resistor A of the test set and another four-terminal resistor B whose value is 0.1 Ω within 0.01 percent. The set generates an error current εI_s which is applied to one winding of a current comparator. The current in the other winding is developed through the application of voltage from the standard resistor B across a precision RC admittance. This gives an error current which is known with an uncertainty of less than 0.1 percent. The turns ratio between the two windings reduces the current which must be drawn from the four-terminal resistor B to balance a given test set error current. The results of this test indicate a discrepancy between the two calibrations of less than 0.2 percent of indicated error current at 50 and 60 Hz on all ranges. At 400 Hz the discrepancy increases to about 0.4 percent. This is due to the phase shift caused by the finite operational amplifier bandwidth.

IV. Conclusion

The instrument has been used for a year in the calibration of current transformers and transformer test sets at the National Bureau of Standards. It has performed well in tests of ratios up to 10 000:5. Increased accuracy and reliability result from the use of active electronics and precision passive components. The active output stage enables the calibration of current transformer test sets and provides a high output impedance for accurate calibration of current transformers. High output impedance is especially important when calibrating transformers with very high ratios, having large magnetizing impedances and significant voltages at the test set output. Under these conditions, passive test sets may have a nonconvergent balance. The active output removes this tendency. Operation of the electronic set is convenient and the results are unambiguously displayed. The electronic ratio-error set thus provides significant improvement over previous passive sets.

Acknowledgment

The author would like to thank T. M. Souders for his ideas on test set design and his useful discussions of current transformer theory and operation. Thanks are also due A. S. Lomnicki who helped with construction details and Mrs. J. C. Palla who typed the manuscript.

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The Utility of the All-Pass Filter

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***Abstract*—The all-pass filter has seen limited application as a phase-correction circuit for many years. This network can also be applied to many other important areas of electronic design. Applications ranging from inductorless bandpass filters to frequency-modulation circuits are discussed to demonstrate the broad utility of the all-pass network.**

I. Introduction

The all-pass filter is a network having a transfer function with constant amplitude response and a phase response that is a function of frequency [1]. Traditionally, the all-pass filter has been used for phase correction in filter design or in automatic control applications. In either of these situations, an adequate amplitude response can be preserved while improving phase response by cascading an all-pass network with the original network. Although this is an important application of the all-pass filter, there are several others that greatly extend the usefulness of this network. This article reviews the use of the active all-pass filter in designing highly selective tuned circuits, oscillators, phase and frequency modulators, and current controllers for SCR power supplies.

Fig. 1 shows two useful versions of the all-pass network [2]. The transfer function of the op-amp realization is given by

$$G_1 = \frac{A}{A+2}\,\frac{1-sCR}{1+sCR} \simeq \frac{1-sCR}{1+sCR} \tag{1}$$

while the transistor circuit is closely approximated by

$$G_2 = \frac{sCR-1}{sCR+1}. \tag{2}$$

In each case the amplitude of G is seen to be unity at all frequencies while the phase shift for the op-amp circuit is

$$\phi_1 = -2\tan^{-1}\omega CR \tag{3}$$

and for the transistor circuit is

$$\phi_2 = 2\tan^{-1}\frac{1}{\omega CR}. \tag{4}$$

Manuscript received August 1, 1977.

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