DoC IAC – Organization / PPP Working Group

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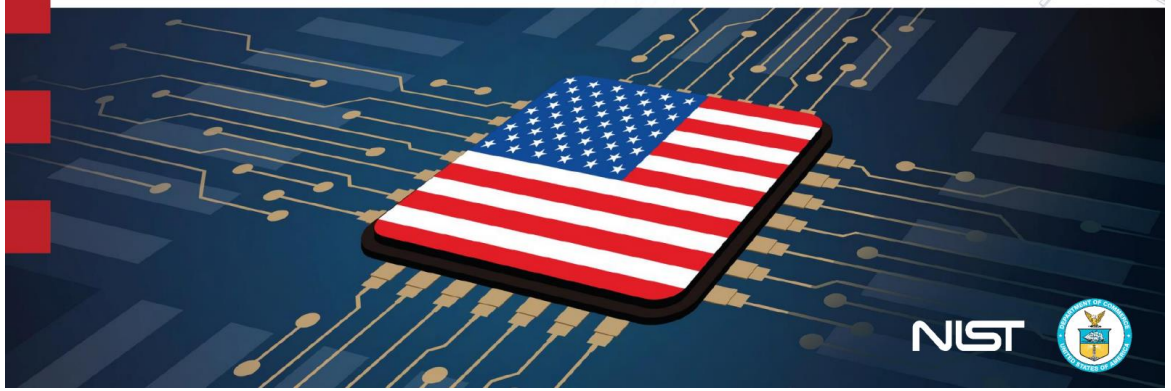
CHIPS for America Research and Development Program

Presented by Jason Boehm and Eric Lin

October 2022



Guiding Principles

1. Meet economic and national security needs
2. Ensure long-term leadership in the sector
3. Strengthen and expand regional clusters
4. Catalyze private sector investment
5. Generate benefits for a range of stakeholders and communities
6. Protect taxpayer dollars

R&D funding will spur:

- A domestic infrastructure for research and prototyping innovations
- R&D collaborations between academia and industry
- Workforce development and training

Research & Development

- To strengthen and advance U.S. leadership in R&D
- An integrated ecosystem that drives innovation
- In partnership with industry, academia, government, and allies
- Informed by the Industrial Advisory Committee

https://www.nist.gov/system/files/documents/2022/11/18/CHIPS%20for%20America%20Strategy%20Paper%20Briefing%20-%20RD%20.pdf

Organization / PPP Working Group

Bill Chappell
Microsoft

Scott DeBoer
Micron

Michael Fritze
Potomac Institute for Policy Studies

Deirdre Hanford
Synopsys

Ken Joyce
Brewer Science

Alex Oscilowski
TEL America

Mark Papermaster
AMD

Willy Shih
Harvard Business School

Anthony Yen
ASML Technology Center

Organization / PPP Working Group Charge

01

This working group will review and examine all the various funding sources for semiconductor R&D and map out the relationships between these entities to ensure spending efficiency and eliminate any overlaps.

02

In addition, this working group will review the essential functions and governance of the NSTC and NAPMP.

03

Finally, this committee will review PPP proposals for both R&D partnerships, the value proposition for industry participation in PPPs, as well as investment funds and support of start ups

At present, the Department is engaged in four high-priority tasks:

1. Evaluating potential gaps in research and engineering that could be filled by the NSTC. As part of the whole-of-government effort, the NSTC will complement the many excellent centers already established by industry, academia, allies, and other governmental agencies. The Department will create a preliminary landscape analysis with the benefit of recommendations developed by the CHIPS Industrial Advisory Committee. Ultimately, the NSTC itself will finalize the focus areas, but this early work will inform further decisions.
2. Evaluating and defining a structure and governance model that fulfills the CHIPS for America goals of promoting U.S. economic and national security and protecting taxpayer investments while ensuring technical excellence and leadership.
3. Creating a preliminary operating, business, and financial model that will serve as a road map for near-term investment informed by an understanding of what will be required for long-term sustainability.
4. Identifying a slate of candidates for the NSTC chief executive.

The Department will release a white paper in the first quarter of 2023 that will summarize the results of the landscape analysis, governance structure, and preliminary operating and financial model. At that time, the Department will issue guidance on when to expect requests for proposals.

https://www.nist.gov/system/files/documents/2022/11/18/CHIPS%20NSTC%20Update%20to%20the%20Community.pdf

Near Term Plan

- November & December 2022
  - Establish baseline knowledge within the team via industry and government briefs
  - Identify which questions our team needs to address in our working group, focusing on 2 of our 3 charges
  - Create a work plan for January

Briefs in November & December

Organization	Topic	Guest
NIST	CHIPS Overview and program mapping	Dr. Jason Boehm, Chief of Staff, NIST
Semiconductor Alliance	NSTC/NAPMP	Dr. Raj Jammy, CTO and Chief Technologist, MITRE-ENGENUITY
DoD OUSD Research and Engineering	DoD Microelectronics Commons	Dr. Dev Shenoy, DoD, PD Microelectronics, OUSD (R&E) Microelectronics Modernization
NIST	Interagency perspective on R&D programs	Dr. Ronald Jones, CHIPS R&D Interagency Coordinator, NIST
INTEL	NAPMP	Dr. Babak Sabi. SrVP and GM of Assembly/Test Development Dr. Tom Rucker, VP Technology and Development
Department of Commerce	NSTC Governance	Donna Dubinsky, Senior Counselor for CHIPS Implementation
IMEC	Best practices on PPP's and IMEC governance structure	Dr. Luc Van den hove, President and CEO, IMEC
American Semiconductor Innovation Coalition	NSTC / NAPMP	Dr. Mukesh Khare, Vice President Hybrid Cloud Dr. Douglas Grose, Chairman of NY Creates

Charge 1 and Charge 2 working teams

Charge 1

- *Review and examine all the various funding sources for semiconductor R&D and map out the relationships between these entities to ensure spending efficiency and eliminate any overlaps.*

- *Team Members*
  - Bill Chappell
  - Alex Oscilowski
  - Mark Papermaster
  - Willy Shih

Charge 2

- *Review the essential functions and governance of the NSTC and NAPMP*

- *Team Members*
  - Scott DeBoer
  - Mike Fritze
  - Ken Joyce
  - Tony Yen

Key Questions - Charge 1

- What is the ***mapping*** between the various funding sources? Are there ***overlaps, redundances or gaps***?
- How will various semiconductor R&D instruments ***work together*** across DoD, DoE, NSF, DoC?
- What ***metrics*** should be used to differentiate between the various funded USG efforts in Microelectronics? – TRL, Application, Industry segment, other?
- How can the department ensure that the ***competition of ideas*** brings forward the most robust and most sustainable strategies to foster long term competitive advantage for our country?
- How will ***coordination*** between these various R&D efforts take place? What org. is responsible for this?
- Which of the R&D instruments will ensure that the modern domestic manufacturing nodes that result from the ***manufacturing grants*** have a healthy design ecosystem, skilled user base, and a user demand from both the design and IP availability perspective?
- To which group (DoC NSTC/NAPMP or DoD Commons) would potential participants submit a ***proprietary*** concept?
- If research activity is focused on ***precompetitive*** work, how will we influence manufacturing options and ***industrial outcomes?***
- How will the DoC programs engage the ***Department of State*** elements of CHIPS?

01

This working group will review and examine all the various funding sources for semiconductor R&D and map out the relationships between these entities to ensure spending efficiency and eliminate any overlaps.

Key Questions - Charge 2

- What are ***successful outcomes*** for NSTC and NAPMP?
- What is the proposed ***governance structure*** for NSTC and NAPMP? Does the group concur?
- What is ***the role of the government*** in the governance and ***decision making process***, and who is the steward of the national interests above and beyond the industry interest?
- What will be the ***relationship between the CHIPS R&D office and NSTC***, and what steps will the CHIPS R&D office take to "incubate" the NSTC?
- How do we ensure ***agility*** in the implementation of NSTC and NAPMP?
- What mechanisms are required to ensure that NSTC, NAPMP, Manufacturing Institutes are ***sustainable*** beyond the initial funding?
- What ***alignment*** exists in the various inputs to DoC on NSTC/NAPMP including ***PCAST, ASIC and MITRE?***
- Does DoC agree with the concept of ***Coalitions of Excellence*** as a key element of NSTC?
- Who has the ***ultimate say*** in which projects are funded - CEO, USG, Industry Stakeholders.
- What should the ***funding*** profile look like ***over time***? (ie % USG and % industry over time)
- Will the scope of governance ensure that the proposed technologies a) ***adopt open standards based interfaces*** to assure an equal access ecosystem, and b) ***create a level competitive playing*** field avoiding a "lock in" to a single proprietary design or manufacturing approach?

02

In addition, this working group will review the essential functions and governance of the NSTC and NAPMP.

Key Questions – Charge 3

- How can the Department of Commerce stimulate ***the deployment of incremental resources from both industry and research institutions*** in public-private partnerships to attack the ***grand challenges*** associated with restoring America's leadership in semiconductor manufacturing?
- How can the Department of Commerce build a mechanism for implementing the CHIPS Act R&D funding that will be ***flexible and adaptable***, able to deploy resources to new approaches and opportunities as they come into view?
- What can we learn from ***prior PPP efforts***?
- What were the ***lessons and best practices*** from the existing models, including the Manufacturing USA centers, which proceed these investments?
- How can we encourage/motivate robust ***industry and VC investments***?
- We understand that Commerce expects that the "NSTC will attract collaborators and research partners from around the world, including from partners in allied countries, to participate in compelling opportunities to advance future technologies." What will be the ***eligibility criteria for non-US entities*** to participate? Will non-US participants be required to invest in US manufacturing and, if so, to what extent?

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Looking Ahead

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  - Establish baseline knowledge within the team via industry and government briefs
  - Identify which questions our team needs to address in our working group, focusing on 2 of our 3 charges
  - Create a work plan for January
- Q1 2023
  - Dive into the questions
  - Converge on charge 1 and 2 recommendations to intercept DoC's Q123 white paper
  - Continue to engage stakeholders via briefs
  - Dive into Charge 3 on PPP structures

Thank You