Industrial Advisory Committee (IAC)
Meeting Summary
National Institute of Standards and Technology (NIST)
Gaithersburg, Maryland
(Virtual)
November 8, 2023

Advisory Committee Members:

Michael Splinter, Chair	MRS Business and Technology Advisors
Susan Feindt, Vice-Chair	Analog Devices, Inc.
Daniel Armbrust	Silicon Catalyst
Michael Fritze	Potomac Institute for Policy
Charles Gray	Ford Motor Company
Deirdre Hanford	Synopsys
Kenneth Joyce	Brewer Science
Ann Kelleher	Intel Corporation
Meredith LaBeau	Calumet Electronics
Tsu-Jae King Liu	University of California, Berkeley
Willy Shih	Harvard Business School
Brandon Tucker	Washtenaw Community College
Philip Wong	Stanford University
Anthony Yen	ASML

NIST Leadership:

Laurie Locascio	Under Secretary of Commerce for Standards and Technology Director, NIST
Lora Weiss	CHIPS R&D Director
Eric Lin	CHIPS R&D Deputy Director

I. Call to Order and Opening Remarks

Mr. Benjamin Davis, serving as the Designated Federal Officer (DFO) for the IAC, called the meeting to order and took roll call of the committee members.

Mr. Davis announced the DOC and NIST are not bound to IAC recommendations, that a recording of the meeting and all presentations will be posted to CHIPS.gov following the meeting, and that a consensus of the body is defined as two-thirds of the committee.

Mr. Davis took roll call with the following results:
- Daniel Armbrust (Silicon Catalyst): *Did Not Respond*
- Susan Feindt (Vice Chair, Analog Devices, Inc.): Present
- Michael Fritze (Potomac Institute for Policy): Present
- Charles Gray (Ford Motor Company): Present
- Deirdre Hanford (Synopsys): Present
- Kenneth Joyce (Brewer Science): Present
- Ann Kelleher (Intel Corporation): Present
- Meredith LaBeau (Calumet Electronics): Present
- Tsu-Jae King Liu (University of California, Berkeley): Present
- Omkaram Nalamasu (Applied Materials): *Not in Attendance*
- Willy Shih (Harvard Business School): Present
- Michael Splinter (Chair, MRS Business and Technology Advisors): Present
- Brandon Tucker (Washtenaw Community College): Present
- Philip Wong (Stanford University): Present
- Anthony Yen (ASML): Present

II. IAC Welcome and Opening Remarks

Mr. Michael Splinter welcomed committee members and guests. Mr. Splinter shared that the IAC was announced and began its formation 13 months ago. Mr. Splinter shared that the IAC has reviewed and approved numerous R&D, organization, and workforce-development recommendations. Mr. Splinter said that today, the committee will report on works in progress.

Mr. Splinter congratulated Congress on moving forward with hiring in support of the CHIPS program, including hiring Lora Weiss, who is heading the CHIPS program and is here today. Mr. Splinter said the IAC expects a lot more progress in the months ahead.

Mr. Splinter previewed that the audience would hear recommendations in three requested areas:
- The focuses of the Metrology Program at NIST.
- The structure of the National Semiconductor Technology Center (NSTC) investment fund.
- An opinion on where CHIPS can have a positive effect on the future of industry standards.

Mr. Splinter thanked all IAC members who have contributed and gave a specific thanks to the following IAC members whose service ended at the end of their one-year terms:

- William Chappell
- James Ang
- Carol Handwerker
- Alexander Oscilowski
- Susie Armstrong

Mr. Splinter shared that Congress will announce new members—which the IAC expects to happen any day now—as soon as they are completely vetted. Mr. Splinter then gave the floor to Ms. Susan Feindt.

Ms. Feindt welcomed everyone and said a lot of progress has been made since June. Ms. Feindt said subgroups have been working hard since the last meeting and each team enlisted additional subject matter experts (SMEs) for learning about and understanding the issues more deeply. Ms. Feindt conveyed that this was followed by more discussion, which brought forth the recommendations that will be presented today.

Ms. Feindt stated that the goal of the meeting is to have alignment on as many of the recommendations as possible, thanked the Department of Commerce for its careful deliberation of the recommendations, and thanked each of the departing IAC members.

III. NIST Welcome Remarks

Dr. Laurie Locascio thanked Mr. Splinter and Ms. Feindt for their leadership, thanked everyone for joining the fourth meeting and for their sustained interest, thanked members of the committee, and thanked the NIST and IAC members who have recently completed terms.

Dr. Locascio shared that the work of the committee has helped to inform milestones, from the vision and strategy to the National Semiconductor Technology Center to the recent Workforce Development Progress Report. Dr. Locascio shared that the Workforce Development Progress Report outlines workforce strategies across CHIPS for America, including one or more potential Workforce Centers of Excellence based at the NSTC. Dr. Locascio shared that the Workforce Centers of Excellence, like NIST, could serve as conveners for stakeholders of many communities (e.g., industry, research, government, labor, and academic communities), developing the training programs that are critical to the semiconductor industry; piloting new programs, including a purchase for engaging all types of communities; and measuring program success to scale up the best of these programs. Dr. Locascio shared that Workforce Centers of Excellence will benefit the entire industry.

Dr. Locascio shared that CHIPS for America will be a continuous exchange between manufacturing and R&D and that NIST is very excited about all aspects of what it plans to do over the coming year.

On the NSTC, Dr. Locascio shared that last month, an independent selection committee announced an inaugural board for the entity that NIST anticipates will operate the NSTC. The board is as follows:
- Robin Abrams

- Craig Barrett
- Reggie Brothers
- Nick Donofrio
- Donna Dubinsky
- Erica Fuchs
- Jim Plummer

Dr. Locascio shared that the board includes experts from industry, academia, and the national security community and that these leaders reflect the requisite qualities to ensure the success of this new entity.

Dr. Locascio reported NIST's progress toward establishing the NSTC as a public-private consortium as stated in the CHIPS Act statute. Dr. Locascio said that on November 9, 2023, NIST will announce that the DOC has reached an initial agreement with a new non-profit—SemiUS—that was established by the board of trustees. Dr. Locascio shared that SemiUS is expected to be the operator of the NSTC once the consortium is formally established.

Dr. Locascio stated that the first planned activities of SemiUS include:
- Hiring a Chief Executive Officer
- Hiring an executive team
- Establishing a membership structure for the consortium
- Developing a timeline for the sequencing of program activities, which are expected to begin in 2024

Dr. Locascio said to look for a press release announcing the formation of SemiUS and the launch of its website at SemiUS.org on Tuesday, November 9, 2023.

IV. CHIPS R&D Update

Dr. Lora Weiss thanked the members of current and past IACs. Dr. Weiss shared that since the last meeting, CHIPS R&D had hired the following new members:
- Eric Lin, Deputy Director
- Richard-Duane Chambers, Associate Director for Integration and Policy
- Marla Dowell, Director of CHIPS R&D Metrology
- Jay Lewis, Director of NSTC
- Subramanian Iyer, Director of National Advanced Packaging Manufacturing Program (NAPMP)

Dr. Weiss shared that CHIPS R&D is in the midst of a hiring sprint with multiple postings—including the CHIPS Metrology Program's recently posted first set of post-doctoral associate positions—on CHIPS.gov weekly.

Dr. Weiss conveyed that since the signing of the CHIPS for America Act into law, the CHIPS for America program has continued to hit milestones. Dr. Weiss shared that three Metrology programs have been announced and R&D programs are staffing up.

Dr. Weiss emphasized that the mission of CHIPS R&D is to "accelerate the development and commercial deployment of foundational semiconductor technologies by establishing, connecting, and providing access to domestic tools, resources, workforce, and facilities." Dr. Weiss reiterated that this mission is critical.

Dr. Weiss stated that the goals for CHIPS R&D are:
- Technology leadership: Establishing the capacity to invent, develop, prototype, and deploy the foundational semiconductor technologies of the future here in America.
- Accelerate ideas to market: Facilitating the commercial scalability of the best ideas as quickly as possible.
- Contribute to a robust semiconductor workforce: Contributing enough inventors, designers, researchers, developers, engineers, technicians, and staff to meet the needs of the government and commercial sectors.

Dr. Weiss reviewed the CHIPS R&D programs' integration. Dr. Weiss described metrology as measurement science and stated that it enables innovation in all CHIPS R&D programs and across the semiconductor ecosystem. Dr. Weiss stated that metrology is needed at all stages of semiconductor technology development and is especially critical as semiconductor dimensions get smaller. Dr. Weiss stated that research and quality measurements are needed to measure, monitor, predict, and ensure quality in manufacturing.

Dr. Weiss described the path through which metrology results advance: CHIPS R&D, NSTC, National Advanced Packaging Manufacturing Program (NAPMP), Manufacturing USA, and commercial manufacturing facilities.

Dr. Weiss stated that much progress has been made in just one year and that she was delighted to hear the announcement of SemiUS and the board of trustees. Dr. Weiss stated that the vision and strategy for packaging will soon be published, and the director of the CHIPS Manufacturing USA program will soon be announced.

Dr. Weiss shared that the Metrology Program has initiated projects and that NIST researchers have begun working on challenges two and four of the seven grand CHIPS R&D challenges (all of which are listed below):
1. Metrology for materials purity, properties, and provenance
2. Advanced metrology for future microelectronics manufacturing
3. Enabling metrology for integrating components in advanced packaging
4. Modeling and simulating semiconductor materials, designs, and components
5. Modeling and simulating semiconductor manufacturing processes
6. Standardizing new materials, processes, and equipment for microelectronics
7. Metrology to enhance security

Dr. Weiss shared that in September, NIST conducted a Standards Summit—which was attended by more than 600 in-person and virtual attendees and seven international standards bodies—to identify the top standard priorities for the semiconductor community. Dr. Weiss shared that a report from this summit will be published soon and that two standards workshops are coming up,

both of which can be registered for on CHIPS.gov.

Dr. Weiss shared that NIST invites attendees of this IAC meeting to read the workforce report on CHIPS.gov.

Dr. Weiss also shared that the Workforce Centers of Excellence have, as part of their goals, to help clearly align semiconductor education—including the tools, mentors, institutions, and programs inherent therein—so trainees receive the training desired by employers.

V. <u>CHIPS R&D Response to the IAC Recommendations</u>

Dr. Eric Lin thanked the IAC and those who are departing.

Dr. Lin shared that his task is to provide direct responses to the specific recommendations that are made by the IAC. Dr. Lin stated that there are more than 40 recommendations at present—with plenty more to come this afternoon—and that CHIPS R&D will be reviewing the recommendations made in February of 2023 to provide NIST's direct response to the IAC's recommendations. Dr. Lin shared that all recommendations will be addressed in due time.

Dr. Lin shared the following notes on CHIPS R&D's responses:
- Responses are a snapshot in time.
- CHIPS R&D recognizes it will take time to implement this very ambitious program fully, so this will be an ongoing conversation into the future.
- Reflecting on the progress to date was a very valuable exercise.
- Much of the value is in the thoughtfulness with which the IAC framed the challenging recommendations.

Dr. Lin shared that the three working groups are as follows:
- R&D Gaps: Chair: Mr. **Dan Armbrust.** The purpose of this working group is to look at the long-term research and development needs of the semiconductor industry. The working group will then need to understand what is being funded by other initiatives and where the gaps are. Then, the working group will suggest priorities to the IAC, including the focus areas for CHIPS funding and the NSTC that provide the best opportunities to sustain US leadership in semiconductor innovation.
- Organization and Public-Private Partnership (PPP): Chair: Ms. **Deirdre Hanford.** This working group will review and examine all the various funding sources for semiconductor R&D and map out the relationships between these entities to ensure spending efficiency and eliminate any overlaps. In addition, this working group will review the essential functions of the NSTC. Finally, this working group will review PPP proposals for R&D partnerships, the value proposition for industry participation in PPPs, and investment.
- Workforce Development: Chair: Dr. **Tsu-Jae King Liu.** This working group will look at the workforce needs across the industry, from high-level R&D personnel to factory workers. It should review programs that will increase the interest in and availability of the necessary skills for the United States to lead the world in semiconductor R&D and

manufacturing.

Dr. Lin, in the CHIPS R&D Response to the IAC Recommendations presentation, shared the recommendations for CHIPS R&D. Following each recommendation, Dr. Lin shared CHIPS R&D's responses, which are as follows:

- R&D Gaps Working Group:
  - o Response to Recommendation 1: CHIPS R&D agrees with the need to lower the barrier to entry and wants to do this to increase the chance of success for ideas in the industry. NIST expects to work with SemiUS to establish a process to identify specific capabilities that advance these goals, including understanding barriers that confront NSTC consortium members.
  - o Response to Recommendation 2: CHIPS R&D agrees with using grand challenges to inspire innovation. NIST expects SemiUS—in partnership with NSTC members and the CHIPS R&D Office—to establish a process for identifying and selecting a specific set of grand challenges in the very near future. NIST notes Ms. Weiss's afore-presented seven grand challenges.
  - o Response to Recommendation 3: CHIPS R&D agrees that CHIPS R&D must provide a clear value proposition to participants, including the benefits to industry and the benefits that merit participants' support for and contribution to the R&D enterprise. Currently, the frameworks for those metrics are under development.
- Organization and Public-Private Partnership Working Group:
  - o Response to Recommendation 1–1: CHIPS R&D agrees with the principles in this recommendation. The NSTC will be established as a public-private consortium as required by statute. SemiUS will operate the NSTC once it is formally established.
  - o Response to Recommendation 1–2: CHIPS R&D agrees with the principles in this recommendation. SemiUS's board of trustees has a fiduciary responsibility to the NSTC.
  - o Response to Recommendation 2–1: CHIPS R&D agrees with the principles in this recommendation. CHIPS R&D anticipates that SemiUS is engaged in recruiting a leader for the NSTC.
  - o Response to Recommendation 4–1: CHIPS R&D agrees with the principles in this recommendation and believes that SemiUS will fulfill this recommendation.
  - o Response to Recommendation 4–2: CHIPS R&D agrees that the long-term financial model of the NSTC will need to incorporate various forms of funding to be sustainable and should be flexible to ensure investments are made to facilitate the broadest participation of organizations of all sizes and needs.
  - o Response to Recommendation 4–3: CHIPS R&D agrees that there should be a variety of approaches to physical and digital enablement, including facilitating the use of volume production sources for members of all types.
  - o Response to Recommendation 4–4: CHIPS R&D agrees with these core concepts. CHIPS R&D uses a slightly different term (i.e., technical centers), but the ideas and framing are largely shared.
  - o Response to Recommendation 4–5: CHIPS R&D agrees with the importance of leveraging existing resources, growing the ecosystem, and connecting resources wherever possible.

- o Response to Recommendation 5b–1: CHIPS R&D agrees with the principles in this recommendation. SemiUS will fulfill this recommendation.
  - o Response to Recommendation 5b–2: CHIPS R&D agrees with this recommendation and expects that competition will be the best avenue to drive innovation.
  - o Response to Recommendation 5b–3: CHIPS R&D agrees with the principles in this recommendation, subject to CHIPS R&D and SemiUS guidance.
- Workforce Working Group:
  - o Response to Recommendation 1: CHIPS R&D agrees with this recommendation. CHIPS for America fulfills this recommendation and will leverage the manufacturing incentive requirements to develop workforce strategies, coordinate workforce initiatives, process R&D efforts, and collaborate with federal, state, and local partners to develop and extend training initiatives. CHIPS for America will also continue to work with the National Science Foundation (NSF) to generate talent across the industry.
  - o Response to Recommendation 2: CHIPS R&D agrees with this recommendation. Both the CHIPS R&D Office and the manufacturing incentives program will establish metrics for success for new and existing programs to guide further investment and ensure the specific functions in the recommendation are under consideration for the NSTC Workforce Centers of Excellence.
  - o Response to Recommendation 3: CHIPS R&D agrees with these goals. The department—through the NSTC Workforce Centers of Excellence—is considering offering low-cost access to shared, curated, physical and digital infrastructure, including existing curricular content. These centers of excellence could also offer a centralized digital repository of industry and worker resources. These centers could also provide physical locations for training with equipment and faculty that leverage new technological advances. Specifics will likely be decided on a program-by-program basis. CHIPS R&D aims to add public and private capital and resources for workforce development.
  - o Response to Recommendation 3–1: CHIPS R&D agrees with these goals and is taking these recommendations into account as programs develop.
  - o Response to Recommendation 3–2: CHIPS R&D is taking these recommendations into account as programs develop.
  - o Response to Recommendation 4: CHIPS R&D agrees with the value of an awareness campaign. The workforce progress report outlines a proposal focused specifically on increasing awareness of semiconductor industry opportunities and notes the IAC's recommendation to establish an awareness campaign in K–12 science, technology, engineering, and mathematics (STEM) advocacy efforts.
  - o Response to Recommendation 4–1: CHIPS R&D is taking these recommendations into account as programs develop.
  - o Response to Recommendation 4–2: CHIPS R&D agrees with this recommendation and with the value of experiential education.
  - o Response to Recommendation 4–3: CHIPS R&D agrees with this recommendation is taking these recommendations into account as programs develop.

The meeting broke for lunch and reconvened at 1:00 p.m. ET.

VI. R&D Gaps Working Group Presentation (Metrology & Standards)

Mr. Dan Armbrust shared that the R&D Gaps Working Group has been meeting weekly over the past year; Mr. Armbrust is grateful for the contributions of the working group's members. Mr. Armbrust acknowledged and thanked Mr. Ben Davis and Dr. David LaVan.

Mr. Armbrust said this presentation will include a discussion of metrology and standards, followed by IAC deliberations and voting. Mr. Armbrust gave the floor to Dr. Todd Younkin. Dr. Younkin said he would discuss the Metrology Program and areas the working group believes are important to focus on.

Dr. Younkin said the big difference this time around is that there is a Metrology Program, there is leadership with Dr. Dowell and her team, and the Metrology Program has issued two public materials the team could use to understand the vision and plans for the Metrology Program and how they map to the CHIPS R&D Working Group.

In the research, Dr. Younkin and the team discovered seven grand metrology challenges:
1. Metrology for materials purity, properties, and provenance
2. Advanced metrology for future microelectronics manufacturing
3. Enabling metrology for integrating components in advanced packaging
4. Modeling and simulating semiconductor materials, designs, and components
5. Modeling and simulating semiconductor manufacturing processes
6. Standardizing new materials, processes, and equipment for microelectronics
7. Metrology to enhance security

Dr. Younkin shared that a competition or stage-gate methodology is paramount to prioritizing R&D efforts and that the Metrology Program is on a directionally accurate path and has started to make initial investments.

Dr. Younkin shared that the goal would become more difficult over time, drawing attention to the fact that:
- The industry-led roadmap emphasized manufacturing, process development, and expert testimony, the latter of which provided a large, diverse perspective. Metrology requires a focus on all of these.
- Hybrid metrology offers the promise of both resolution and greater throughput through the marriage of complementary techniques; this includes the combination of out-of-line and in-line techniques.
- The CHIPS R&D Working Group can close the cultural and knowledge gaps between the fab, lab, and equipment providers.

Dr. Younkin shared that in advanced packaging, failure is not an option, as you are taking known good die (KGD) and then building failed system(s): a top priority should be KGD combined with multi-die validation for heterogeneous integration (HI) that competes economically with monolithic die. The end-use-application-based binning of chiplets will become increasingly

important for enabling die matching and maximizing yield in an HI package.

Dr. Younkin presented that CHIPS R&D investments and industrial partners can provide precompetitive and prototyping samples that accelerate the community by allowing for the evaluation of a technology, the gathering of nonproprietary data, debugging equipment, etc. Dr. Younkin said that NIST has a role to play as a trusted hub supplier for data and applied data analytics by establishing standards and metrology, such as blockchain, that enable information exchange yet provide security/provenance throughout the manufacturing flow.

Dr. Younkin described the Metrology Program plan and its engagement in three categories: forever off-line characterization, individual characterization/off-line metrology, and standalone. Dr. Younkin then described what the working group believes to be the three overarching drivers of communities of practice that serve CHIPS R&D: 3D IC failure analysis; 3DHI test, addressing KGD; and photonics/optical integration.

At the conclusion of his presentation, Dr. Younkin submitted the following 10 recommendations on behalf of the Metrology Sub-Group:
1. Accelerate GC3 (advanced packaging), with a high-level emphasis on KGD for chiplets
2. Place a higher priority on failure analysis (GCs 1, 2, 4, and 5) and photonics (GCs 2 and 3)
3. Create standardized contractual arrangements for industry-led engagement (Memoranda of Understanding) and investments (Cooperative Research and Development Agreements), including start-up funds that amplify the program's plans and create momentum
4. CHIPS R&D investments and industrial partners should provide precompetitive and prototyping samples that accelerate the metrology community, allowing for the evaluation of technology, the gathering of nonproprietary data, benchmarking, debugging or matching equipment, and developing protocols
5. Within the Metrology Program and CHIPS R&D investments, while NIST's technical focus should be on both out-of-line and in-line efforts (industry-informed), in-line efforts should be industry-led (NIST-supported)
6. Become a trusted hub supplier for data and applied data analytics by establishing standards and metrology, such as blockchain, allowing for exchange with security/provenance throughout the manufacturing flow
7. For events, tie updates and engagement plans to NSTC/NAPMP annual or semi-annual reviews and these industrially relevant conferences: International Electron Devices Meeting (wafer), Electronic Components and Technology Conference (packaging), Optical Fiber Communication Conference (photonics), and International Conference on Frontiers of Characterization and Metrology for Nanoelectronics (metrology)
8. Priority should be on enabling the R&D programs of the NSTC and NAPMP, serving in a consultive role as technology centers are established. Priority should also be on reviewing metrology requirements, leveraging existing and new domestic capabilities coming online, or seeking synergy in the development of new capabilities
9. NIST and the Metrology Program can serve as a trusted hub supplier for standards, data format, secure data exchange, and applied data analytics for new, smarter models
10. CHIPS R&D investments should capture the intellectual property (IP) rights of metrology

inventions by the Metrology Program, NSTC, NAPMP, etc. such that IP can be licensed to industrial partners in the metrology community to accelerate technologies' impact

Dr. Mukesh Khare, on behalf of the Standards Sub-Group, shared the charter of the Standards Sub-Group to provide feedback and recommendations for opportunities and strategies to support the private sector-led semiconductor and microelectronics standards ecosystem in becoming even smarter, faster, and more inclusive and agile in enabling innovation.

Dr. Khare reviewed potential grand challenges for the NSTC that were shared at an earlier IAC meeting:
1. Establish easily accessible prototyping capabilities in multiple facilities and enact the ability to try out CMOS+X rapidly at a scale relevant to industry
2. Create a semiverse digital twin
3. Establish a chiplets ecosystem and 3D heterogeneous integration platform for chiplet innovation and advanced packaging
4. Build an accessible platform for chip design and enable new electronic design automation (EDA) tools that treat 3D (monolithic or stacked) as an intrinsic assumption
5. Create a nurturing ecosystem for promising start-ups

Dr. Khare said the working focused on opportunities in the long-term needs for advanced packaging:
- Review the advanced packaging needs of the United States and use ecosystem gaps to suggest focus area priorities
- Outline the best opportunities to develop and sustain US leadership in semiconductor advanced packaging
- Suggest mechanisms for ecosystem development

Dr. Khare shared a graphic describing how Moore's Law of economics will be driven by three axes: microchips, advanced packaging, and architectures.

Dr. Khare then shared the following list of high-level questions within the scope of chiplet-related standards:
- How can CHIPS R&D/NSTC incentivize the formation of alliances to support the mission to grow a competitive and open chiplet ecosystem?
- How can CHIPS R&D/NSTC ensure these alliances are driving a common set of relevant standards for the ecosystem?
- How can CHIPS R&D/NSTC ensure technological advancement and standardization is well thought out, sustainable, and able to benefit all alliance members?
- What could be the overarching body to harmonize various open chiplet, 2.5D, and 3D standards?
- What are your thoughts on exploring the acceleration of standards processes?
- What could be some approaches to linking community standards goals to relevant pre-standards research needs?
- What could be some standards developed/implemented for 2.5D, 3D, and chiplet integration in packaging and manufacturing?

Dr. Khare shared the following key outcomes of the first Standards Workshop, which was centered on technology, infrastructure, security, and people:

- **How can CHIPS R&D/NSTC incentivize the formation of alliances to support the mission to grow a competitive and open chiplet ecosystem?**
  - o CHIPS R&D/NSTC can incentivize this formation by facilitating communication between industry, government, and standards development working groups; supporting face-to-face meetings; advertising the availability of standards once they are ready to be used; encouraging industry leaders and other standards to reference new and old content; and ensuring representation of start-ups in standards groups.
- **How can CHIPS R&D/NSTC ensure these alliances are driving a common set of relevant standards for the ecosystem?**
  - o CHIPS R&D/NSTC can ensure these alliances are driving a common set of relevant standards by influencing standards development through inviting select global organizations to participate in NIST-led workshops with all relevant stakeholders and encouraging conformance to standards in government-funded projects.
- **How can CHIPS R&D/NSTC ensure technological advancement and standardization is well thought out, sustainable, and able to benefit all alliance members?**
  - o CHIPS R&D/NSTC can ensure this outcome by helping sustainability through R&D in key areas such as advanced packaging options, testing, security, cooling, power delivery, and optics; ensuring broad market potential and technology trends are comprehended in the development of new standards; creating a knowledge environment for easy access to existing standards; and ensuring the needs of analog/RF and the automotive area are included during the formation of standards.
- **What could be the overarching body to harmonize various open chiplet, 2.5D, and 3D standards?**
  - o The CHIPS R&D Office can ensure this outcome by creating an alliance of alliances and consortia; leveraging the convening power, resources, and technical expertise within the alliance of alliances and consortia; and including (or establishing as the overarching body) JEDEC, the Institute of Electrical and Electronics Engineers, the Open Compute Project, or Universal Chiplet Interconnect Express.
- **What are your thoughts on exploring the acceleration of standards processes through standards incubators and accelerators?**
  - o CHIPS R&D's thoughts are to promote precompetitive prototyping efforts, allowing companies to collaborate on chiplet prototypes and accelerating the development process; provide capabilities for testing and validating prototypes including developing new test standards, especially for advanced 2.5D and 3D packaging (e.g., fine pitch probing); enable standards-aligned reference designs to facilitate the introduction of new chiplets; implement IP control and data sharing guidelines; and promote the idea of introducing standards education for workforce development.
- **What could be some approaches to linking community standards goals to relevant**

pre-standards research needs? (What type of research agenda should be driven in support of standard development?)

- CHIPS R&D's approaches are to invite key stakeholders to regular workshops to exchange ideas; note that research should not be limited to standards and should enable a roadmap view within the standard; and note that the NSTC should fund precompetitive demonstrators to validate standards in support of the chiplets ecosystem.

- **What could be some standards developed/implemented for 2.5D, 3D, and chiplet integration in factories for packaging?**
  - CHIPS R&D believe some standards could drive toward secure data exchange; address the lack of manufacturing tests and standardized interfaces in the analog/RF area; and enhance interoperability and reduce supply chain complexity (e.g., those used in the automotive industry) by standardizing highly utilized semiconductor components. Test standards are key: electrical DFT combined with wafer metrology and full inspection; encourage open sharing of the interface protocol; share electrical models for driver and receiver circuits (output stage); I/O footprint pads; ensure electrostatic discharge requirements; and, most importantly, standardize external I/O (lanes/mm).

Dr. Khare shared the following five recommendations that resulted from the Standards Working Group:

1. Use CHIPS R&D's convening power to bring chiplet-related standards bodies (industry-led consortia and associations) together to create an alliance of alliances
2. Accelerate standards processes by enabling infrastructure and data access that allows entities to collaborate on chiplet prototypes
3. Ensure broad market potential and technology trends are comprehended in the development of new standards
4. Allocate funding from CHIPS R&D programs to incentivize the development of standards that foster an open chiplet ecosystem
5. Promote the idea of introducing standards education in semiconductor workforce programs

Questions and Remarks:

Q. Willy Shih: Does "bringing together alliances that are already creating some of these standards and trying to make them broader" mean picking from what others are already doing and trying to make it more global, or do you anticipate setting new standards? If setting new standards, how do you anticipate creating the demand for these new standards in competition with some of the other approaches we are seeing?

A. Mukesh Khare: The recommendation is not to create any new standards. There is already extremely good work going on in various industry-led alliances and the proposal is to bring them together; that's all.

Q. WillyShih: What happens when you have IP that reads out of standards? We see this in the telecom space. Have you thought through some of the questions around that as well?

A. Mukesh Khare: No. That was not the scope of our activity.

General Comment
Anthony Yen: 3D IC is still relatively new technology, but it is so important going forward for the United States to lead this area in the future (metrology as well as standards technologies). Mr. Yen is for all the recommendations.

Q. Deirdre Hanford: Question on Metrology Program. On recommendation number 10, are you talking about metrology inventions, or are you sweeping all inventions and making an IP licensing recommendation?
A. Todd Younkin: The focus here was on the Metrology Program and the IP associated with those investments.
Q. Deirdre Hanford: Request to change the wording of metrology recommendation number 10 to "Capture the IP rights of metrology inventions . . ."
A. Todd Younkin: Accepted this recommendation.

Q. Deirdre Hanford: Requested clarification on the subject of recommendation number eight.
A. Todd Younkin: The Metrology Program that sits inside NIST is the subject of this recommendation as well as all others. All of the recommendations made were pertaining to the CHIPS Metrology program.

Q. Michael Fritze: Were security standards acting as a demand driver in one of the conversations?
A. Mukesh Khare: Yes. This was a part of our conversation.

Q. Tsu-Jae King Liu: With regard to recommendation number two (contrasting it with recommendation number four), is recommendation number two going to require funding (like four)? If so, from where will this funding be derived?
A. Mukesh Khare: Recommendation number two should say "enable" rather than "create." There would have to be some funding allocated for standards-related activity. Dr. Khare will clarify that in the recommendation.

Q. Deirdre Hanford: For the standards recommendations, who do you see leading these efforts?
A. Mukesh Khare: A standards team, which is eventually under the broader umbrella of the NSTC, should be leading this.

Q. Deirdre Hanford: How have you thought about bringing some of these standards together?
A. Mukesh Khare: CHIPS R&D has the convening power, which was already demonstrated in the first workshop where most of these entities came together. We will be bringing them together in this way.

VII. Consensus Period

Ben Davis called the IAC to consensus vote on the metrology and standards recommendations.

Metrology Recommendations Consensus Vote:

Recommendation 1: 0 Opposed
Recommendation 2: 0 Opposed
Recommendation 3: 0 Opposed
Recommendation 4: 0 Opposed
Recommendation 5: 0 Opposed
Recommendation 6: 0 Opposed
Recommendation 7: 0 Opposed
Recommendation 8: 0 Opposed
Recommendation 9: 0 Opposed
Recommendation 10: 1 Opposed [Deirdre Hanford]

Clarifying Question on Recommendation 10 during Consensus Period
Q. Deirdre Hanford: If there is a metrology start-up that is funded through one of these programs, and they come up with a great idea, are we saying that idea is now licensed to all members of the community?
A. Todd Younkin: The Metrology Program would have, within its arsenal, the ability to serve that start-up company first and look for ways to amplify the ambitions of that organization or corporation.

Vote Result:
All recommendations were passed.

Standards Recommendations Consensus Vote:
Recommendation 1: 0 Opposed
Recommendation 2: 0 Opposed
- This recommendation was revised to "Accelerate standards processes by enabling infrastructure and data access that allows entities to collaborate on chiplet prototypes," during this consensus.
Recommendation 3: 0 Opposed
Recommendation 4: 0 Opposed
Recommendation 5: 0 Opposed

Vote Result:
All recommendations were passed.

VIII. **Organization and Public-Private Partnership Working Group Presentation**

Mrs. Deirdre Hanford shared that the working group asked itself three questions:
- Is there a problem with venture investing in the semiconductor industry?
- What is the nature of the problem?
- Is there anything we can do to help address that problem?

Mrs. Hanford shared that the working group's initial charge was to:
- Provide recommendations for how the investment fund for the NSTC could be best structured to meet the goals of the program and the statutory charter; and

- Recommendations could include input on the scale of the program, goals, focus areas, and how best to partner with the private sector.

Mrs. Hanford thanked the working group members (all of whom were displayed in her presentation).

Mrs. Hanford shared the details of 17 Innovation Fund meetings and briefs, which spanned the subjects of venture capitalism, government investing, industry, and working professional conversations.

Mrs. Hanford shared the names of companies and individuals who presented to the PPP Working Group. (These individuals can be found on slide six of the presentation.)

Mrs. Hanford examined semiconductor investments from 1987 through the end of 2022. The percentage of total investments revealed a downward trend. Mrs. Hanford stated the potential reasons for this are the large upfront and ongoing capital investment requirement, time to liquidity being long, and payout returns not being as substantial as other markets.

Mrs. Hanford described the Innovation Funnel in three stages: technology risk, product market-fit risk, and scaling risk. Ms. Hanford shared that the goal of the Organization and Public-Private Partnership Working Group was to level the playing field and retire risks so disruptive and technically underrepresented areas look more attractive to profit-seeking venture capitalists in later stages.

Ms. Hanford shared that the NSTC Innovation Fund:
- Will be **uniquely different** in that it will support national and economic security interests.
- Should be "**tech forward**" to focus on disruption beyond what the market would pursue.
- Can **guide the investment community** to areas it wouldn't be comfortable investing in.
- Will allow **high-risk tolerance** for failure commensurate with taking outsized risks. Lower returns on investment are therefore expected.
- Will **leverage NSTC expertise** and technical insight. The fund should wait to be established until after the NSTC function is operational.

Ms. Hanford introduced the following Organization and Public-Private Partnership Working Group recommendations to the IAC [along with their associated innovation fund principle(s)]:
9-1. Adopt a vision for a different kind of fund *[Uniquely Different]*
9-2. Leverage naming of fund to set tone and expectations *[Uniquely Different]*
9-3. Make the Innovation Fund segmented, not monolithic *[Uniquely Different]*
9-4. Include non-cash vehicles as a currency for investments *[Uniquely Different]*
9-5. Target underrepresented technical areas and ecosystems *[Tech Forward and High Risk Tolerance]*
9-6. Avoid barriers to leveraging the Innovation Fund *[High Risk Tolerance]*
9-7. Develop and maintain ability to judge technical merit *[Tech Forward and Leverage NSTC Expertise]*
9-8. Exploit synergies with NSTC wrap-around services *[Guide the Investment*

Community and Leverage NSTC Expertise]

     9-9. Domicile the Innovation Fund within NSTC or as an affiliate *[Guide the Investment Community and Leverage NSTC Expertise]*

     9-10. Stage start-up of the Innovation Fund *[Leverage NSTC Expertise]*

     9-11. Structure success metrics to reflect long-term goals *[Tech Forward]*

Questions and Remarks:

Q. Dan Armbrust: Maybe the use of a modified Small Business Innovation Research program could go a long way to addressing some of the pent-up expressions of interest from start-ups. It could make a more immediate impact, and the modifications would be aligned to some of the start-ups. That would really go a long way to addressing some of the expressed interest.

A. Deirdre Hanford: Thank you.

A. [Michael Fritze: Our suggestion is that the fund be focused—that it doesn't go into the general fund, but that it is focused on the goals of the NSTC.

Q. Rajarao Jammy: When you said the fund is not an evergreen fund, do you mean that in totality or are you expecting that some of the funds will go back into the fund to keep the fund going in addition to support you expect to receive down the road?

A. Deirdre Hanford: If we did have returns, the windfalls should go back into the fund. If they are modest returns, then perhaps they would offset some of the costs, but NSTC leadership will have that work ahead of them. The primary challenge is that we don't anticipate the dollars will be sufficient to keep the fund going forward.

Q. Michael Splinter: So, Deirdre, you are implying that you are expecting further tranches?

A. Deirdre Hanford: If NSTC leaders felt this was worthwhile, then the NSTC leaders (or, perhaps, member companies) would decide whether or not to allocate further dollars.

Q. Ann Kelleher: Did you consider picking a sample of very gnarly problems with the industry and actually dedicating something from the venture fund to those? And having a method by which they could be dealt with and addressed?

A. Deirdre Hanford: We didn't get to that level of specificity. I would be curious as to whether other members of our working group had comments or thoughts on that.

Q. Deirdre Hanford: Do you think the technical advisory boards could be charged with considering recommendations for where to consider investing?

A. Ann Kelleher: I think it is. The question is, "How do we and the ventures as we go forward have enough patience and have enough foresight to stick with stuff long enough [to solve the problem]?" I think we should consider that seriously.

Q. Dan Armbrust: Should we be thinking about building out a studio model of start-ups—not waiting for start-ups to occur but actually spinning them up on specific problems as a model? It occurs to me that some of these may be opportunities but there may not be start-ups waiting in the wings and we may need to think about creating start-ups to address specific problems.

A. Deirdre Hanford: Through convening we can start helping make connections.

Q. Philip Wong: Has the team thought about whether focusing on high-risk projects and focusing on underrepresented (and not necessarily high-risk) areas is an "and" or an "or" recommendation?

A. Deirdre Hanford: We have. We do think there is an opportunity to invest in ideas that probably would not see the light of day in the regular venture community and bring those forward.

Organization and Public-Private Partnership Consensus Vote:
Recommendation 9-1: 0 Opposed
Recommendation 9-2: 0 Opposed
Recommendation 9-3: 0 Opposed
Recommendation 9-4: 0 Opposed
Recommendation 9-5: 0 Opposed
Recommendation 9-6: 0 Opposed
Recommendation 9-7: 0 Opposed
Recommendation 9-8: 0 Opposed
Recommendation 9-9: 0 Opposed
Recommendation 9-10: 0 Opposed
Recommendation 9-11: 0 Opposed

IX. Public Comment Period

Mr. Davis read the following list of public comments:

- How can relevant industry experts help ensure organizations/entities are properly prepared to offer the services they intend to offer as part of their application?

- What are the entry/sector expectations from the NSTC? Are they an enabling body for the industry R&D, a governing body for the industry R&D, etc.?

- How will industry collaborate to advance US leadership beyond CMOS R&D in a highly competitive landscape?

- The semiconductor industry uses over 400 chemicals. Many chemicals used are carcinogenic and environmentally harmful. Will there be any government incentives to address the creation and discovery of green alternatives?

- Will NAPMP be run like the NSTC or more like other federal research programs such as those administered by NSF or the Defense Advanced Research Projects Agency?

- Will the NSTC or NAPMP find centers, programs, and phases (e.g., phase 0, phase 1, phase 2, etc.)?

- What role do we see small, US-based, printed circuit board manufacturers playing in supporting CHIPS Act objectives?

- What is the role of small- and medium-sized companies? How can the speed and agility of smaller companies help in a unique way?

- To what degree will the committee be working with and supporting the development of small start-up companies that are not aligned with big players such as Intel, AMD, Nvidia, etc.?

- Semiconductors require both active and passive components to work. Thus far, the emphasis seems to be put on active electronics like logic and memory. What is the direction or what are the passive components like conductors, capacitors, and connectors?

- What will the role of academic institutions—whether four-year, higher-education, community college, or high-school—be in the NSTC? Will there be opportunities for direct funding for academia as opposed to through industry as we have seen thus far?

X. Summary Remarks and Next Steps

Dr. Laurie Locascio thanked everyone who participated, thanked everyone who came, thanked everyone for thinking so deeply on these topics, thanked the chairs of the meeting, and briefly summarized the meeting's topics.

XI. Adjournment

Mr. Davis shared that a recording of this meeting, a summary of this meeting, and all presentations will be posted online at CHIPS.gov for public access.

Ben Davis adjourned the meeting at 3:05 p.m. ET.

I hereby certify that to the best of my knowledge; the foregoing minutes are accurate and complete.
IAC Chair: Scott DeBoer
Date: 11/27/24