IAC R&D Gaps Working Group

Standards sub-group report

New R&D Gaps WG Charge: Standards Sub-Group

Provide feedback and recommendations for opportunities and strategies to support the private sector-led semiconductor and microelectronics standards ecosystem in becoming even smarter, faster, and more inclusive and agile in enabling innovation. Examples for consideration could include:

- Leveraging CHIPS R&D convening capabilities to facilitate community consensus around strategic standards needs;
- Exploring the acceleration of standards processes through standards incubators and accelerators;
- Evaluating approaches for linking community standards goals to relevant pre-standards research needs.

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R&D Gaps Working Group recommendations – Feb 7 IAC Meeting

Recommendation 1:

Establish a set of five key capabilities aimed to lower the barriers to entry and success for innovators. These capabilities will rely on a network of physical and virtual facilities with a digital backbone to reduce design and experimentation cycle time. These capabilities should benefit the *entire community of stakeholders and it should be of primary importance to increase access to and reduce the effective cost of accessing these capabilities over time.*

1) Establish easily accessible prototyping capabilities in multiple facilities and enact the ability to rapidly try out CMOS+X at a scale that is relevant to industry

2) Create a semiverse digital twin

3) Establish chiplets ecosystem and 3D heterogeneous integration platform for chiplet innovation and advanced packaging

4) Build an accessible platform for chip design and enable new EDA tools that treat 3D (monolithic or stacked) as an intrinsic assumption

5) Create a nurturing ecosystem for promising startups

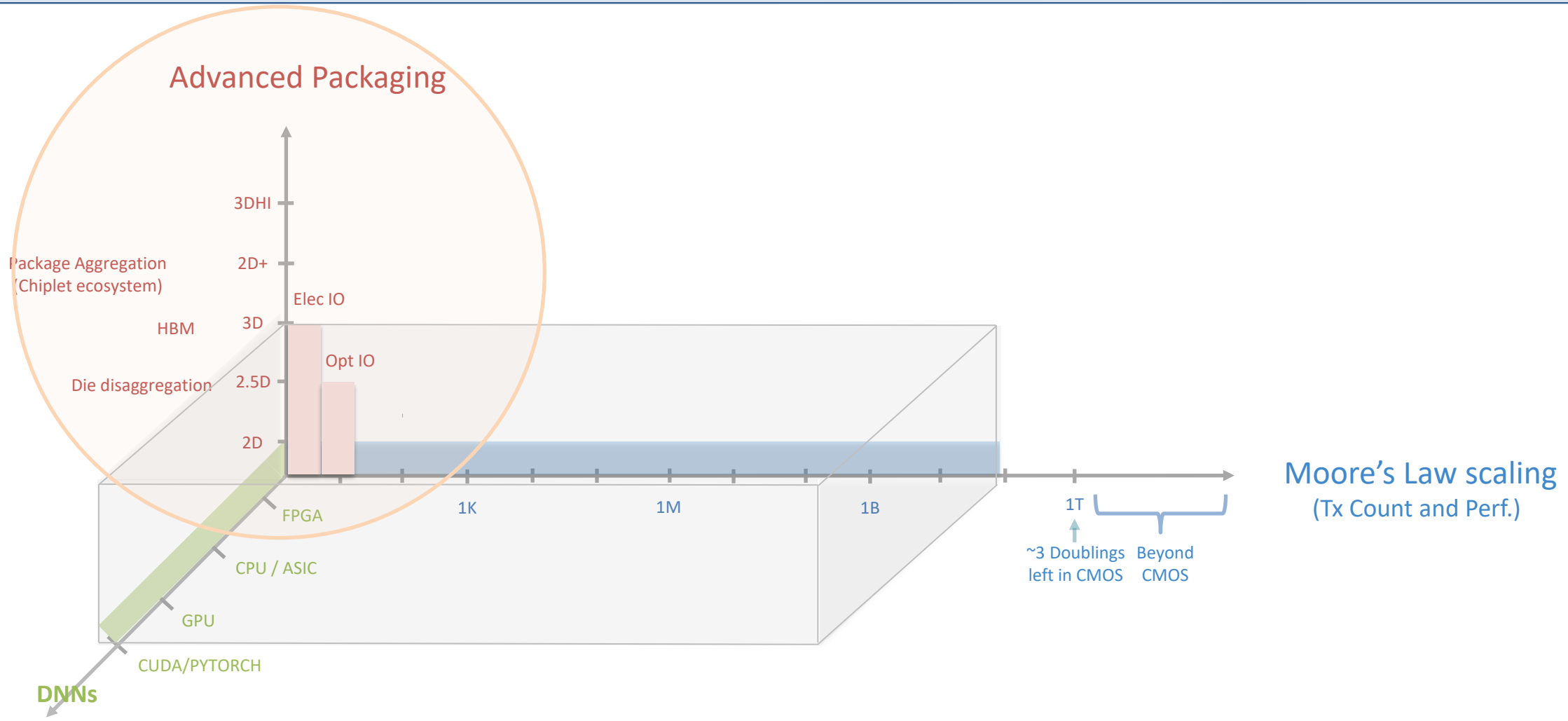
New WG charge: Advanced Packaging → IAC June 2023 sprint

Provide recommendations for strategies and investments for the long-term research needs for advanced packaging that will help establish and sustain a viable domestic advanced packaging ecosystem in the US.

The working group could:

- review the advanced packaging needs of the U.S. and ecosystem gaps suggest focus area priorities
- outline best opportunities to develop and sustain US leadership in semiconductor advanced packaging
- suggest mechanisms for ecosystem development

Moore’s Law economics will be driven by chips, advanced packaging and architectures



Application driven systems with specialized architectures/algorithms
w/ software stack

High Level Questions on Standards

Scope:

- Standards workgroup narrowed focus to: Chiplet related standards
- Developed a set of questions on standards that can help build open ecosystem for chiplets

List of questions:

- How can CHIPS R&D/NSTC incentivize the formation of alliances to support the mission to grow a competitive and open chiplet ecosystem?
- How can CHIPS R&D/ NSTC ensure that these alliances are driving to a common set of relevant standards for the ecosystem?
- How can CHIPS R&D/ NSTC ensure that technology advancement and standardization is well thought out, sustainable, and able to benefit all alliance members?
- What could be overarching body to harmonize various open chiplet, 2.5D, 3D standards?
- What are your thoughts on exploring the acceleration of standards processes?
- What could be approaches for linking community standards goals to relevant pre-standards research needs?
- What could be standards developed/implemented for the 2.5D, 3D chiplet integration packaging manufacturing?

Expert Testimonials

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Adam Cron
Distinguished Architect
Synopsys

Debendra Das Sharma
Senior Fellow
Intel

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TSMC

Scott Sikorski
Packaging Technology
IBM

Yatin Trivedi
Standards Development
IEEE

Bapi Vinnakota
Technologist and Architect
LBL, Open Compute Project

11 speakers from industry, consortia, standards body and national labs provided expert testimony.
Thank you to those that shared their time and perspective!

Special thanks to Chris Greer, Leader of Standards effort at CHIPS R&D Office

Chris Greer
Sr. Exec. Standards
CHIPS R&D Office

Provides overview of strategy to bring ecosystem together

- Role that CHIPS R&D may envision to play
- Conducted workshop with more than 600 participants
- Provided early assessment of learning from the workshop

Summit main outcomes

- Energized the semiconductor and microelectronics standards community
- Identified community consensus around initial strategic priorities
- New informal interaction of standards organizations and industry alliances
- Chiplets and digital twin selected as subject of the first 2 technical workshops (Dec. 12-15)

Initial strategic priorities from the first workshop on Standards

1) Priority Areas

- Technology – Adv Packaging, Chiplets, Materials, Sustainability
- Infrastructure – Digital Twin, Automation, Data Sharing
- Security – Supply Chain Assurance
- People – Standards-Capable Workforce

Key learning from questions

High Level Questions on Standards – key themes 1/3

- **How can CHIPS R&D/NSTC incentivize the formation of alliances to support the mission to grow a competitive and open chiplet ecosystem?**
  - Facilitate communication between industry, government, and standards development working groups
  - Support face-to-face meetings
  - Advertise the availability of standards once they are ready to be used
  - Encourage industry leaders and other standards to reference the new and old content
  - Ensure representation of start-ups in standards groups

- **How can CHIPS R&D/NSTC ensure that these alliances are driving to a common set of relevant standards for the ecosystem?**
  - Influence standards development by inviting select global organizations to participate in NIST led workshops with all relevant stakeholders
  - Encourage conformance to standards in government funded projects

- **How can CHIPS R&D/NSTC ensure that technology advancement and standardization is well thought out, sustainable, and able to benefit all alliance members?**
  - NSTC can help sustainability through R&D in key areas such as advanced packaging options, test, security, cooling, power delivery, and optics
  - Ensure broad market potentials and technology trends are comprehended in the development of new standards
  - Create knowledge environment for easy access of existing standards
  - Include needs for analog/RF and automotive area

High Level Questions on Standards – key themes 2/3

- **What could be the overarching body to harmonize various open chiplet, 2.5D, 3D standards?**
  - CHIPS R&D office can create alliance of alliances and consortia
  - Leverage the convening power, resources and technical expertise within the alliance of alliances and consortia
  - Some speakers recommended JEDEC, IEEE, OCP, or UCIe as the overarching body (our opinion is that they should rather be included)

- **What are your thoughts on exploring the acceleration of standards processes through standards incubators and accelerators?**
  - Promote pre-competitive prototyping efforts allowing companies to collaborate on chiplet prototypes, accelerating the development process
  - Provide capabilities for testing and validation of prototypes including development of new test standards, especially for advanced 2.5D and 3D packaging (e.g., fine pitch probing)
  - Enable standards-aligned reference designs to facilitate introduction of new chiplets
  - Implement IP control and data sharing guidelines
  - Promote the idea of introducing standards education for workforce development

- **What could be approaches for linking community standards goals to relevant pre-standards research needs? (What type of research agenda should be driven in support of standard development?)**
  - Invite key stakeholders to regular workshops to exchange ideas
  - Research should not be limited to standards and should enable a roadmap view within the standard
  - NSTC should fund pre-competitive demonstrators to validate standards in support of chiplets ecosystem

High Level Questions on Standards – key themes 3/3

- **What could be standards developed/implemented for the 2.5D, 3D chiplet integration in factories for packaging?**
  - Drive toward standards for secure data exchange
  - Address lack of manufacturing test and standardized interfaces in the analog/RF area
  - Enhance interoperability and reduce supply chain complexity (e.g., such as those used in automotive industry) by standardizing highly utilized semiconductor components
  - Test standards are key: Electrical DFT combined with wafer metrology and full inspection
  - Open sharing of the interface protocol
  - Share electrical models for driver and receiver circuits (output stage)
  - I/O footprint pads
  - ESD requirements
  - Most important: standardize external I/O (lanes/mm)

Workgroup Recommendations

Recommendations

Build Alliance/Ecosystem:

1) Use CHIPS R&D convening power to bring chiplet related standards bodies (industry-led consortia and associations) together to create an Alliance of Alliances

- Bring together standards organizations and alliances (e.g. JEDEC, IEEE, OCP, UCIe, 3Dblox) each of which has its own focus/strength
- Facilitate communication between industry, government, and standards development working groups
- Create knowledge environment for easy access of existing standards
- Advertise the availability of standards once they are ready to be used
- Ensure representation of start-ups in standards groups

Recommendations

Accelerate standards processes:

2) Accelerate standards processes by enabling infrastructure and data access that allows entities to collaborate on chiplet prototypes

- Provide capabilities for testing and validation of chiplet prototypes
- Enable standards-aligned reference designs to facilitate introduction of new chiplets
- Provide access to data that can expedite design cycle and tooling development
- Facilitate infrastructure access for chiplet development (e.g. MOSIS was formed to facilitate chip development)
- Encourage conformance to standards in government funded projects

Ensure Long-term Viability:

3) Ensure broad market potentials and technology trends are comprehended in the development of new standards

- Encourage formation of pre-standard study groups to ensure broad market potential and trend
- Include needs for analog/RF and automotive area
- Coordinate with EDA vendors to ensure viability needs are supported by interoperable design tools
- Periodically review standards to ensure competitiveness and relevance

Recommendations

Funding for Standards work:

4) Allocate funding from CHIPS R&D programs to incentivize development of standards that foster open chiplet ecosystem

Examples of areas that needs to be funded:

- Pre-standards research areas: Advanced packaging options, test, security, chiplets, cooling, power delivery, and optics
- Pre-competitive prototyping projects
- Plugfests utilizing reference modular chiplet architectures
- A small team to facilitate and organize standards activities

Enable Workforce:

5) Promote the idea of introducing standards education in semiconductor workforce programs

- Encourage early professional participation in standards development
- Incorporate analysis of standards documentation in existing curricula
- Create continuing learning opportunities about standards for the community

Recommendations Summary

1) *Use CHIPS R&D convening power to bring chiplet related standards bodies (industry-led consortia and associations) together to create an Alliance of Alliances*

2) *Accelerate standards processes by enabling infrastructure and data access that allows entities to collaborate on chiplet prototypes*

3) *Ensure broad market potentials and technology trends are comprehended in the development of new standards*

4) *Allocate funding from CHIPS R&D programs to incentivize development of standards that foster open chiplet ecosystem*

5) *Promote the idea of introducing standards education in semiconductor workforce programs*