IAC // R&D Gaps // Metrology Program

11-08-2023

New R&D Gaps WG Charge: Metrology Sub-Group

Provide feedback and recommendations for opportunities and strategies to maximize the impact of the **CHIPS Metrology Program** in advancing semiconductor technology. The working group will review the current strategy of the CHIPS Metrology Program, and

1) Recommend initial areas of attention within **focus area priorities**,
2) Recommend approaches and practices for the best opportunities for metrology advances to reach **use in the industry**, or
3) Recommend approaches and practices to ensure integration with the **other CHIPS R&D programs**

James Ang
Pacific Northwest National Laboratory

Rajarao Jammy
IMEC USA

Gregg Bartlett
Global-Foundries

Ken Joyce
Brewer Science

Todd Younkin
SRC

Lead: Todd Younkin

Special acknowledgement to Dan Armbrust, Mukesh Khare, Ben Davis, and David LaVan

Metrology Sub-Group :: Source Materials (1 of 2)

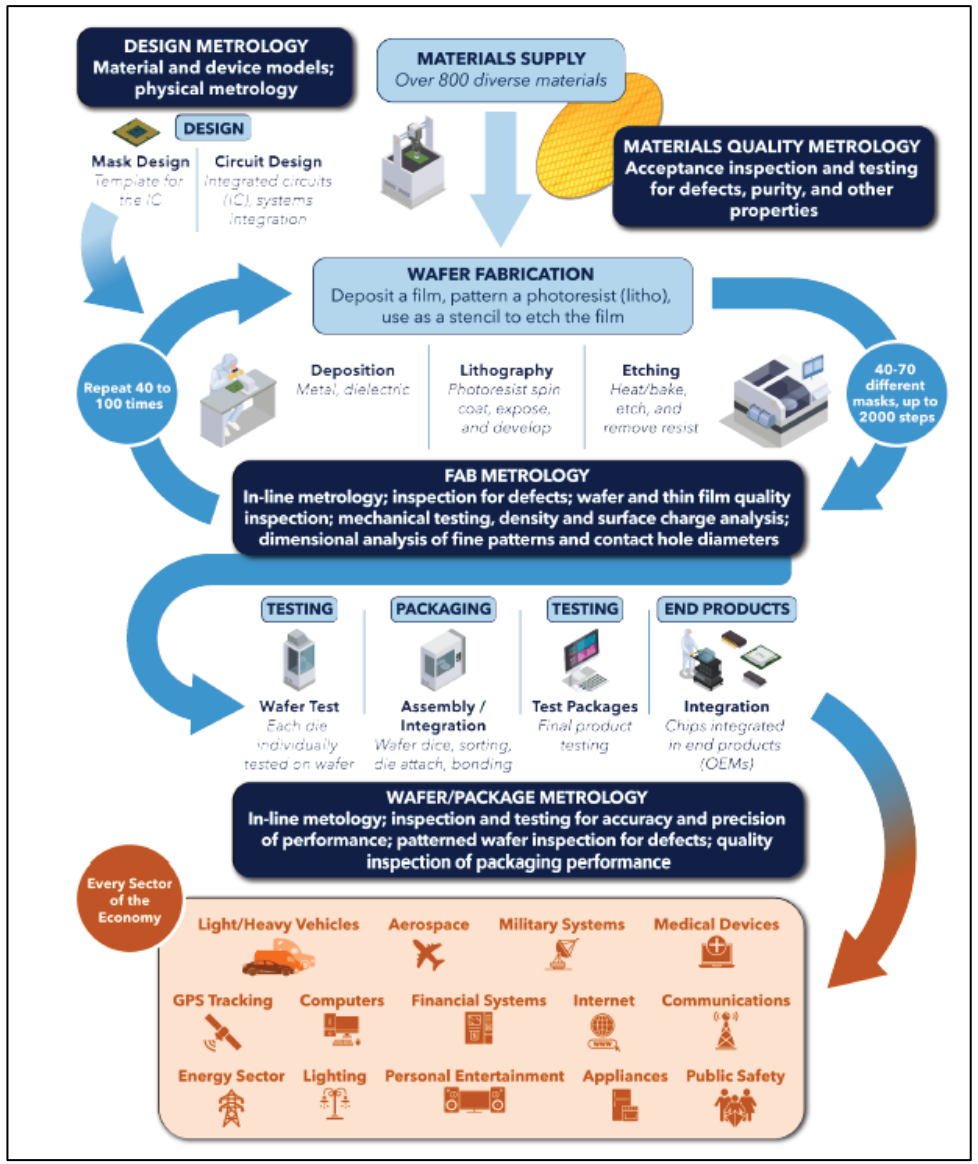
Aug '22

Facilitating US Leadership and Competitiveness through Advancements in Measurements and Standards – LINK

Jun '23

Metrology Gaps in the Semiconductor Ecosystem - LINK

Metrology Program – 7 Grand Challenges



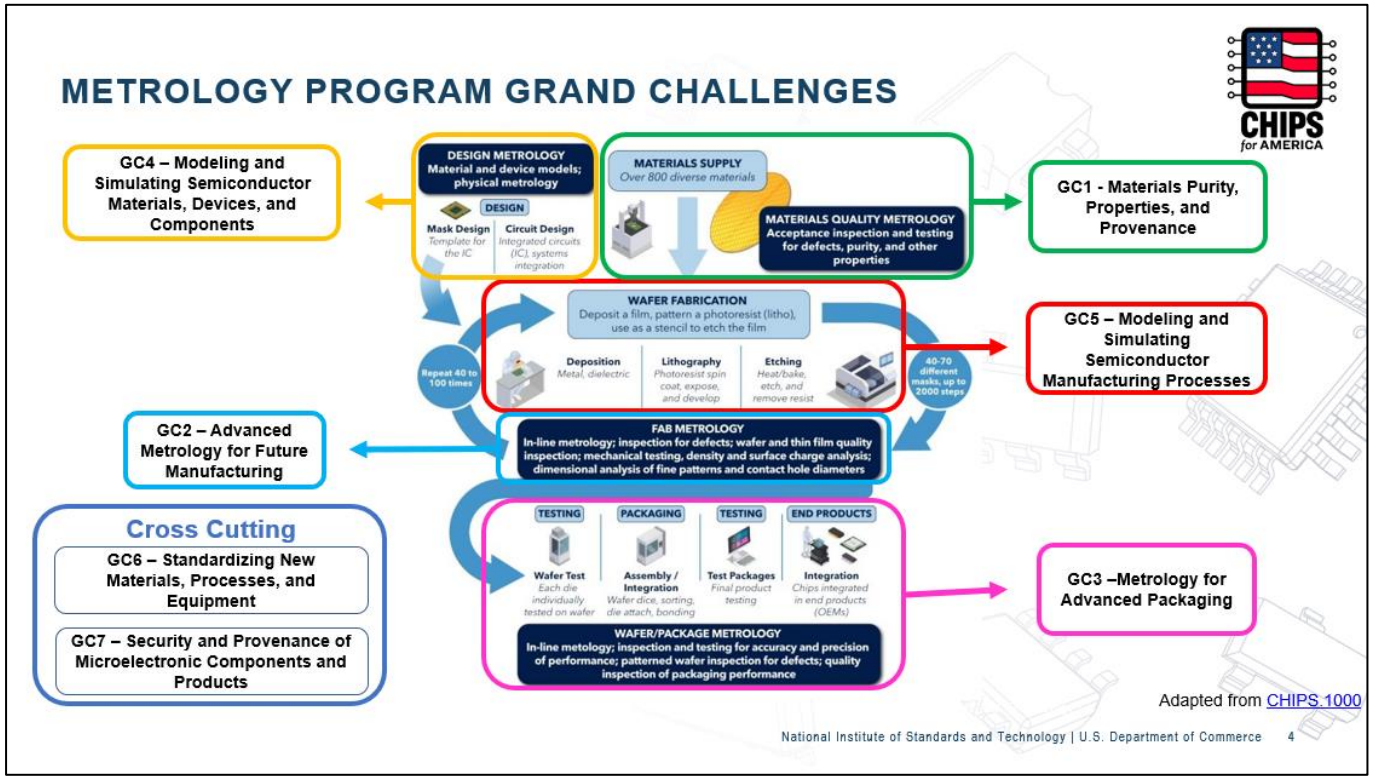
Metrology Grand Challenges

1. **GC1** : Metrology for Materials Purity, Properties, and Provenance
2. **GC2** : Advanced Metrology for Future Microelectronics Manufacturing
3. **GC3** : Enabling Metrology for Integrating Components in Advanced Packaging
4. **GC4** : Modeling and Simulating Semiconductor Materials, Designs, and Components
5. **GC5** : Modeling and Simulating Semiconductor Manufacturing Processes
6. **GC6** : Standardizing New Materials, Processes, and Equipment for Microelectronics
7. **GC7** : Metrology to Enhance Security and Provenance of Microelectronic based Components and Products

7 Metrology Grand Challenges – Responding to Industry Trends

- GCs include new techniques, models (AI/ML), data management, and standards

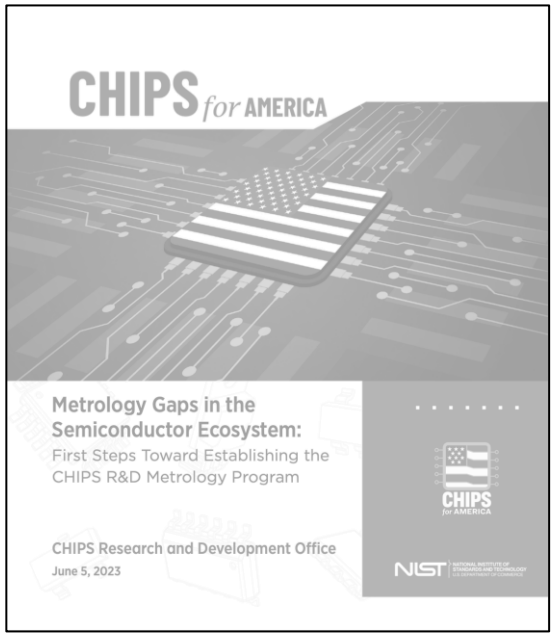
- Consistent themes:
  - Must see through multiple layers at smaller length scales with faster timing and/or scanning rates
  - Need the fusion with modeling, simulation, and reliability that spans a wider range of products and operating conditions
  - Must adopt a broader use of the electromagnetics spectrum (EUV, THz) and build upon advances in ion/electron microscopy
  - Needed to drive the innovation and development of future materials, processes, and products

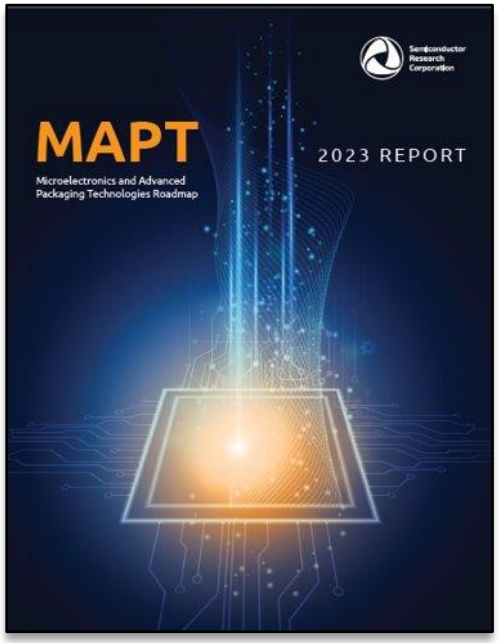


Our committee received a readout from CHIPS leadership on the 1st tranche of Metrology Program investments, primarily associated with GCs #2 and 4.

We appreciate the deliberate nature of these investments and the progress made by Marla's team.

Metrology Sub-Group :: Source Materials (2 of 2)





Aug '22

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Oct '23

NIST MAPT Roadmap by SRC - Ch. 10 Manufacturing and Process Development Metrology - LINK

Oct'23

Invited Expert Testimonials

Expert Testimonials

Mehdi Vaez-Iravani
Applied Materials
Corp CTO Imaging & Metrology

Prof. Margaret Murnane
Univ. of Colorado-Boulder
Educator & Director, STROBE Center

Alan Hart
Advantest
Sr. Director of R&D

John Kibarian
PDF Solutions
President & CEO

Markus Kuhn
Rigaku Corporation
VP of Tech & Pathfinding; Fellow

David Su
Member of Electron Device
Failure Analysis Society

Prof. Paul McIntyre
Stanford Univ.
Educator & Assoc Lab Director, SLAC SSRL

Stefan Vogt
Argonne National Laboratory
Associate Division Director

Rick Burns
Teradyne
President, Semi Test Division

Kris Bertness
NIST
Physicist

Wen-Hsien Chuang
TSMC
Director of QnR and
Metrology Pathfinding

11 invited speakers from industry, gov't, academia, and national labs provided expert testimony.
A special thank you to those that shared their time and perspective!

Trends / Key Points (1 of 2)

- Metrology is a **growing** % of the process steps, equipment, and costs associated with advanced semiconductor manufacturing
- "Metrology" requires equal balance and vigor for **manufacturing, process, reliability, yield, and test**
- The metrology program should **emphasize** :: Advanced Packaging > Wafer Metrology >>> Legacy Packaging Metrology
- **Hybrid metrology** offers the promise of both resolution and greater throughput through the marriage of complementary techniques. This includes the combination of out-of-line and in-line techniques.
- There are **cultural and knowledge gaps** between the fab, lab, and equipment providers that CHIPS R&D investments can help to close.
    - Currently, the semi metrology ecosystem is stagnant with lab and fab communities having limited interactions that accelerate or catalyze

Trends / Key Points (2 of 2)

- In advanced packaging, **failure is not an option** as you are taking known good die and then building failed system(s)
  - A top priority should be Known Good Die (KGD) combined with multi-die validation for heterogeneous integration (HI) that **competes economically with monolithic die**
  - The **end-use-application-based binning of chiplets** will become increasingly important for enabling die matching and to maximize yield in an HI package
- CHIPS R&D investments and industrial partners can provide **pre-competitive and prototyping samples** that accelerate the community by allowing for the evaluation of a technology, the gathering of nonproprietary data, debugging equipment, etc.
- NIST has a role to play as a **trusted hub supplier** for data and applied data analytics by establishing standards and metrology, such as blockchain, that enable information exchange yet provides **security / provenance** throughout the manufacturing flow

Define Metro Program Plans that Spans & Engages 3 Categories

Pursue emerging tech that **transitions to commercial out-of-line and in-line capabilities**, further categorized by 4 target descriptors:

Forever off-line characterization
(e.g., Synchrotron, X-ray)

(NIST can engage with National Labs and leading academics)

Individual characterization / off-line metrology

(may benefit from automation)

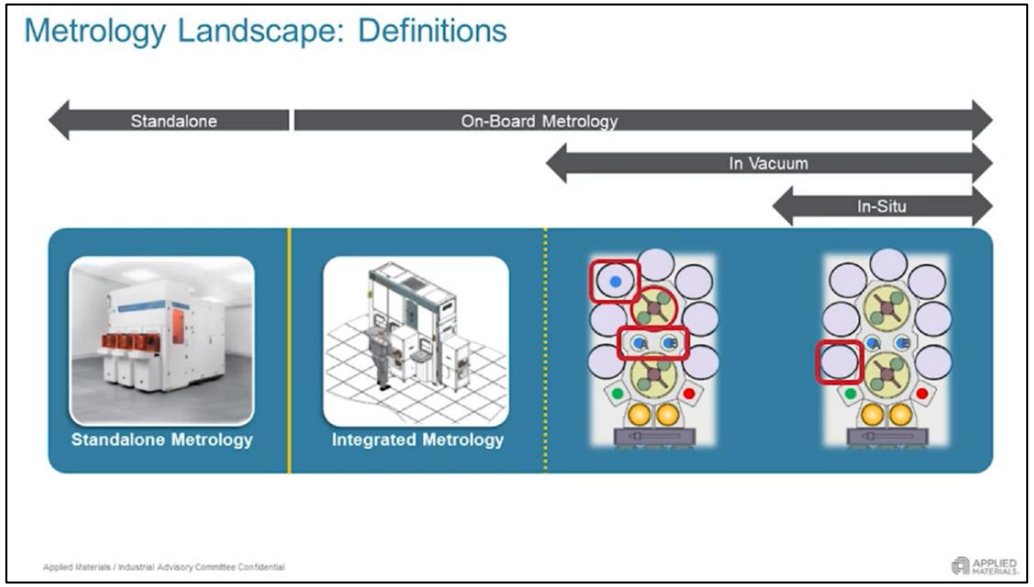
NIST **Goal** Industry

Standalone

Onboard/integrated

Module (in Vac)

Component (in Situ)



Special acknowledgement to Mehdi Vaez-Iravani, AMAT

3 Overarching Drivers for Communities of Practice that Serve CHIPS R&D

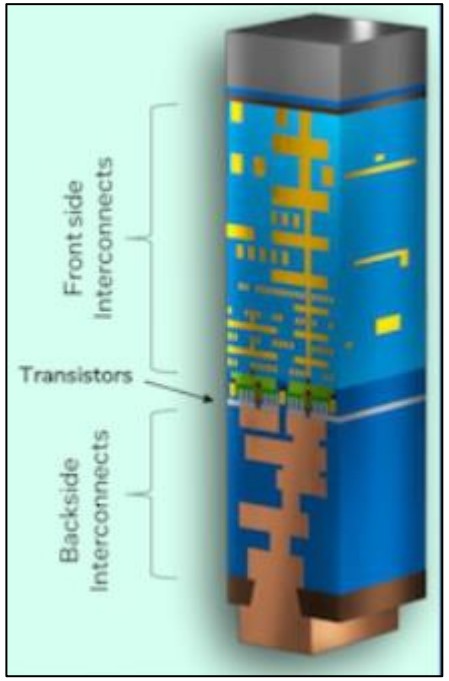


Image: Intel

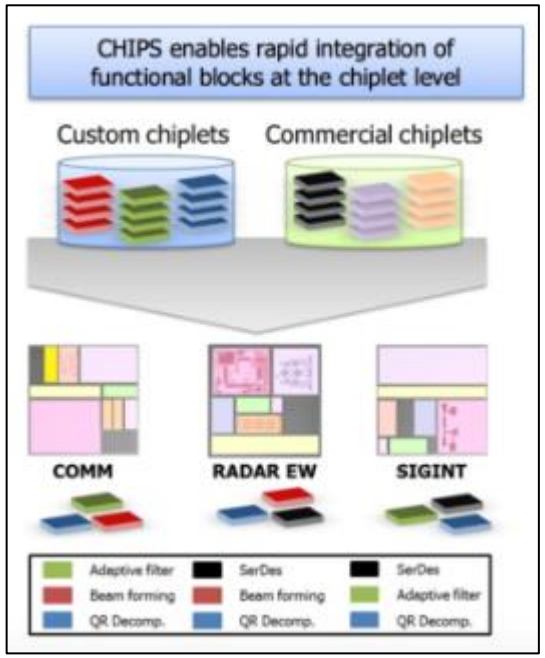


Image: DARPA

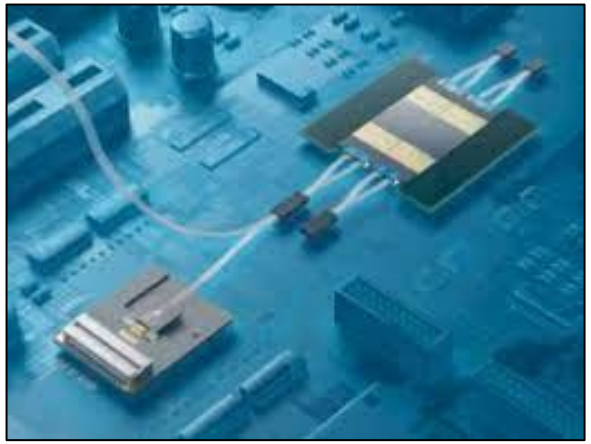


Image: Ayar Labs

3DIC Failure Analysis

- Focus on materials, devices, wafers
- In- and out-of-line needs
- 3D structure & composition
- Close partnerships with NSTC, engaging EDFA Society

➢ **Emphasize GCs 1, 2, 4, and 5**

3DHI Test, Addressing KGD*

- Focus on Chips & SiPs
- Test, Reliability, Models, Co-design
- Design, Yield, and Provenance
- Close partnerships with NAPMP & Standards

➢ **Accelerate 3, Emphasize 6-7**

Photonics / Optical Integration

- Spans Wafer & Packaged System Needs
- Benchmarking, Test, Reliability
- Prototyping and Standard Flows
- Close partnership with NSTC & NAPMP

➢ **Emphasize GCs 2-3, Explore 4-5**

*KGD = Known Good Die

Initial areas of attention within focus area priorities

Crisp execution of 1st Tranche of Metrology Program investments….plus,

Recommendations

1. **Accelerate GC3 (Adv Packaging)**, with a high-level emphasis on Known Good Die (KGD) for Chiplets

2. Place a **higher priority on Failure Analysis** (GCs 1, 2, 4, and 5) and **Photonics** (w/ GCs 2 and 3)

3. Create **standardized contractual arrangements for industry-led engagement (MOU) and investments (CRADA)**, including start-up funds that amplify the program's plans and create momentum:

    - Break down the cultural and knowledge gaps between the "fab," lab, and equipment vendors
    - Balance the needs of "bench level experts" (with challenges today!) against "industry leaders" (seeking breakthrough capabilities and a longer-term competitive advantage)
    - Seek partners who can transition capabilities into HVM*

*HVM = High Volume Manufacturing

Approaches and practices for the best opportunities for metrology advances to reach use in the industry

Recommendations

4. CHIPS R&D investments and industrial partners should provide **pre-competitive and prototyping samples that accelerate** the metrology community - allowing for the evaluation of technology, the gathering of nonproprietary data, benchmarking, debugging or matching equipment, and developing protocols

5. Within the Metrology Program and CHIPS R&D investments, while NIST's technical focus should be on both out-of-line and in-line efforts (**industry informed**), in-line efforts should be industry-led (**NIST-supported**)
   - NIST can serve as an honest broker, a neutral / science-led partner, and funding accelerator
   - Look to the End Markets – the Semi Ecosystem will not be successful unless the products succeed
   - Data is a very important consideration in these arrangements

6. Become a **trusted hub supplier for data and applied data analytics** by establishing standards and metrology, such as blockchain, allowing for **exchange with security / provenance** throughout the manufacturing flow

7. **Events** - Tie your updates and engagement plans to NSTC (/NAPMP) annual or semi-annual reviews and these industrially-relevant conferences: IEDM (wafer), ECTC (pkg), OFC (photonics), & FCMN (metrology)

Approaches and practices to ensure integration with the other CHIPS R&D programs

Recommendations

8. Priority should be on **enabling the R&D programs** of the NSTC and NAPMP, serving in a consultive role as Tech Centers are established. Priorities should be on reviewing metrology requirements, leveraging existing and new domestic capabilities coming on-line, or seeking synergy in the development of new capabilities

9. NIST and the Metrology Program can serve as a **trusted hub supplier** for standards, data format, secure data exchange, and applied data analytics into new, smarter models

10. CHIPS R&D investments should **capture the IP rights** of metrology inventions by the Metrology Program, NSTC, NAPMP, etc. such that IP can be **licensed to industrial partners** in the Metrology community to accelerate technology impact

All Recommendations

1. Accelerate GC3 (Adv Packaging), with a high-level emphasis on Known Good Die (KGD) for Chiplets
2. Place a higher priority on Failure Analysis (GCs 1, 2, 4, and 5) and Photonics (w/ GCs 2 and 3)
3. Create standardized contractual arrangements for industry-led engagement (MOU) and investments (CRADA), including start-up funds that amplify the programs plans and create momentum:
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Supporting Information

Metrology Needs for Inline Measurement and Simulation

Category	Item	Gap/Challenge	Metrology Needs
Inline measurement	Monolayer/ 2D Composition	• Not fast and cost effective enough for inline monitoring (XPS, XRF, Raman, XRD, …) • Interface monitoring lacks sufficient materials contrast	• High throughput and cost-effective solutions • High contrast and quantitative solutions for interface monitoring
	3D Structure	• Complex 3D structures (GAA, CFET, …) • High-aspect-ratio structures (aspect ratio > 10) • Insufficient sensitivity and contrast for small dimensions	• Innovative high signal-to-noise ratio solutions and cost-effective for small dimension structure (small volume and low contrast) • Low correlation between targeted parameters and underlayer structure • Profile monitor of high aspect ratio measurement (top/middle/bottom CDs, depth)
	3D Composition	• Not fast and cost effective enough for inline monitoring (XPS, XRF, Raman, XRD, …) • Complex 3D structures (GAA, CFET, …) • Modeling is required for 3D structures	• High throughput and cost-effective solution • A model-less solution for 3D composition and structures
	Machine Learning	• Current machine learning approaches are still not robust enough for inline measurement • Serves as a “black box” and is not easily used to aid analysis	• Robust and reliable solutions • User-friendly to inline troubleshooting • Good tool matching solutions
Simulation/ Automation	Simulation/ Automation	• Model building can be complicated and it is not easy to input data measured from different tools	• Automation with machine learning and AI for fast and reliable data measurement • Standardized data format from different tools for multi-domain simulation with built-in models

Special acknowledgement to Hsien-Hung Chang and Wen-Hsien Chuang, TSMC

Metrology Needs for Advanced Packaging

Category	Item	Gap/Challenge	Metrology need
Advanced Packaging	3D Physical Analysis	• Deeply buried in complex 3DIC structures • Thermomechanical data collection (i.e., warpage, thermal resistance) • Non-destructive methods are a must or preferred	• Tomographic strain analysis capability • <100nm-level XY resolution/10nm-level Z resolution to detect hairline cracks, delamination, defects, and voids in structures and joints • Wafers and die on wafer/frame warpage measurement with <1um resolution • Measurement on 3D profile of structures such as uniformity of u-bumps in a 12inch wafer within 10 minutes with 0.1um resolution • Material/mechanical property measurements before- & post-reliability burn-in tests including enhancement from specimen preparation • High throughput for 3D Xray imaging (3 to 5 seconds per 1.2mm X 1.2mm field of view) • Overlay/alignment measurement with accuracy better than 20nm
	3D Compositional Analysis	• Detects surface water absorption only with 1% resolution • Can only measure surface layer or need pretreatment to remove the top layer, and then down to the area of interest	• Detect surface water absorption (surface humidity & bonding water) with resolution of 0.1% • Non-destructive in-layer composition/thickness analysis with whole wafer scanning for solder mask, oxide, and polyimide
	Thermal Analysis	• High power consumption on AI or HPC chips that need optimization of heat dissipation on chip design and testing • Prefer non-invasive with no-embedded sensor • Rapidly increasing structure size/complexity	• Thermal property or thermal resistance measurements of multi-layered materials • Heat dissipation or thermal profile measurements on 3DICs

Special acknowledgement to Wen-Hsien Chuang, TSMC

Metrology Needs for Lab Analysis

Category	Item	Gap/Challenge	Metrology need
Si Process	True 2D Surface Imaging	• High resolution for surface topography • Lack of good materials contrast – especially for materials with low mass-density such as Carbon, Si oxide and Si nitride	• Need innovative solution to generate and collect mass contrast signals from top 5Å surface with 2Å lateral resolution
	3D Structural Analysis	• Complex 3D structure with high aspect ratio (GAA, CFET, ..) • Sub-surface or buried structure • Cannot resolve actual 3D stress/strain field • Lack of contrast for low mass density materials • Insufficient depth resolution • Non-destructive is a must or preferred	• Metrology with Angstrom or nm resolution, mass contrast signals, and high throughput to detect structure integrity • Tomographic strain analysis capability • Surface characterization with atomic resolution
	3D Compositional Analysis	• Current techniques are not fast and cost effective enough • Complex 3D structure with high aspect ratio (GAA, CFET, ..) • Sub-surface or buried structure • Some techniques use high electron dosage – sample damaged easily. EELS signal favorable for light elements and EDS signal favorable for heavy elements. Resolution limited at ~2nm. • Non-destructive is a must or preferred	• Metrology with high sensitivity on dopant-level additives ($10^{14\text{-}15}$ atoms/cm2) & chemical bonding, often in nm-thick layers for high-Z and low-Z material
Circuit Debug	Fault isolation	• Current optically-based techniques (emission, stimulation) do not have enough resolution and not work for new device architectures/materials such as buried power rails, 2D materials, or III-V materials	• New techniques (emission, stimulation) to provide better spatial resolution of ~100nm • New techniques to temporarily stimulate single device (can recover within msec) for new device architectures/materials such as buried power rails, 2D materials, III-V materials in addition to Si or SiGe • New techniques (emission, stimulation) to isolate devices with vertical stacked structures such as CFET

Special acknowledgement to Wen-Hsien Chuang, TSMC