Accelerating the next technology revolution

Mask Metrology – Current and Future Challenges

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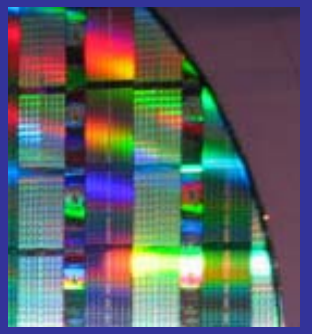
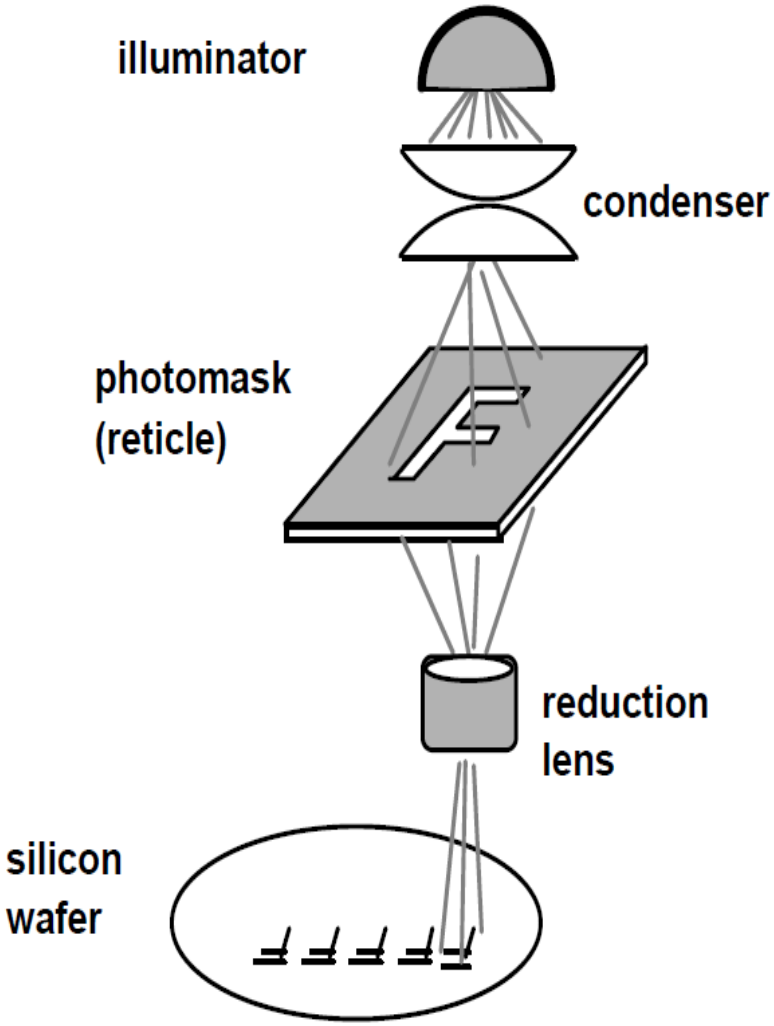


Outline

- Mask Making Process Flow
- Process Control – Enabled by Metrology
- Metrology in the Real Pattern Environment
- Challenges of Changing Environment
- Key Take-away Points

Photomask – In use



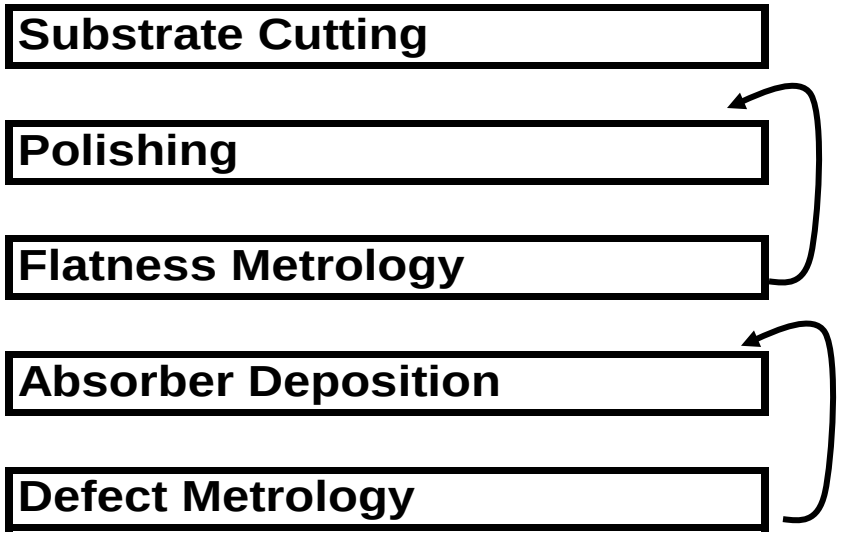
Mask Substrate/Blank

Patterned Mask

Wafer Printing

- Substrate Cutting
- Polishing
- Flatness Metrology
- Absorber Deposition
- Defect Metrology
- Resist Coat
- Patterning
- Develop
- Absorber Etch - Resist Strip
- CD Metrology
- Registration Metrology
- Defect Inspection
- Repair
- Repair Qualification
- Pellicle
- Defect Inspection
- Wafer Print
- Wafer Inspect
- Wafer CD and Overlay

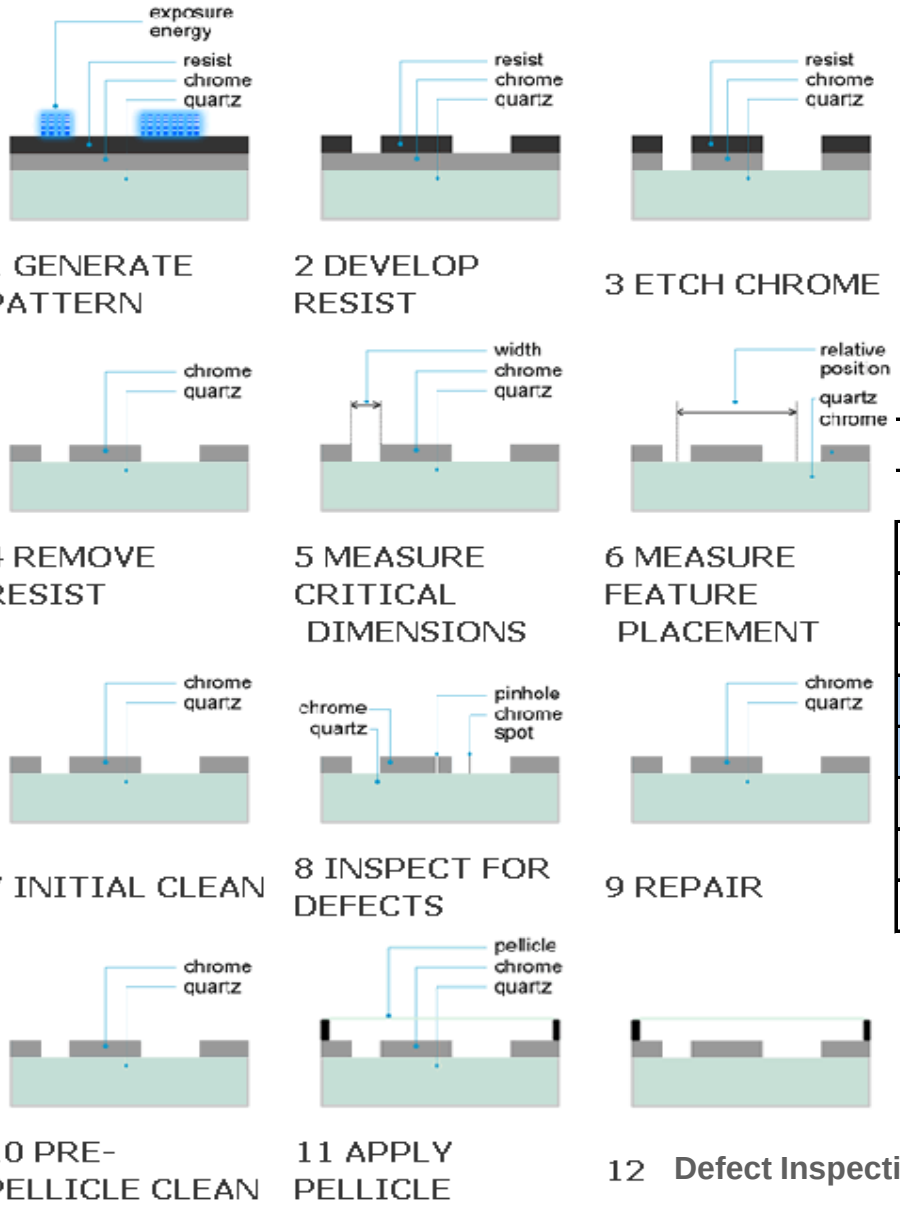
Substrate to Blank Fabrication



Metrology Needed
- Flatness
- Absorber Quality
- Defects

Year of Production	*2010*	*2013*	*2016*	*2019*
(contacted)	*45*	*32*	*23*	*16*
*Defect size (nm) [N] **	**36**	**25**	**18**	**13**
Blank flatness (nm, peak-valley) [O]	**165**	**117**	**83**	**59**

Mask-Making Process Flow



Metrology Required on the Product (Every Mask)

- CD
- Registration
- Defect Inspection

Year of Production	*2007*	*2010*	*2013*
DRAM/ ½ pitch (nm)	*68*	*45*	*32*
Mask magnification [B]	**4**	**4**	**4**
Sub Res feature size (nm)	**107**	**71**	**50**
Registration	**8.2**	**5.4**	**3.8**
MEEF isolated lines	**1.6**	**2.2**	**2.2**
CD uniformity (nm, 3 sigma)	**3.3**	**1.8**	**1.4**
MEEF contacts	**3.5**	**4**	**4**
CD uniformity (nm, 3 sigma)	**3.2**	**1.9**	**1.3**
*Defect size (nm) [N] **	**55**	**36**	**25**

Metrology P/T 0.1

Process Control – Enabled by Metrology

Metrology best close to the point of generation

Pattern Writing

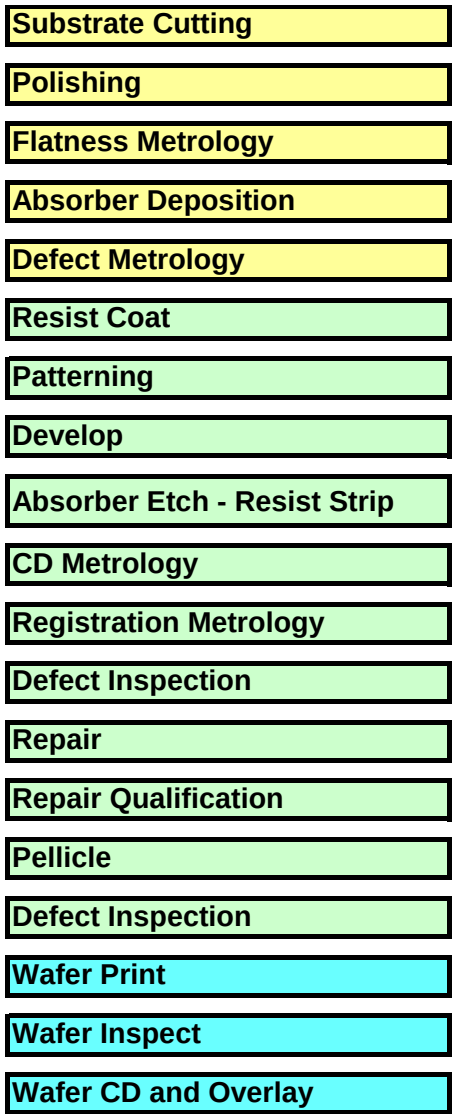
- CD
- Registration

Pattern Etching

- CD
- Registration – Stress Pattern Stress relief

Defect Creation – Everywhere

- Substrate, Blank, Resist Coating, e-beam, Develop, Etching, Cleaning



Best Process Control – CD

Today

Global Signatures

Full-loop feedback

-Based on final metrology

- Second mask fabrication

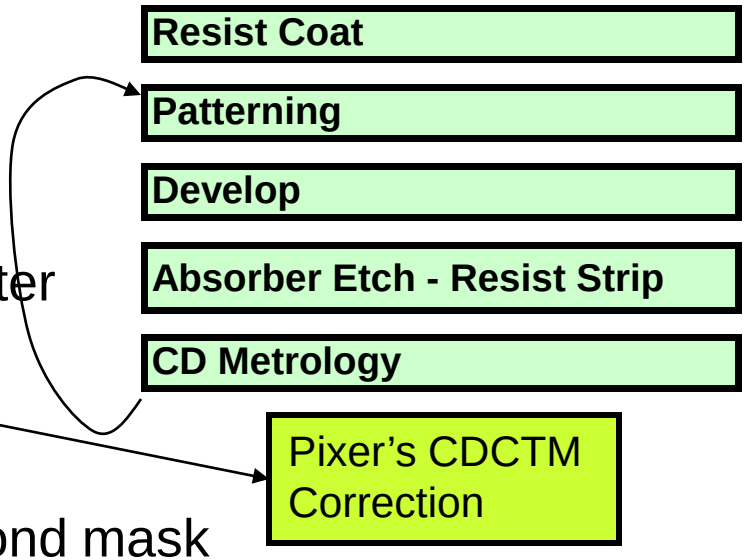
Dose map correction to the mask writer

-Grayscale mask correction

Pixer's CDC™ – tool by Carl Zeiss

- Customer (stepper uniformity correction)

- Mean correction – biasing write data - second mask



Fine Pattern Signatures

-e-beam proximity correction

-Wafer OPC

No feedback loops today

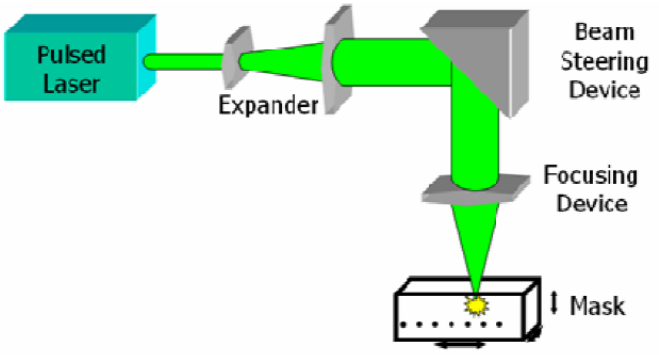
Redo – wafer OPC – big effort not done

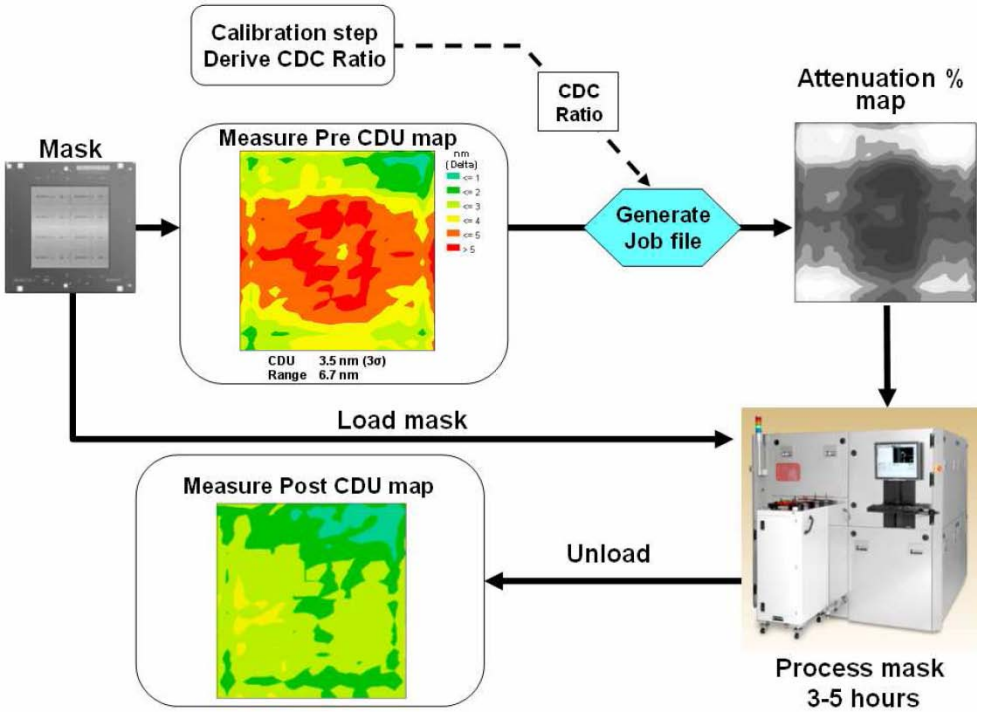
Keep process constant (unique writers, etchers, etc., of process)

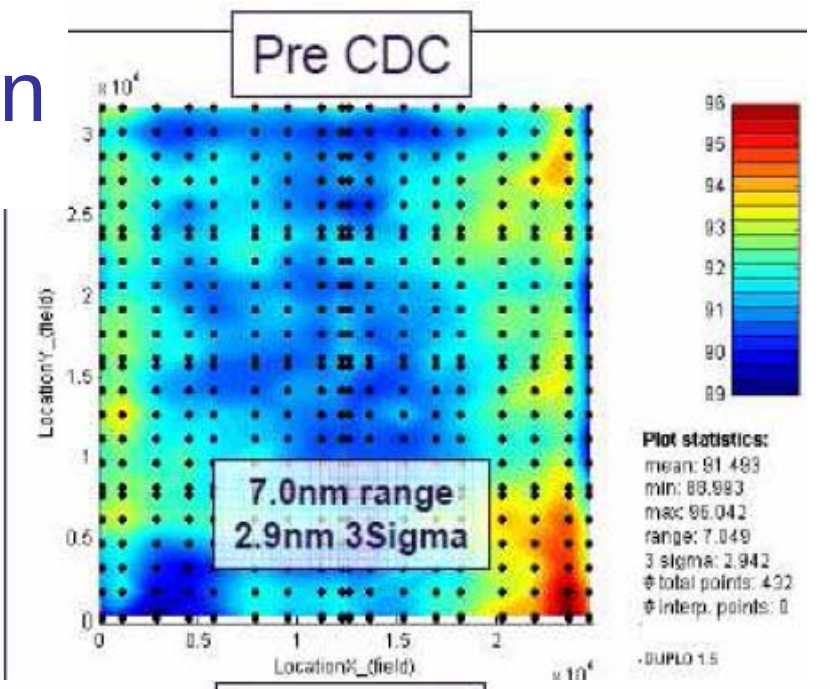
Future

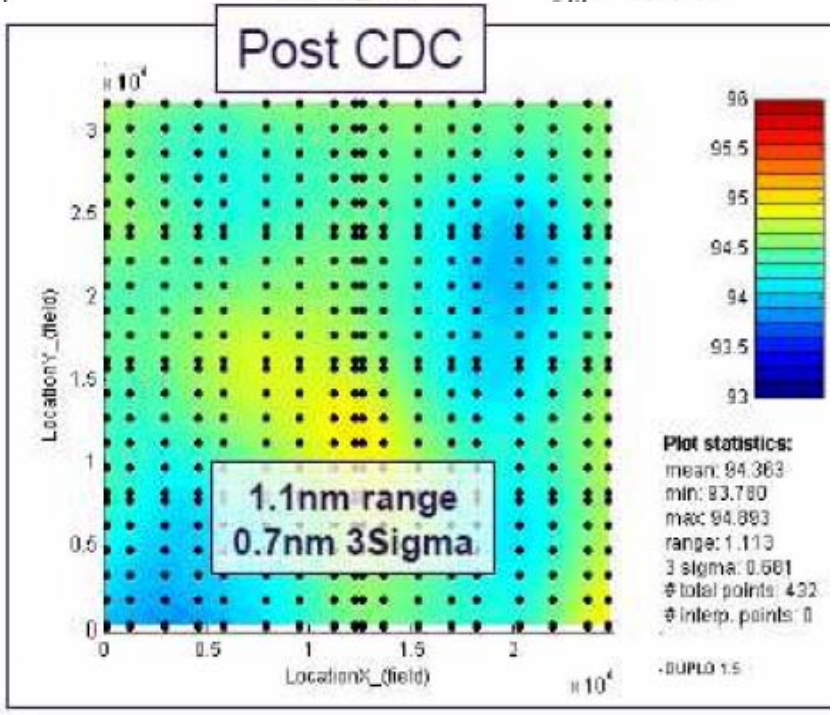
- Post-develop metrology for feed-forward correction – mean

Pixer's CDC™ CD Correction



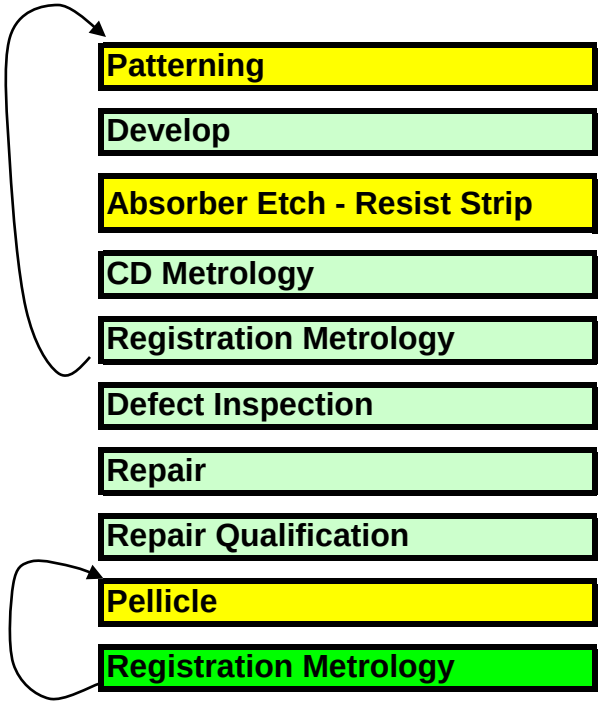






Best Process Control – Registration

Metrology best close to the point of generation



Registration Signatures

Pattern Writing

- Pattern registration global
  - Charging, mask placement sag shifts, mask clamping or slipping
- Fine shot placement

Pattern Etching

- Absorber stress relief
- Pattern-dependent registration error

Pellicle Application

- Re-apply or improve process

Registration Correction – Second Mask

- Global terms
- Writing the second mask with corrected registration grid

Future –

- Calculate stress errors, charging errors and correct before writing the mask

Best Process Control – Defects

Metrology best close to the point of generation

Defect Creation – everywhere

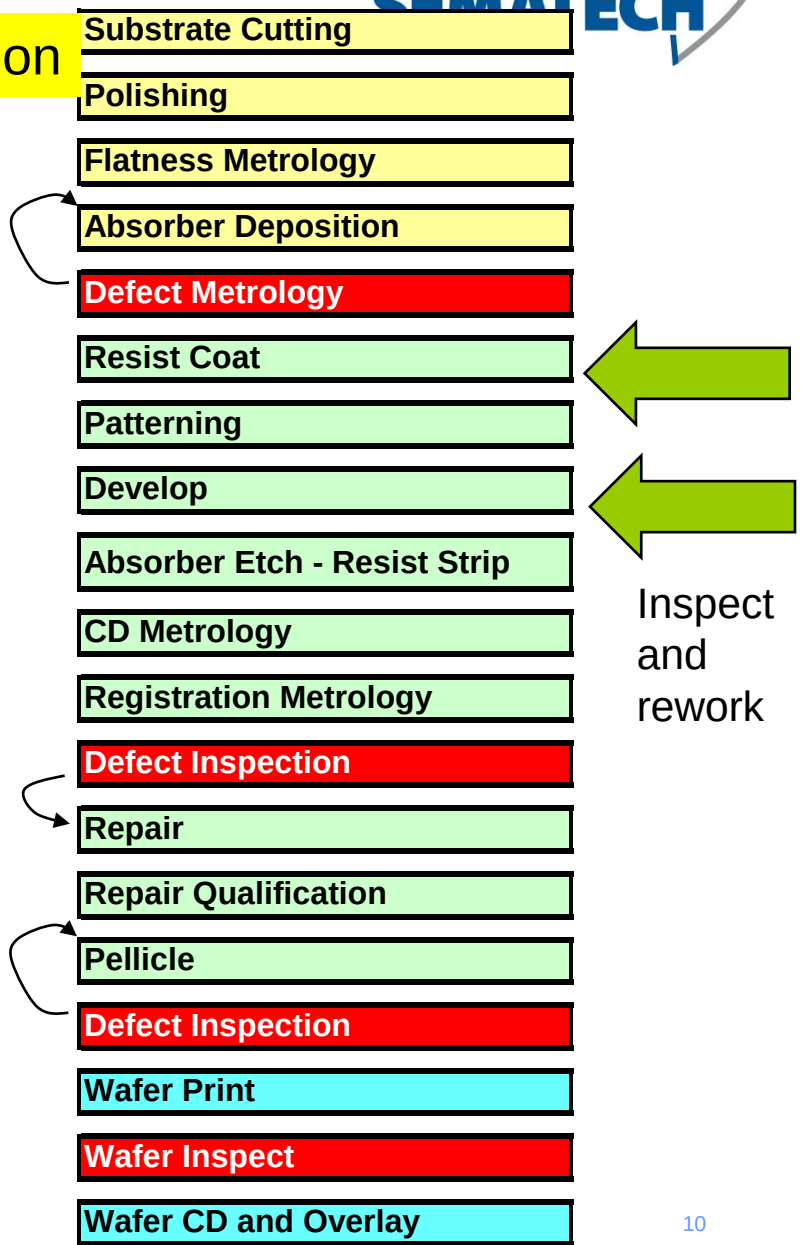
- Substrate
- Blank
- Resist Coating
- e-beam
- Develop
- Etching
- Cleaning

Defect Correction

- Find, repair, qualify repair
- Second mask and hope
- Analysis and improve the process

Future Approach (some now)

- Institute control of each process step and tool
- Continued sorting quality at each step
- Mapping defect locations
  - and placing pattern to correct for defect



Defects Analysis - Metrology

- Locate the defect such that it can be found in metrology tool
- Analysis of the defect
  - SEM / EDACS / AFM
  - Issue – Smaller defects less material to study
    - Often things that cause small defects cause big ones
  - Pareto of defects
  - Understanding of process and tool to see what needs fixing or redesign

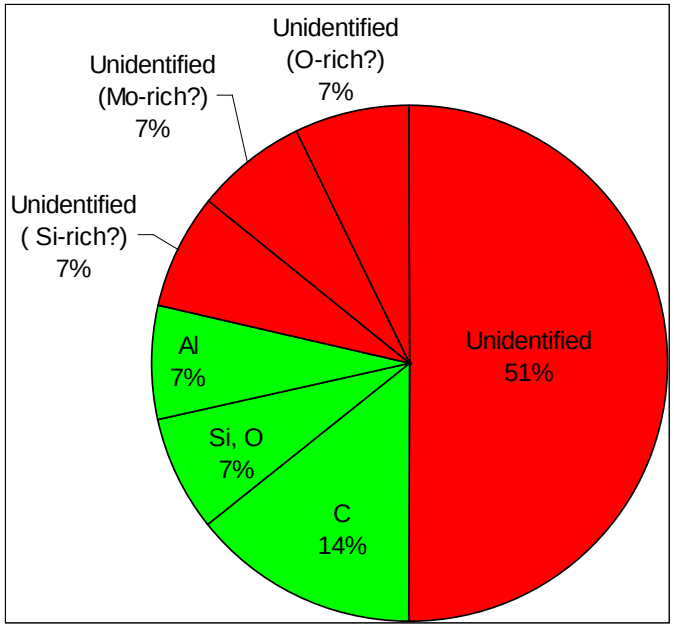
EUV Mask - Defect Size Requirement

ITRS 2008 update

Year of production	2011	2012	2013	2014	2015	2016	2017	2018	2019	2020
DRAM 1/2 pitch (nm) (contacted)	40	36	32	28	25	23	20	18	16	14
Flash 1/2 pitch (nm) (contacted)	32	25	25	23	20	18	16	14	12	11
Defect size	32	29	25	23	20	18	16	14	13	11

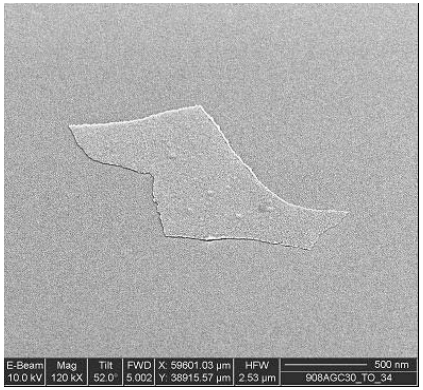
- 25 nm defects must be eliminated
- Identifying the source of defect is very challenging

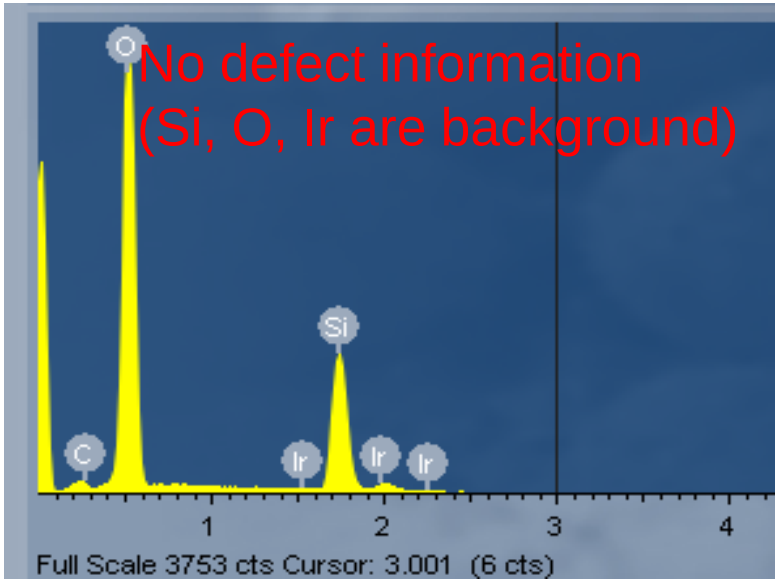
- Even at 70 nm,
  only 30~50% of the defects' elements can be identified



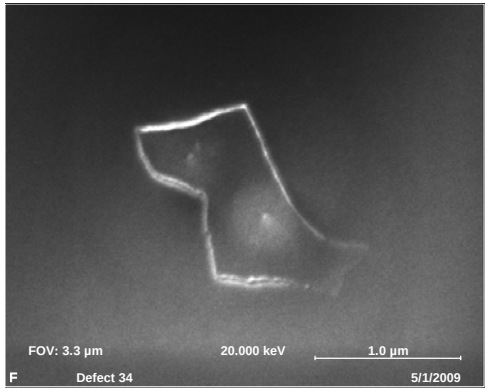
Demo Results – Non-conductive Surface (1)

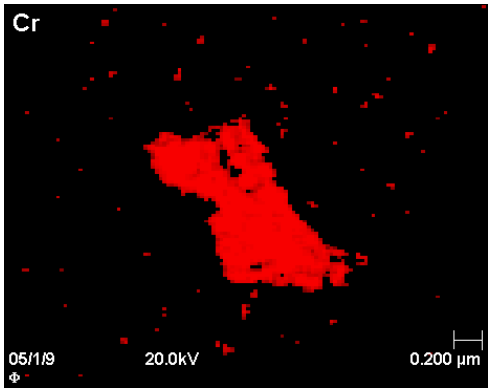
EDX (current system)

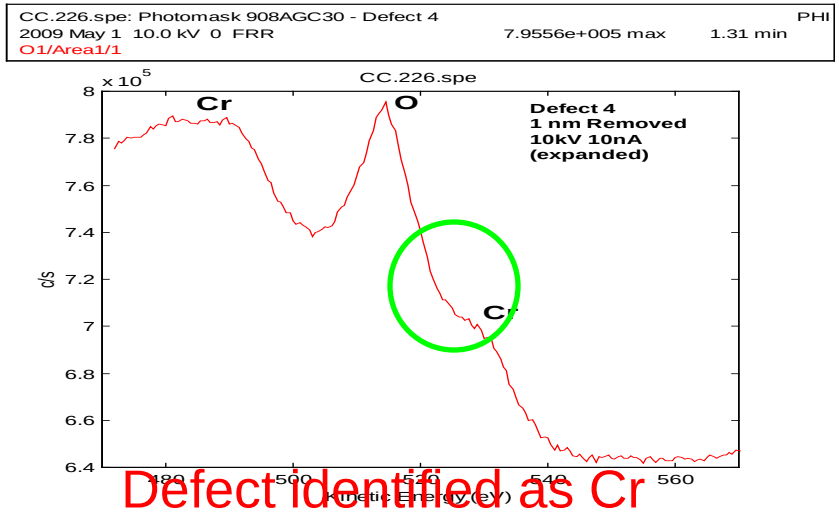




Auger





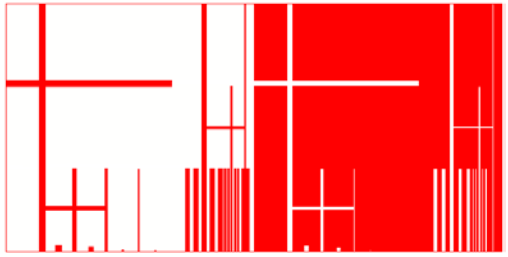


Defect identified as Cr

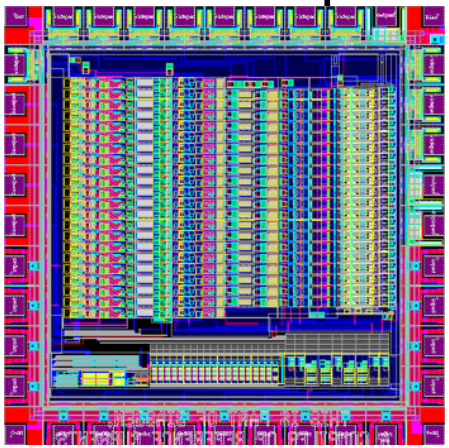
* Plate ID: 908AGC30, quartz substrate with thin Ir coating

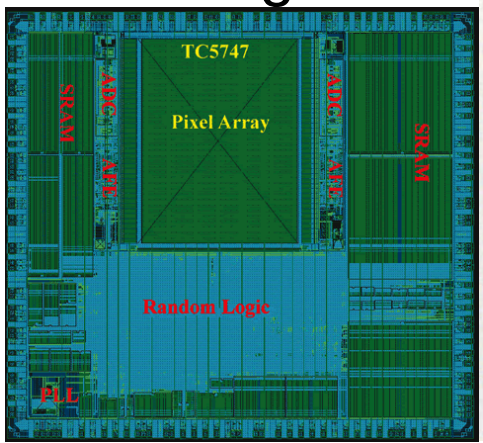
Metrology in the Real Pattern Environment

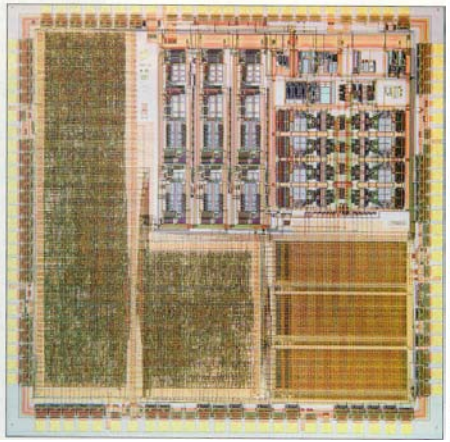
- Most metrology works best with special targets

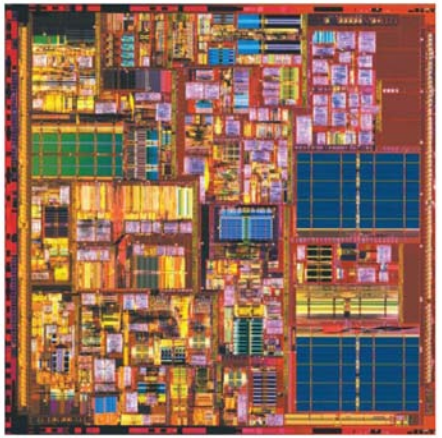


- Not the true story
  - Real patterns
  - Real pattern loading and environment

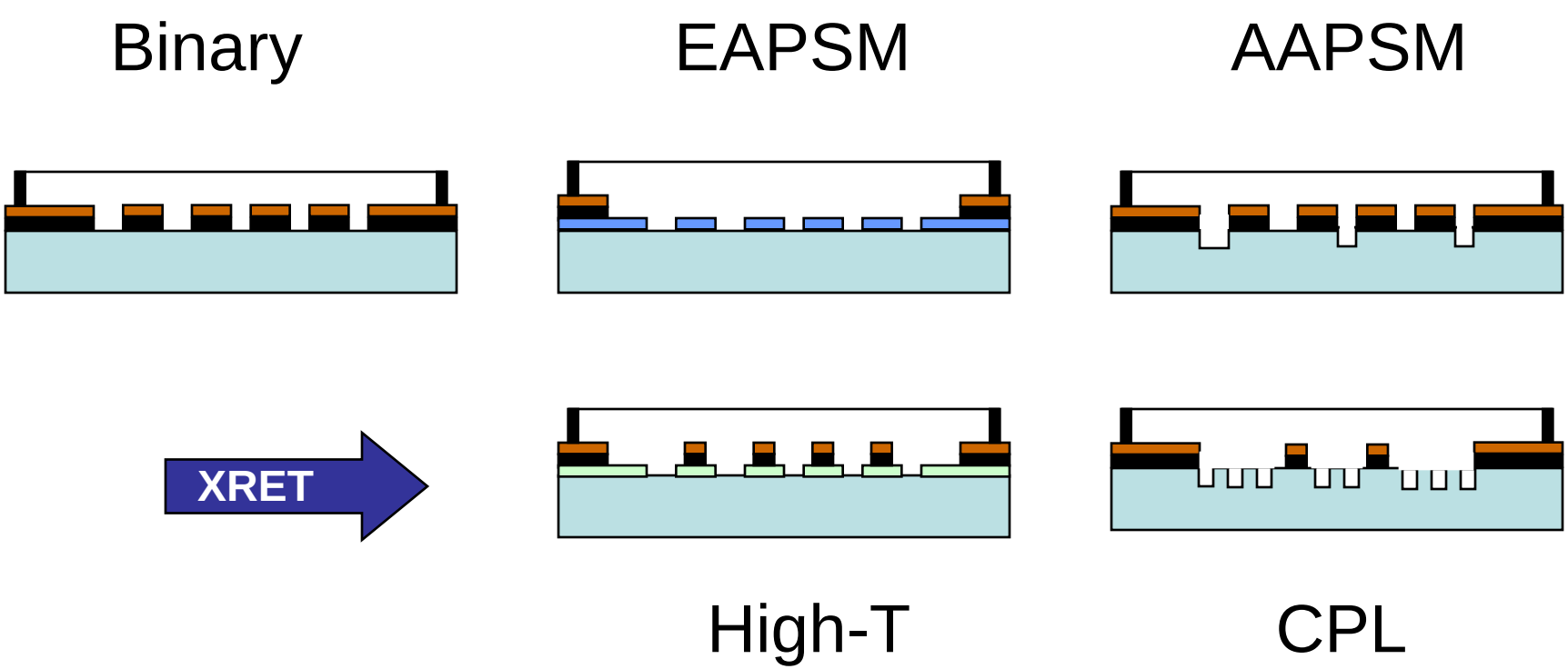








Real Mask Cross Sections

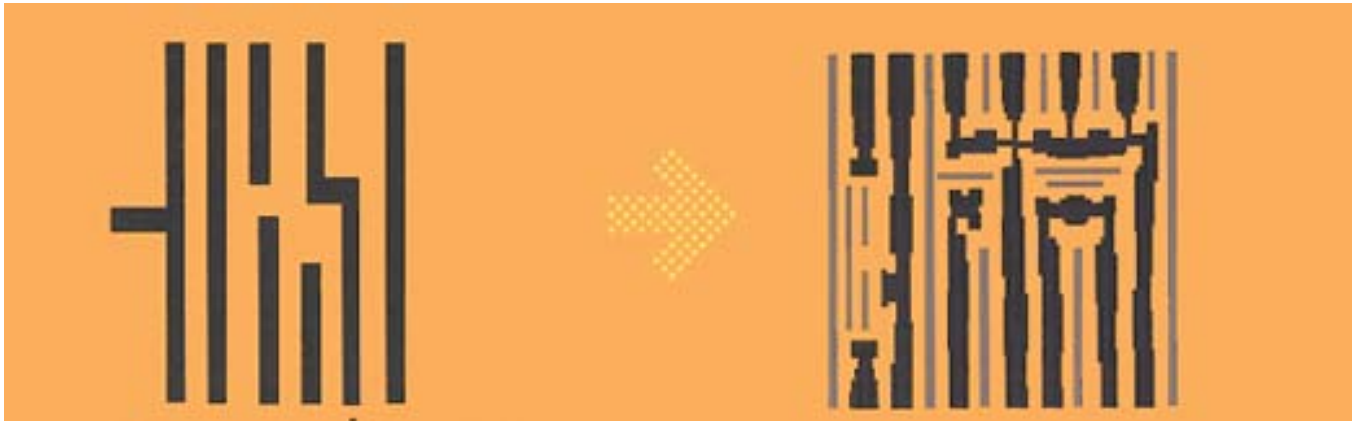


Challenges of Changing Environment

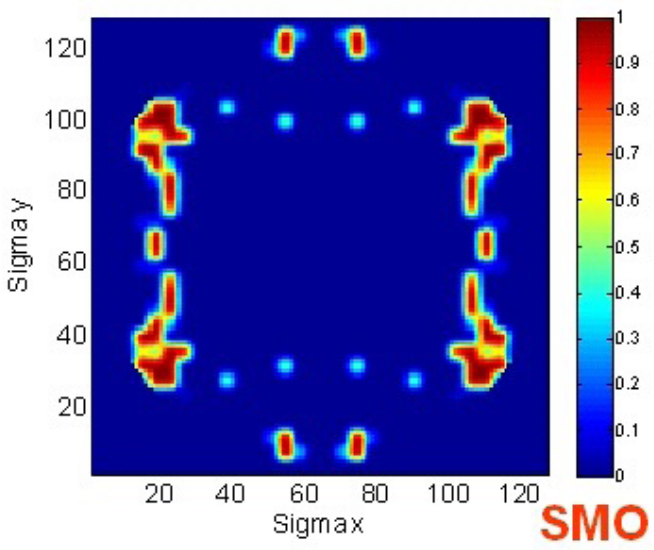
SEM images of the mask no longer represent the wafer image
MEEF – Driven by different Illuminations

- OPC Patterns
- Subresolution Patterns
- Source Mask Optimization Patterns
- Inverse Lithographic Patterns

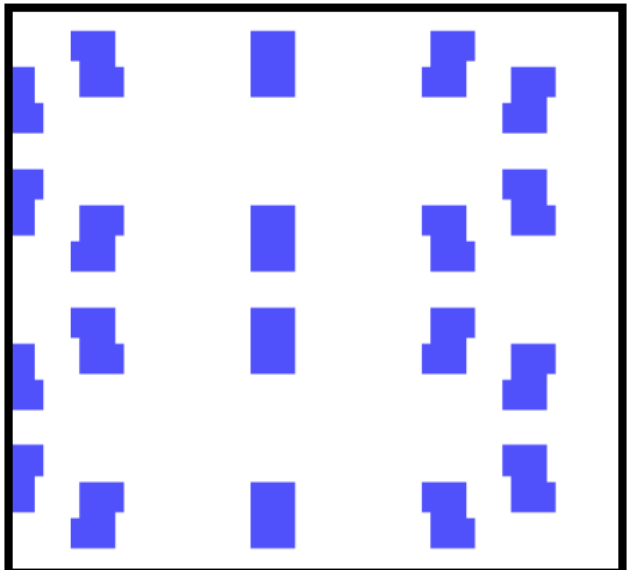
Combination OPC



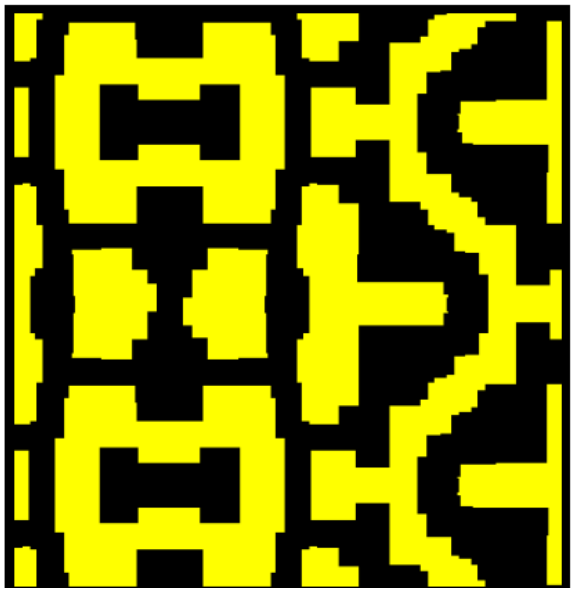
Source Mask Optimization Challenge



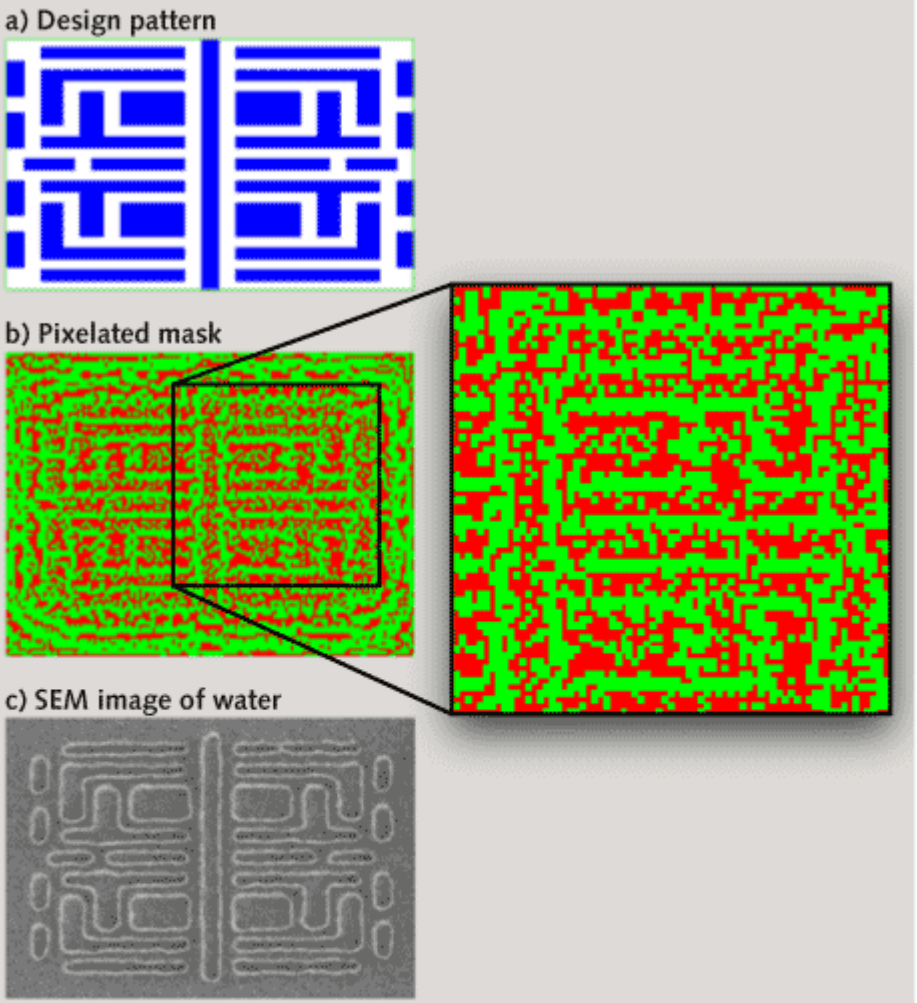
Design Layout



Mask Design



Inverse Lithography Masks



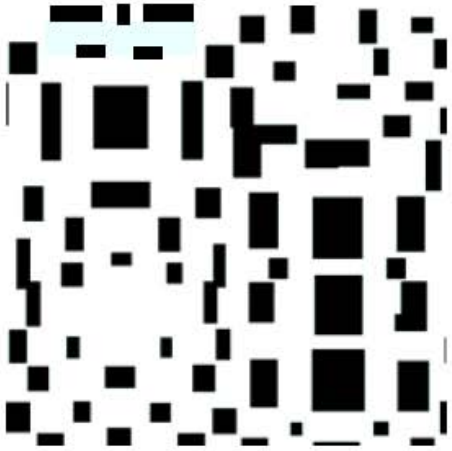
A portion of the 65nm metal 1 design (a) is converted to a pixelated phase mask design (b), where red represents 180° phase shift pits and green represents 0°, and projected by the stepper forming the resist image in (c).

WaferNews source: Intel Corp.

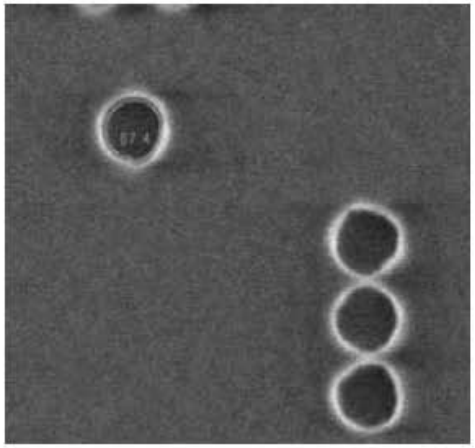
Common Solution

- Wafer Lithography?
- AIM Metrology
  - Represents real Imagery
  - Does not tell what the problem is

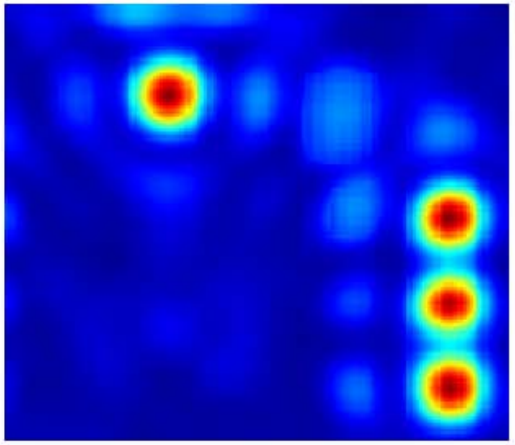
Aerial Imaging



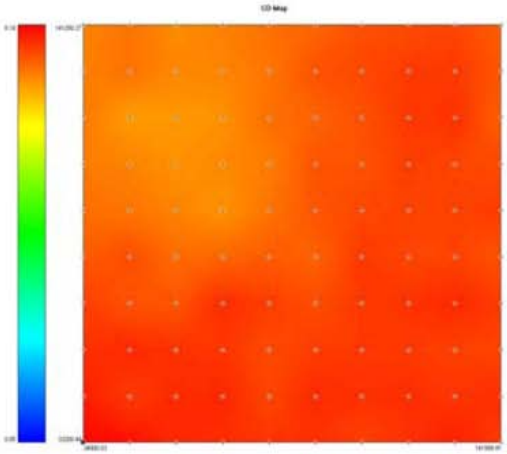
Mask Layout



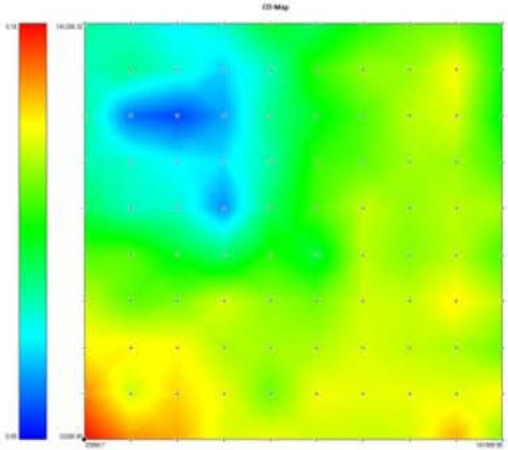
Wafer Print



Aerial Image



Setting 1: Disar Illumination
CDU = 12.5 nm (3σ @ mask)



Setting 2: Annular Illumination
CDU = 74.2 nm (3σ @ mask)

Aerial imaging
•Shows what wafer will image

But it needs Illumination to be the same as the stepper

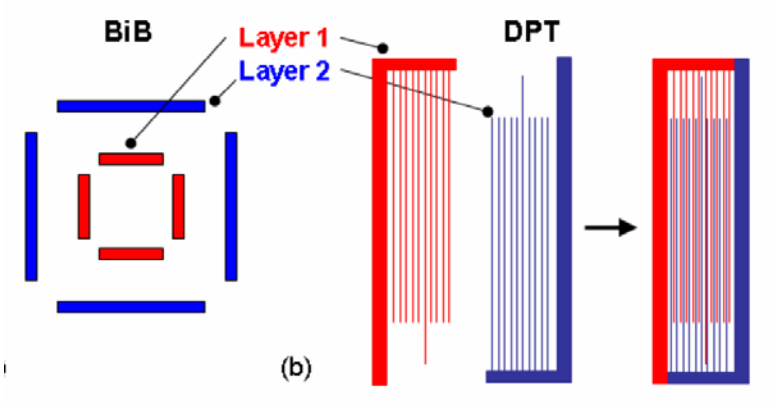
Challenges of Changing Environment

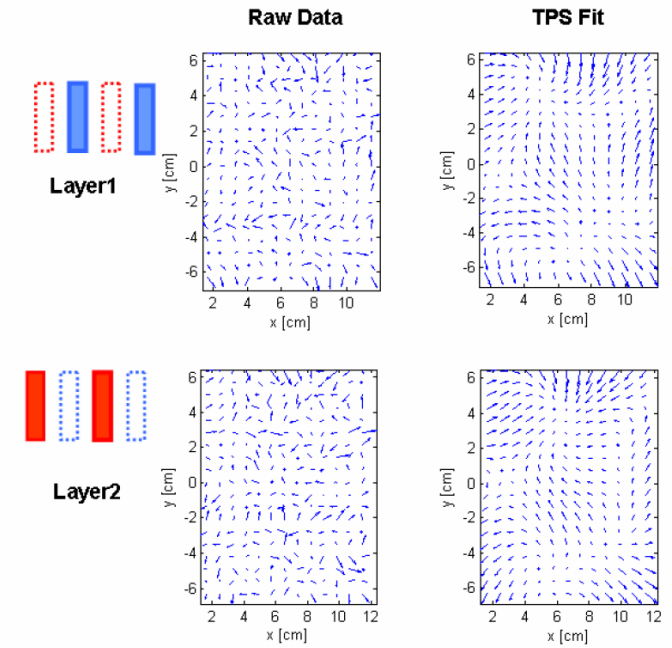
- Optical Double Patterning – Near-Term
- EUV Lithography
- Imprint Lithography

Specification Challenges

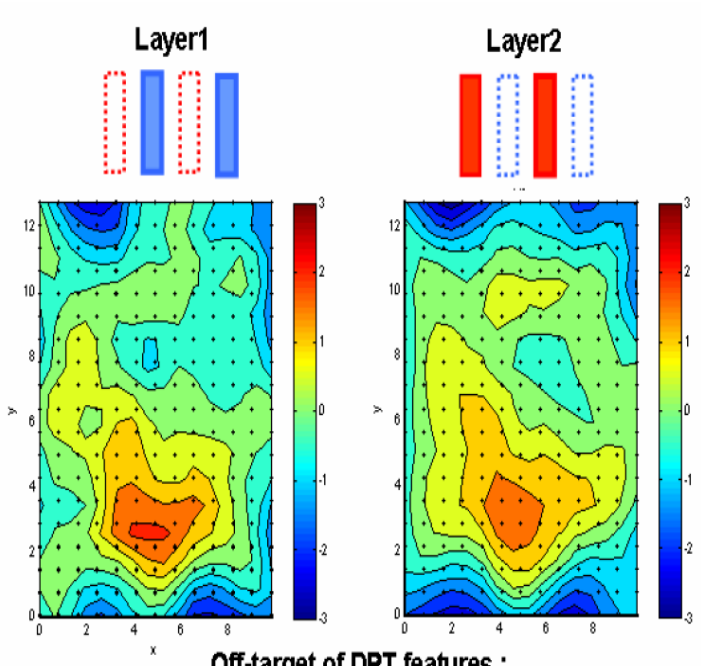
	Optical	EUVL	Imprint
Year of Production	*2013*	*2013*	*2013*
DRAM ½ pitch (nm) (contacted)	*32*	*32*	*32*
MPU Gate CD control (3 sigma) (nm) [B]	*1.4*	*1.4*	*1.4*
Overlay (3 sigma) (nm)	*6.4*	*6.4*	*6.4*
Mask magnification [B]	**4**	**4**	**1**
Image placement (nm, multipoint) [F]	**3.8**	**3.8**	**2.1**
Double exposure: dual line, image placement	**2.7 / 0.9**		
Mask minimum primary feature size [D]	**59**	**59**	**21**
Mask sub-resolution feature size (nm) opaque [E]	**42**		
CD uniformity (nm, 3 sigma) **isolated lines (MPU gates)**	**1.0**	**2.0**	**1.3**
CD uniformity (nm, 3 sigma) contacts/vias [K]	**1.3**	**3.5**	**3.9**
*Defect size (nm) [N] * (EUV I)*	**36**	**26**	**3.2**
Blank flatness (nm, peak-valley) [O]	**175**	**50**	**126**

Optical Double Patterning – Near-Term





[nm]	3σOVL	3σd1sys	3σd2sys	Rsys1/2	3σsys	3σres
x	4.7	2.1	2.4	0.84	1.3	4.5
y	5.8	3.1	2.2	0.91	1.5	5.6



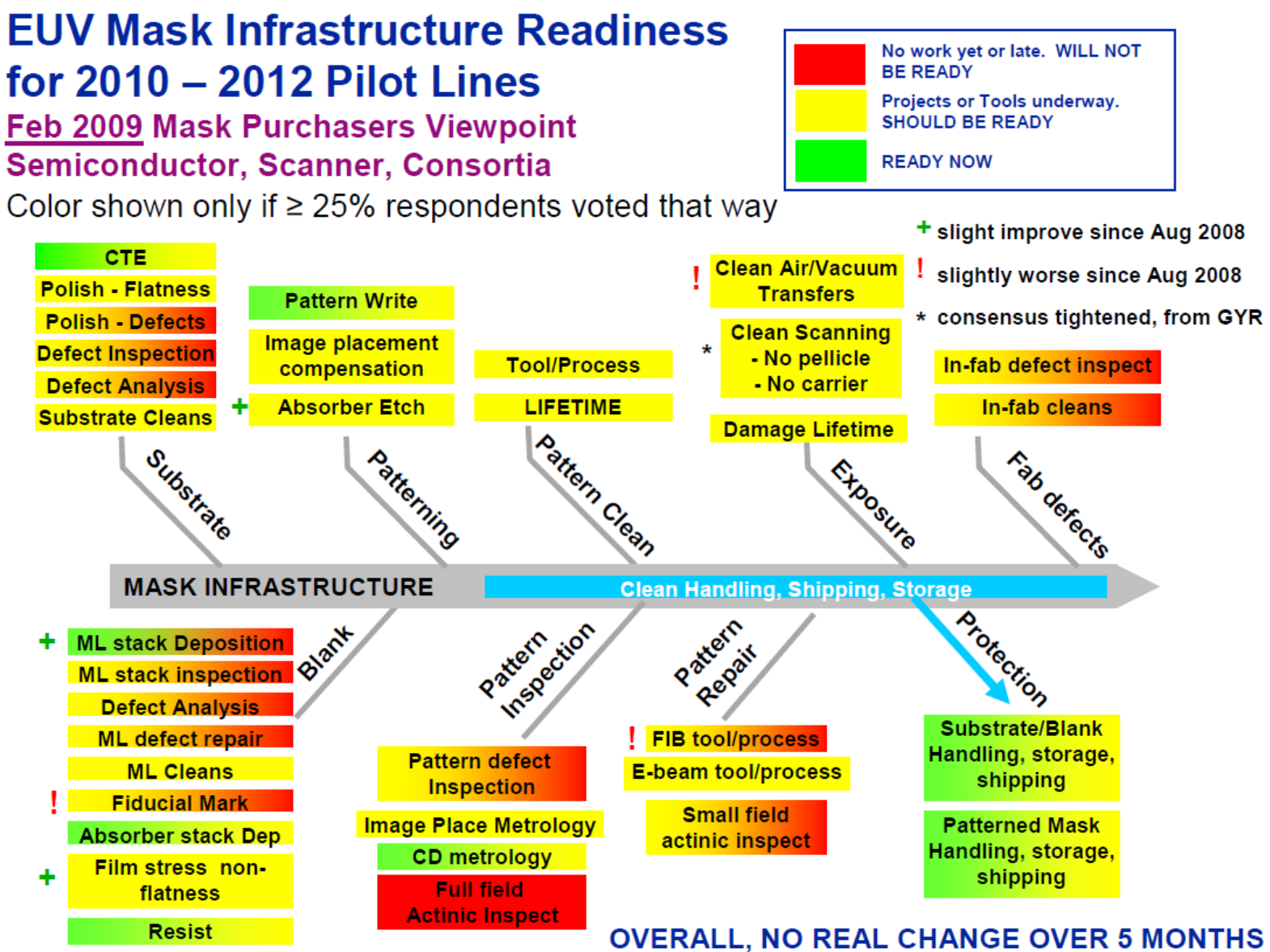
Off-target of DPT features :

Layer	Off-target (nm)	CDU (nm,3σ)
1	1.3	3.0
2	1.6	3.3

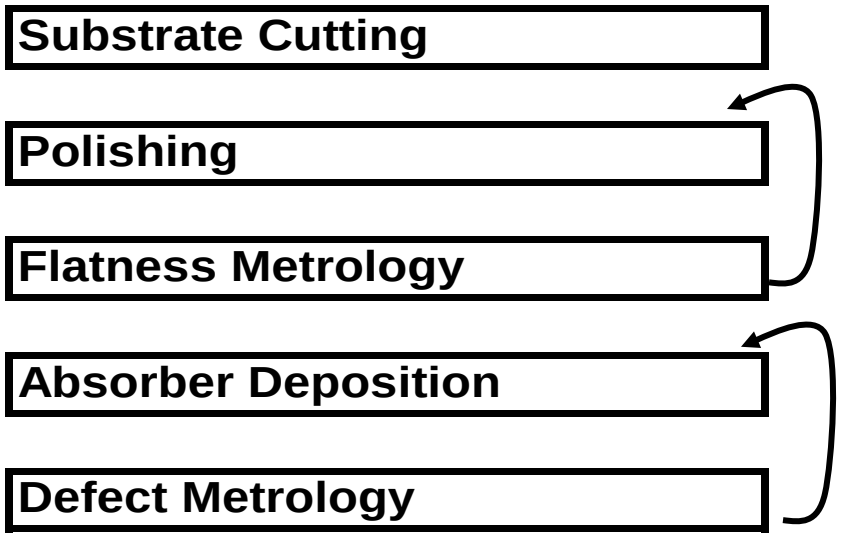
Matching of Signatures :

Correlation Coefficient	Max Deviation (nm)
0.86	1.9

EUV Lithography Challenges (ieuvi.org)



EUV Substrate to Blank Fabrication



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- Flatness
- Absorber Quality
- Defects

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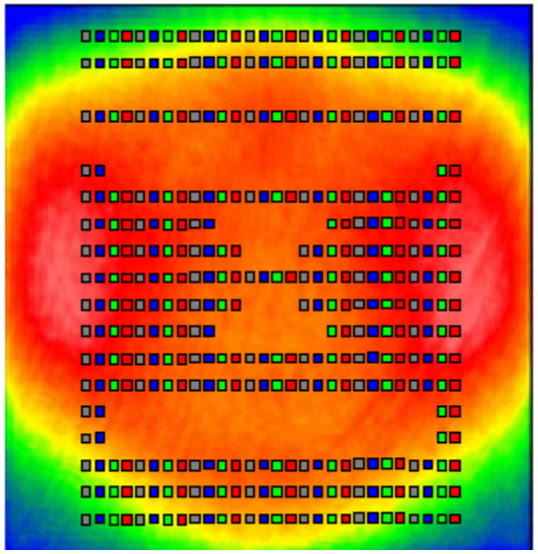
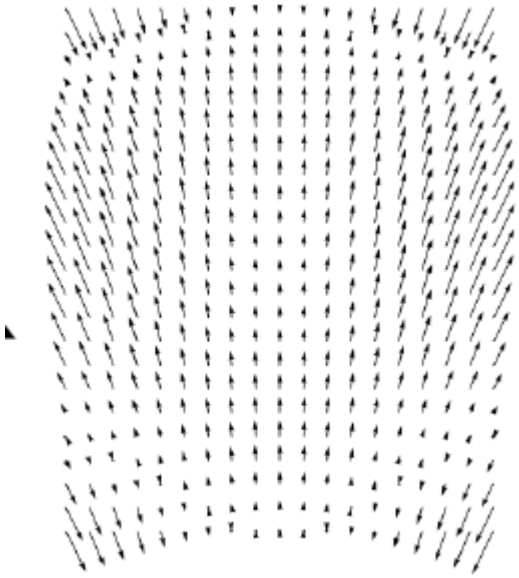
*Defect size (nm) [N] **	**36**	**25**	**18**	**13**
Blank flatness (nm, peak-valley) [O]	**165**	**117**	**83**	**59**
EUVL Mask substrate flatness (nm peak-to-valley) [O]	**46**	**32**	**23**	**16**

Flatness Thickness Metrology and Correction

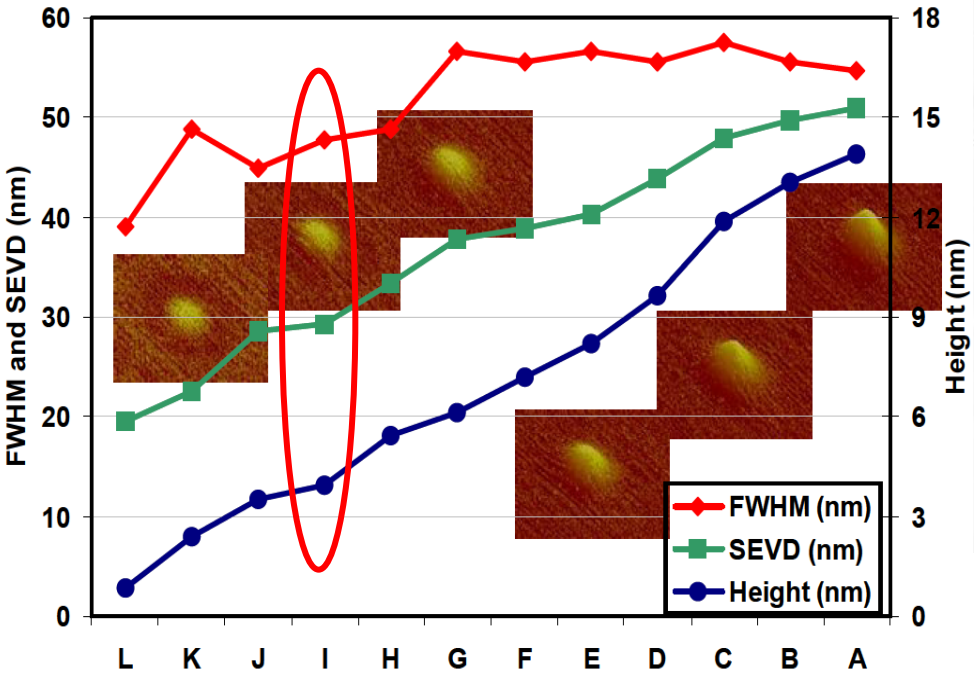
ITRS Roadmap (2007): Requirements for Masks

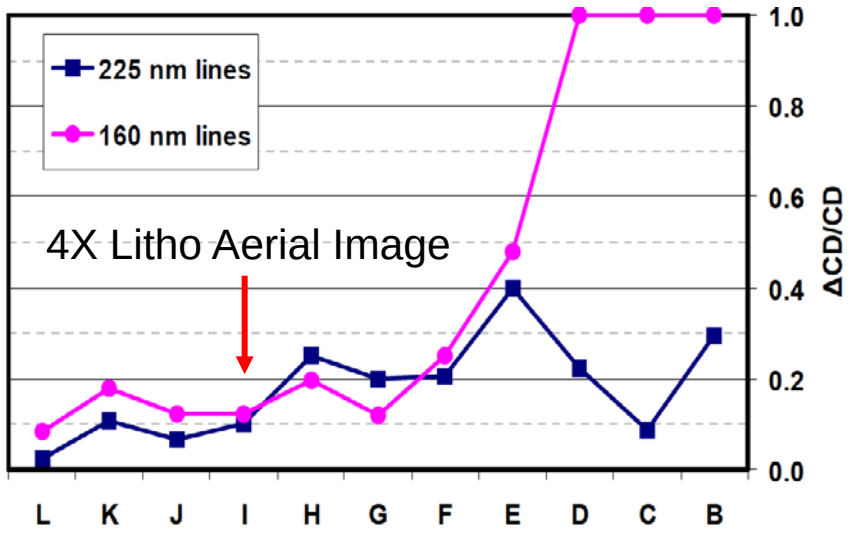
All values are on the mask	2009	2013
Required Mask Image Placement (IP)	6.4nm	3.8nm
EUV Substrate Flatness	57nm	36nm
» IP contribution from Z height	5.7nm	3.6nm





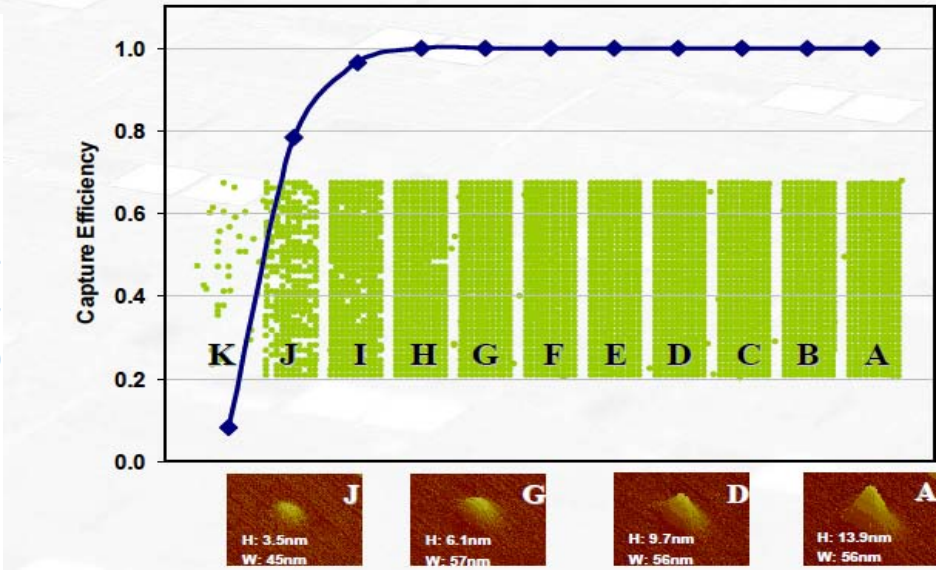
40 nm L/S EUV Litho





EUVL Capture with Lasertec 7360

Down to 3.5 nm high / 45 nm wide defects on ML.



Year of Production	*2007*	*2010*	*2013*
DRAM/ MPU ½ pitch (nm)	*68*	*45*	*32*
*Pattern Defect size (nm) [N] **	**55**	**36**	**25**
EUVL Substrate defect size (nm)		**37**	**32**
EUVLsubstrate flatness (nm ptv)		**46**	**32**

Key Take-away Points

- Metrology is the key to process control and improvement –
  - Stability of process and metrology key to improving
- Metrology of the real device pattern drive performance
- Addressing the needed metrology of the future is key to meeting the future needs
- Metrology is not only an enabler; it is a necessity

Thanks

- SEMATECH Mask & EUV Group
  - Yun, Cha, Sohn, Linn, Gabella, Litt
- Commercial Mask and Blank manufacturers
  - Toppan, Photonics, DNP, Hoya, AGC