In-line, Non-destructive Electrical Metrology of Nitrided Silicon Dioxide and High-k Gate Dielectric Layers

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SSM®

Electrical Characterization for MOS

- Device performance depends heavily on electrical properties of MOS structure
  - Bias dependence
  - Current dependence

- Atomic Profiles(SIMS), physical measurements(TEM) and optical measurements(Ellipsometry) do not correlate to final device behavior as well as electrical measurements

- Electrical data can be used for
  - Rapid monitoring of semiconductor processes
  - Monitoring Product Wafers
  - Predicting device performance
  - Determining reliability issues

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Primary Parameters

- Gate Engineering
  - On-state Drive Current
    - Capacitance Effective Thickness(CET)
    - Equivalent Oxide Thickness(EOT)
    - Effective Dielectric Constant
  - Off-state Leakage Current
    - Gate Leakage Current(I_{LK})
  - Interface Trap Density(D_{IT})
  - Gate Dielectric Charge and Stability
  - Current-Voltage Behavior
    - Current Transport Mechanisms
      - Current-Voltage(IV) Profile
    - Stress Induced Leakage Current(SILC)
    - Reliability
      - Time Dependent Dielectric Breakdown(TDDB)
      - Time Zero Dielectric Breakdown and Defect Density
  - Alternate High-k Dielectrics

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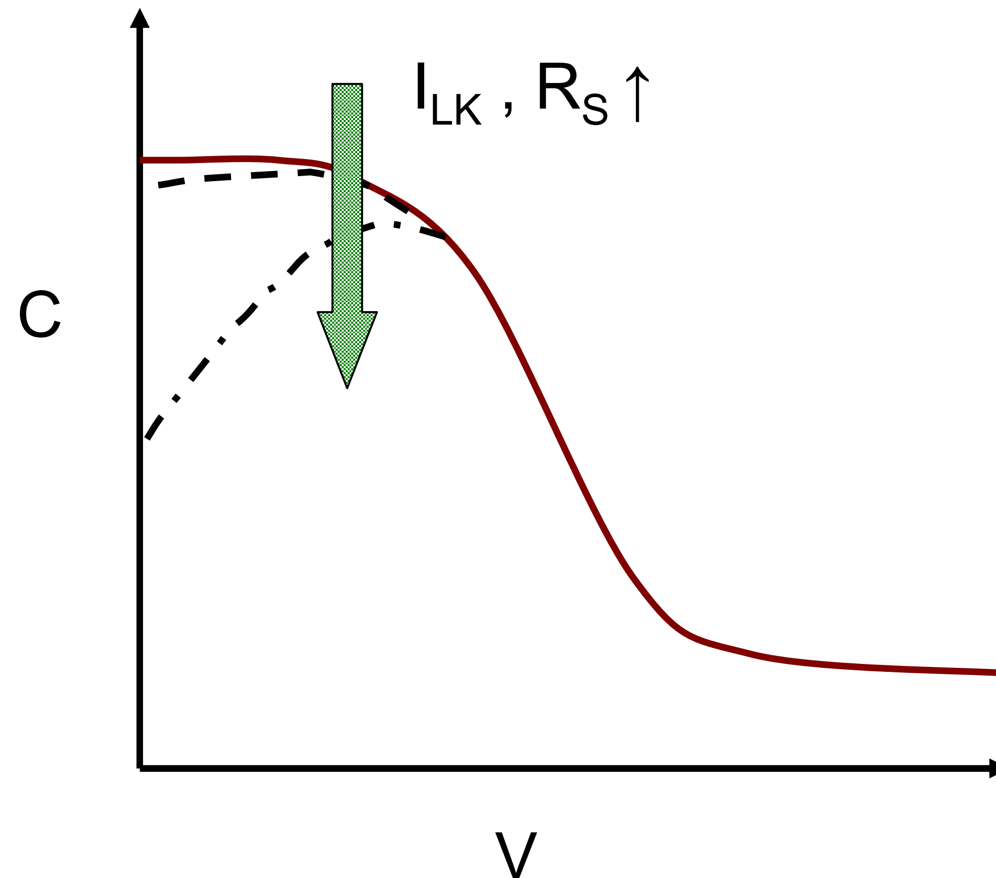
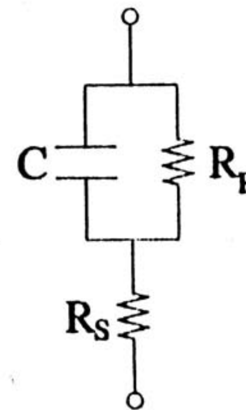
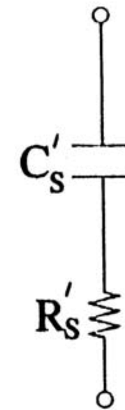
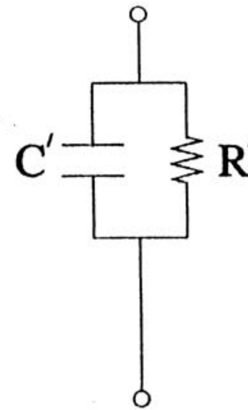
Ultra-thin (<3 nm) Leakage Effects on CV



- Modeling Approach:
  - Henson, EDL-20, Apr (1999)
  - Choi, EDL-20, June (1999)
- Dual Frequency Approach:
  - Yang, TED-46, July (1999)







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Multi-frequency CV Dispersion

EM-gate Multi-frequency Comparison
Thin High K HfO_2

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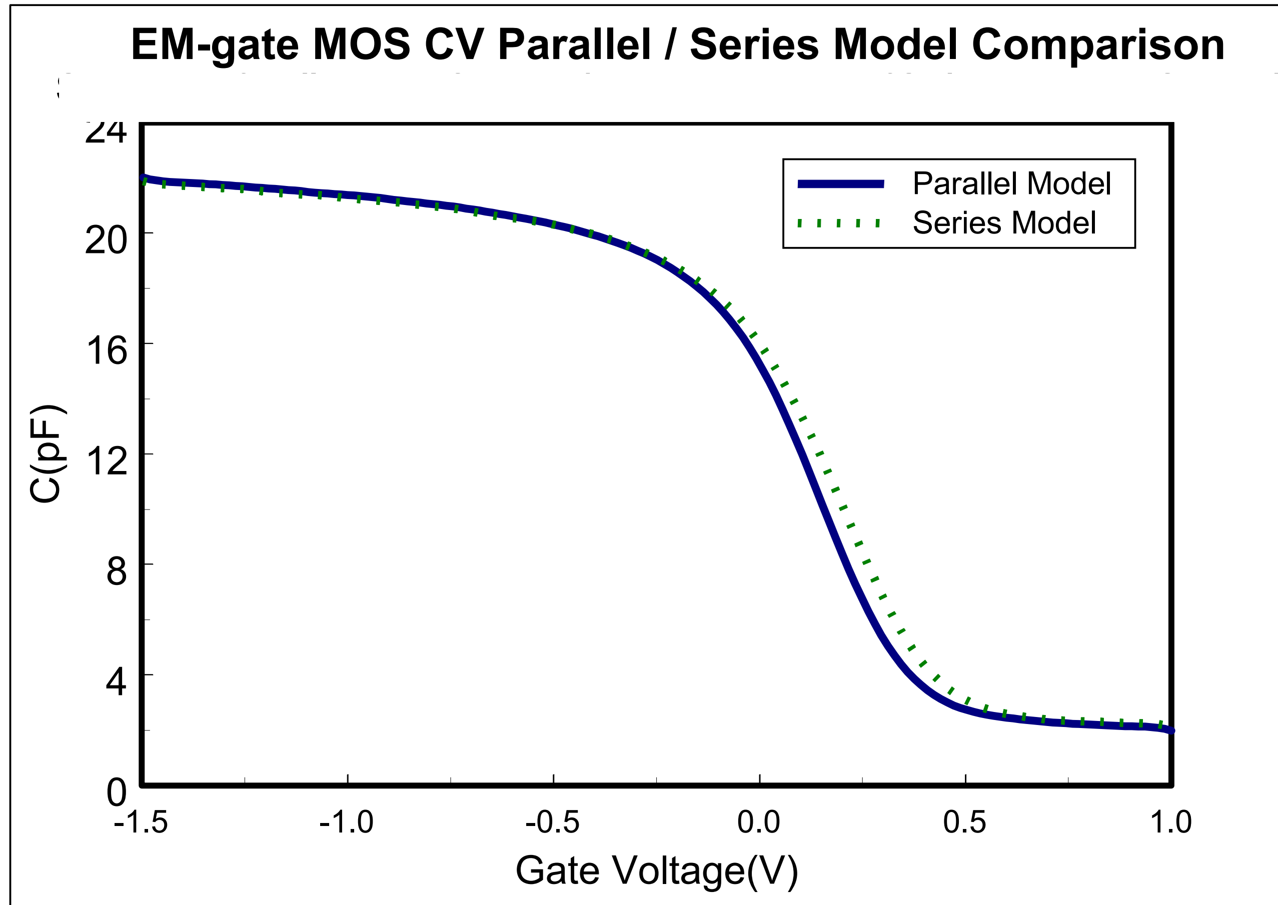
Series/Parallel Model Comparison



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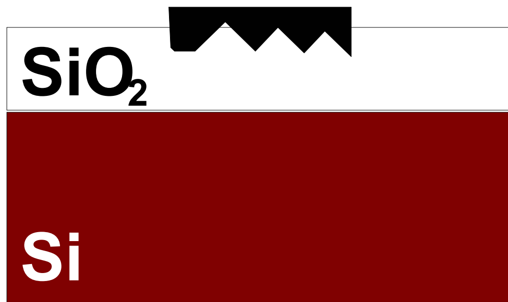
Evolution of Alternate Gate Formations

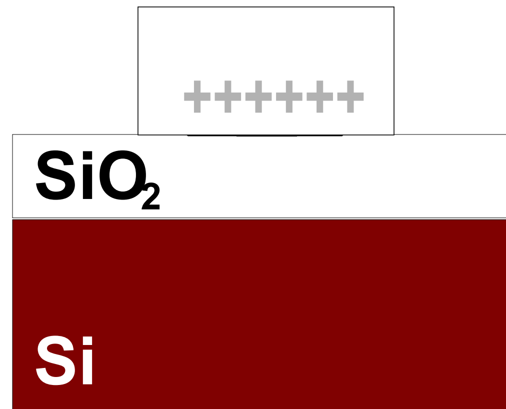
Poly Gate



Conventional Method:

1. MOS gate formed by depositing polysilicon
2. Gate formation time: 6 hours to days
3. Processing required to form gate
4. For monitor wafers only

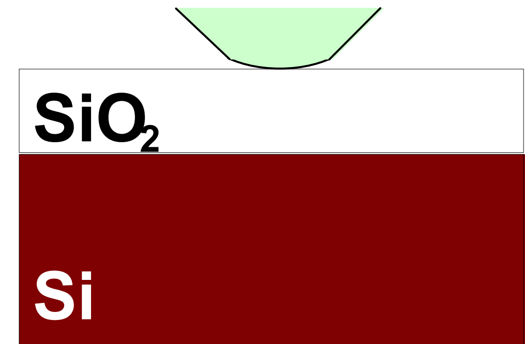
Corona Biasing



Introduced in 1995:

1. COS gate formed through deposition of corona charge
2. charge formation time: 5 min. for 1 Q-V sweep.
3. Smallest test area: 5 mm diameter
4. For monitor wafers only

EM-gate



1. MOS gate formed through elastic deformation of non-invasive probe.
2. Gate Formation Time: 2 seconds
3. Small diameter gate for scribe line positioning
4. Measures Product Wafers

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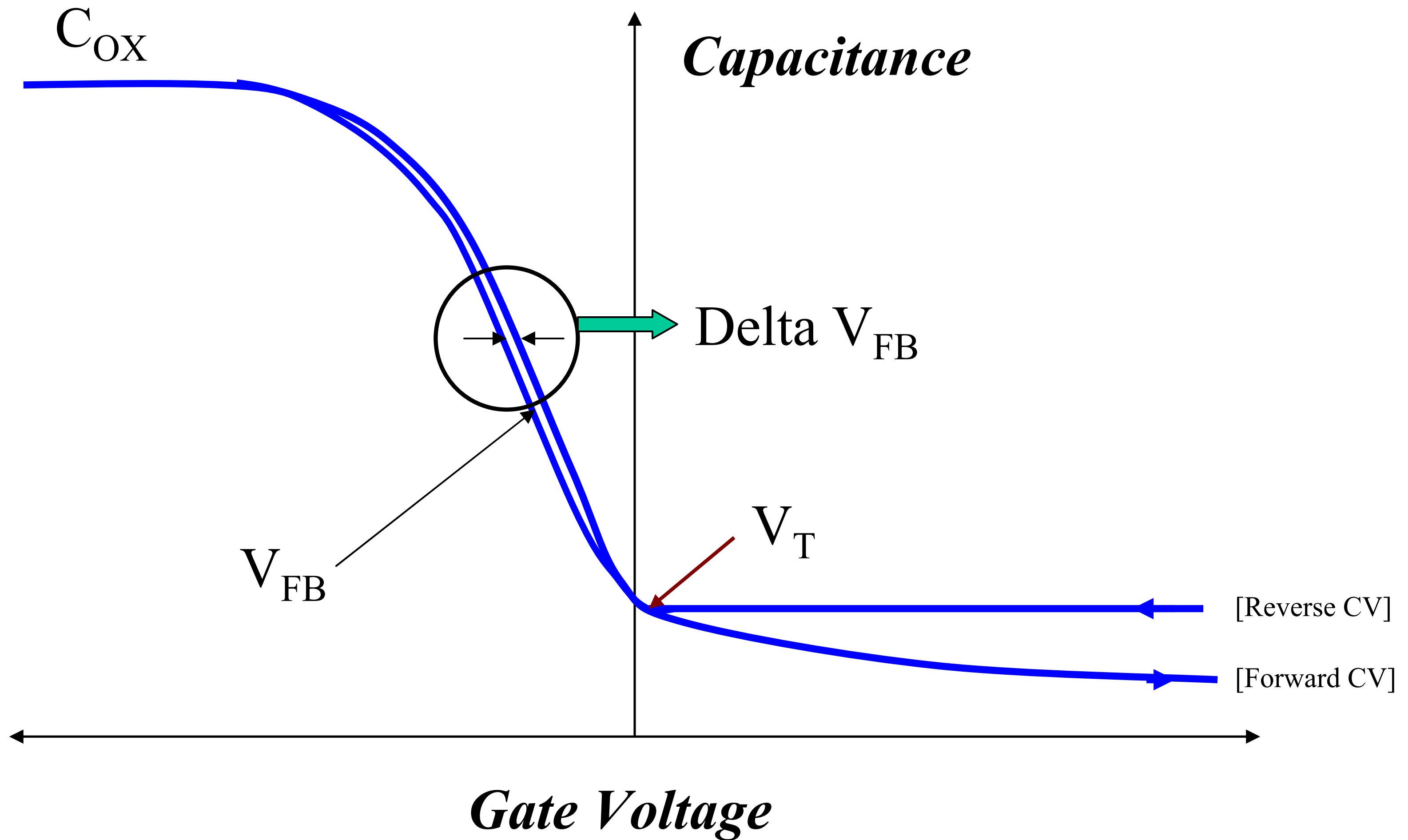
High Frequency MOS CV Curve



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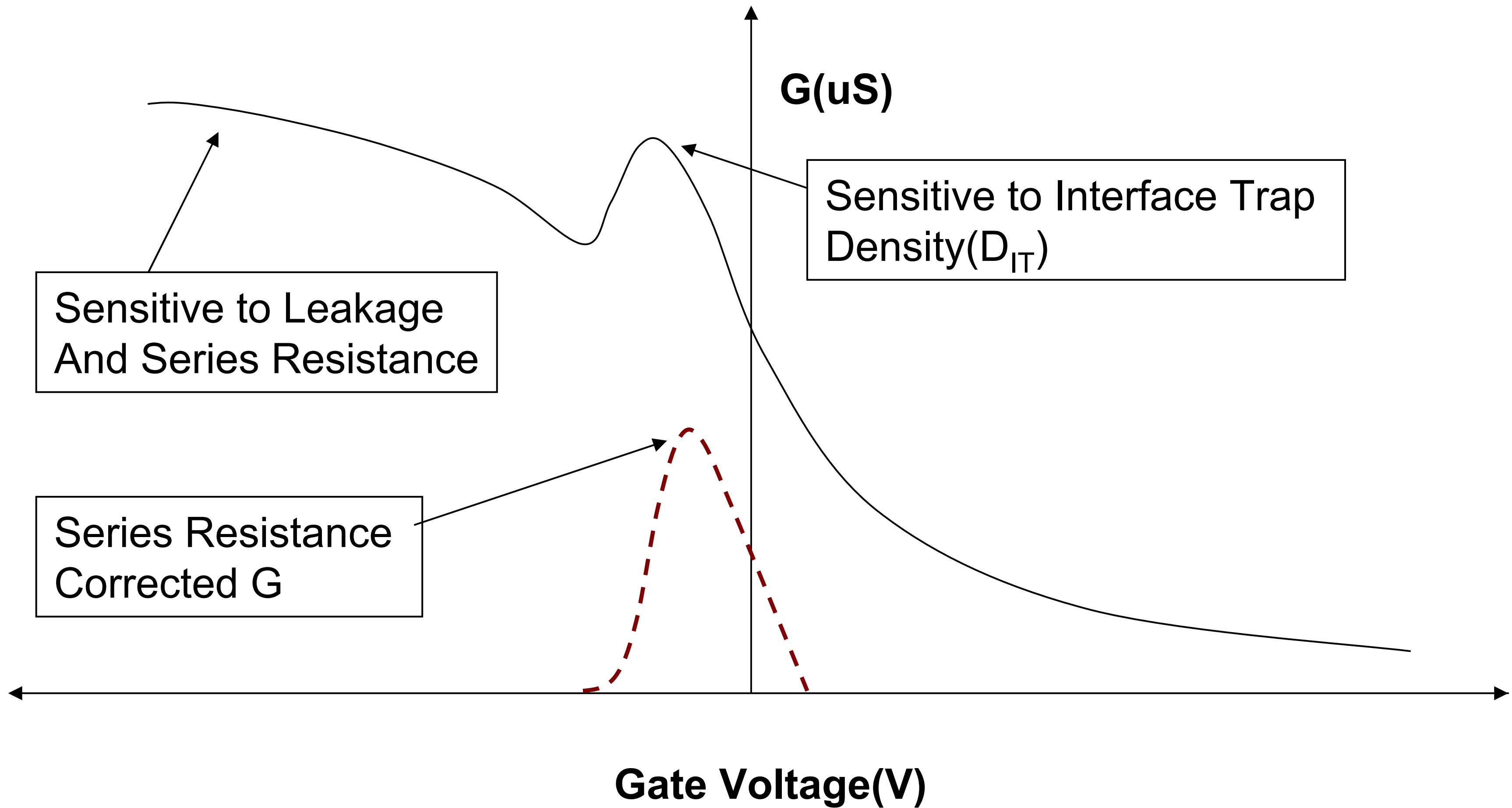
Conductance-Voltage(GV) Curve



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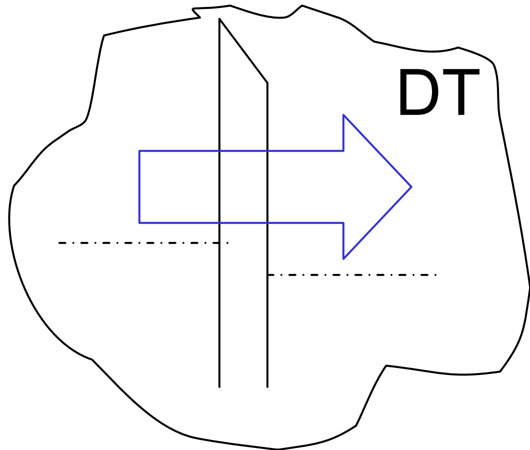
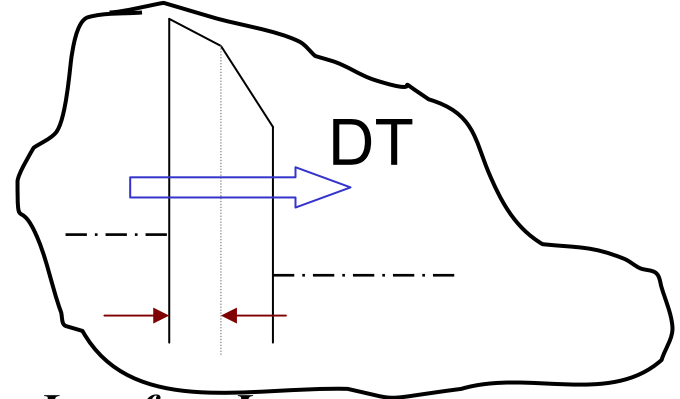
Calibration: Contact Models





Interface Layer

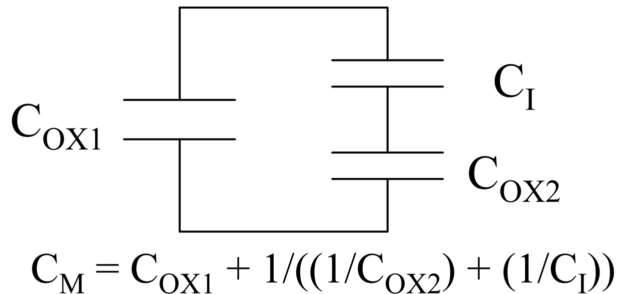
Metal Probe

Metal Probe

SiO_2

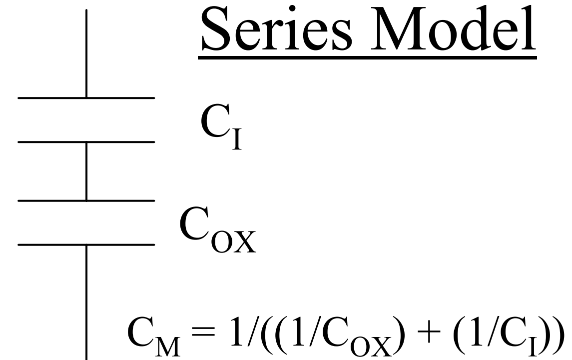
SiO_2

Series/Parallel Model



$C_M = C_{OX1} + 1/((1/C_{OX2}) + (1/C_I))$

Series Model



$C_M = 1/((1/C_{OX}) + (1/C_I))$

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CET Short Term Repeatability

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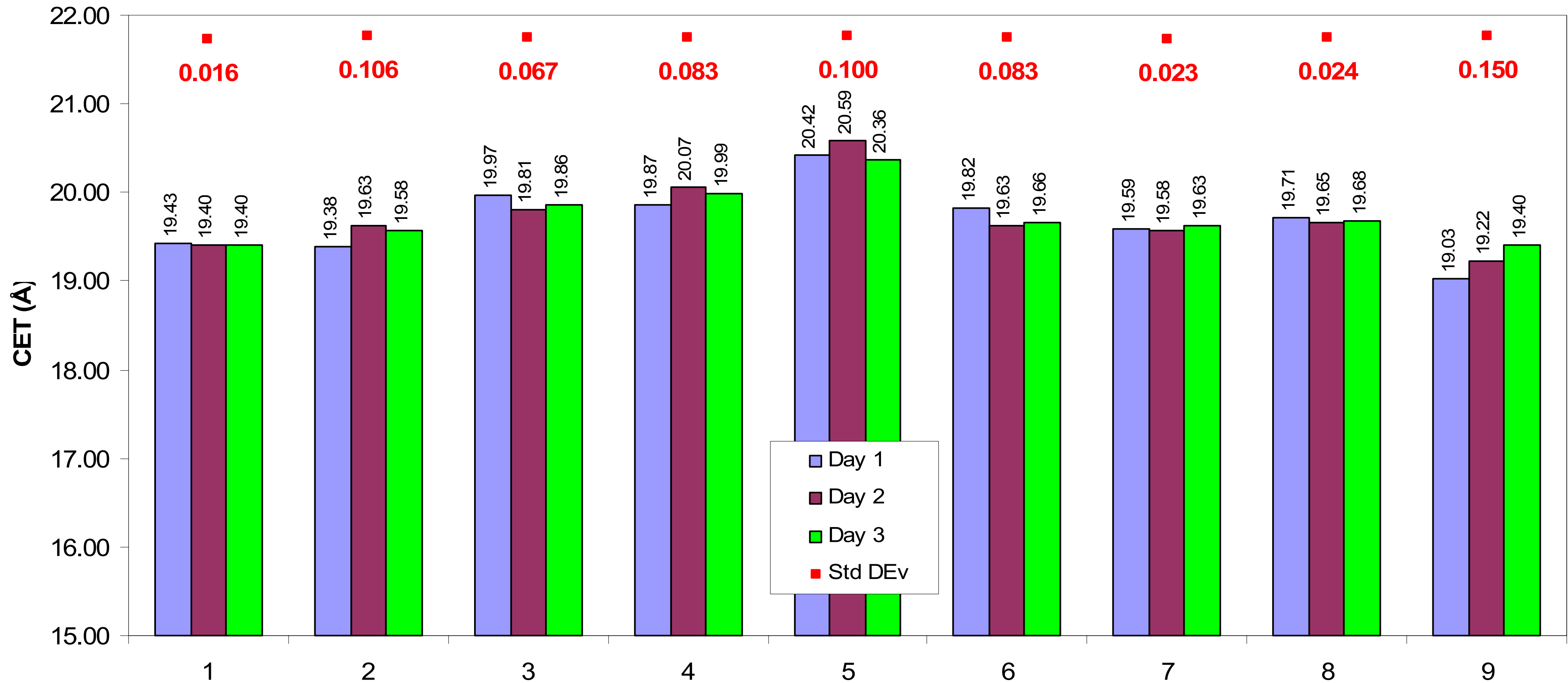
EM-gate Repeatability

- **Short Term**
  - CET: <0.1 Ang.
  - VFB: ~ 6 mV
  - DIT: ~ 1 %

- **Multiple Day**
  - CET: ~0.1 Ang.
  - VFB: ~12 mV
  - DIT: ~ 2 %



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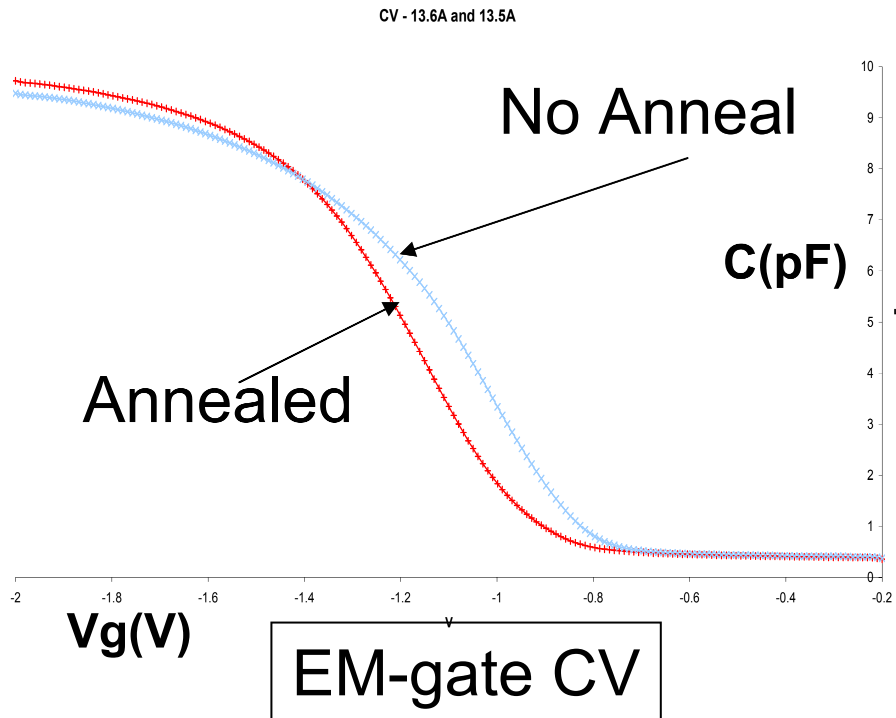
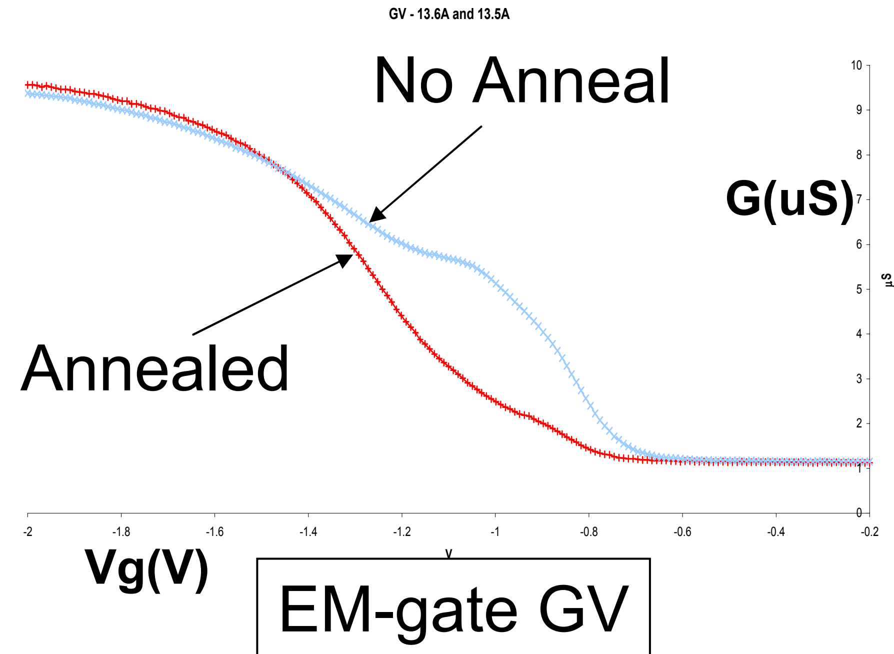
EM-gate CV and GV: ~13.5 Ang. SiO_2





- Un-annealed Oxides Exhibit lower C_{OX} , Higher D_{IT} and V_{FB} Shift
- No Leakage Effects Present

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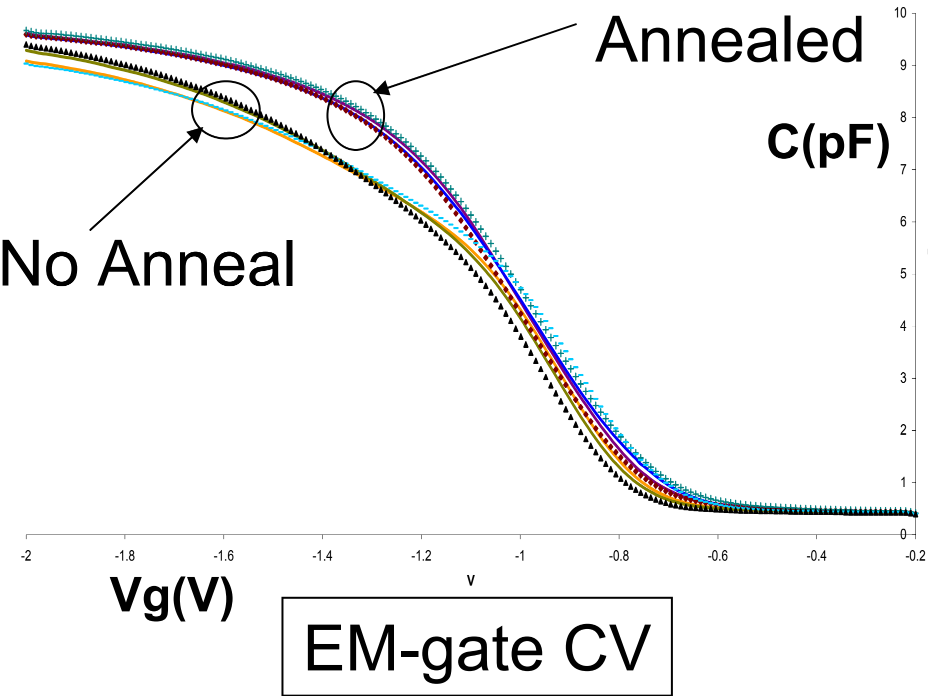
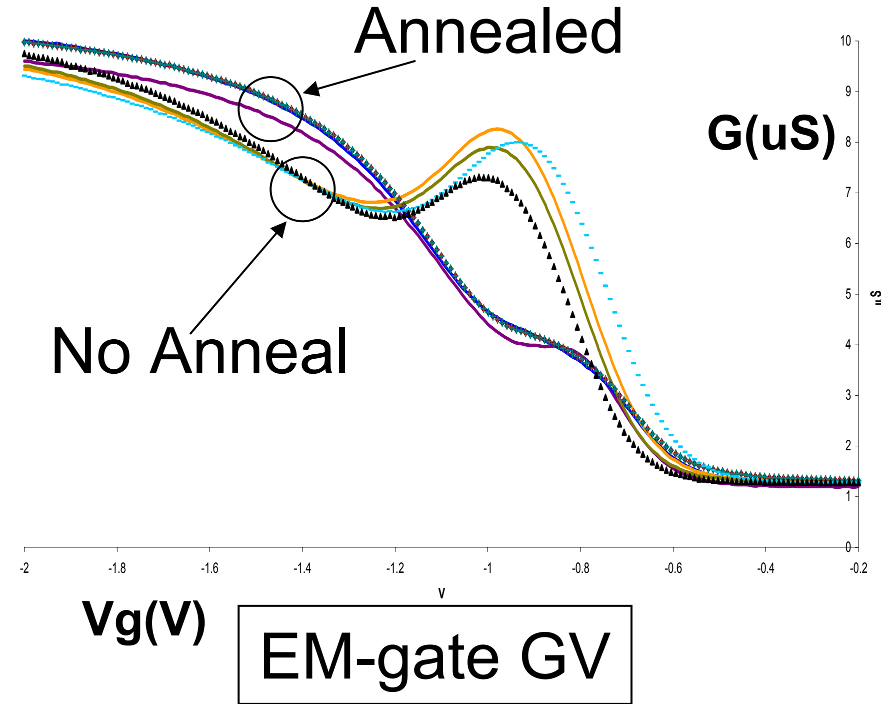
EM-gate CV and GV: < 20 Ang. SiON





- Un-annealed Oxides Exhibit lower C_{OX} , Higher D_{IT} , V_{FB} Shift and Distortion in CV Curve
- No Leakage Effects Present

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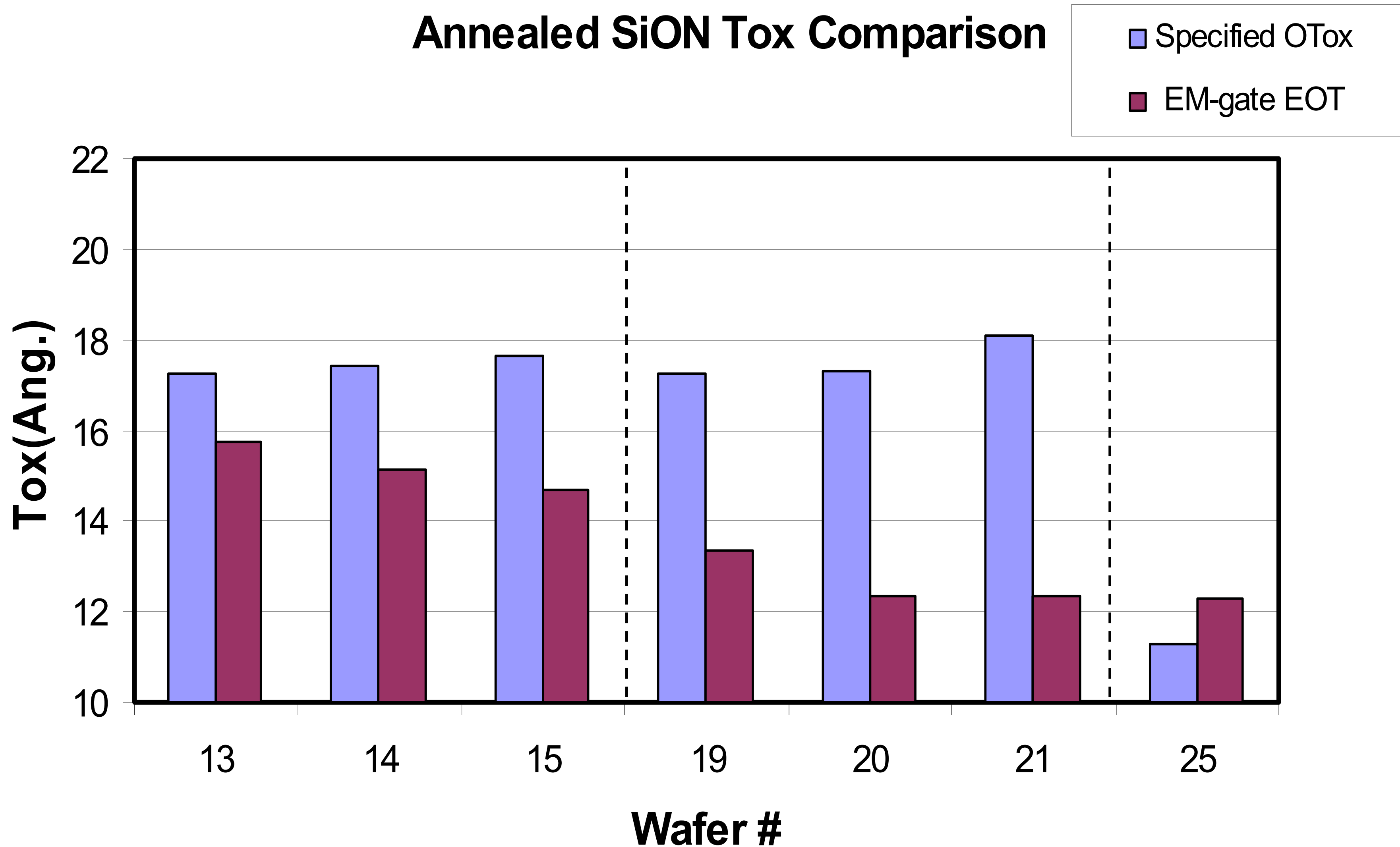
EM-gate CV: EOT Comparison



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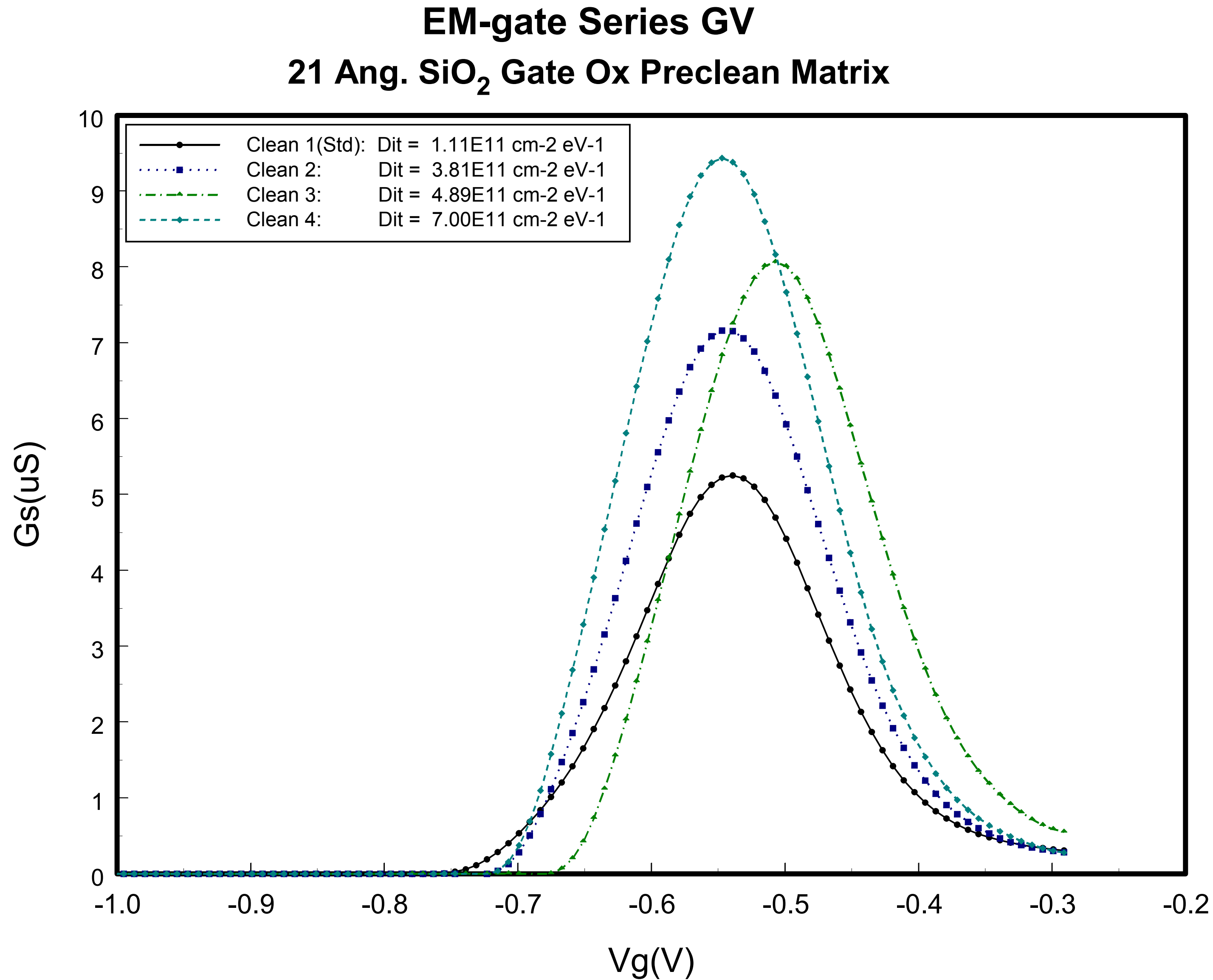
EM-gate GV Comparison: 21 Ang. Oxides



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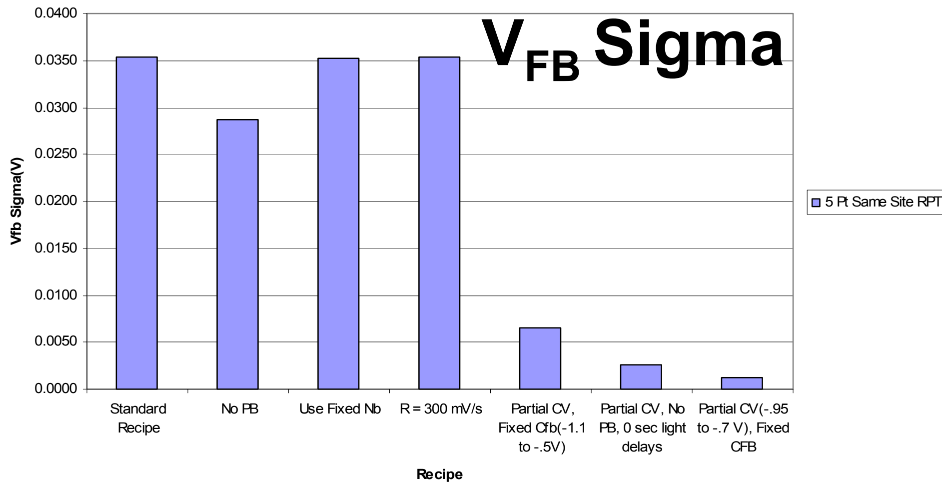
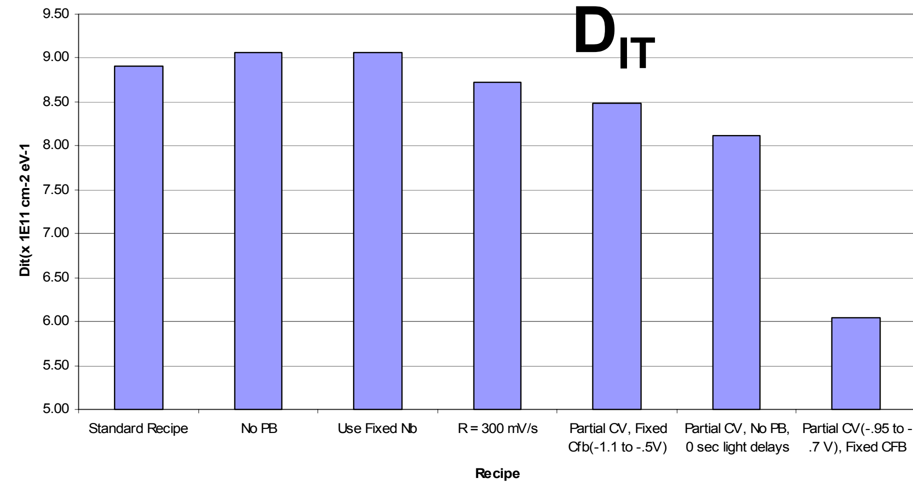
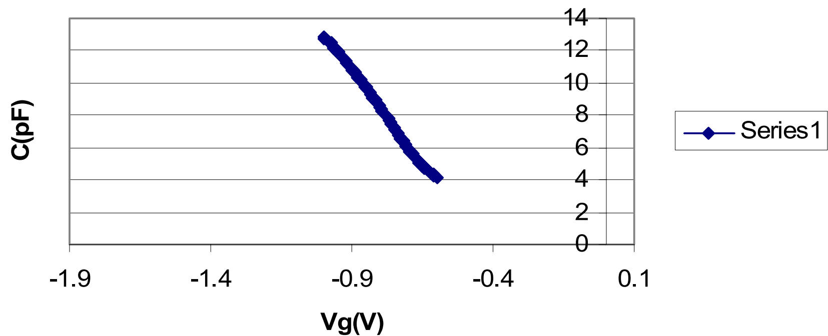
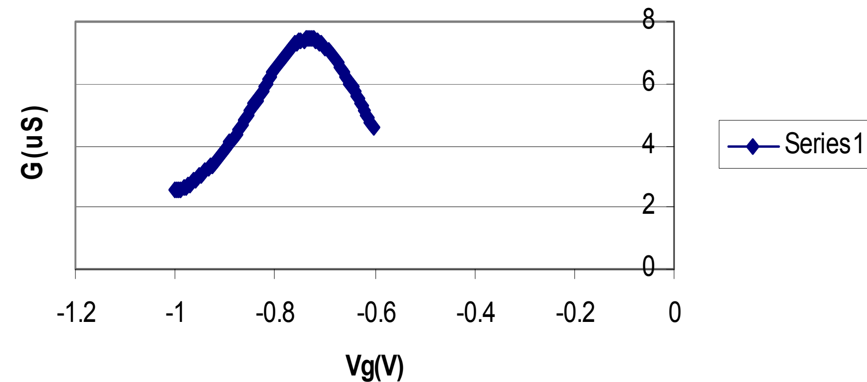
Effects of Electrical Stress on Vfb









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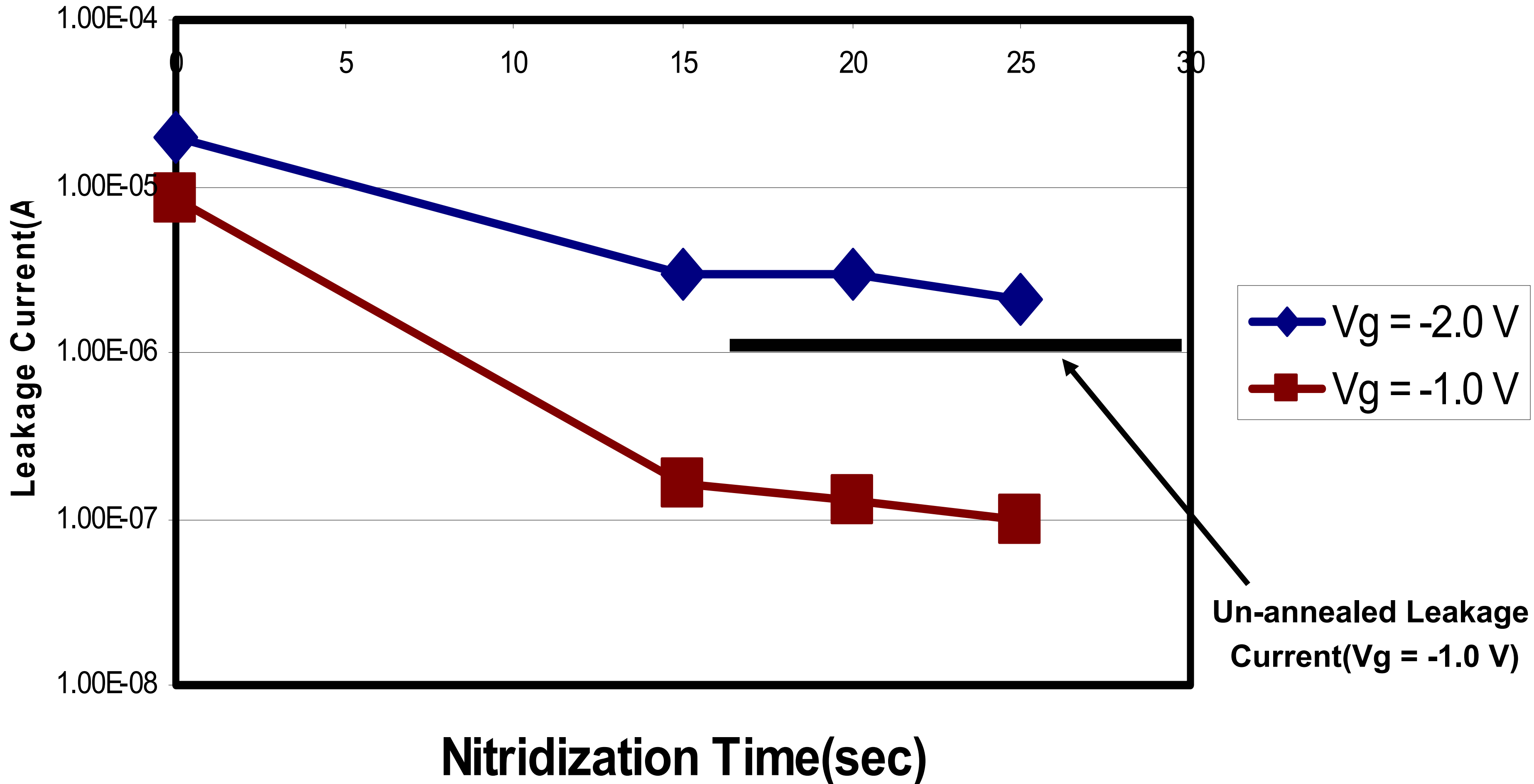
MOSCAP IV: SiON Leakage Current Comparison



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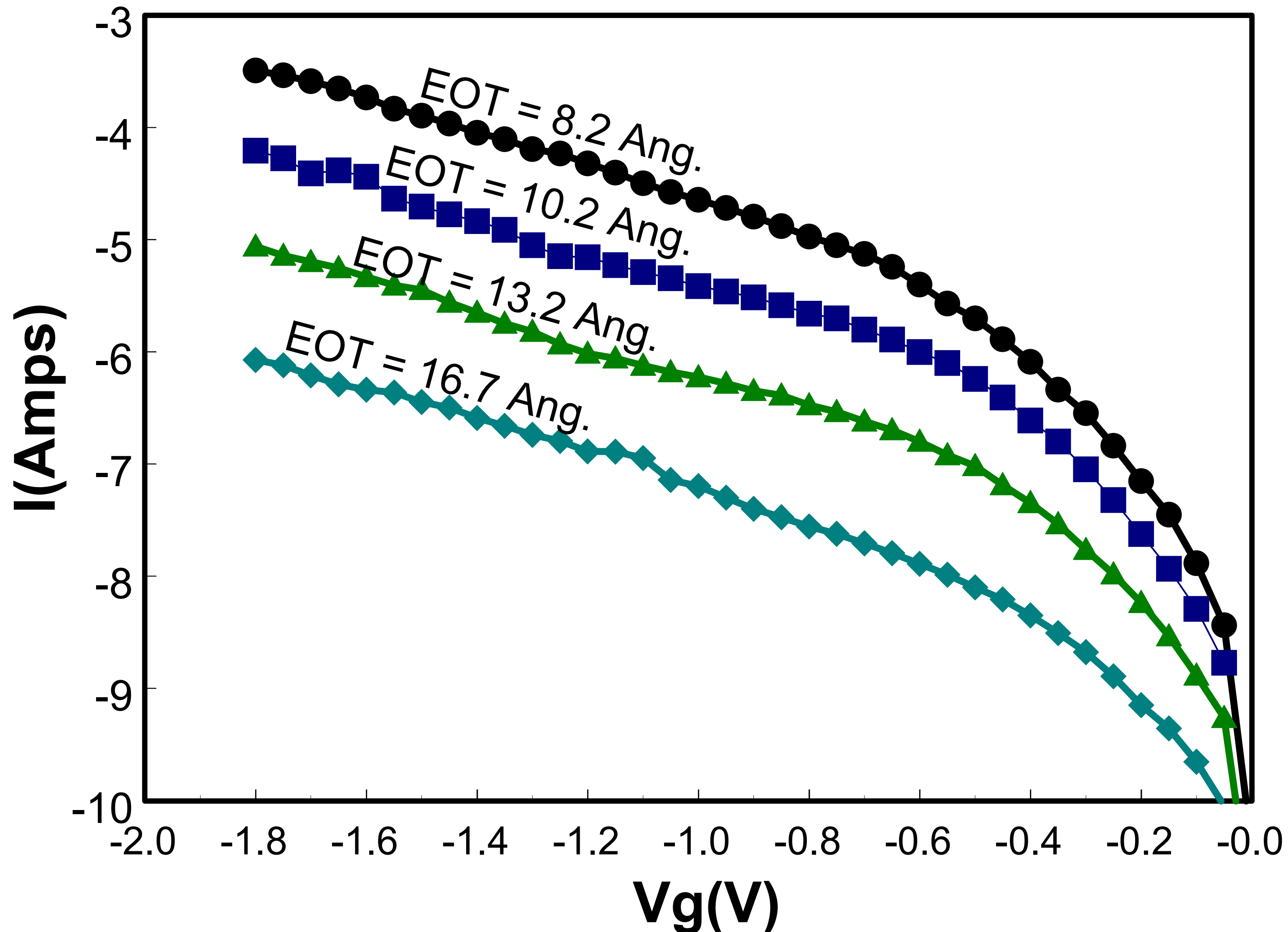
MOSCAP IV Example A: 8 to 17 Ang. SiO_2



EM-gate IV Example A: 8 to 17 Ang. SiO_2 & SiON

EM-gate Leakage Current, (Vg = -1.8 V)
50 % Cumulative Probability for SiO2 & SiON groups

1.E-03
1.E-04
1.E-05
1.E-06
1.E-07
1.E-08

5
10
15
20

Leakage Current(Amps)

slot 1
slot 2
slot 8
slot 4
slot 3
slot 5
slot 6
slot 7

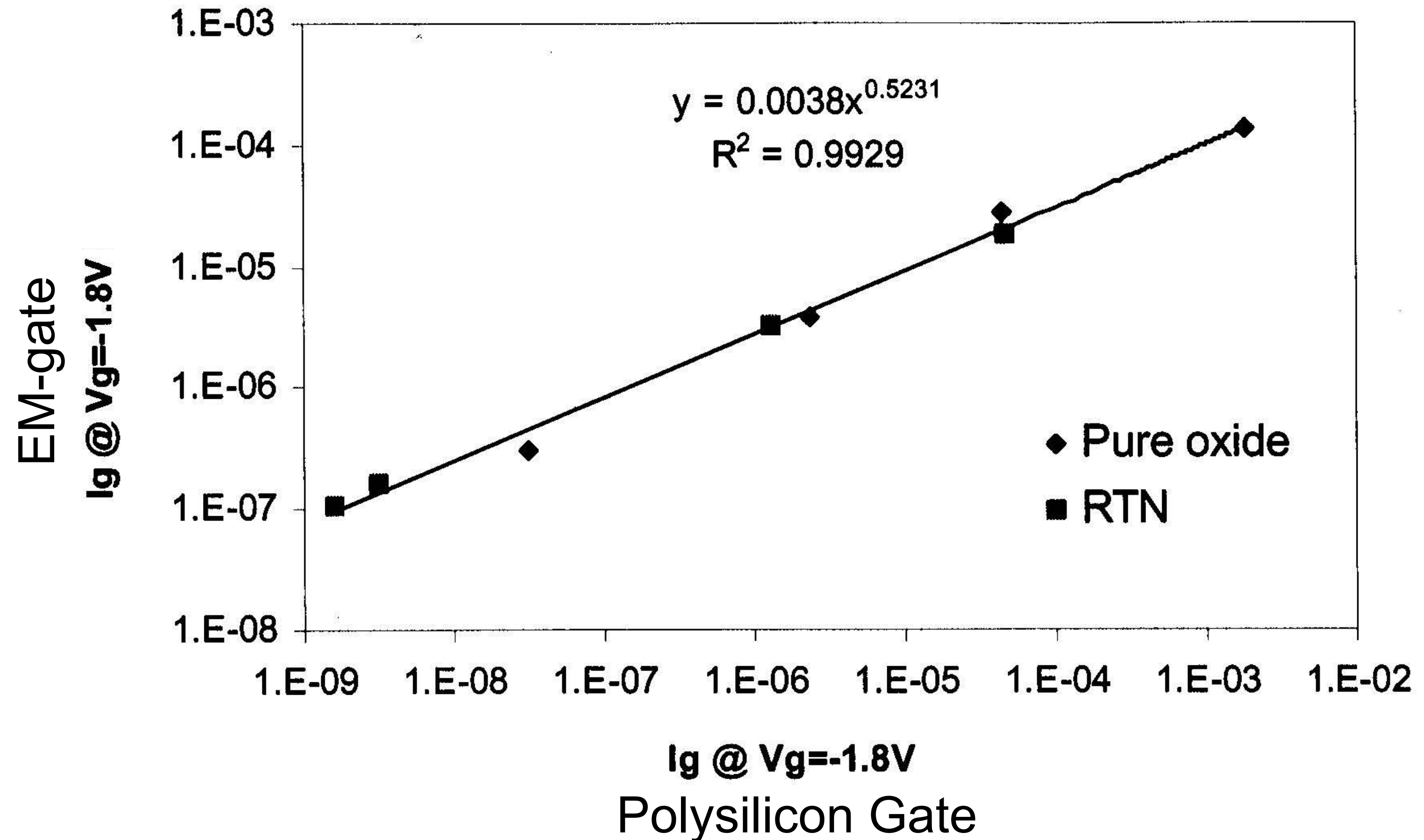
$y = 0.0269e^{-0.6921x}$
$R^2 = 0.9988$
(3.33 Ang./Decade)

$y = 0.0388e^{-0.6548x}$
$R^2 = 0.9975$
(3.52 Ang./Decade)

SiO2 SiON Expon. (SiO2) Expon. (SiON)

OTox(Ang.)

EM-gate vs Polysilicon Gate IV Leakage Correlation



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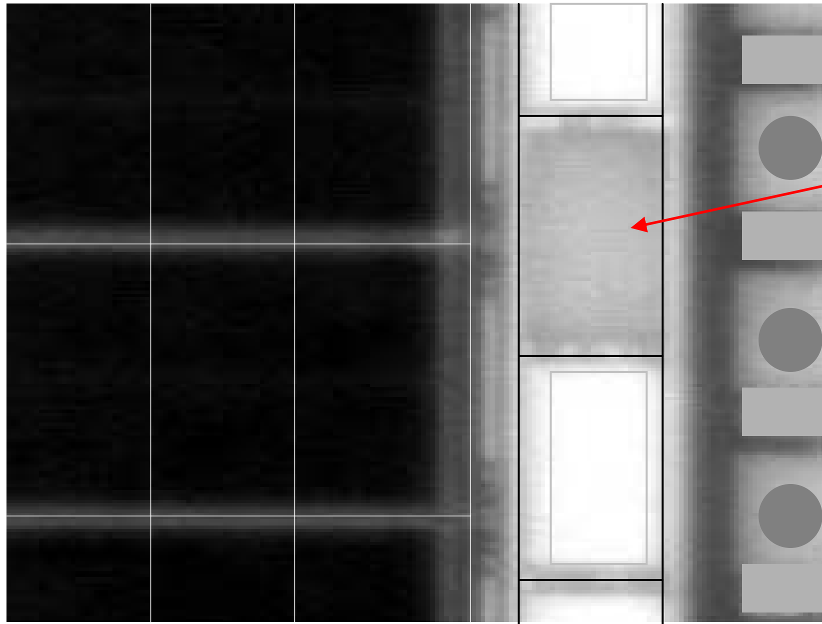
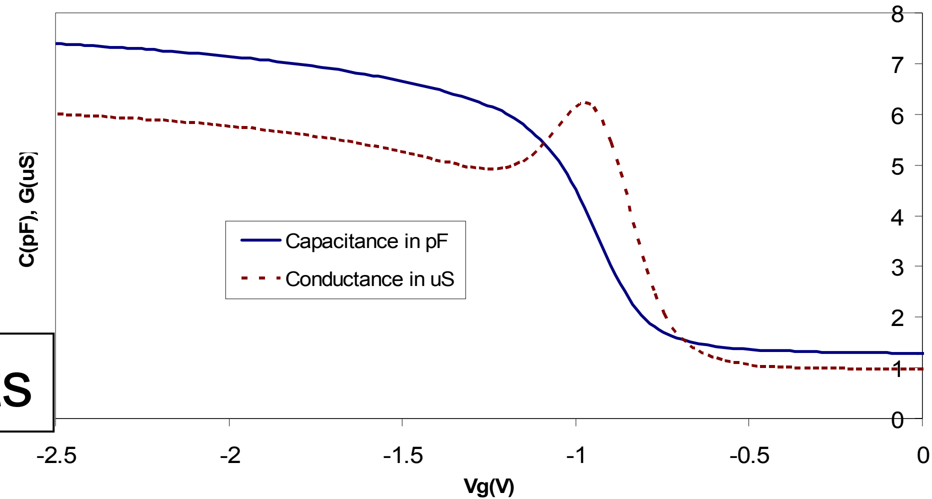
EM-gate CV, GV: Scribe Line Test Areas on Patterned Wafer



80 µm x 120 µm Test Area

CMOS Product Wafer

CV and GV Measurements



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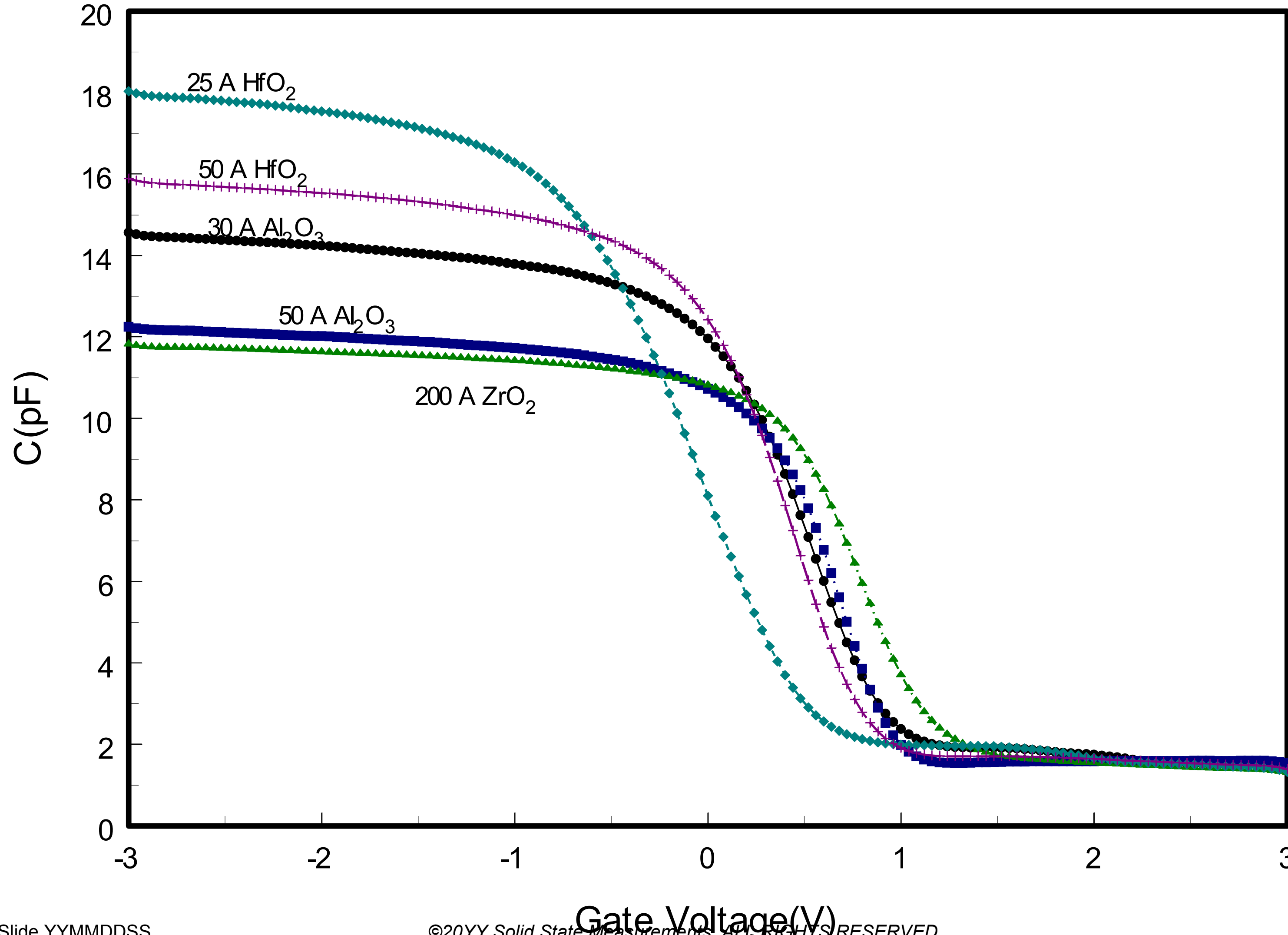
EM-gate MOS CV: High k Dielectrics



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Summary

- FastGate^{TM} Technology
  - Is Rapid(60 Wafers/Hr)
  - Is Repeatable
  - is Non-damaging and non-contaminating
  - Can measure Oxides and Oxynitrides as thin as 7 Ang.
  - Can measure Product Wafers
- EM-gate CV and IV Capability Includes
  - CET, EOT
  - V_{FB} and $V_{T,CV}$
  - D_{IT}
  - Delta V_{FB} Hysteresis
  - N_{SURF} and Carrier Density Profile
  - Leakage Current
  - IV Profile
- Applications on thin SiO_2 , SiON with EOT values between 8 Ang. and 20 Ang. have been shown

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