Nanoelectronics and *More-than-Moore* at IMEC

M. Heyns

IMEC Fellow

Moore's Law
In 1965, Intel co-founder Gordon Moore predicted that the number of transistors on a piece of silicon would double every couple of years—an insight later dubbed "Moore's Law." His prediction has held true, as ever-shrinking transistor sizes have allowed exponential growth in the number of transistors on a single chip.
1962
1965
1970
Relative Manufacturing Cost per Component
10^4
10^3
10^2
10
1
1
10
10^2
10^3
10^4
10^5
Number of Components per Integrated Circuit
Cost scaling
Improved performance

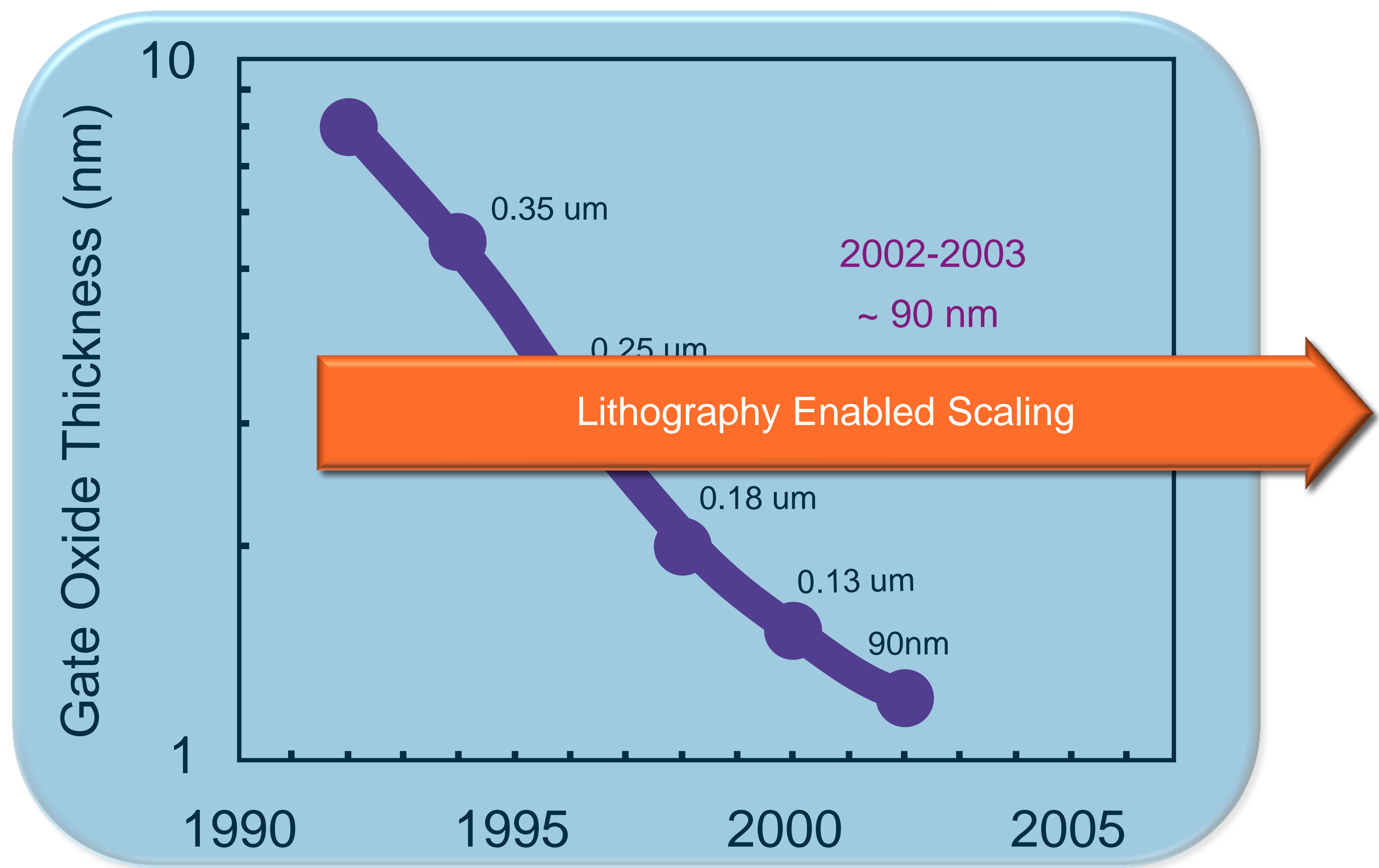
Node-to-Node Transistor scaling requires:

- 50% area reduction
- 25% performance increase @ scaled V_{dd}
- 20% power reduction
- Repeats every 2-3 years

Transistor scaling

Power… Performance… Area

Moore's law & transistor scaling



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Rayleigh equation defines litho roadmap

Wavelength λ ↓

$$resolution = k_1 . \frac{\lambda}{NA}$$

Exposure wavelength (λ)

436nm : g-line
365nm : i-line
248nm : Deep-UV (KrF)
193nm : Deep-UV (ArF)
157nm : Vacuum UV (F2)
13.5nm: Extreme UV (EUV)

Lord Rayleigh

k_1 factor ↓

Low k_1 lithography (k1 ≥ 0.25)

Resolution enhancement techniques, process control.

NA ↑

Projection lens NA

Dry lithography : ≤ 0.93
Immersion lithography : ≤ 1.35

EUV lithography: 0.25 – 0.32NA

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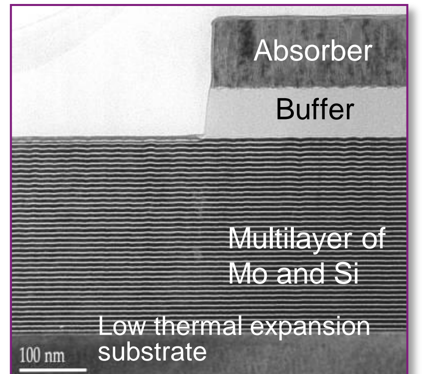
What is EUV lithography ?

The EUV radiation (13.5nm) is strongly absorbed by all known materials and gases. As a consequence:

- The **optics** must be **reflective** and fully contained in **vacuum**
- The **reticle** must be **reflective** too, and **no pellicle** can be used to keep the possible defects out of focus.



- All mirrors (including the reticle) use an alternating stack of Mo/Si layers with a theoretical maximum reflectivity (under normal incidence) of only 74%. Keeping the mirror count to a minimum is a priority.
- Lots of EUV **intensity** is **lost** (high power is needed).

CRITICAL ISSUES: source power, masks and resists

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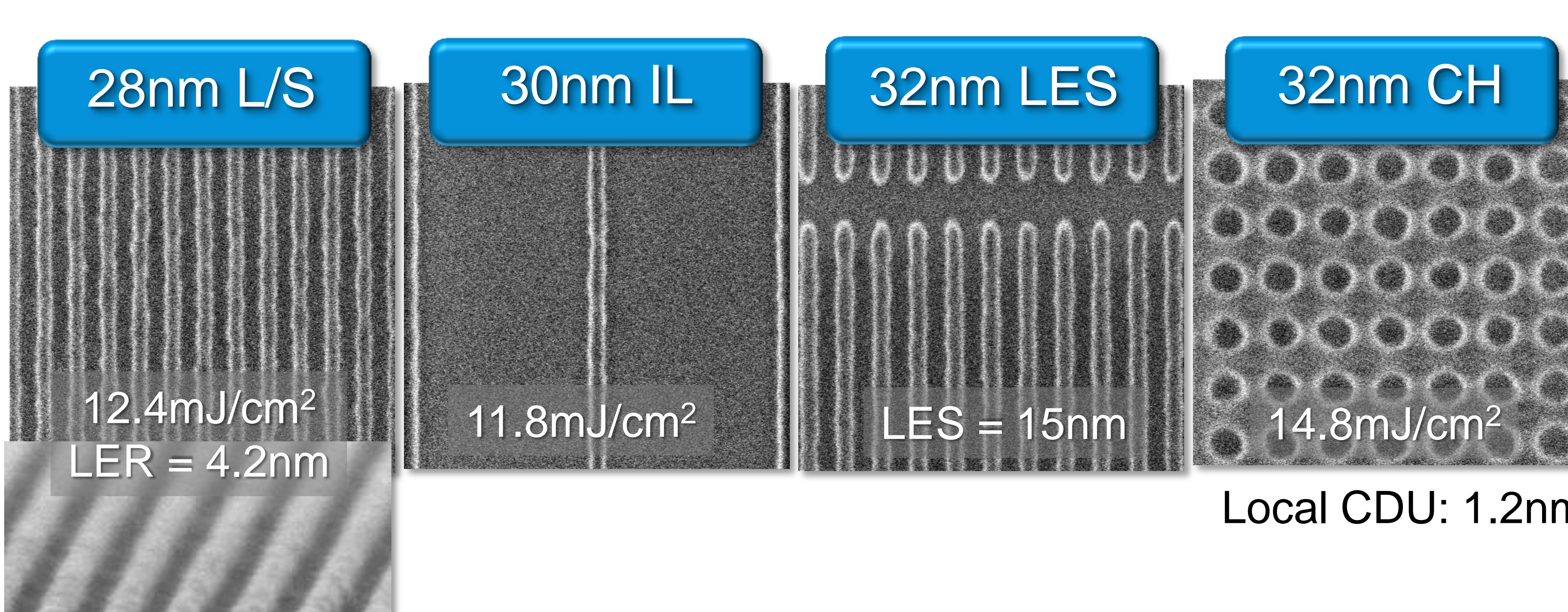
EUV performance



Good process window for 28nm L/S

Good photo speed and good resist profiles

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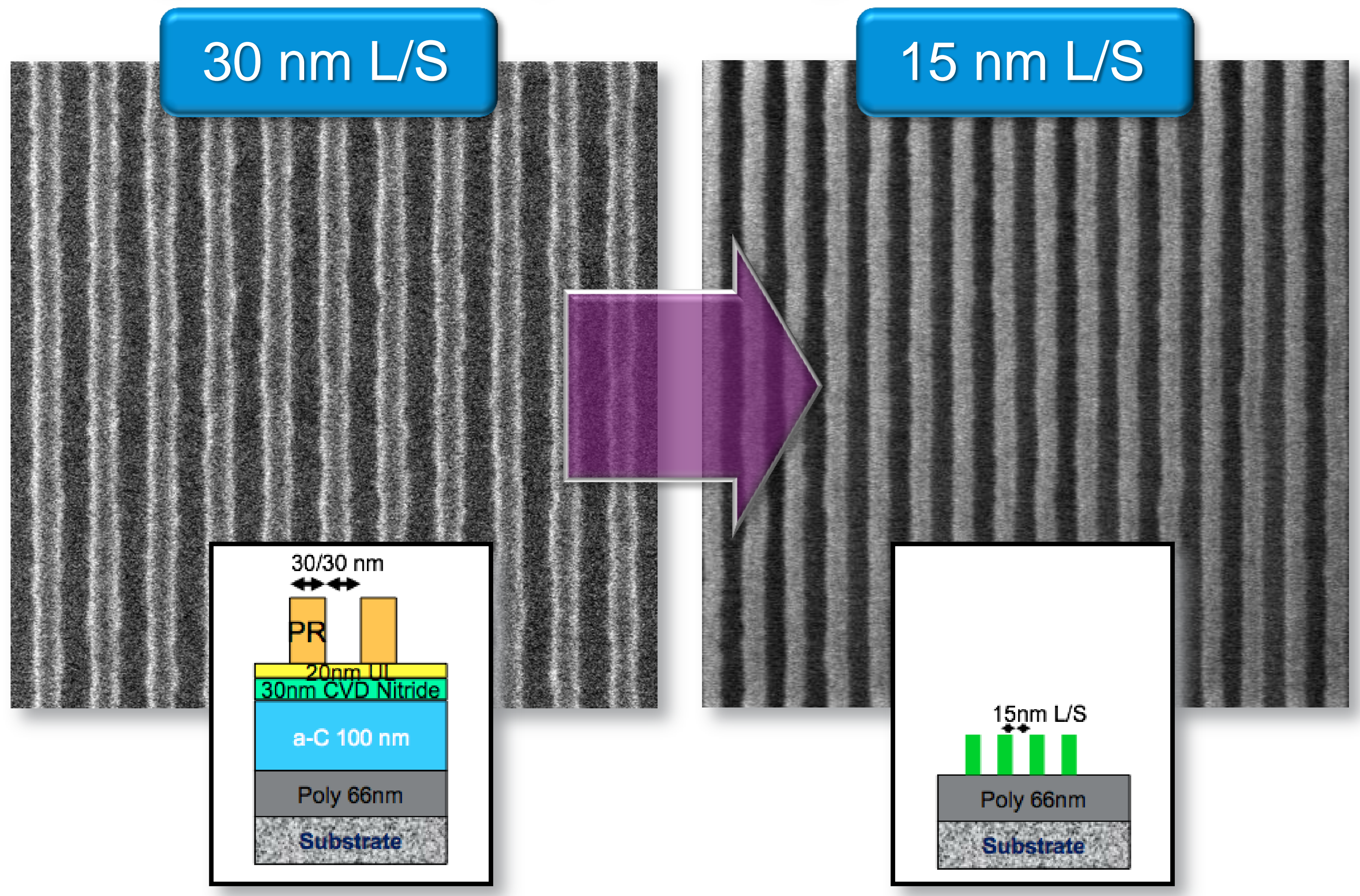
EUV extendability
Self-aligned double patterning



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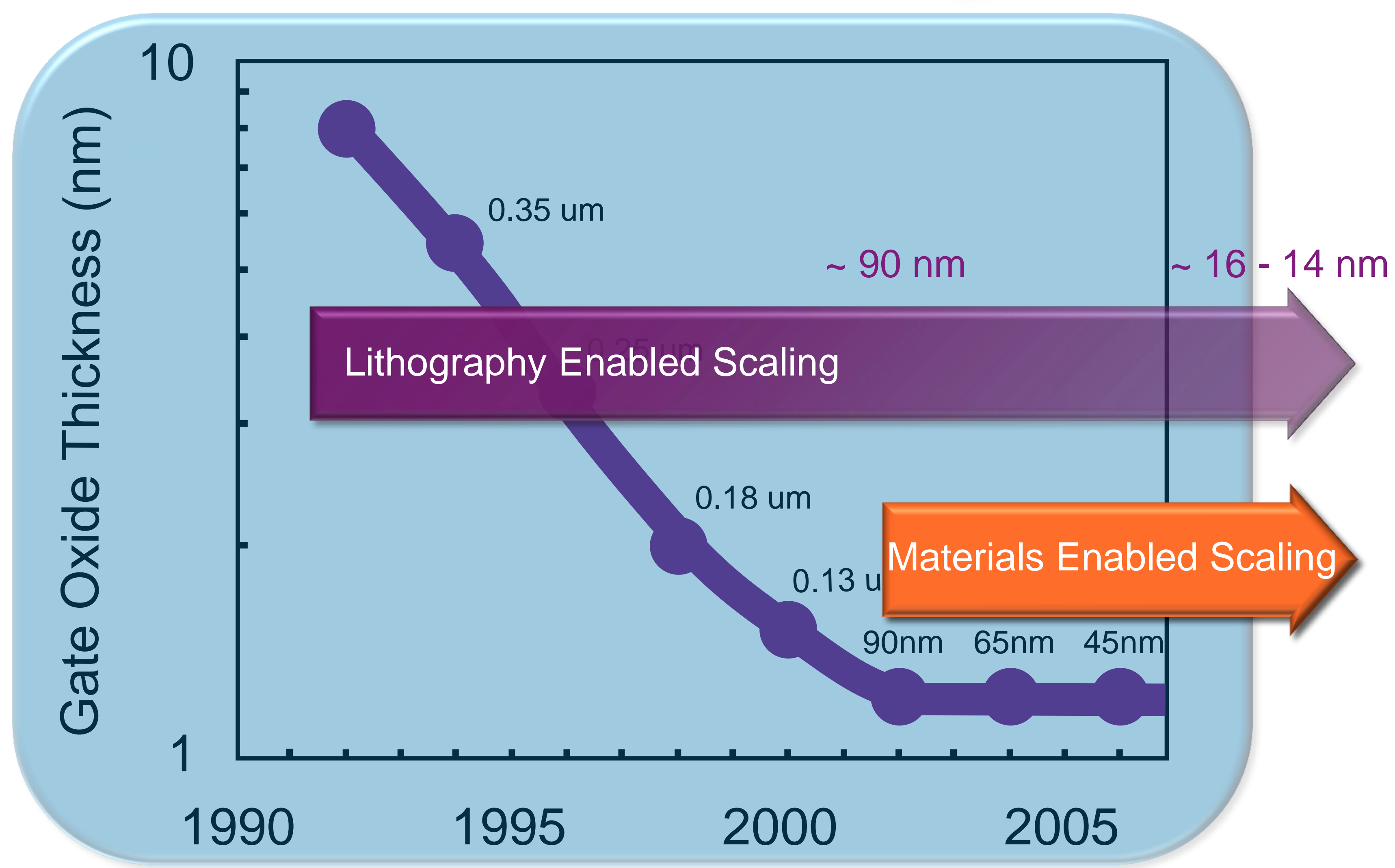
Moore's law & transistor scaling



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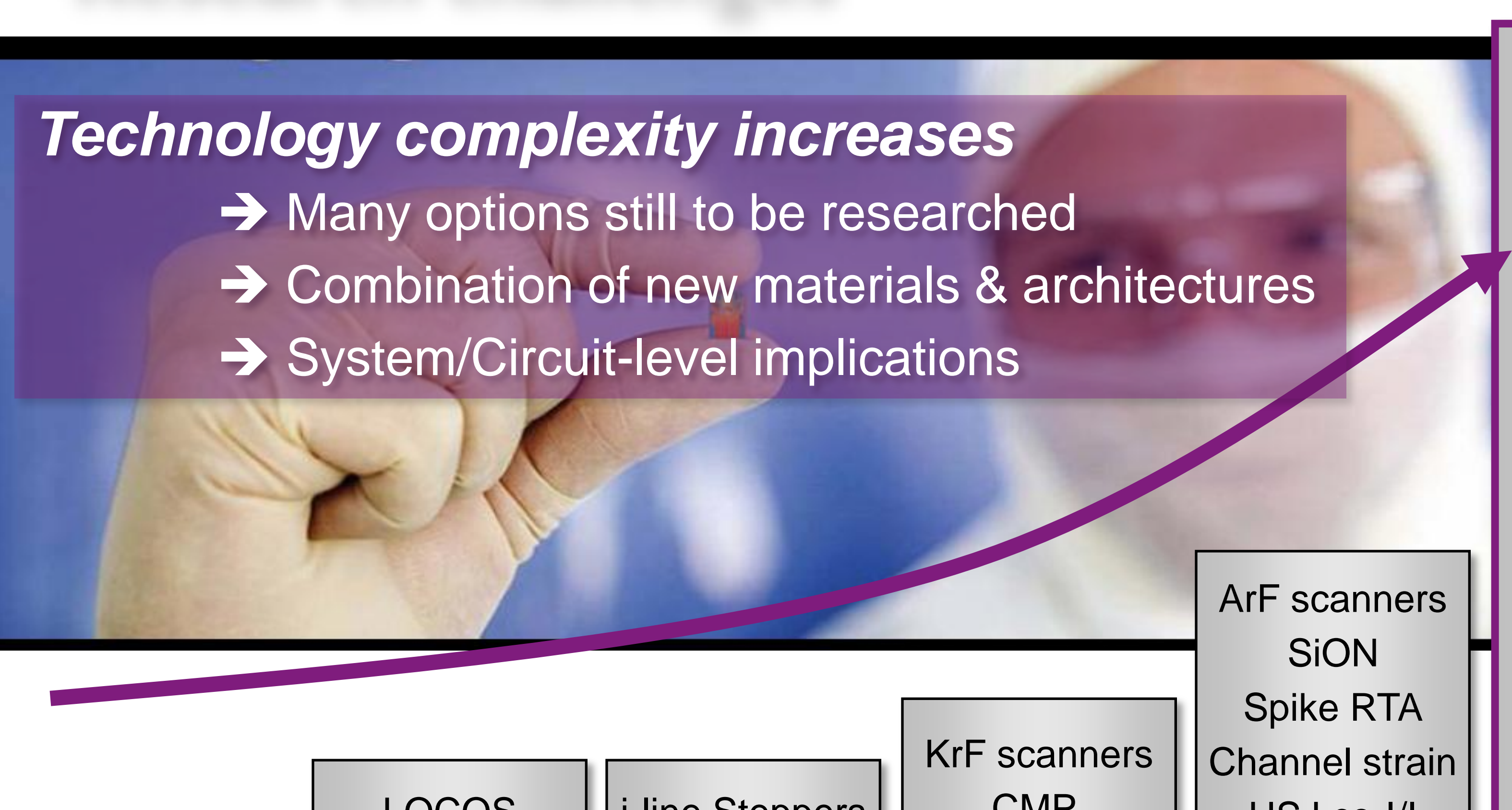
Research challenges



'60	'70	'80	'90	'00	'10
MOSFET SiN Passivation	LOCOS Ion implant Plasma Etch	i-line Steppers LDD Silicide	KrF scanners CMP Ext / HALO Cu metal	ArF scanners SiON Spike RTA Channel strain USJ co-I/I Immersion litho GL: HK / MG	HK / MG Multi-Gate SMO TSV EUV scanner FBRAM Super-HK VFET III-V channel Mask-less Air-gap RRAM 3D-NAND TANOS SAM HTFET CNT Graphene SystemCircuitTechno

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Transistor scaling

Power... Performance... Area

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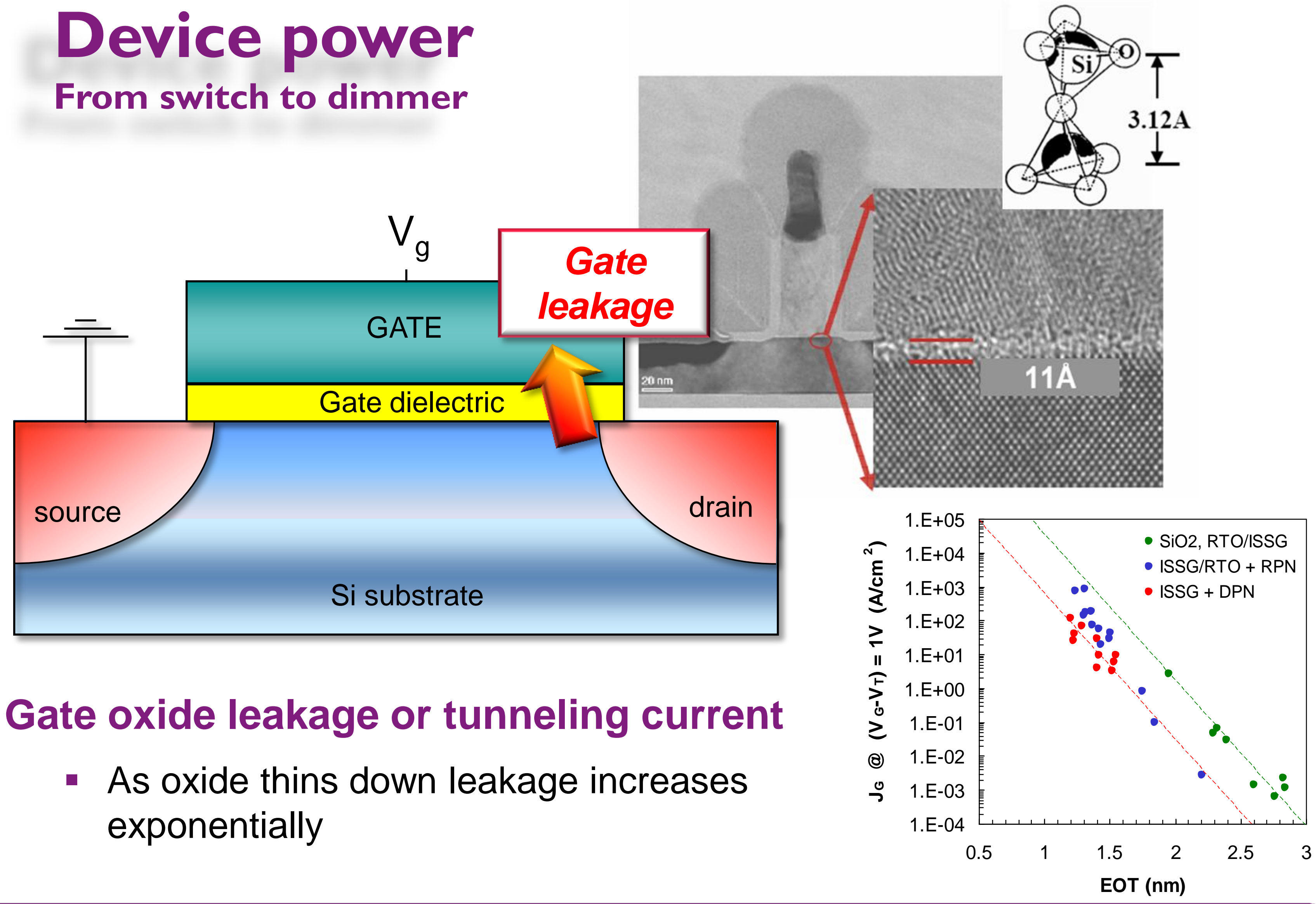
Device power

From switch to dimmer



Gate oxide leakage or tunneling current

- As oxide thins down leakage increases exponentially

Need new materials and/or new architectures !

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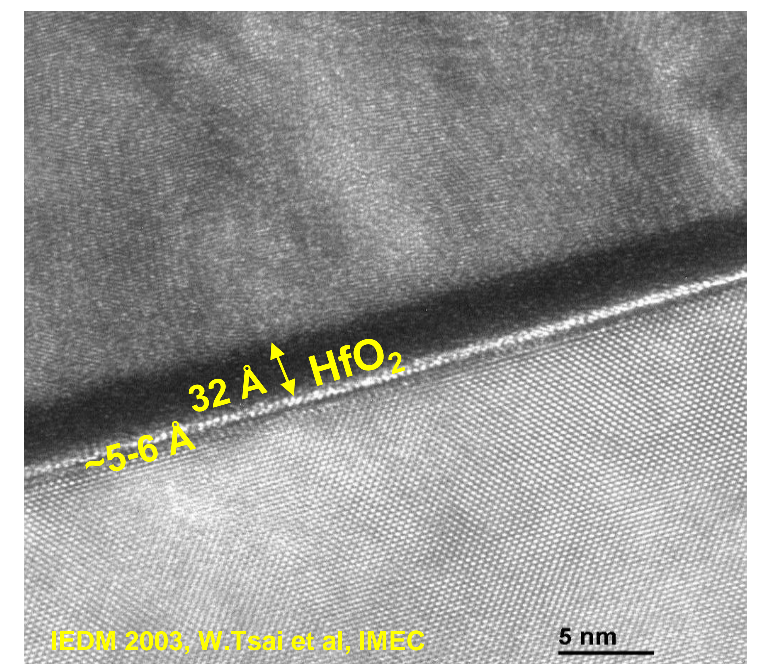
Device power

How to tackle the problem?

Solution → new materials

e.g. high-K dielectric



Constant Capacitance Density

$C = \varepsilon_0 \varepsilon_{SiO2} / t_{SiO2} = \varepsilon_0 \varepsilon_{hk} / t_{hk}$

$t_{high\text{-}k} = \varepsilon_{hk} / \varepsilon_{SiO2} * t_{SiO2}$

Atomic Layers

1000

100

10

1

~ 90 Layers

SiO_2

SiON

3 Layers

1 nm

~ 5 nm

High-k

(schematic

1980 1985 1990 1995 2000 2005 2010 2020

Year

Direct tunneling

Oxides < 3nm

ϕ_b

Vox

e

n+ poly

sub

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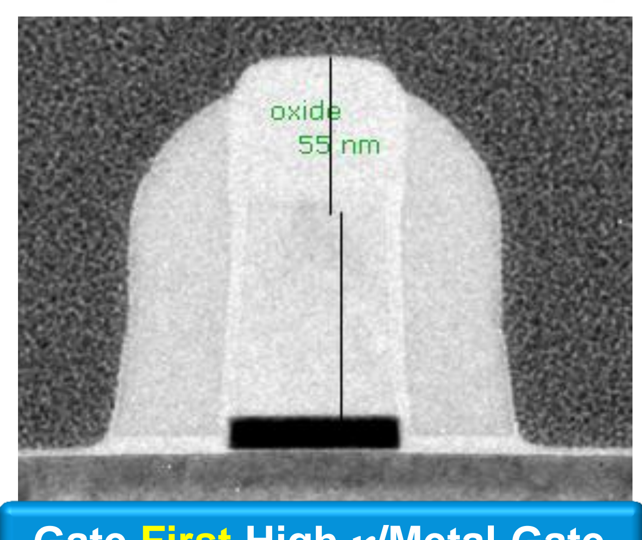
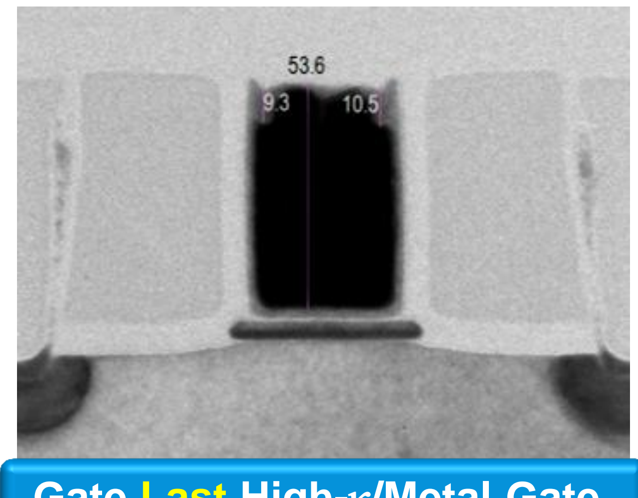
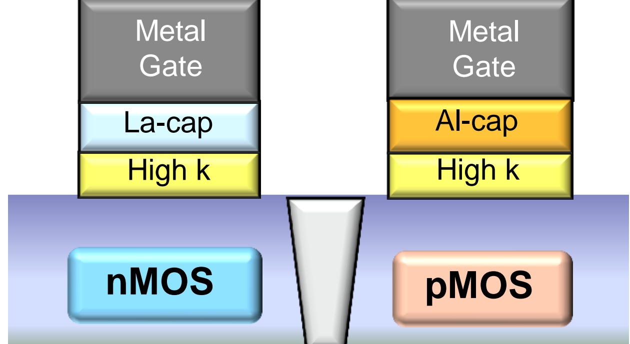
High-κ / metal gate

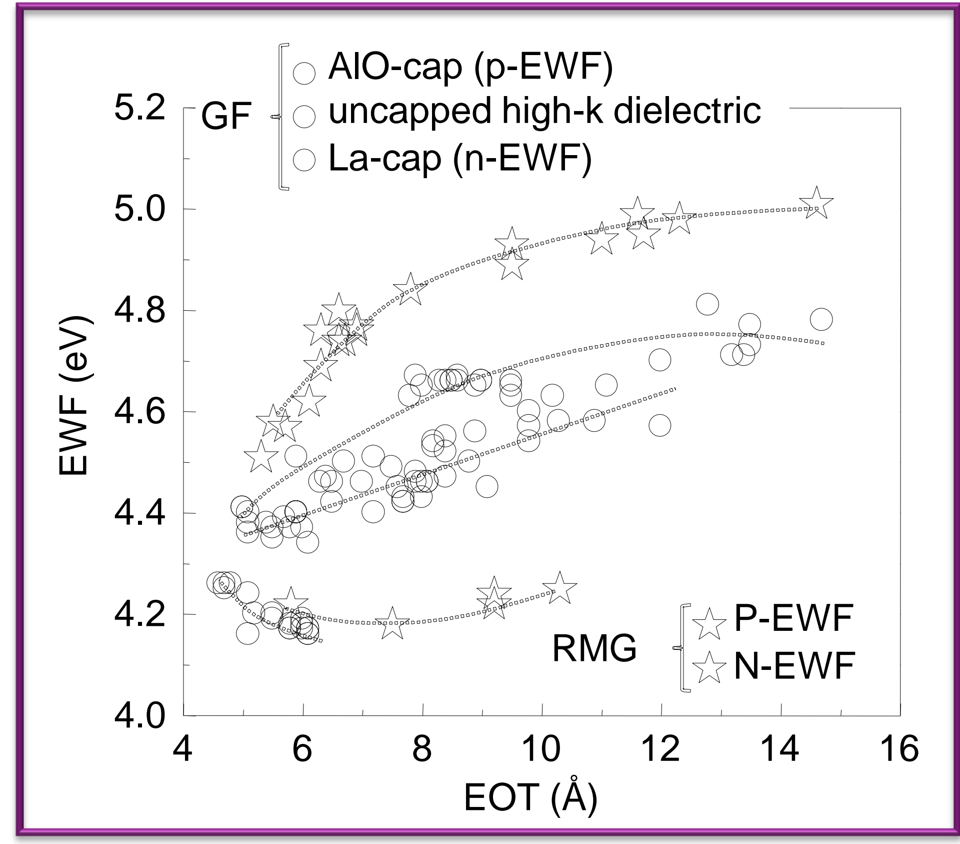


Gate First High-κ/Metal Gate



Gate Last High-κ/Metal Gate





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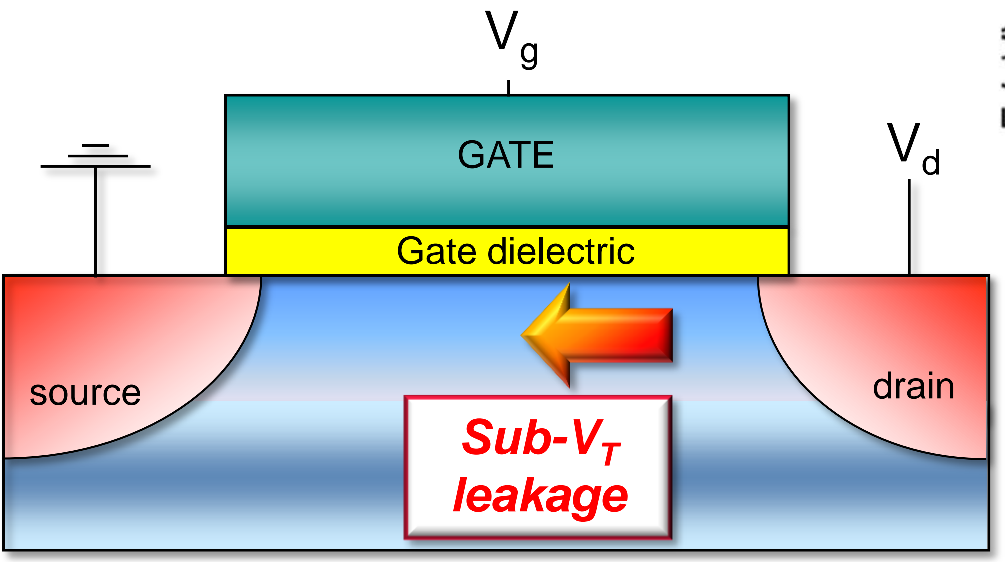
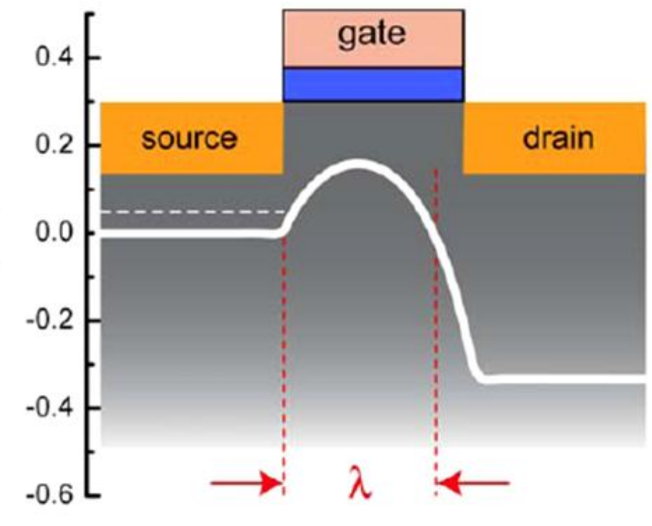
Device power

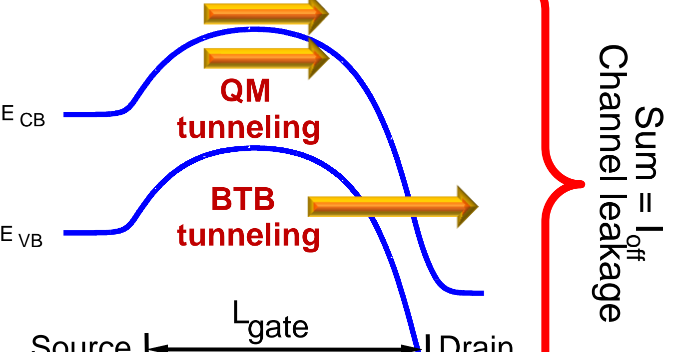
From switch to dimmer





Subthreshold leakage

- Short channel forms no effective barrier
- Threshold voltage not scaling as fast as V_{DD}



Need new materials and/or new architectures !

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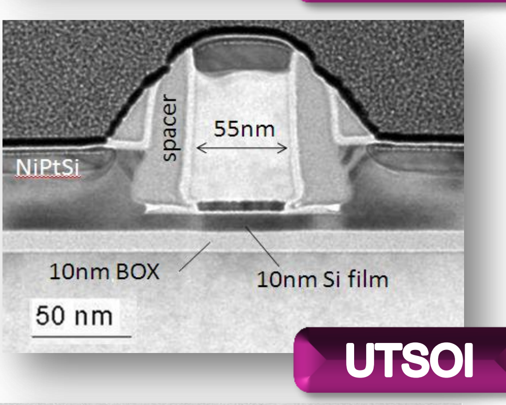
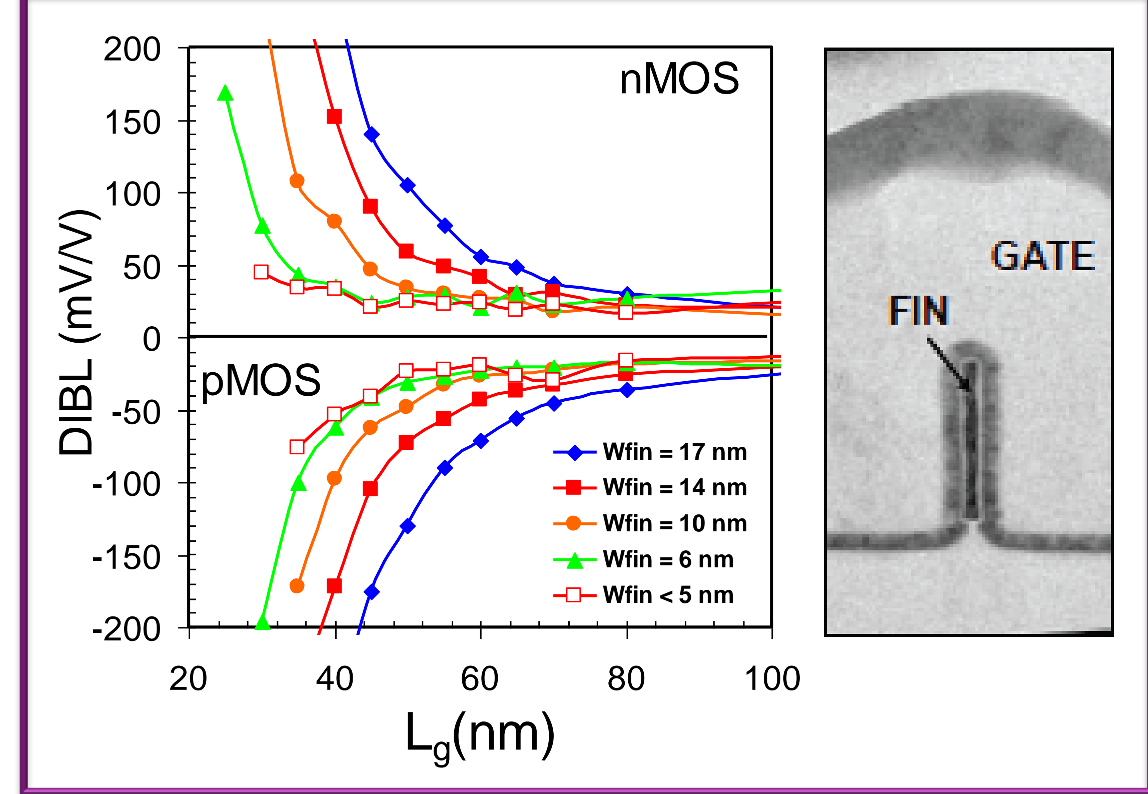
Fully depleted devices



Solution → New Architecture
e.g., **Fully Depleted Devices**
for better short-channel control



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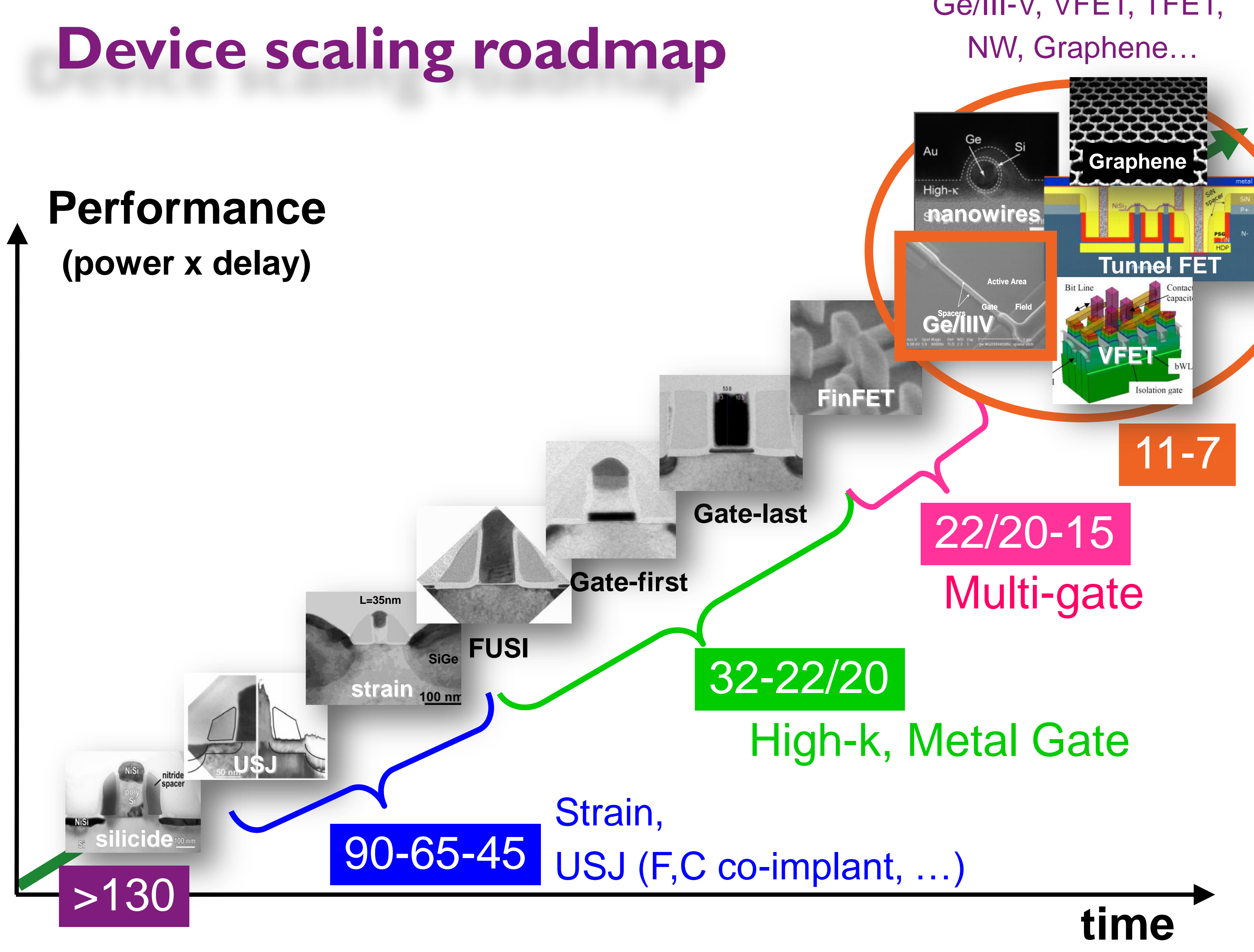
Transistor scaling

Power... Performance... Area

Device scaling roadmap



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Device performance

Strain engineering and high-mobility channels

	Hole mobility (cm^2/Vs)	Electron mobility (cm^2/Vs)
Si	430	1600
Ge	**3900**	3900
GaAs	400	**9200**
InAs	500	**40000**

W=10um
V_{DD}= -20mV / -1V
REF. SiGe-45% with implants
REF. IFQW SiGe 45%
IFQW SiGe 45% + eSiGe
DIBL [mV/V]
LG_physical [nm]

eB:SiGe
SiGe(45%) QW
rB:SiGe(25%)
W=10um, V_{DD}=-1V
REF IFQW SiGe 45%
SiGe-55% LA + I/I Mitard et al IEDM'10
IFQW SiGe-45% Hellings et al IEDM'10
I_{ON}=1mA/um
IFQW SiGe 45% + epi S/D booster 25%
Ioff_drain @VG=0V (uA/um)
Ion @VG=-1V (uA/um)

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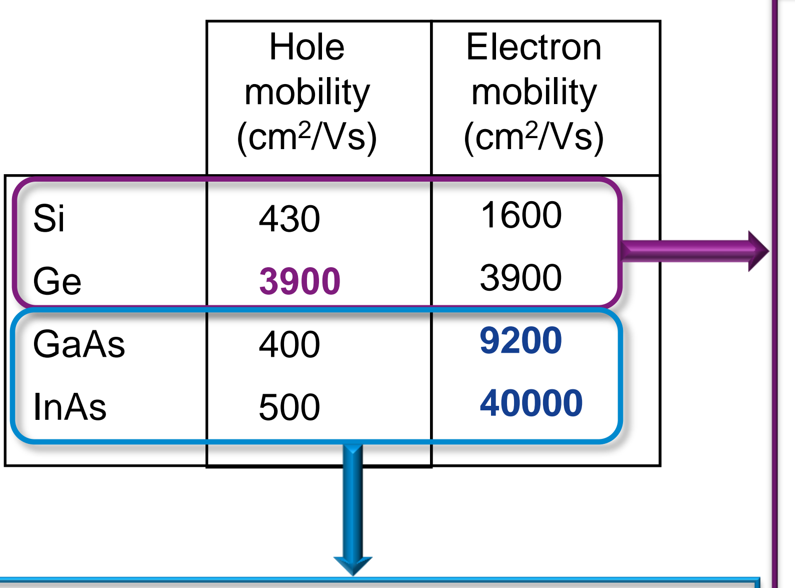
Device performance

Strain engineering and high-mobility channels



	Hole mobility (cm^2/Vs)	Electron mobility (cm^2/Vs)
Si	430	1600
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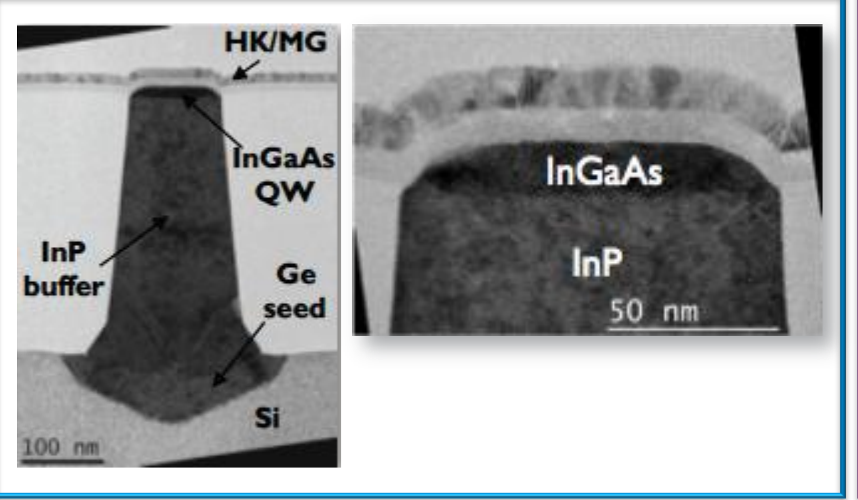

eB:SiGe

SiGe(45%) QW

rB:SiGe(25%)

W=10um, V_{DD}=-1V

REF IFQW SiGe 45%

SiGe-55% LA + I/I Mitard et al IEDM'10

IFQW SiGe-45% Hellings et al IEDM'10

I_{ON} =1mA/um

IFQW SiGe 45% + epi S/D booster 25%

Ioff_drain @VG=0V (uA/um)

10^{0}, 10^{-2}, 10^{-4}, 10^{-6}

0, 200, 400, 600, 800, 1000

Ion @VG=-1V (uA/um)

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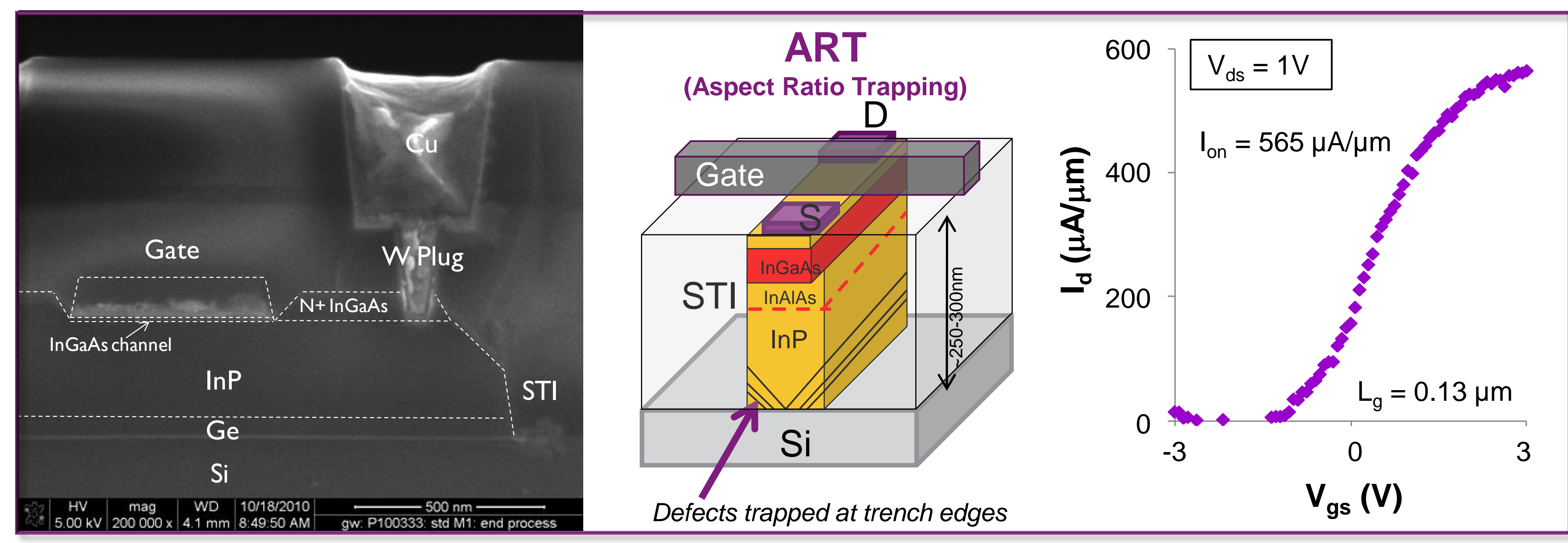
Selective (in STI trenches) III/V QW MOSFET

Key Characteristics

"ART" (Aspect-Ratio-Trapping) with InP-on-Si buffer

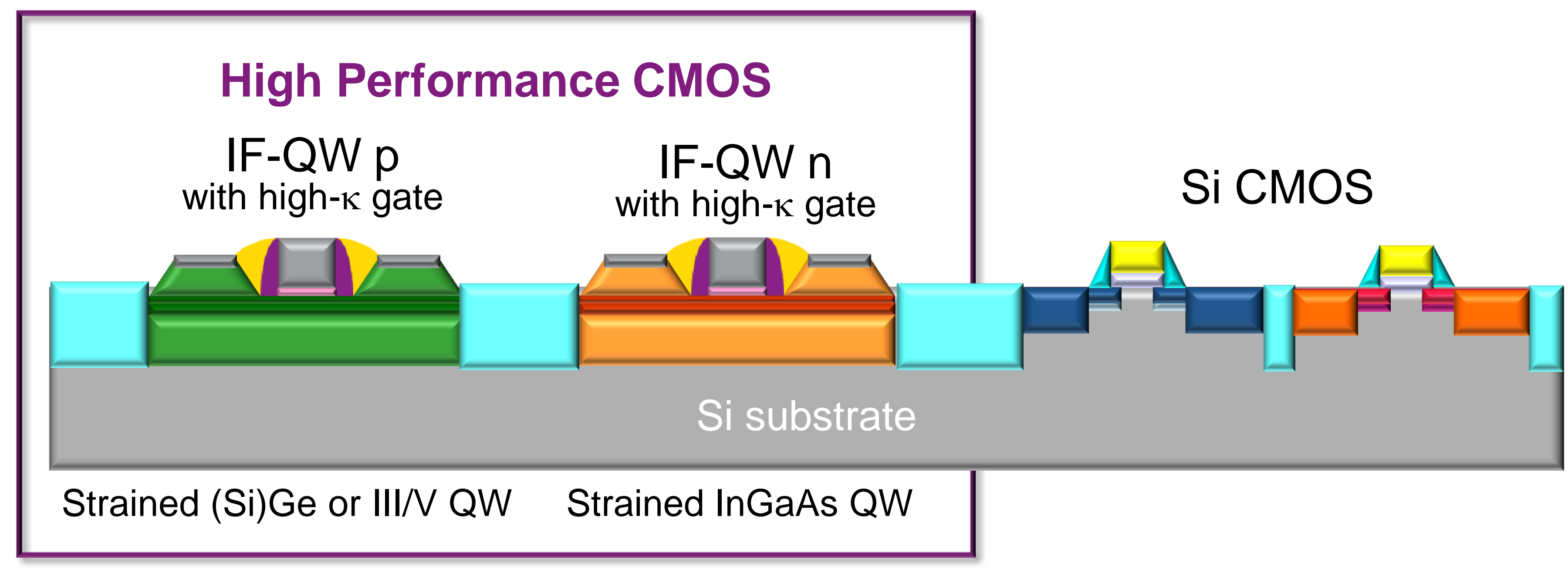
MOCVD 8" Epi (AIXTRON), with raised (n+)-InGaAs S/D



1st functional transistor characteristics !

Work on-going for further improvement in buffer defectivity and doping (insulation)

High mobility channel materials
Co-integration with standard Si CMOS



1. **Selective growth** of (Si)Ge and/or III/V in STI trenches
2. **High-κ gate stack** for low EOT
3. Self-aligned **doped raised S/D** for contacts
4. Further **strain engineering** for mobility boost

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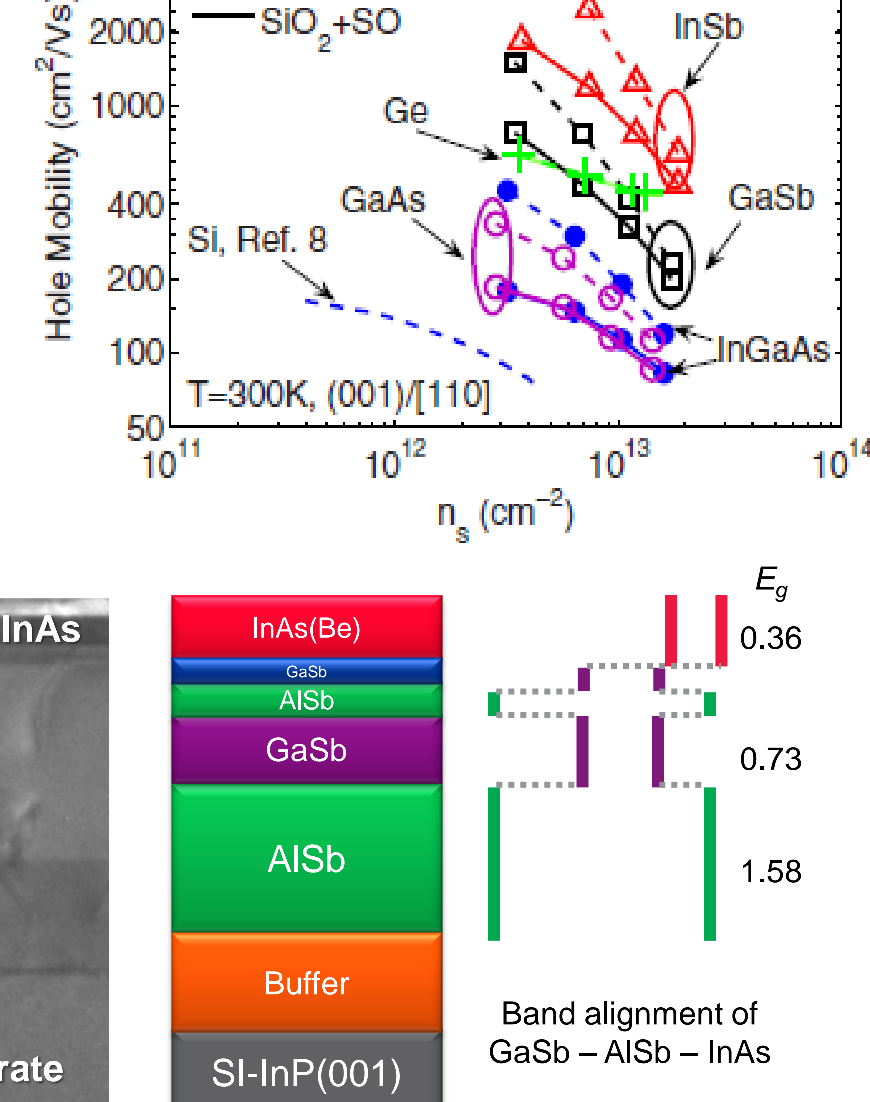
p QW FET

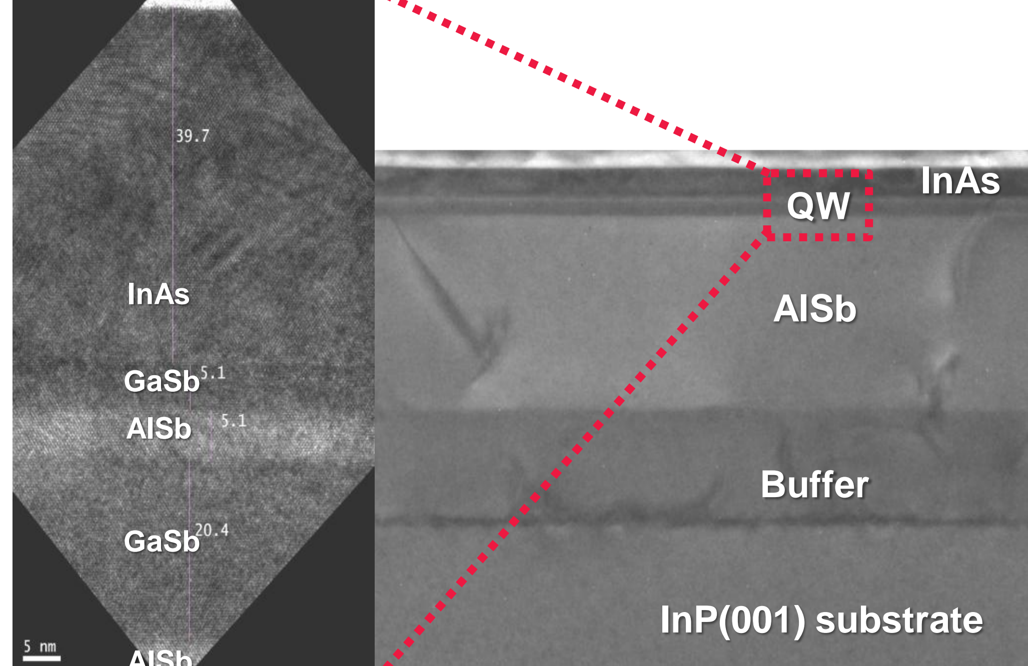
High hole mobility for III-Sb p-channel

InSb followed by GaSb has the largest hole mobility compared to Ge, InGaAs and GaAs

Optimized structural stack quality

The **AlSb interfacial layer** plays a key role in the growth of high quality QW stack





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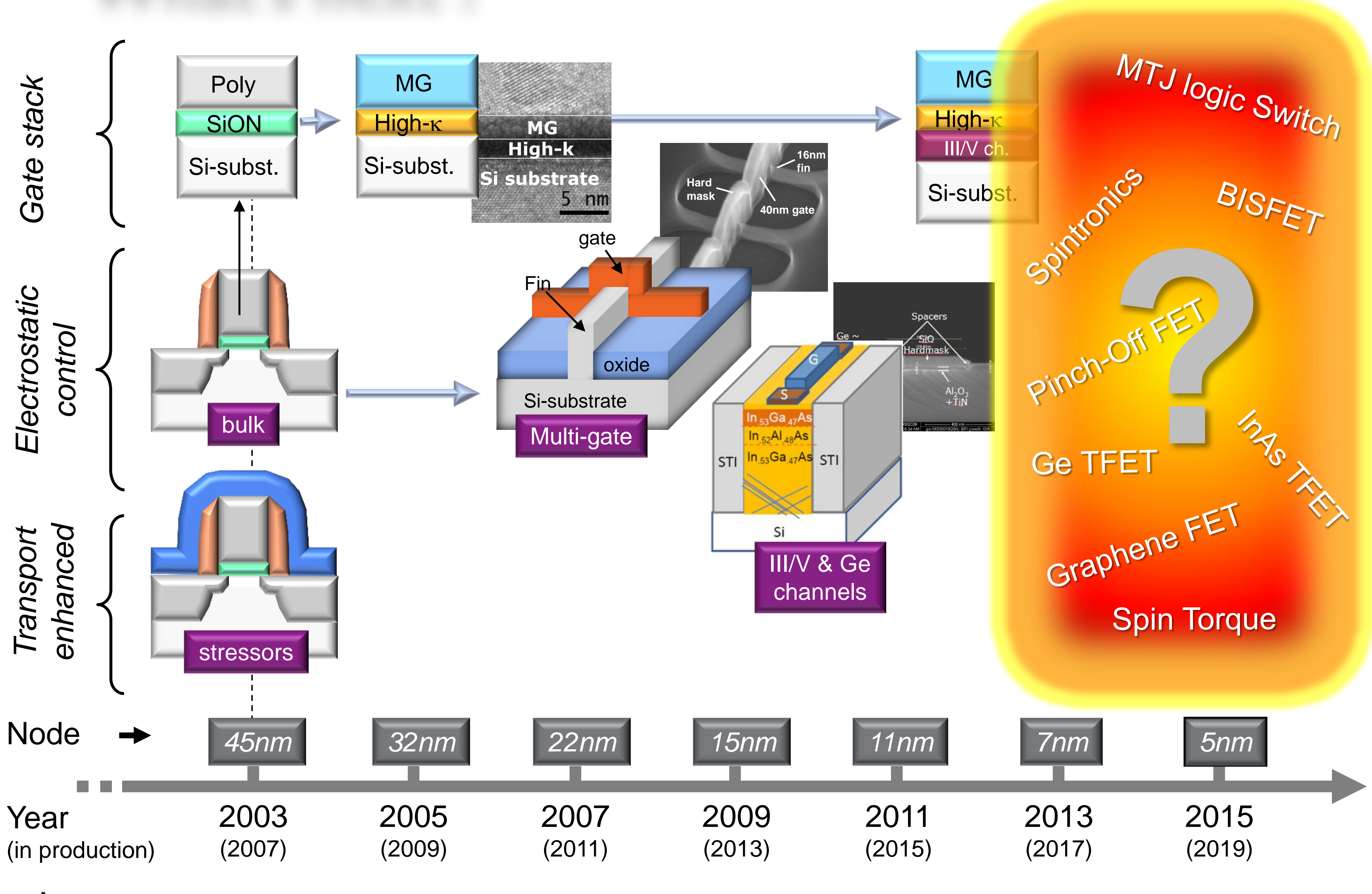
What's next ?



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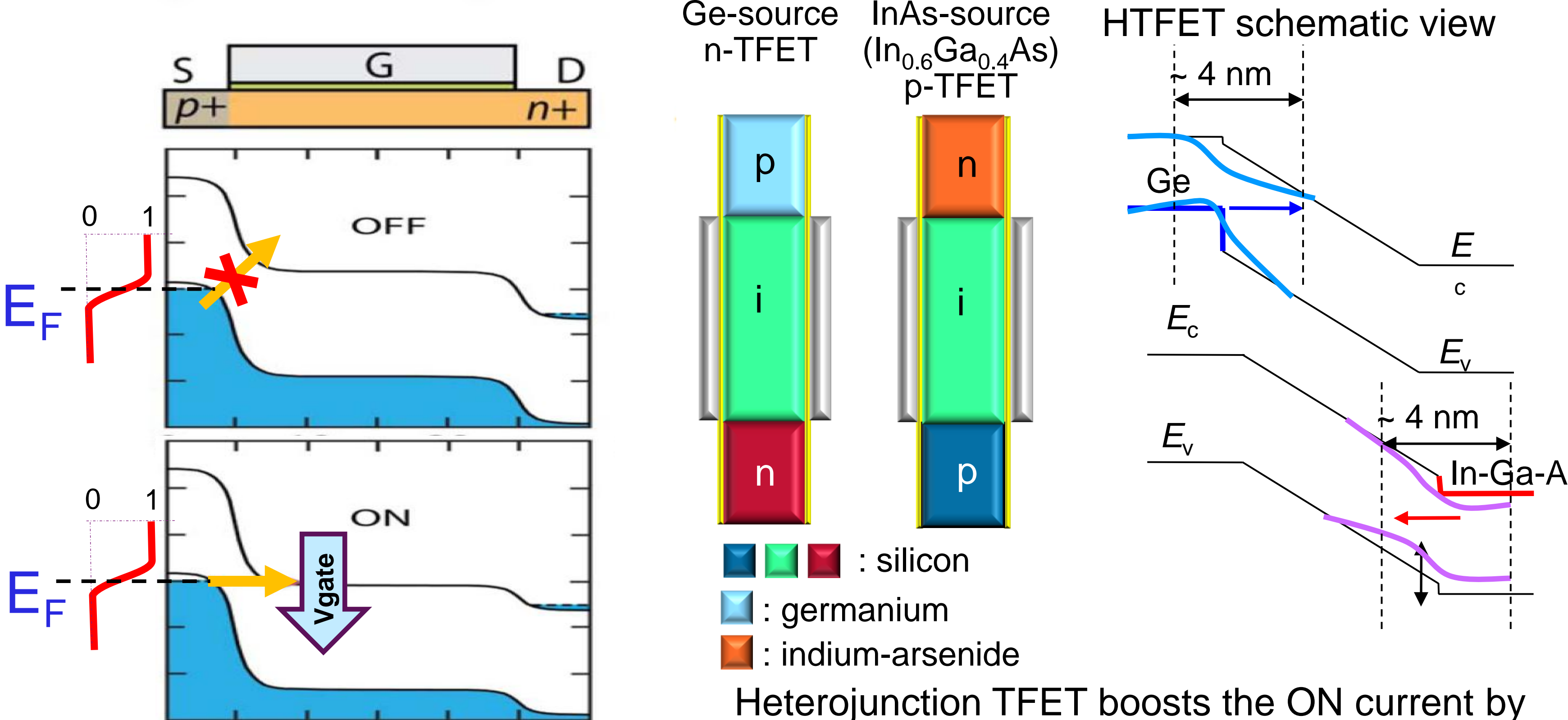
Exploratory devices: TunnelFETs



Heterojunction TFET boosts the ON current by increasing the source tunneling efficiency by using low bandgap material in the source

Tunnel-FET basic idea: *use the band-to-band tunneling in p-i-n device as an energy filter to overcome the 60mV/decade subthreshold slope limitation*

ON/OFF switching determined by band-to-band tunneling at source side

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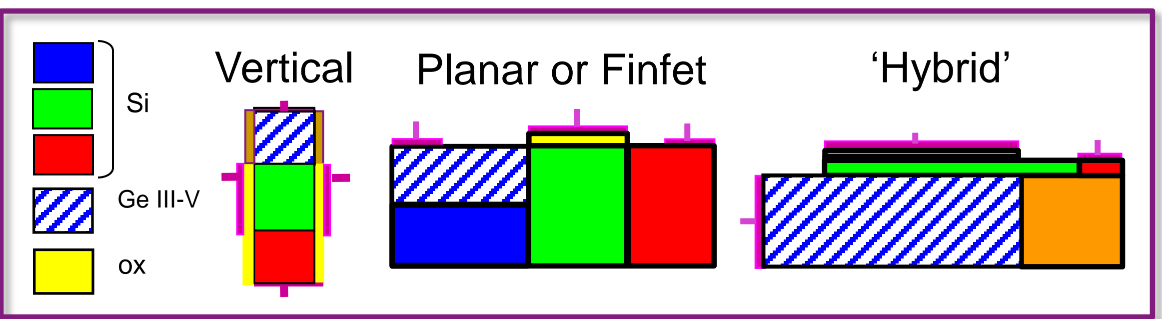
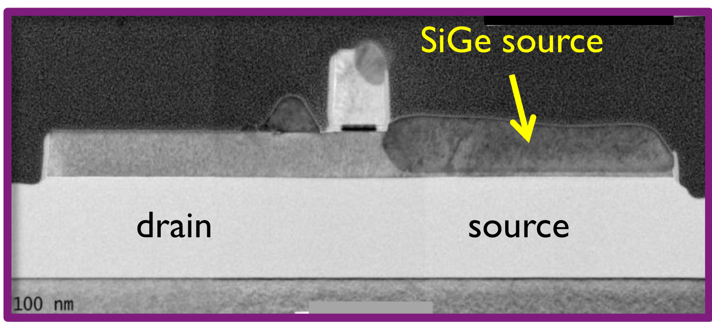
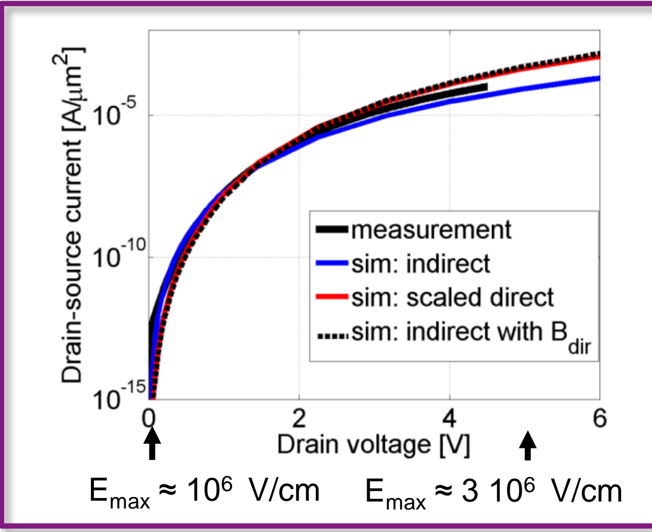
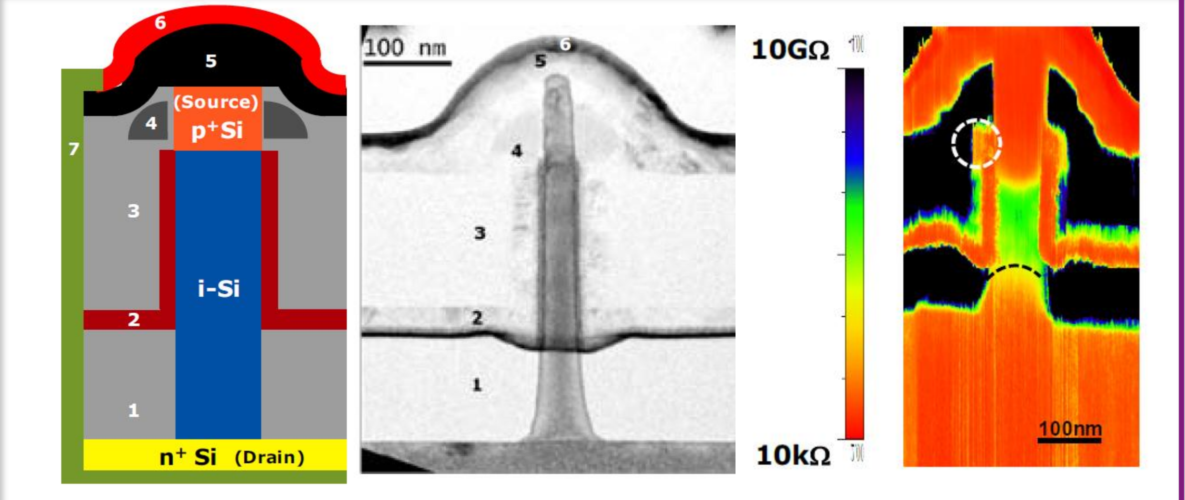
Exploratory devices: TunnelFETs









- Extensive modeling effort to calibrate tunneling efficiency (using P-i-N diodes)
- Enable exploration of new device concepts
- Integration of demonstrators (vertical & horizontal) in progress

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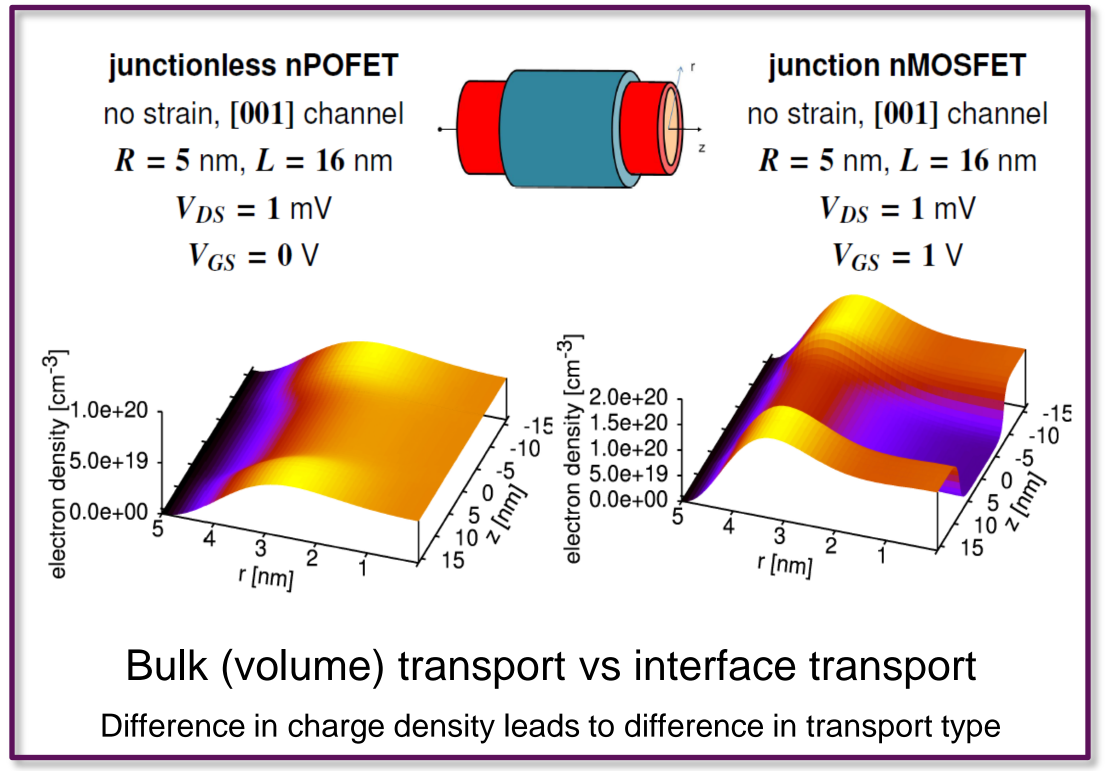
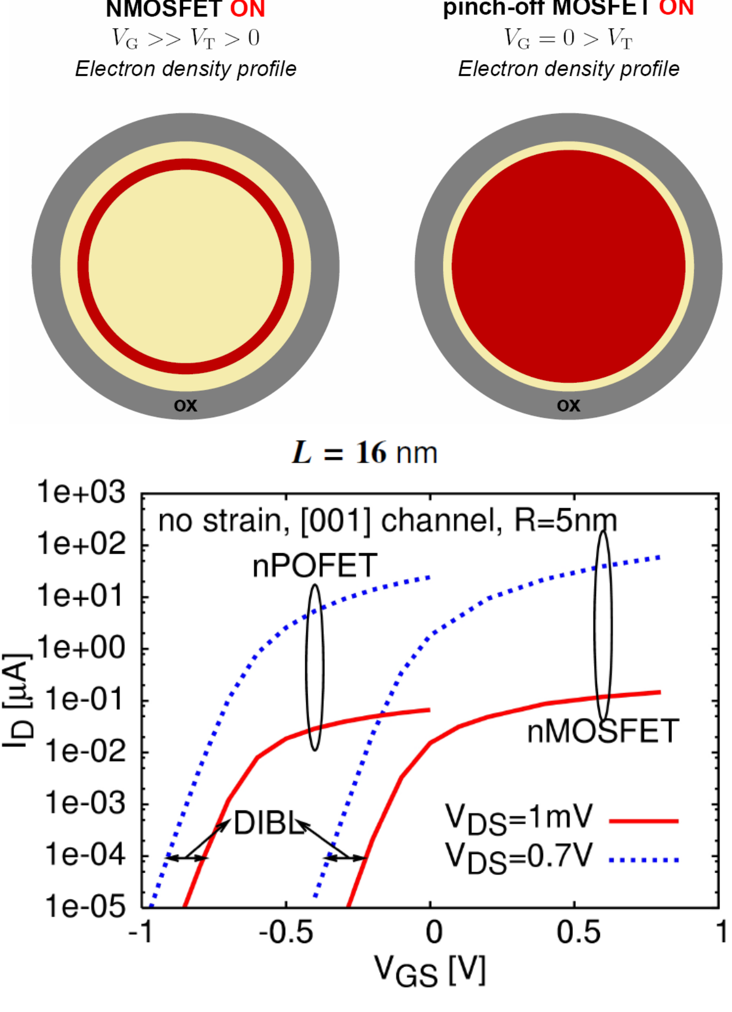
The pinch-off nanowire MOSFET

A junctionless device

- Negative gate voltage will push the majority carriers (electrons) to the middle of the wire. For sufficient negative gate voltage the channel is pinched off.
- No source and drain needed





DIBL (nPOFET) ≈ DIBL (nMOSFET) ≈ 177 mV/V
SS (nPOFET) ≈ SS (nMOSFET) ≈ 60 mV/dec

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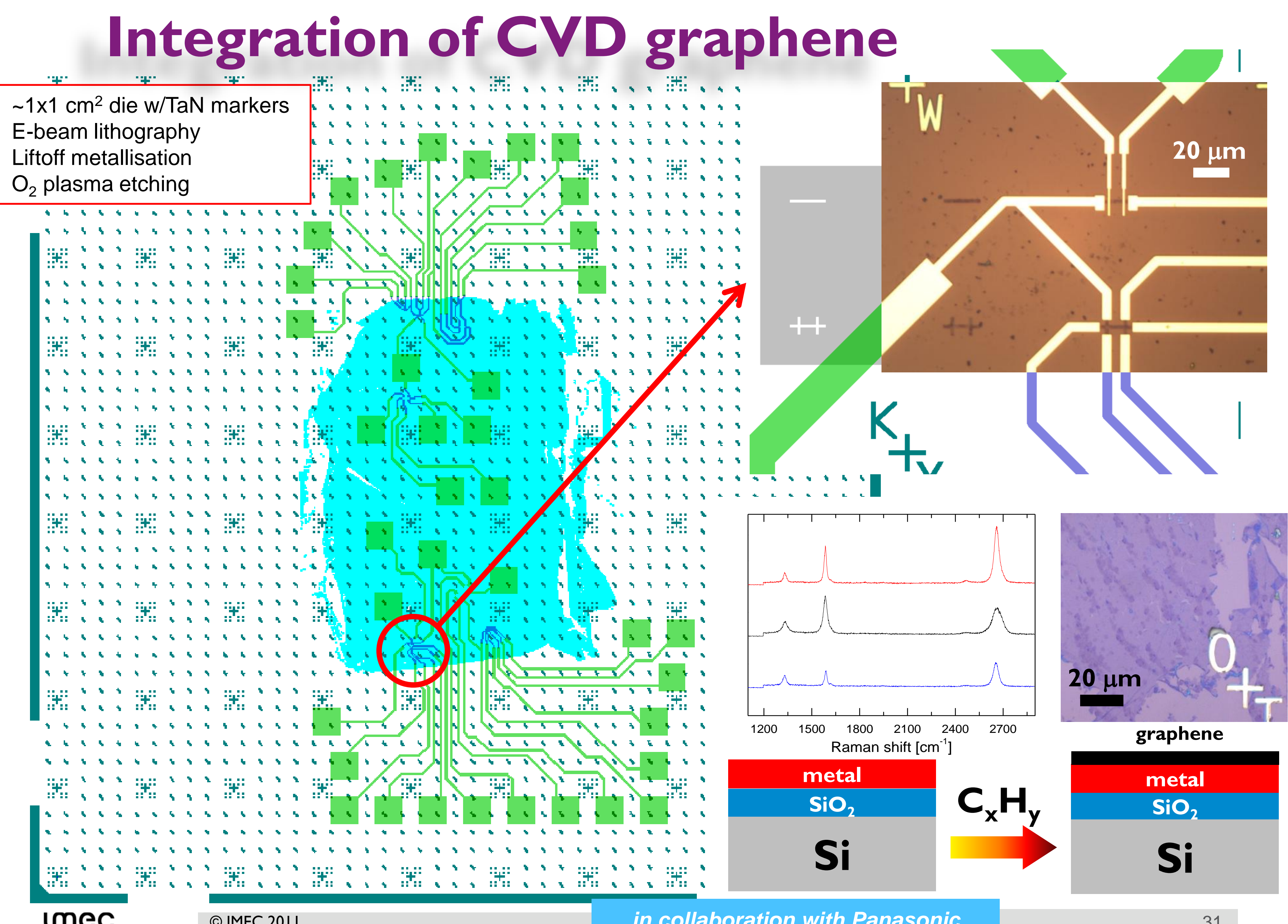
Integration of CVD graphene



in collaboration with Panasonic

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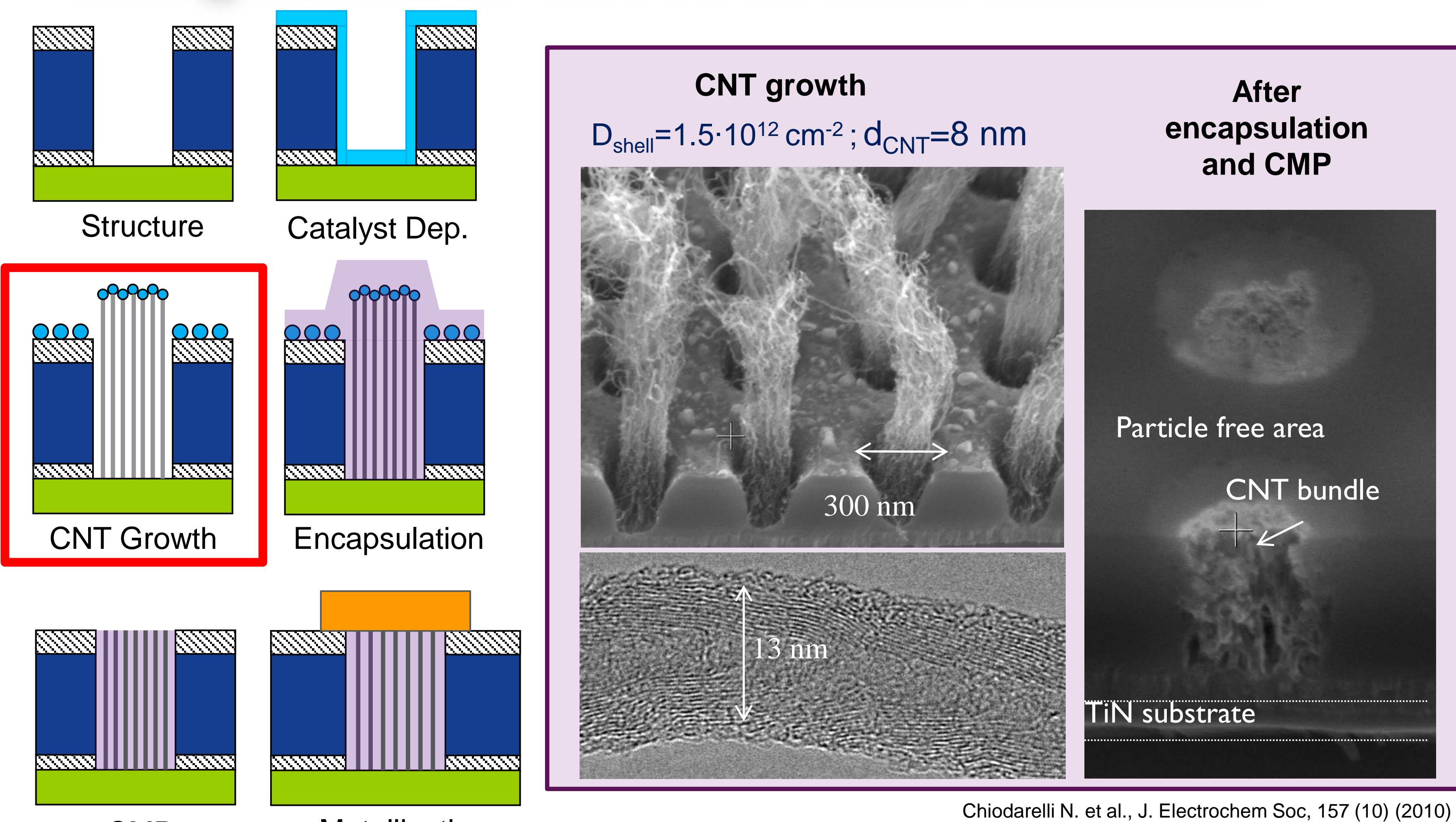
Integration of CNTs in interconnects



Chiodarelli N. et al., J. Electrochem Soc, 157 (10) (2010)

Demonstration of CNT interconnects in VIAs and contacts

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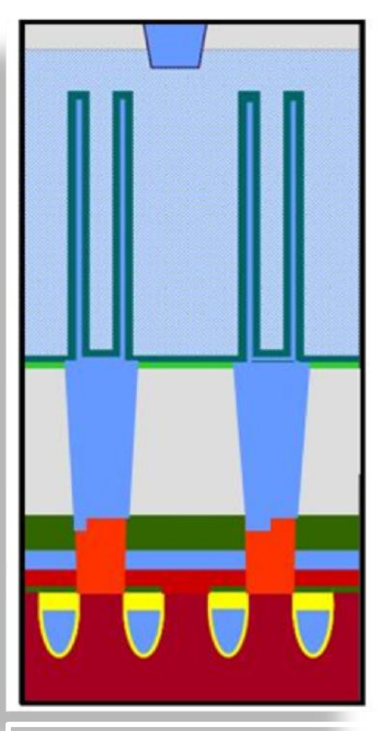
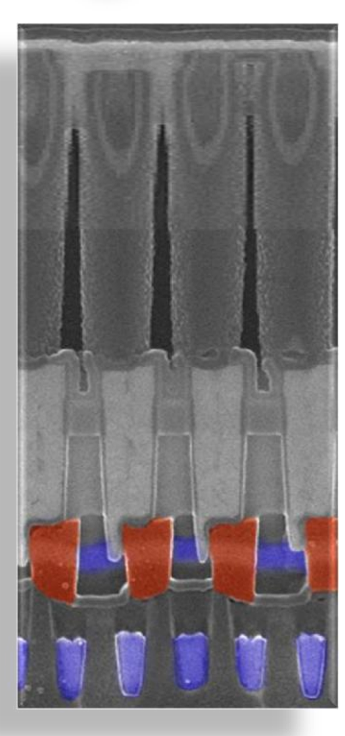
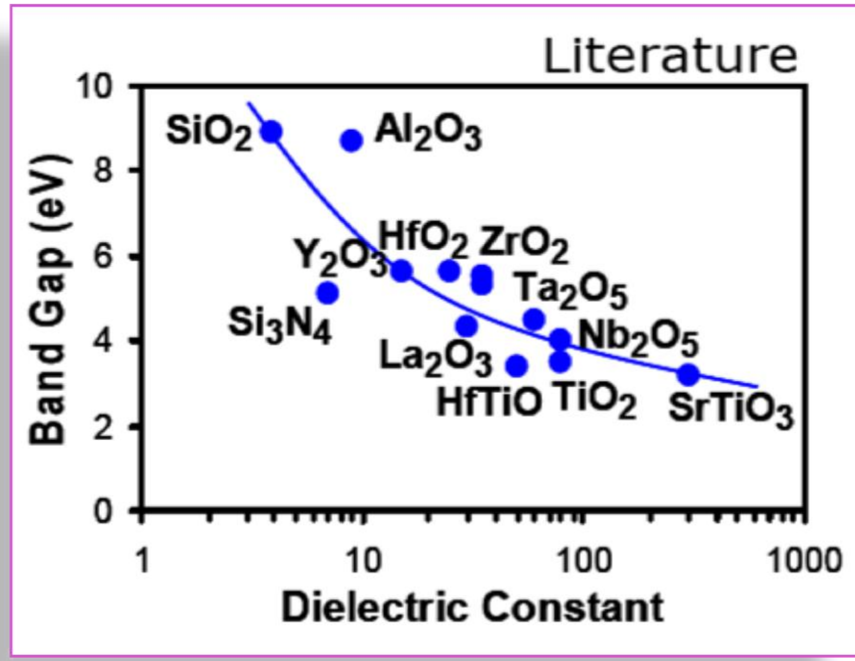
DRAM scaling challenges







Source: Qimonda

DRAM Capacitor scaling: EOT and physical thickness scaling at target leakage current

New high-k dielectrics with k > 100 and noble metal electrodes with large WF required to enable DRAM scaling below 20 nm node

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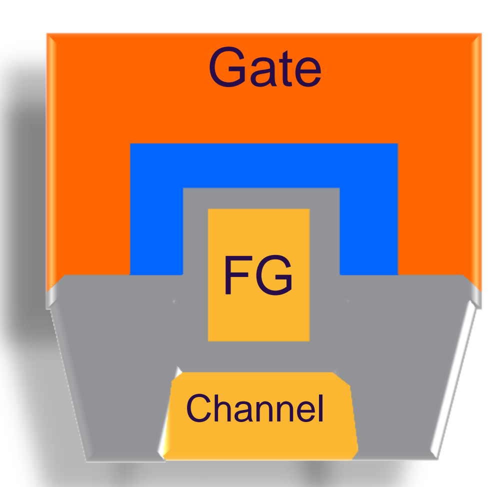
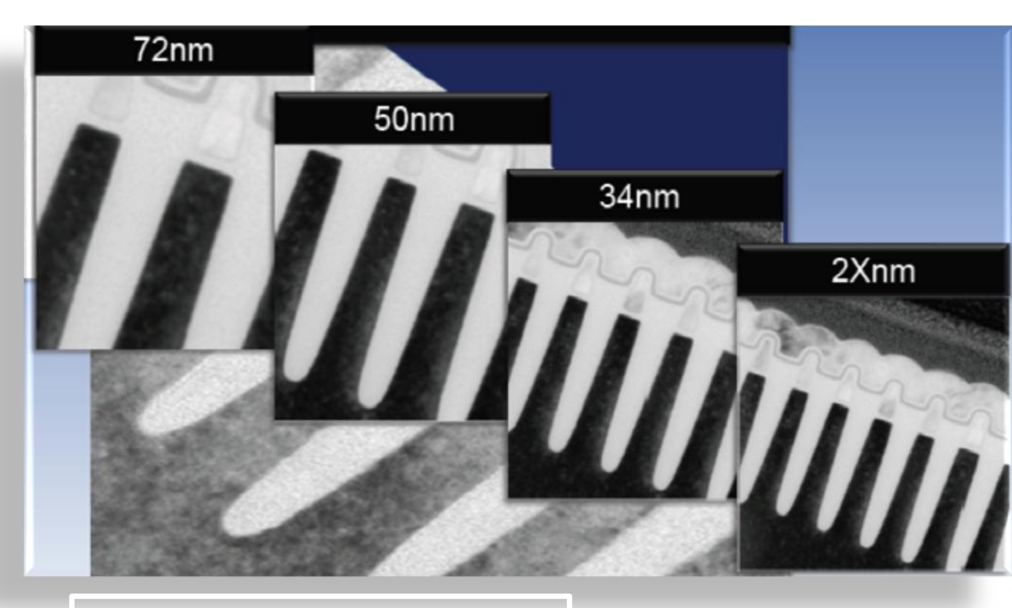
FLASH scaling challenges





Source: Micron

Floating Gate scaling: cell interference and coupling ratio (CR) reduction are the major issues when scaling and planarizing the floating gate (FG) Flash memory cell

High-k dielectrics for Inter Poly Dielectric to increase CR & FG stack engineering required to enable Flash scaling below 20 nm

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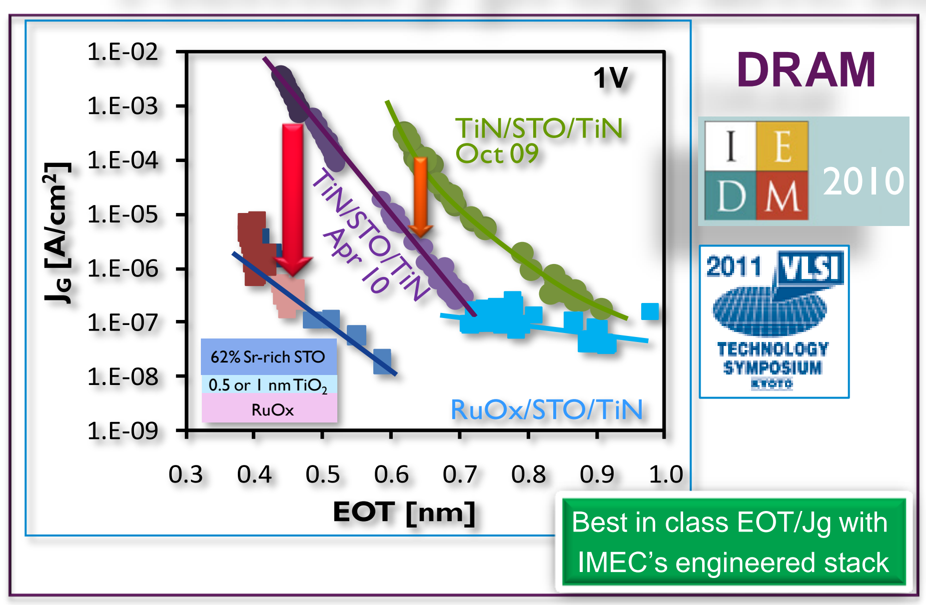
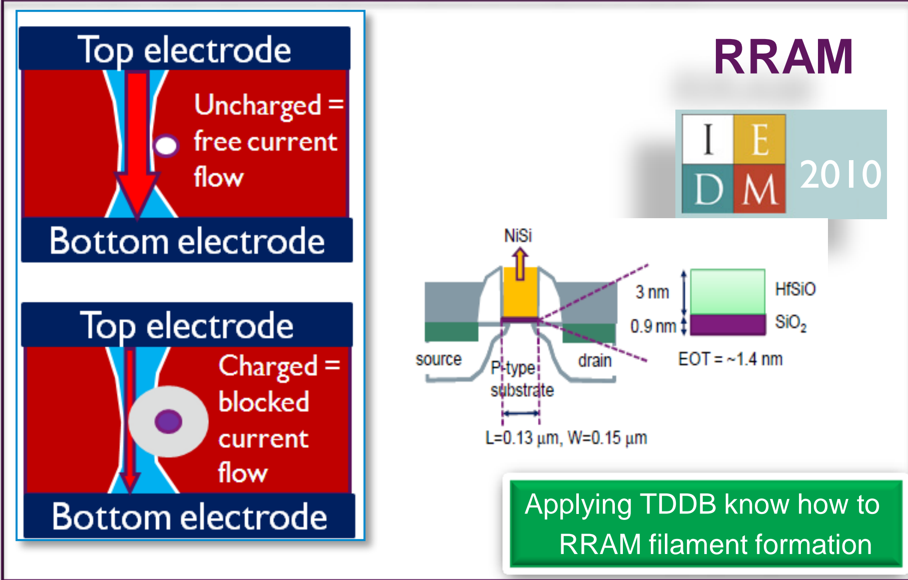
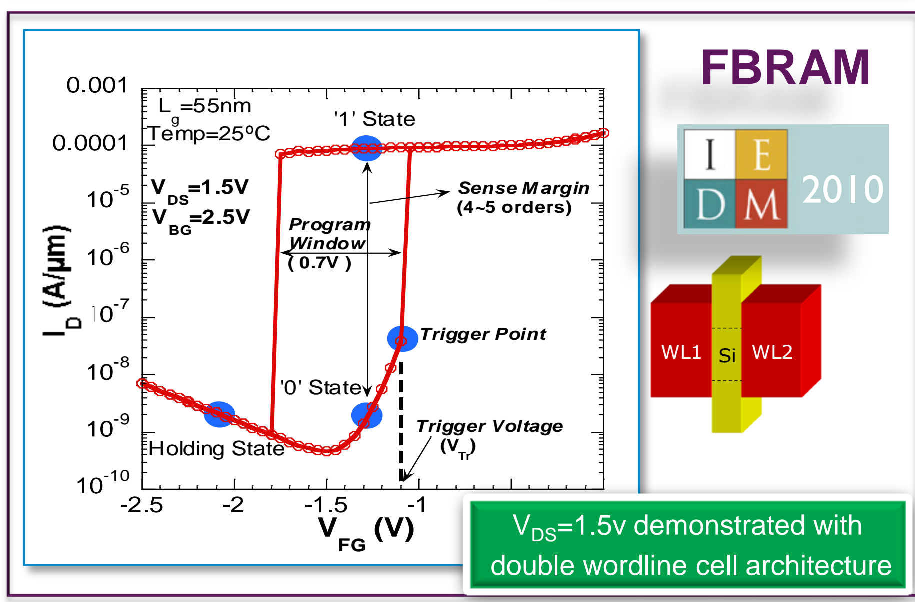
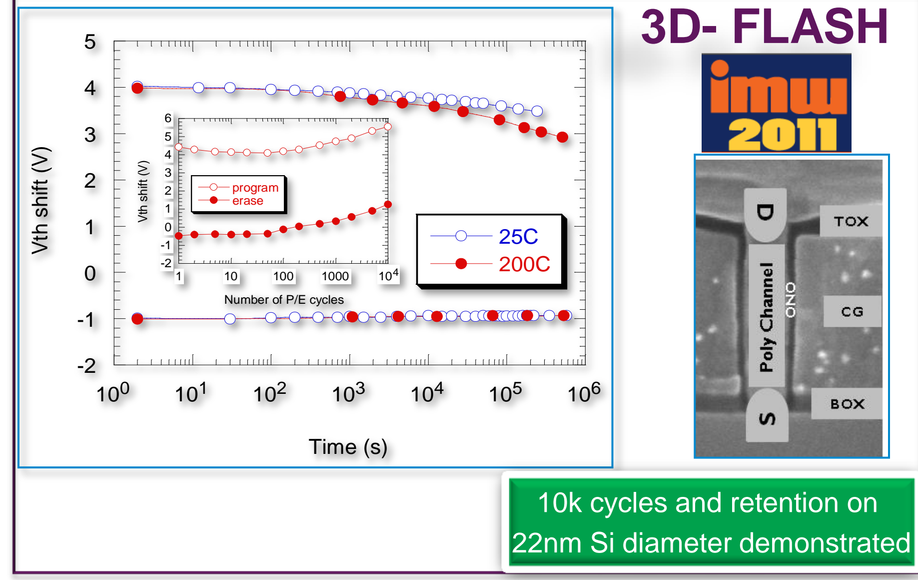
Memory program: some achievements









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Moore's law & transistor scaling

1965

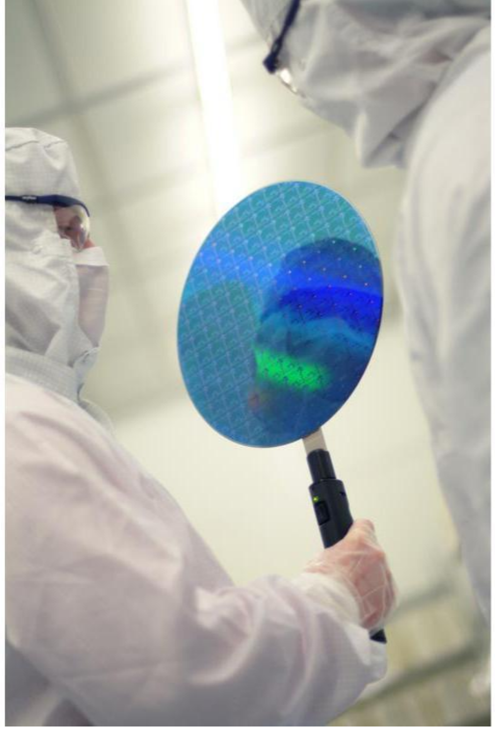
2002-2003
~ 90 nm

~ 16-14 nm

Lithography Enabled Scaling

Materials Enabled Scaling

3D Enabled Scaling



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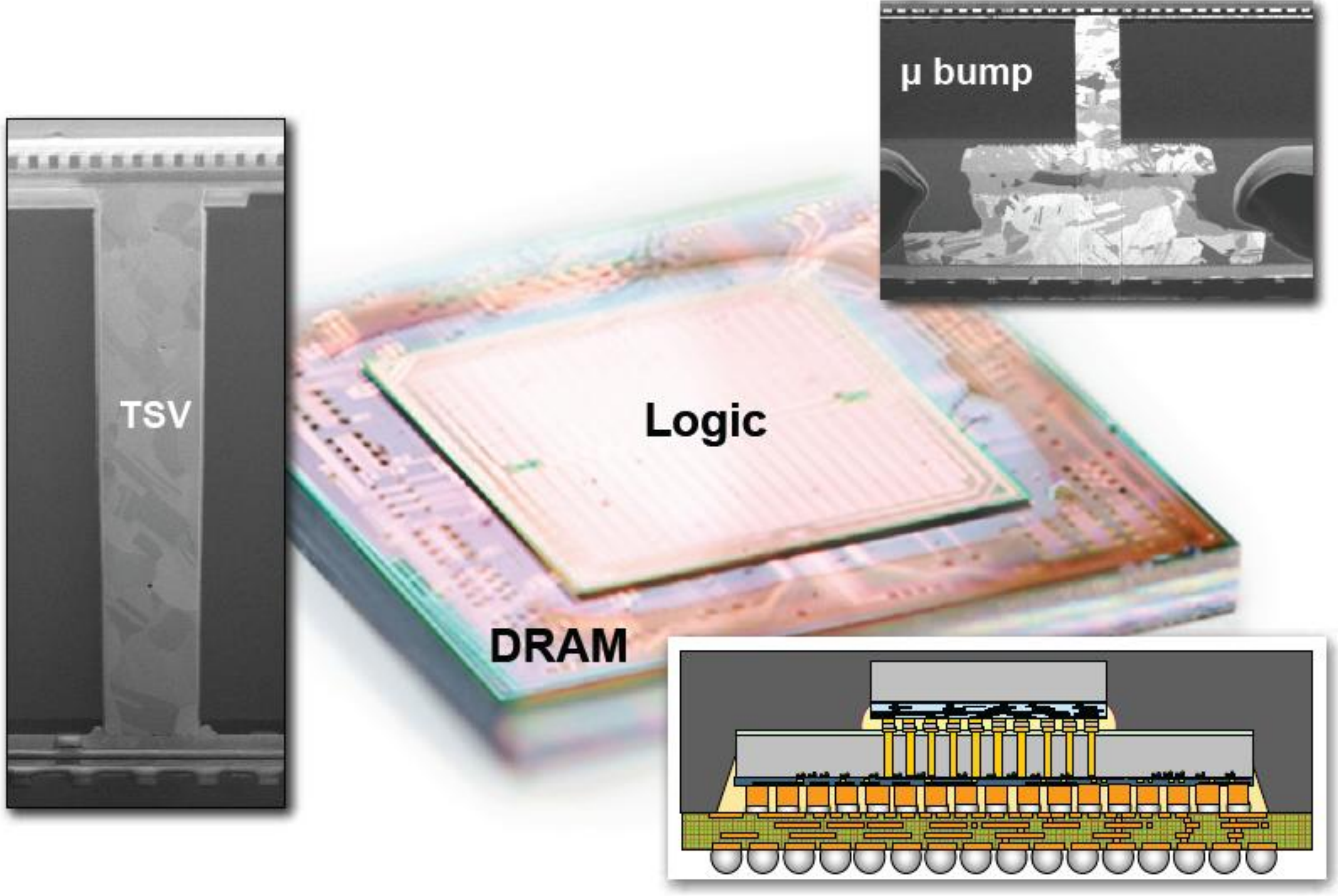
3D stacked interconnect



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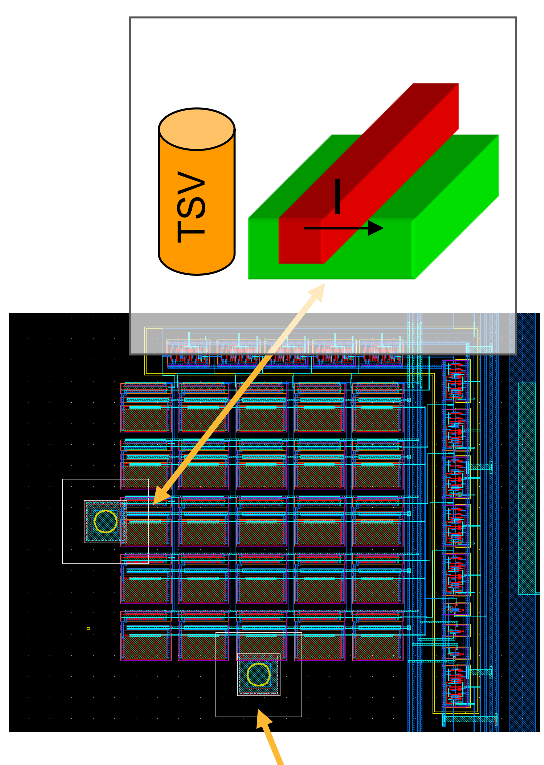
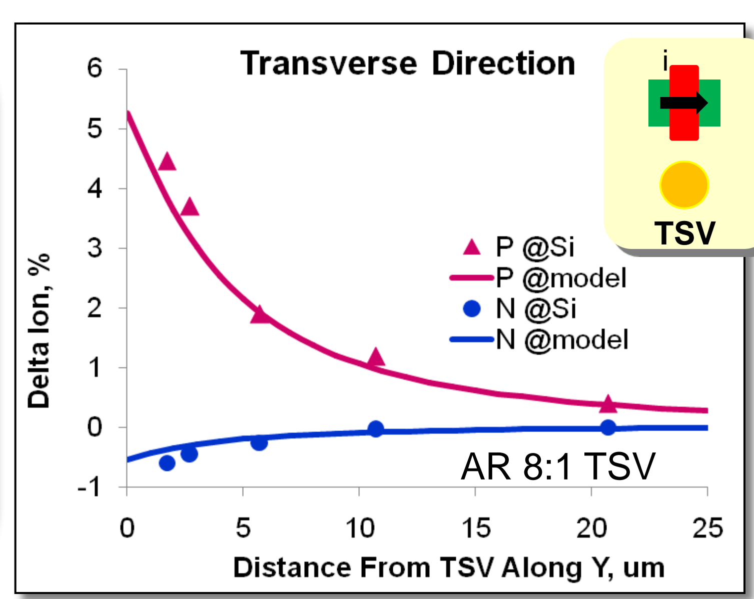
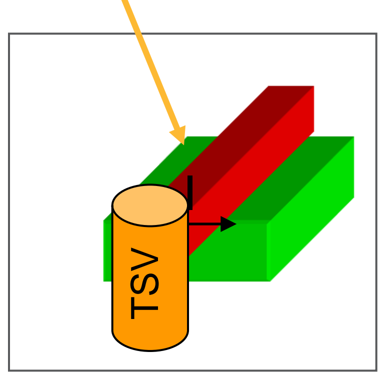
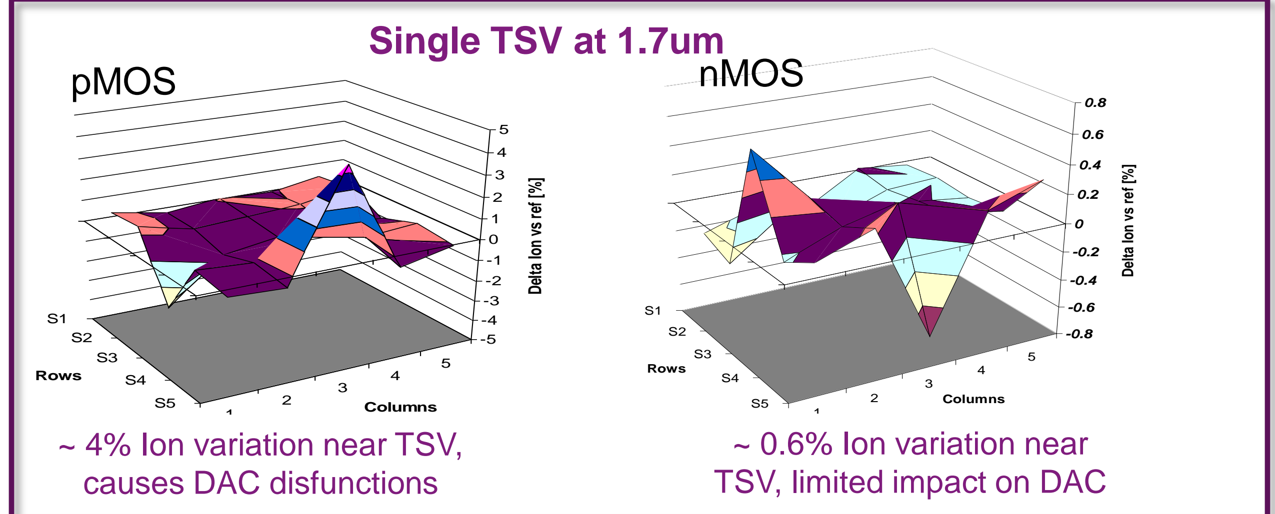
Impact TSV proximity on transistor



Keep-Out-Zone determined to minimize TSV impact on CMOS device using TCAD model in combination with experimental data







~ 4% Ion variation near TSV, causes DAC disfunctions

~ 0.6% Ion variation near TSV, limited impact on DAC

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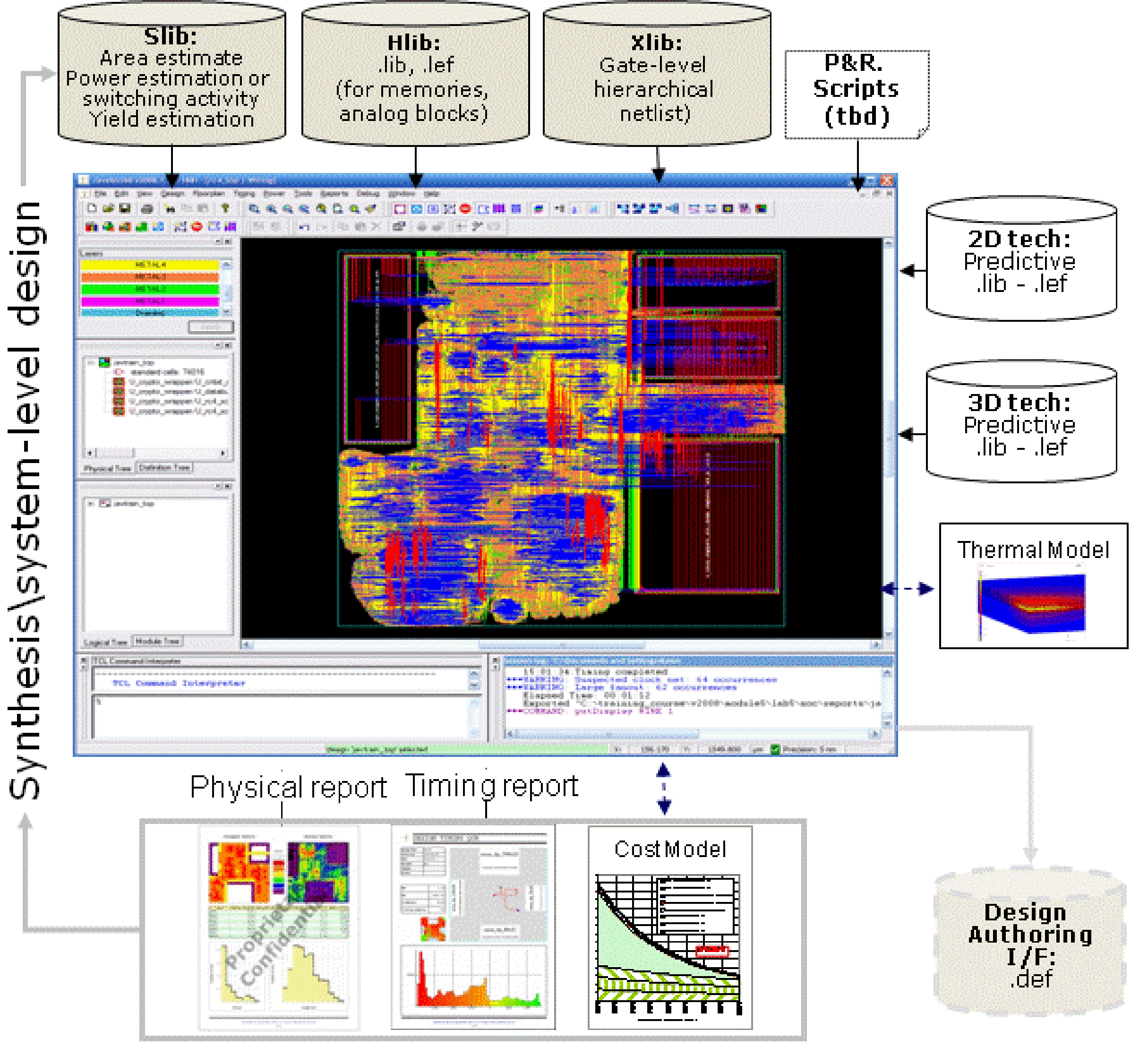
3D Design path finding tool



Path-finding

- Fast prototyping tool trades accuracy for rapid turn-around
- Based on early compact models and design rules
- Output spatially aware estimate of performance and power
- Output data for cost and thermal evaluation
- Output specs for design authoring tools

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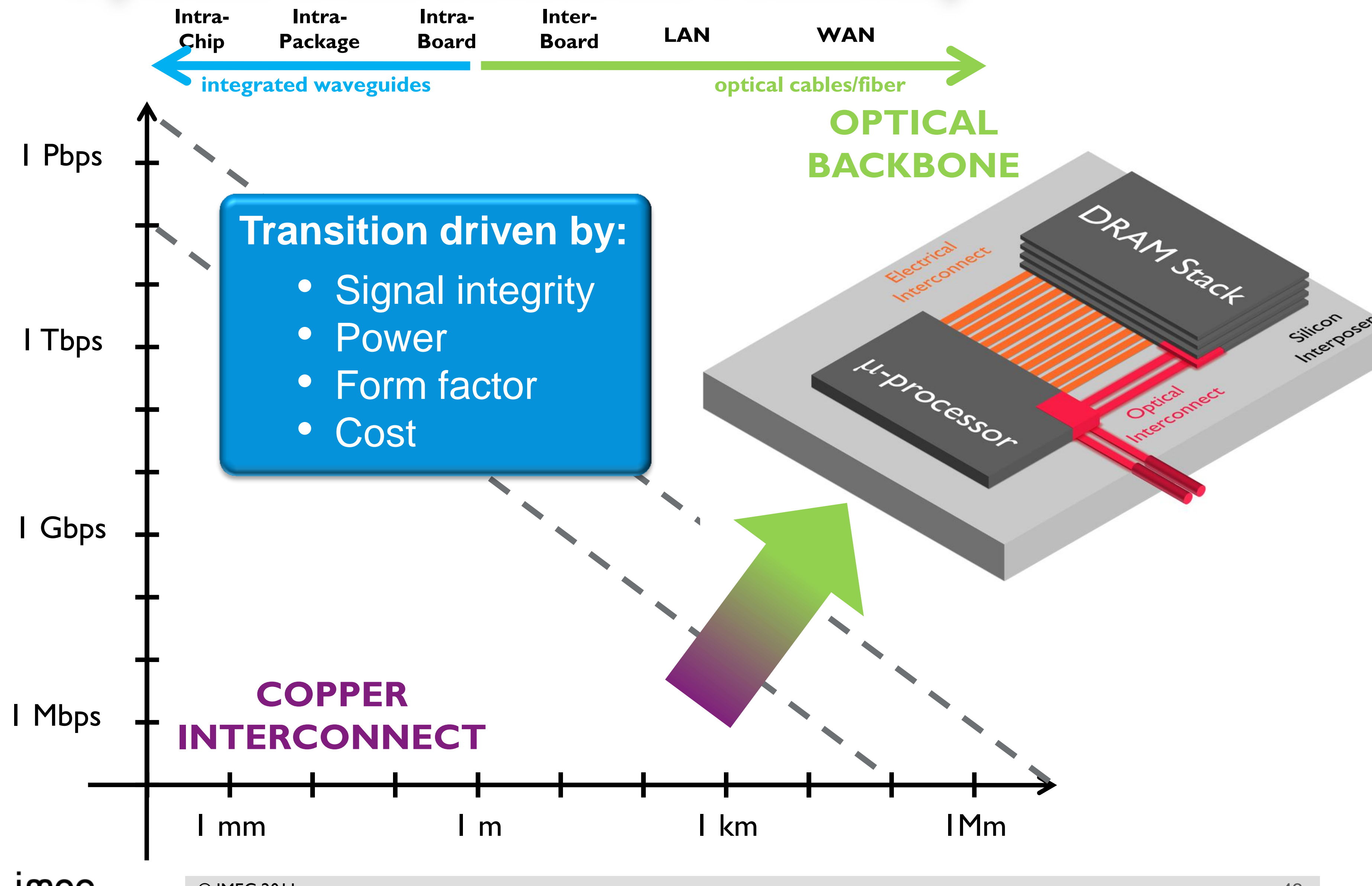
Optical interconnects roadmap



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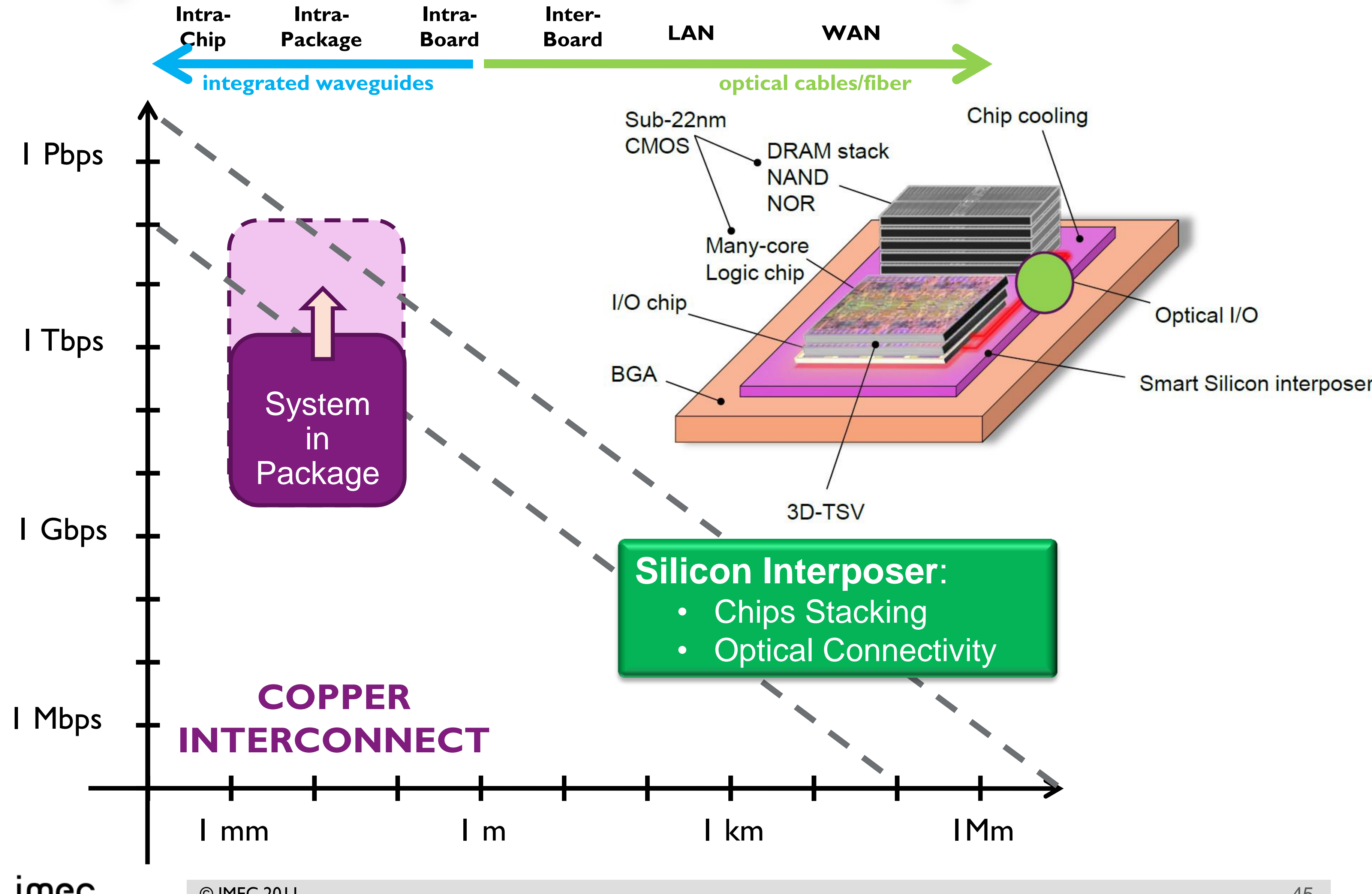
Optical interconnects roadmap



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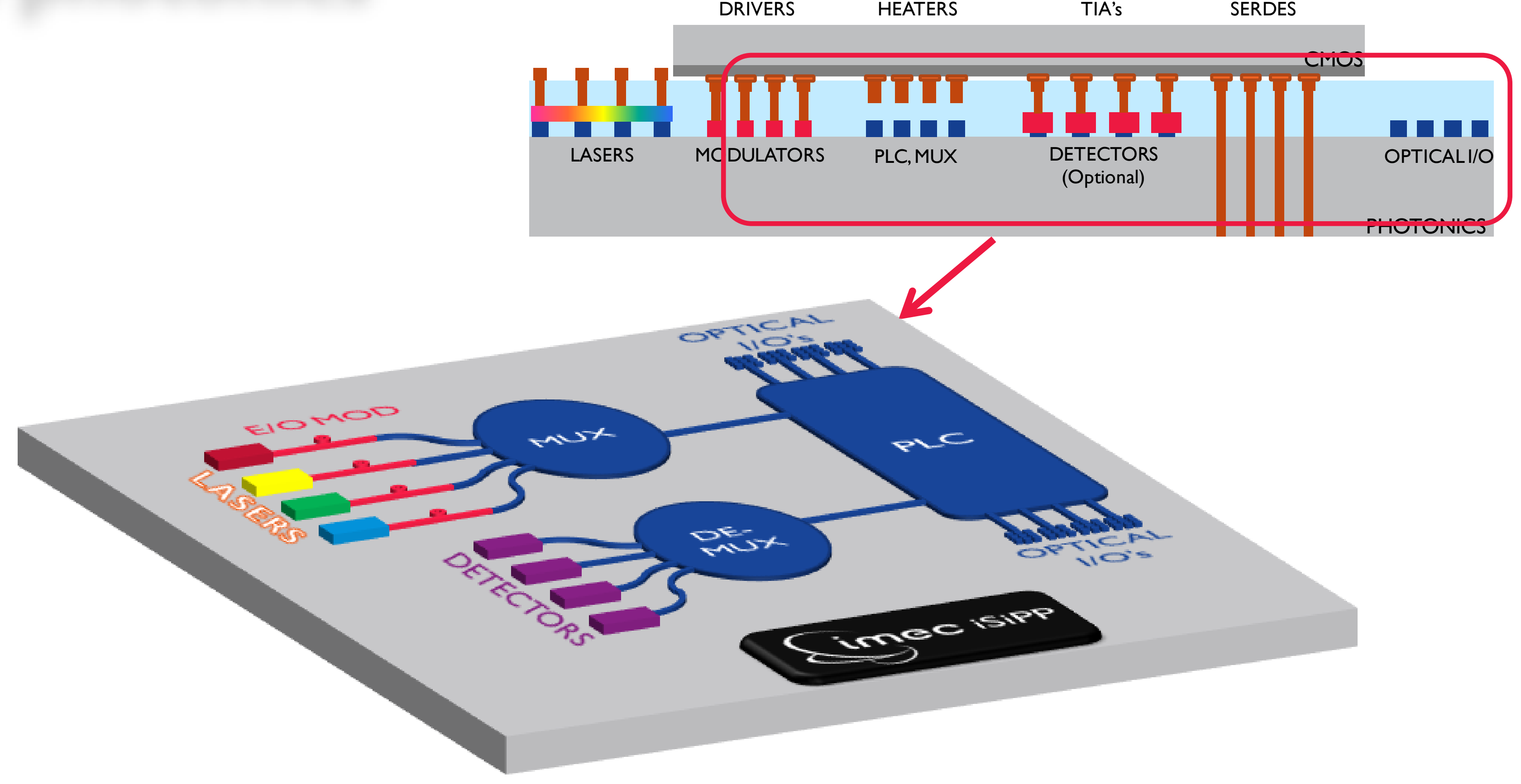
Si photonics



E-O-E transceiver : Key Features

- Single platform integrating all optical functionalities
- CMOS-like fabrication processes
- Small photonics component footprint
- 3D connectivity to CMOS wafers for improved O-E performance

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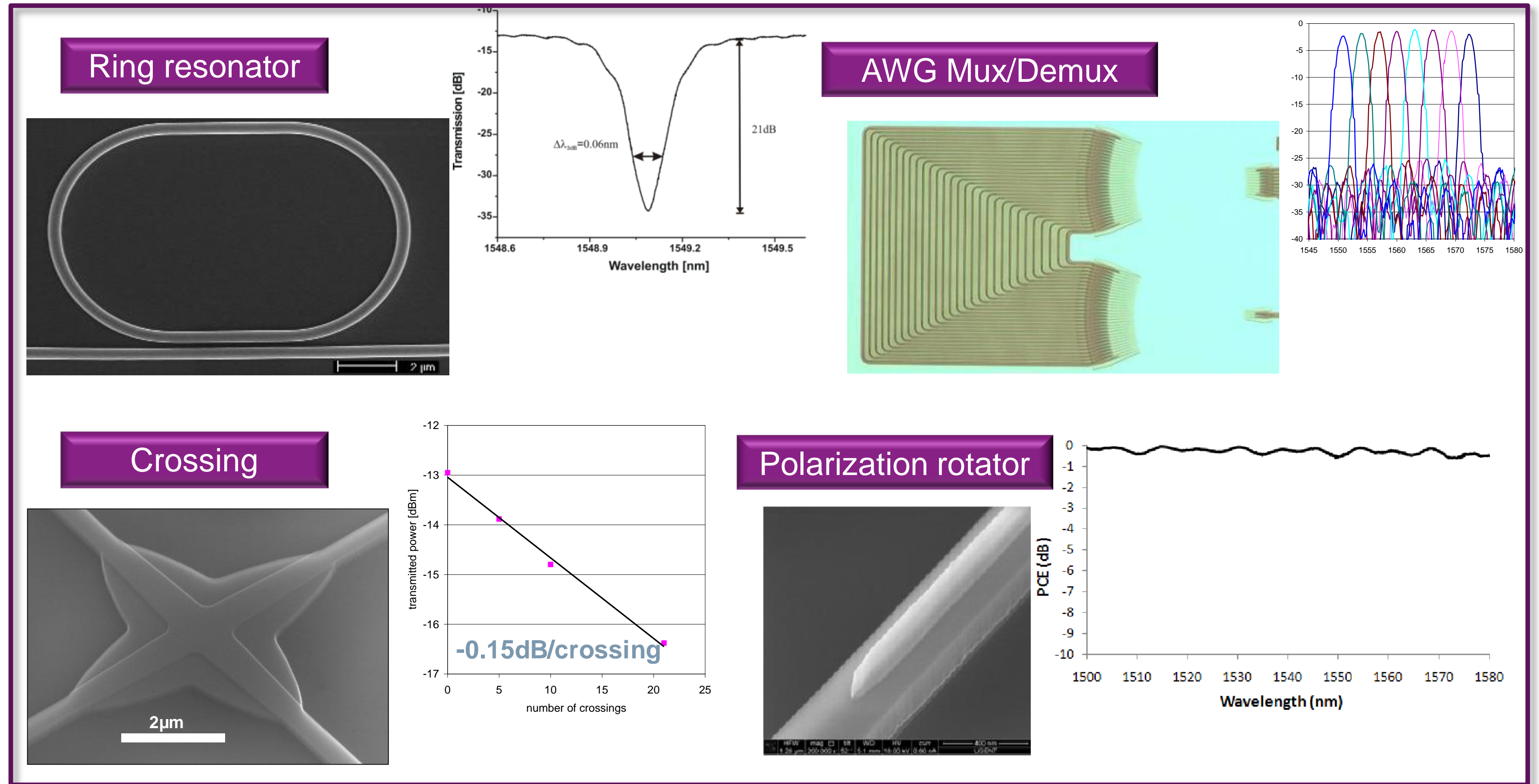
Si photonics
Passive components library



All devices are fabricated on the same platform

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More Moore vs More than Moore

CMOS
CMOS Scaling

Interconnects

Cu

Low k k=3.0

Low k k=2.7

Low k k=2.5

3D SIP

Air gap

3D TSV

FEOL Device roadmap

silicide

USJ

strain

FUSI

HfO_2 high -κ

metal gate

FinFET

Ge/IIIV

time

x-section

100nm

0.099µm²
6T-SRAM

SC22

V_{OUT} (V)

V_{IN} (V)

CMORE
Multi-functional SOC/SIP

Si Photonics

Micro Mirrors

Bio-Electronic interface

CMOS

Thermal sensors

Chemical sensors

Optical detectors

Battery

MEMS

DNA Chip

Image Sensor

RF Chip

Processor

Memory

Source SAMSUNG

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MEMS technology options

For tight integration with driver IC

	SIP: Stacked die	SIP: F2F	SIP: 3D vias	SoC: monolithic
Interconnect pitch	~ 50 um	~10um	~10um	~1um
Interconnect parasitics	few pF	>100fF	<100fF	few fF

Monolithic approach:

- Most compact solution
- Best solution when needing high density interconnect and low parasitics
- Requires compatible die sizes

3D stacking

- Wirebond, flip chip, TSV depending on interconnect density and parasitics
- Offers more choices in MEMS technologies and die size combinations

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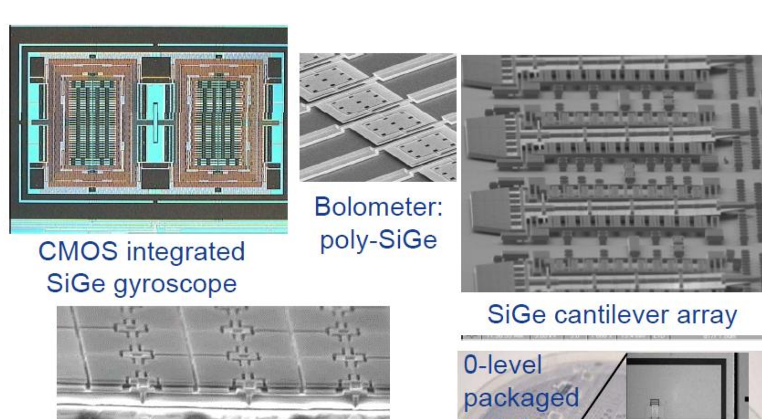
IMEC MEMS last technology

Different above CMOS MEMS approaches		
	Al	**Poly-SiGe**
Post CMOS integration	yes	yes
Fracture strength [GPa]	0.2	> 2
Mechanical Q	low	> 10.000
Reliability	creep: hinge memory effect	No creep



Poly-SiGe:

- better mechanical properties than Al: higher strength and Q factor
- better reliability properties than Al: less creep and fatigue

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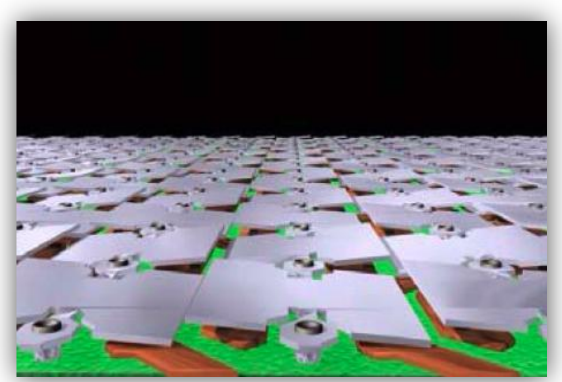
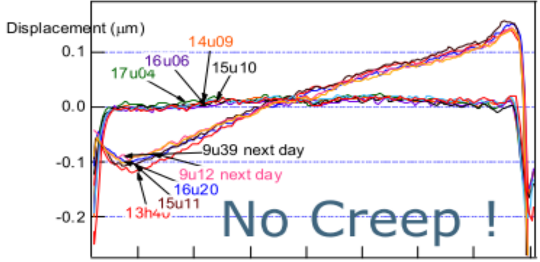
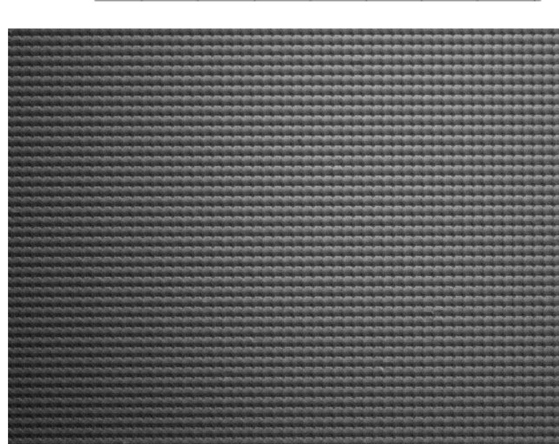
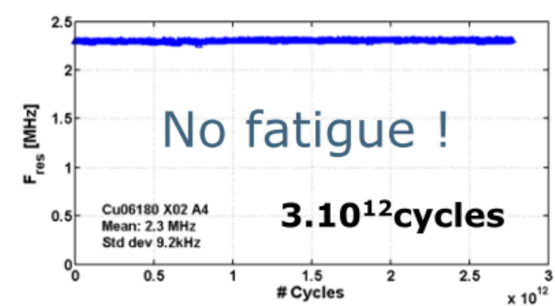
11 Mega pixel micro mirror chip

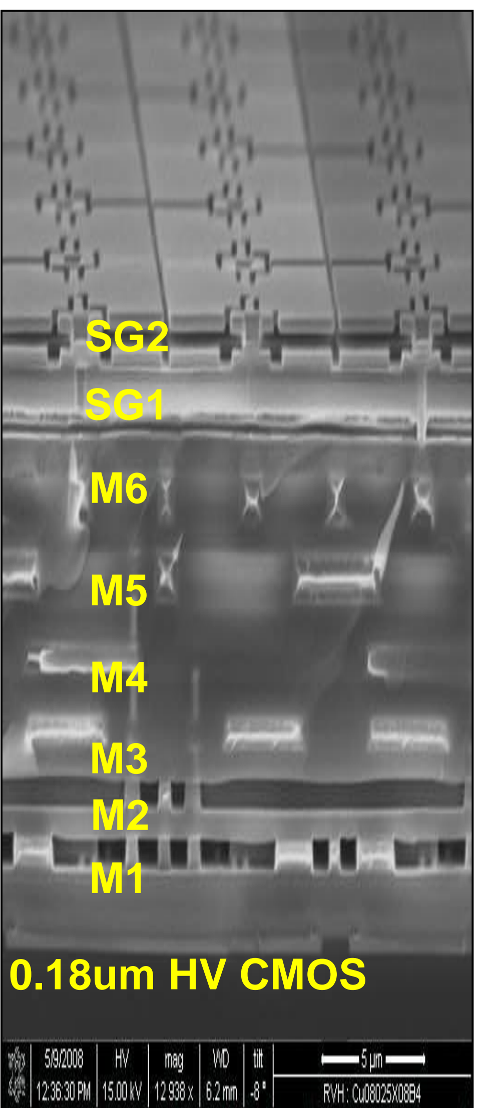


- 11M pixel MEMS + CMOS integration
- 8x8 µm pitch on SiGe platform (Al coating)
- 6 kHz update rate
- Analog tilt angle control
- Extreme mirror flatness <10 nm
- No mirror fatigue & creep









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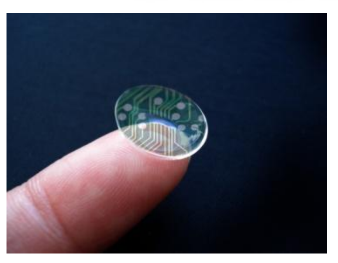
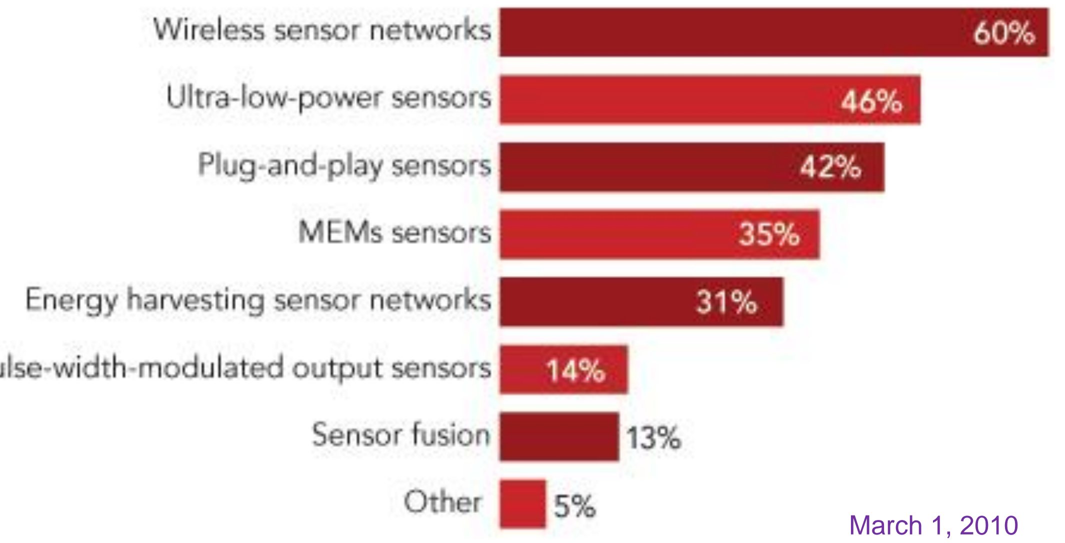
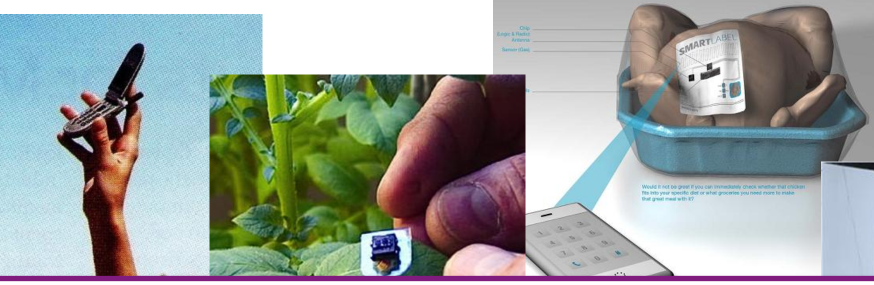
Sensors everywhere



The 2010 Trend Watch Sensor Survey Results



March 1, 2010



McKinsey: "Get Ready For Sensor-Driven Business Models" (March 3, 2010)

Underlying the Internet of Things are technologies such as RFID, sensors and smart-phones

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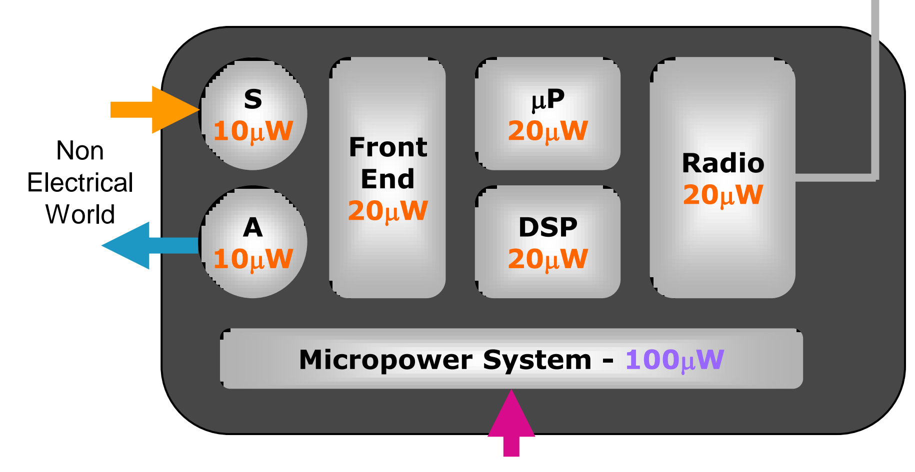
Vision for sensor development

Mission statement:

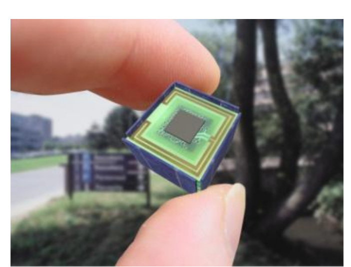
Development of ultra-low power micro/nanosensors for (bio-) chemical detection including the required read-out and driver circuits implemented in standard cleanroom environment

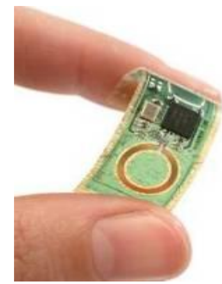
Main targets

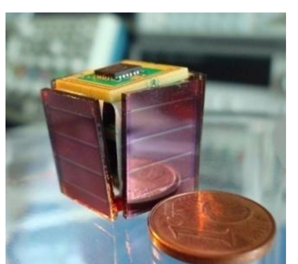
- Increased sensitivity and/or selectivity
- Ultra-low-power (< 20mW)
  → energy autonomous
- Miniaturized integrated sensors
- Cost-effective fabrication



Thermal, Vibrational, RF, Light







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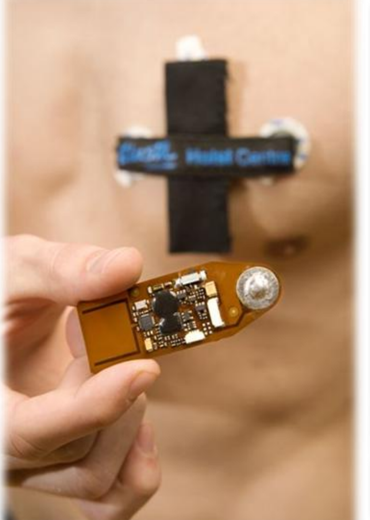
Body area networks examples
Personal healthcare & lifestyle solutions

Necklaces/patches Watch-type Headsets Base Stations



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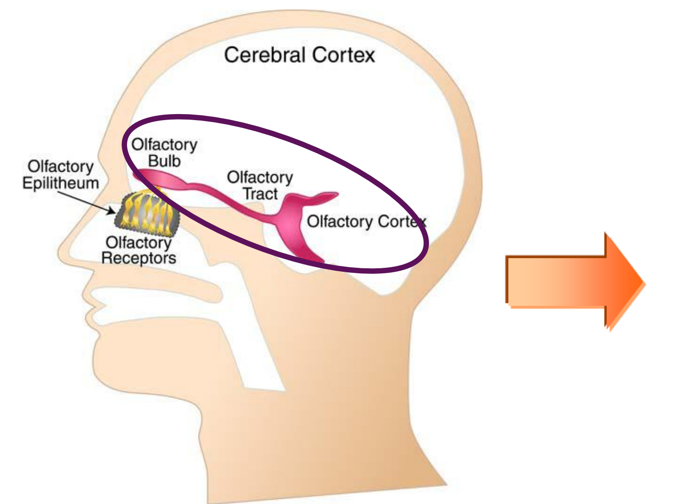
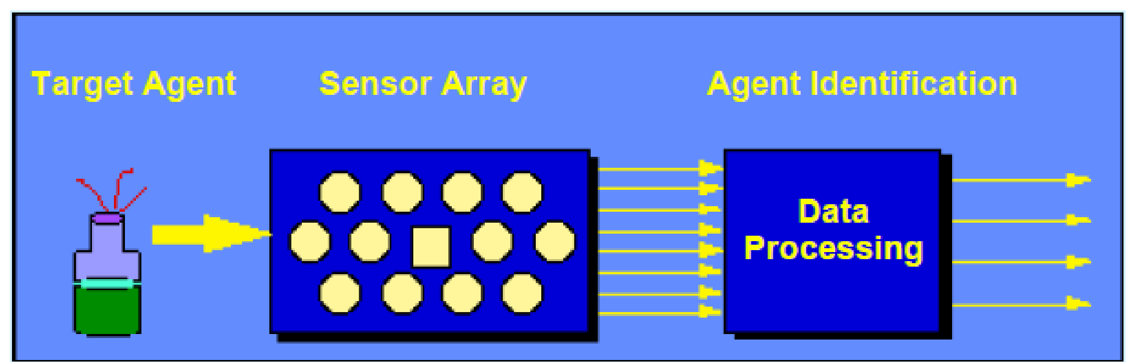
e-Nose
Advanced sensing in complex environments

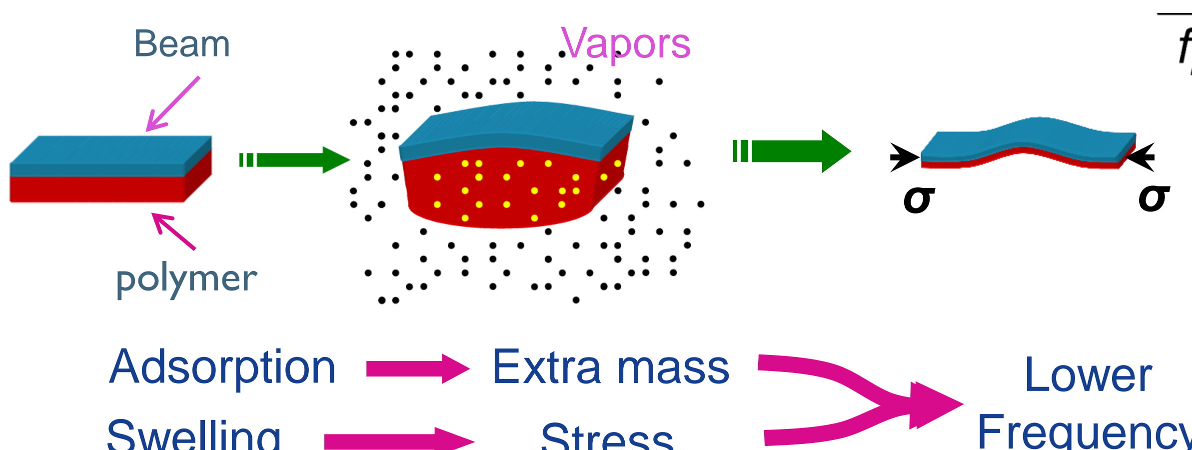
Human olfactory system

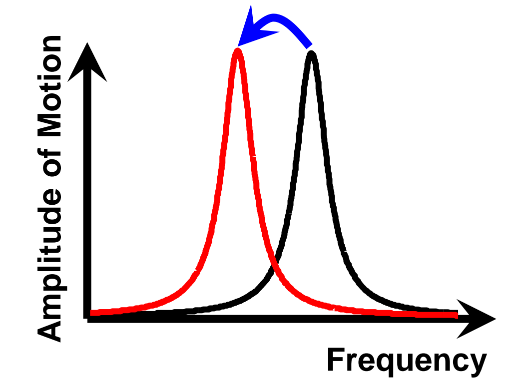


e-nose: array of non-specific, cross-reactive sensors combined with an information processing system

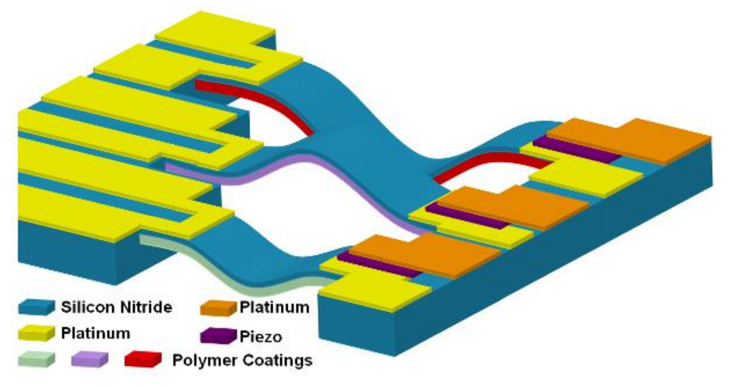


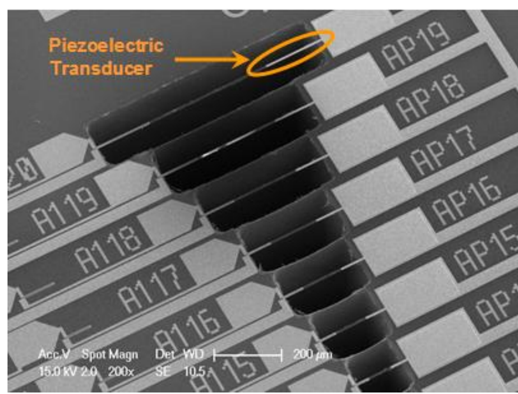
$$\frac{\Delta f_n}{f_n} = \frac{1}{2}\left(-\frac{\Delta m}{m} + \frac{\Delta k}{k} + \frac{\alpha_n \Delta\sigma}{1+\alpha_n\sigma}\right)$$

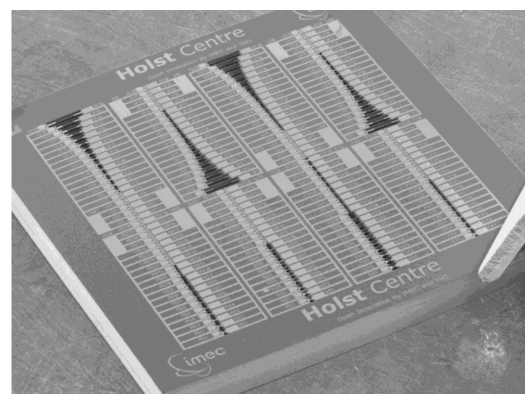




e-Nose: low power is the key







e-Nose: from vision to reality:

Die = 8.8 mm x 8.8 mm, 160 resonators

IBM

500 µm

w **= 100 µm**
L **= 500 µm**
h **= 8 µm**
Coating: PMMA
Detection: Optical Beam

Power = 2 mW

10^{-5} frequency shift / %EtOH

imec

w **= 65 µm**
L **= 750 µm**
h **= 500 nm**
Coating: PMMA
Transduction:
Piezoelectric actuation/detection

Power = 0.00017 mW (170 nW)

2.6 10^{-3} frequency shift / %EtOH

10.000 times more power efficient
260 times responsivity increase

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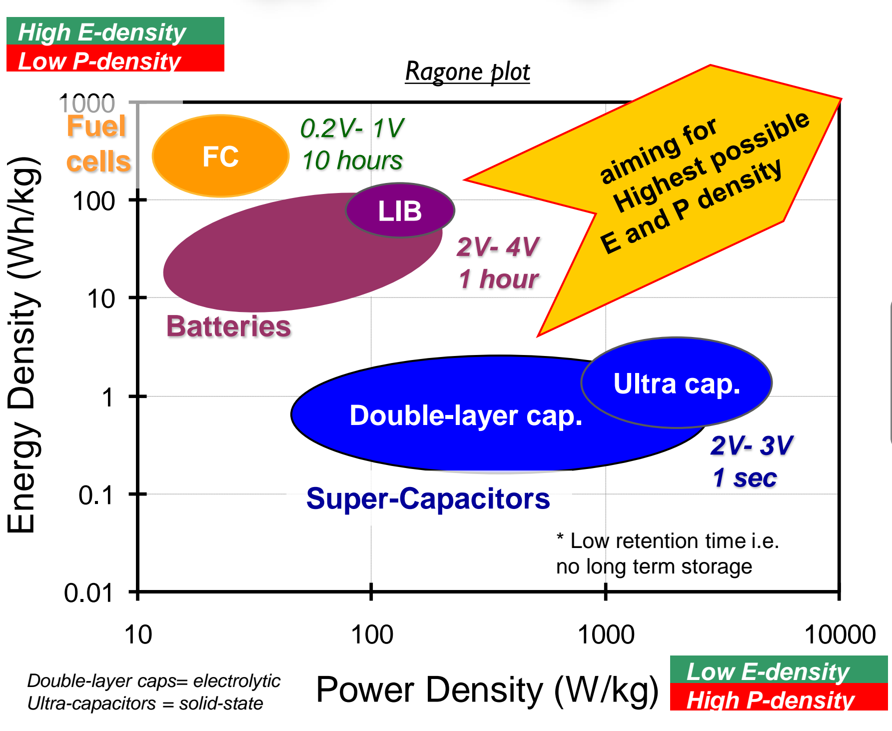
Energy storage



Thin film | **Battery packs**

Miniature
<~1g
<~0.1cm³
10uAh-1mAh
disposable & autonomous systems

Emerging Technologies

Portable
~10-100g
1-10cm³
10mAh-1Ah
portable electronics

Li-ion battery pack:
8cells
14.4V, 73Wh
(5A.h)

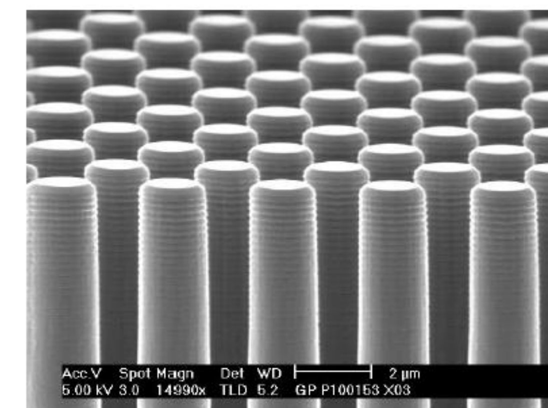
Mobile
~1kg-100kg
0.1-1m³
10Ah-100Ah
automotive transportation

Tesla-Roadster (340km)

Li-ion battery pack:
450kg (200kW)
375V, 56kWh (eq. 8L gaz)
6800 cells (18mmx65mm)

Storage for micro systems:
- All Solid-State devices (integrated systems)
- Microelectronic fabrication techniques

Size determines total capacity:
- High energy density even more important for small form systems



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3D charge storage roadmap and application drivers

Module development:

Application drivers:

Roadmap

Module	Application drivers
3D-TF Ucap	*Decaps on interposer (3D)* *Solid-State Ultracapitors*
3D-TF battery half-cell (wet)	*Prismatic Battery cells targeting high-P with competitive E-density*
Solid electrolytes	*Battery cells targeting durability and safety (extended temperature window)*
SS 3D-TFB	*Battery on foil (large area)* *small-form batteries, micro batteries* *Smart solar modules*
Integrated batteries	Microsystems *Autonomous wireless sensors* (WATS)

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Nano-electronics will continue to drive innovation in many fields.

Societal progress will be enabled by the merger of nano-electronics, nano-technologies, bio sciences and energy efficient technologies.

Global collaboration including entire value chain is required to address the huge R&D challenges.