Recent advances in lithography and high level metrology needs for lithography

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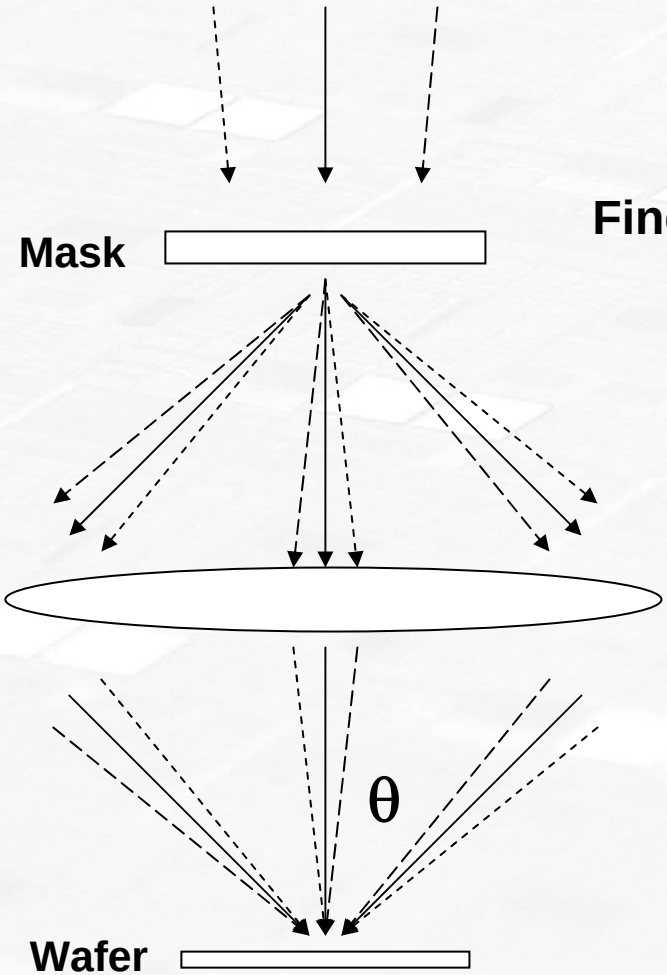
Acknowledge: Ben Bunday Andrew Grenville, Stefan Wurm, Kim Dean, Jonathan Cobb, and Sergei Postnikov

Outline

- Future lithography in next five years
  - Overview of immersion lithography
  - Overview of EUV lithography
- CD and LWR control for lithography
- DFM and metrology needs

Resolution of Optical Lithography



$$HP_{MIN} = k_1 \frac{\lambda}{NA}$$

Finer resolution can be achieved by:

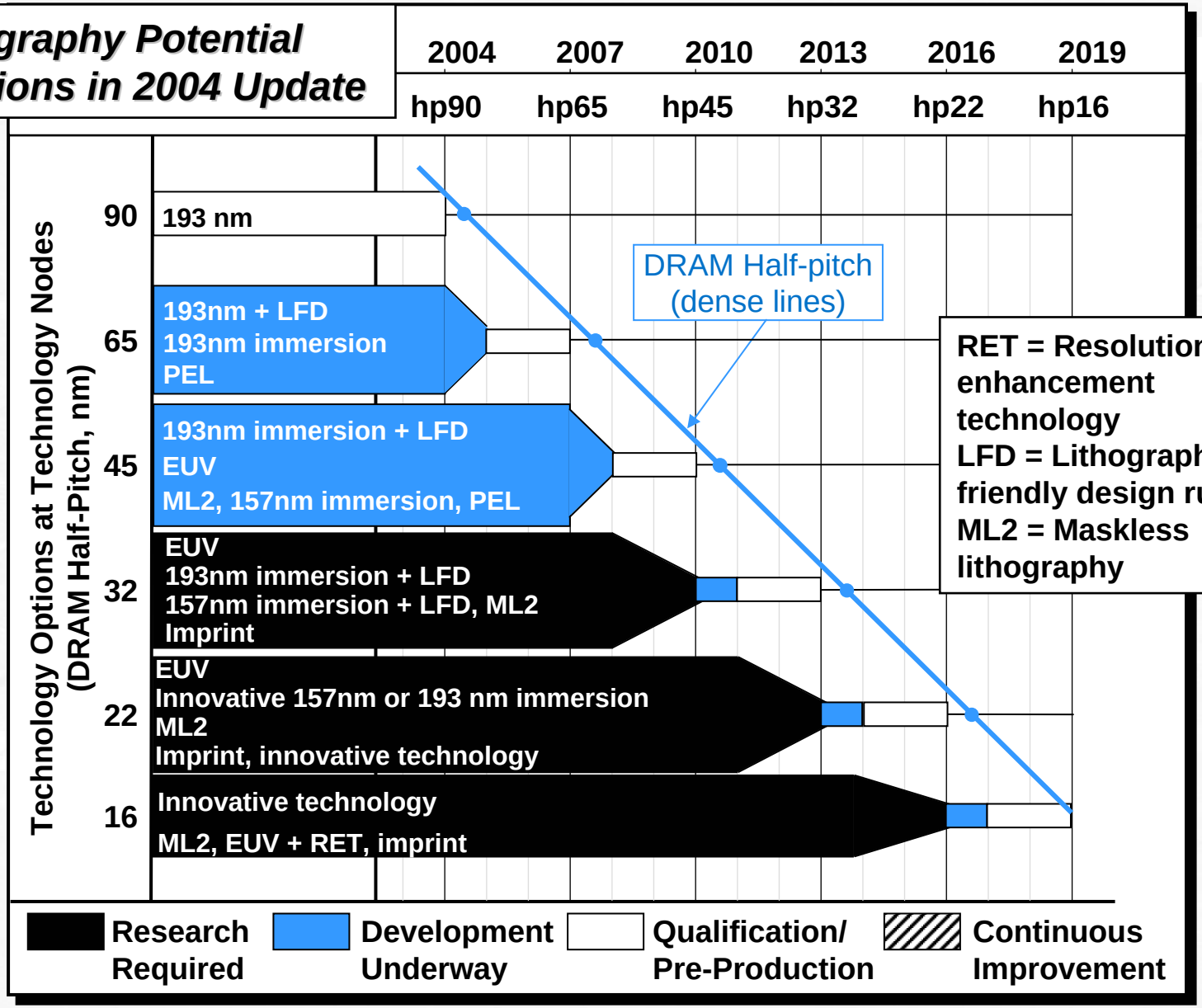
- Shorter wavelength (436 nm…365 nm …248 nm…193 nm…13.5 nm)
- Increased numerical aperture
  - Immersion with NA>1
- Reduced k_1
  - Improved masks (CD control, Phase Shift masks)
  - Improved lenses (aberrations)
  - Better photoresists
  - Better process controls
  - Resolution Enhancement Techniques (RET)

General requirements for lithography

- Critical dimension (CD) control
  - Size of many features in a design needs to be accurate and precise
  - CD control needs to be maintained within each exposure field, over each wafer and from wafer to wafer
- Overlay
  - The placement of the image with respect to underlying layers needs to be accurate on each integrated circuit in all locations
- Defect control
  - The desired pattern must be present in all locations, and no additional patterns should be present.
  - No particles should be added to the wafer during the lithography process.
- Low cost
  - The cost of tools and masks needs to be as low as possible while still meeting the CD control, overlay and defect control requirements
  - The lithography step should be performed as quickly as possible
  - Masks should be used to expose as many wafers as possible
  - Equipment needs to be reliable and ready to expose wafers when needed

Metrology plays a critical role in all of these requirements

Lithography Potential Solutions in 2004 Update



Notes: EPL is a potential solution at the 65, 45 and 32-nm nodes for one geographical region, and PEL is a potential solution at the 32-nm node for one geographical region. RET will be used with all optical lithography solutions, including with immersion; therefore, it is not explicitly noted.

Unofficial version of Figure 34; Not for publication

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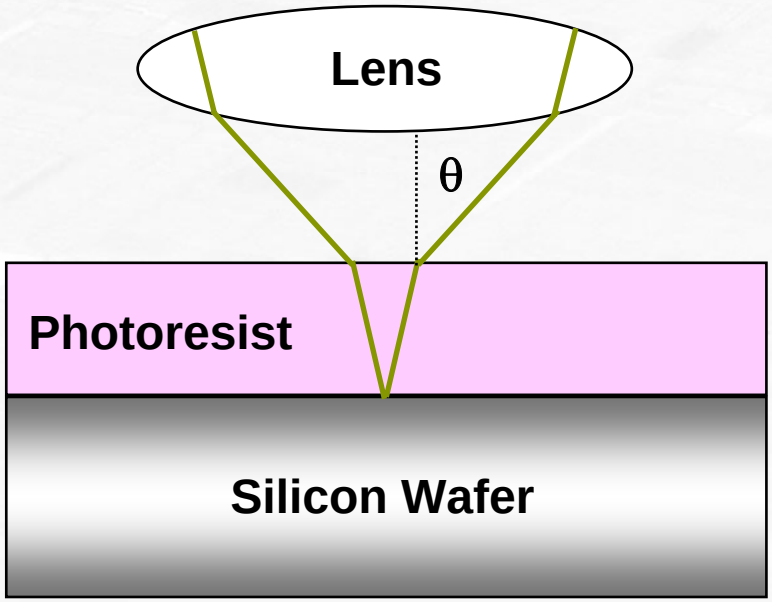
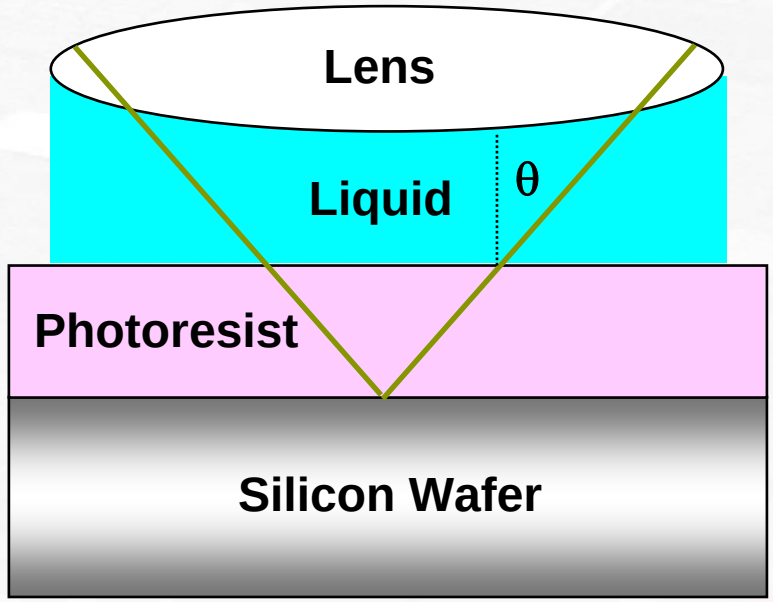
Resolution Improvement by Immersion

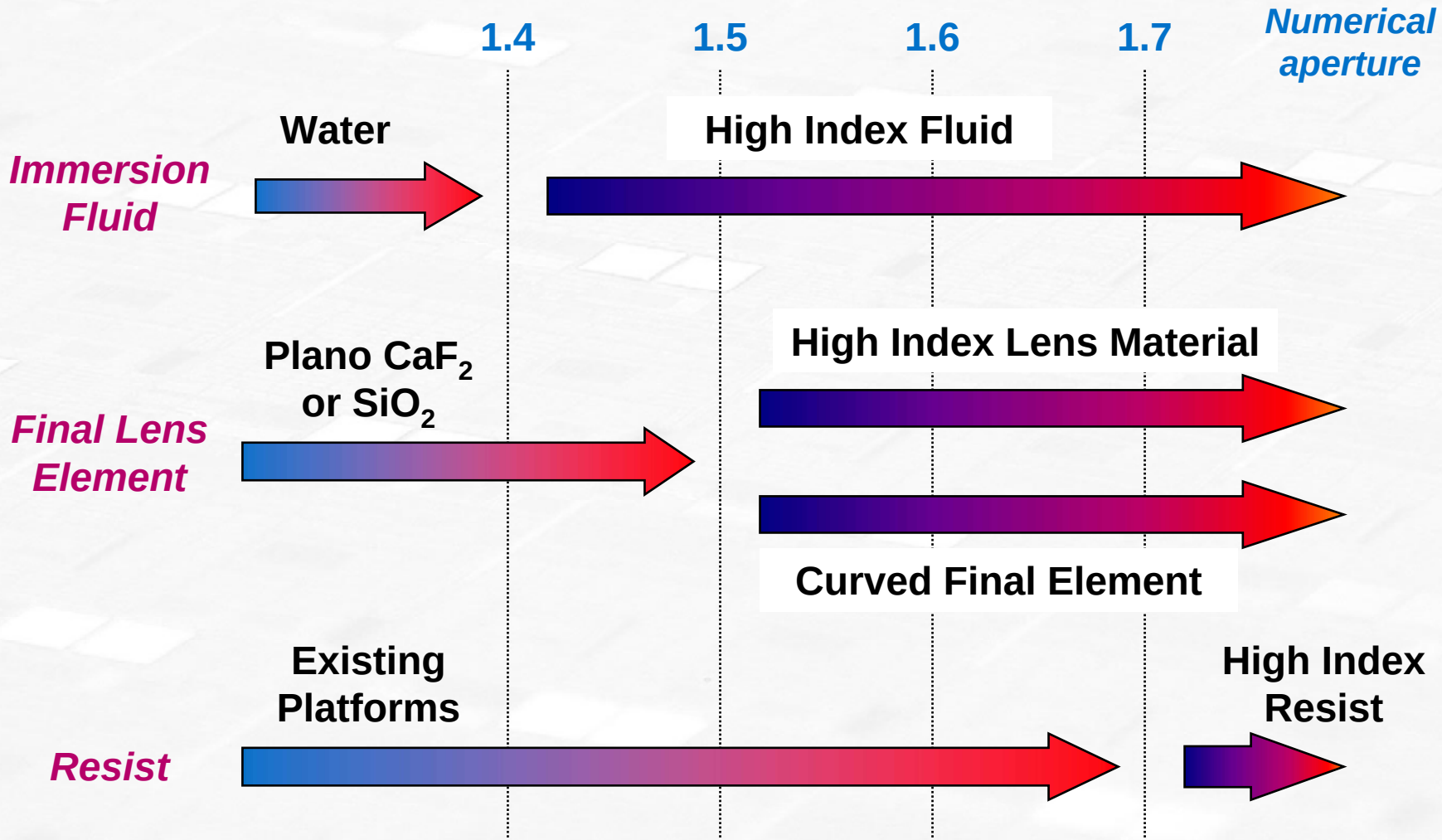
$$HP_{MIN,DRY} = \frac{1}{4}\frac{\lambda_{RESIST}}{\sin\alpha_{RESIST}} = \frac{1}{4}\frac{\lambda_{AIR}/n_{RESIST}}{\sin\theta/n_{RESIST}} = \frac{1}{4}\frac{\lambda_{AIR}}{\sin\theta}$$

$$HP_{MIN,WET} = \frac{1}{4}\frac{\lambda_{RESIST}}{\sin\beta_{RESIST}} = \frac{1}{4}\frac{\lambda_{AIR}/n_{RESIST}}{n_{LIQUID}\sin\theta/n_{RESIST}} = \frac{1}{4}\frac{\lambda_{AIR}}{\sin\theta}\Big/ n_{LIQUID}$$





Enabling NA > 1.3



Earlier increase in index of fluid and/or resist yields process latitude improvement

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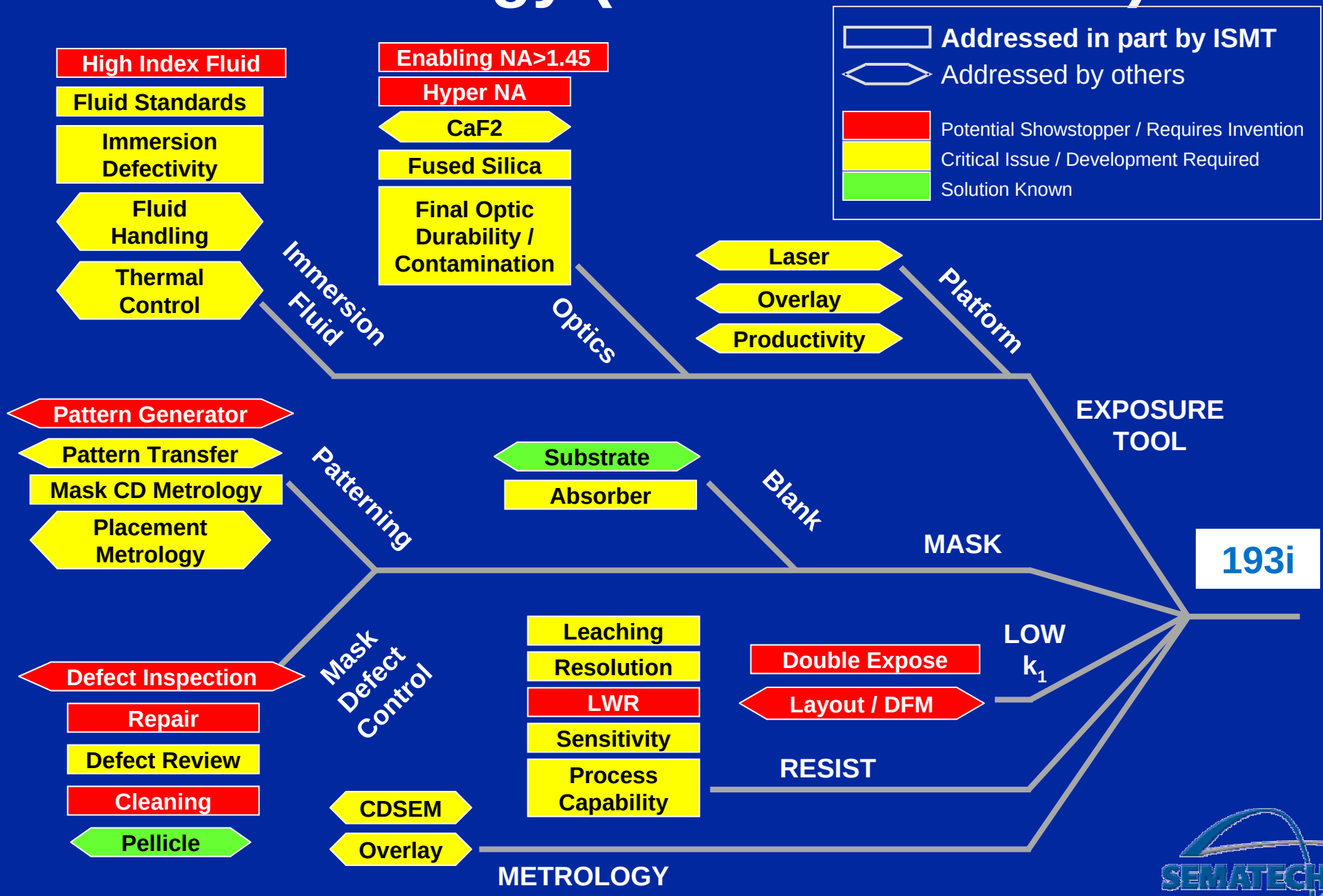
193i Technology (45nm Half Pitch)



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Extreme Ultraviolet Lithography (EUV)

λ = 13.5 nm

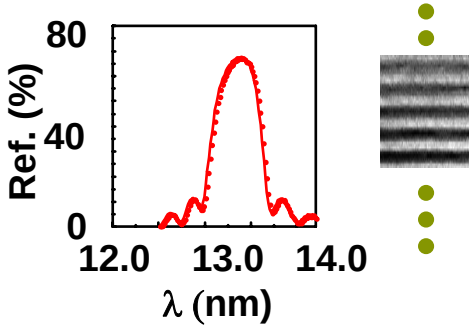
Ring Field Illumination
Scanning mask and wafer stages
Flat, square mask with multilayers

Reflective Reticle

Laser Produced Plasma

Laser

All optics surfaces coated with multilayer reflectors (40 - 80 layer pairs, each layer approx $\lambda/4$ thick, Control ~0.1 Å)

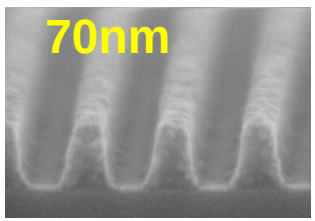


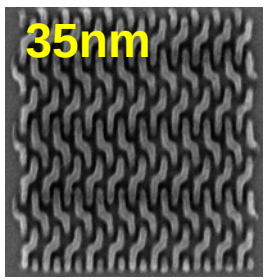
Condenser Optics

4X Reduction Optics

Wafer

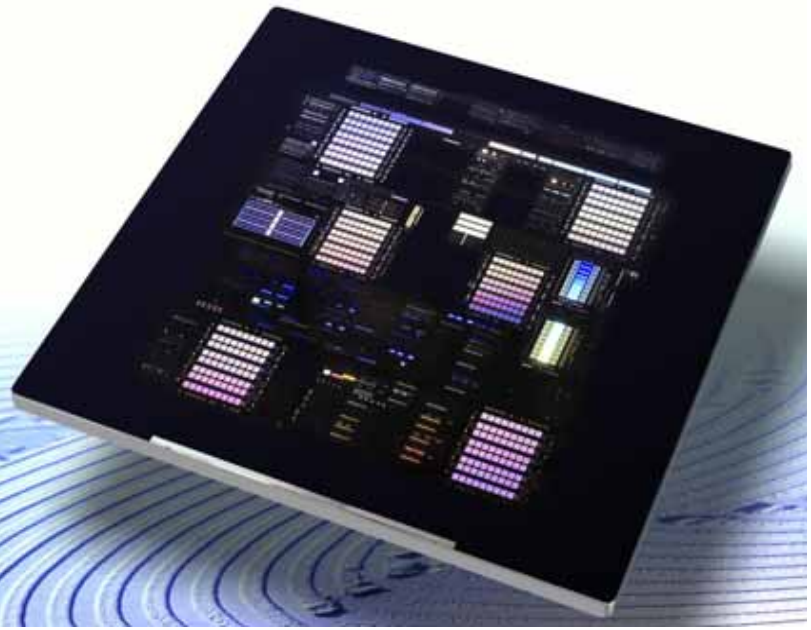
EUV imaging with ultrathin resist (UTR)



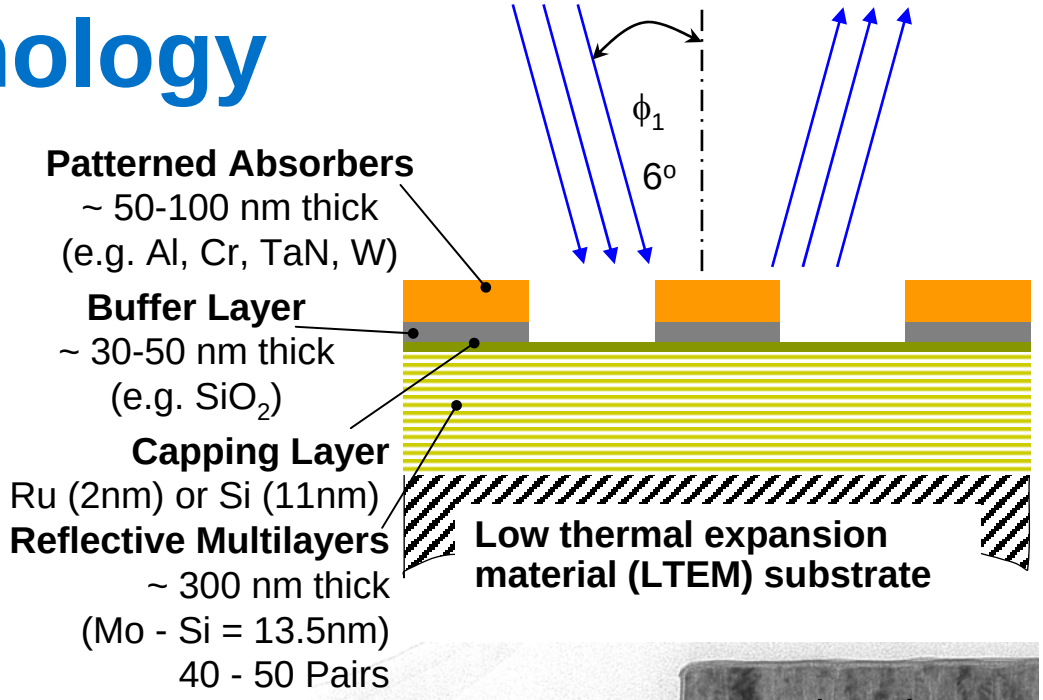


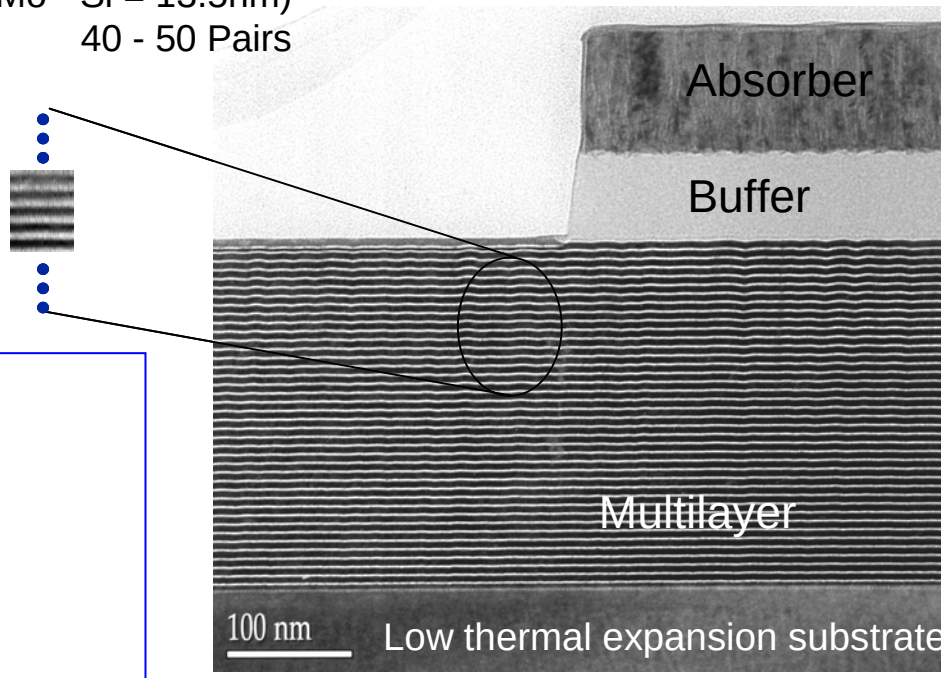
Reflective Optical Surfaces are Aspheric with Surface Figures & Roughness < 3 Å

EUV Mask Technology



Full Field 6” EUV Mask with 100-nm node CMOS
Multilayers: Mo - Si
Absorber Stack: Cr/SiON
120 mm x 104 mm field size
(Courtesy of P. Mangat & S. Hector, Motorola)

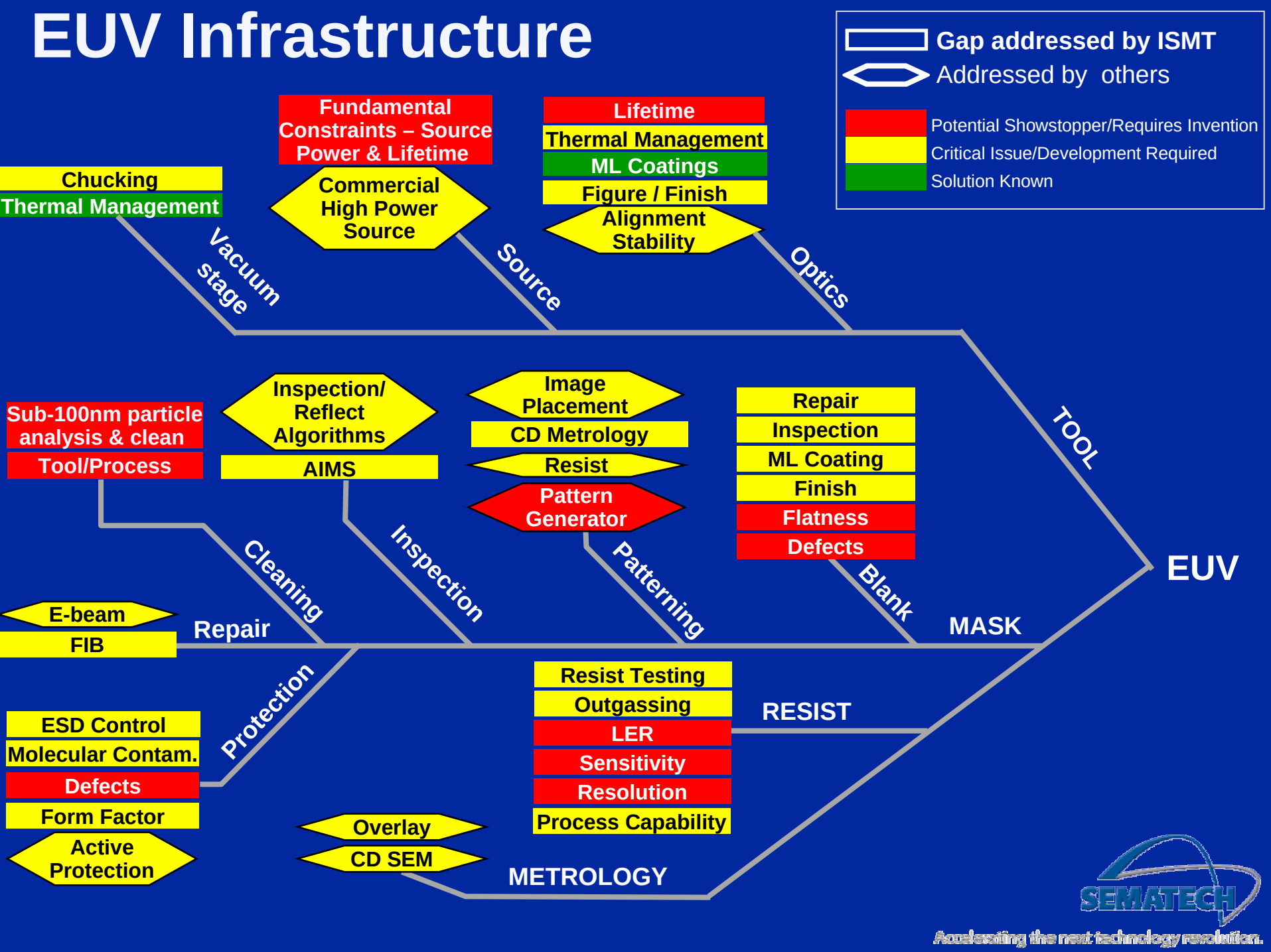




TEM courtesy of AMD

- Key challenges for EUV mask multilayers
  - High uniformity of thickness
  - No printable defects
  - Temperature stability

EUV Infrastructure



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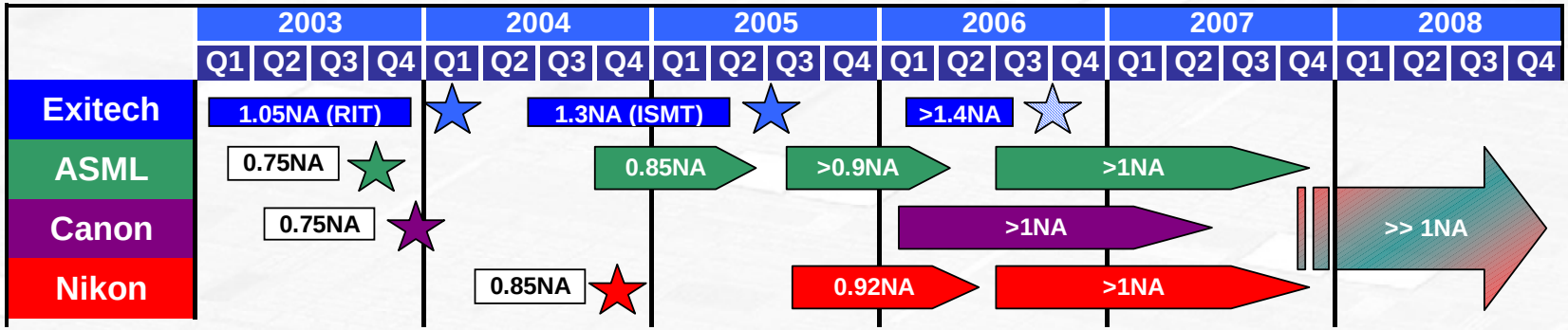
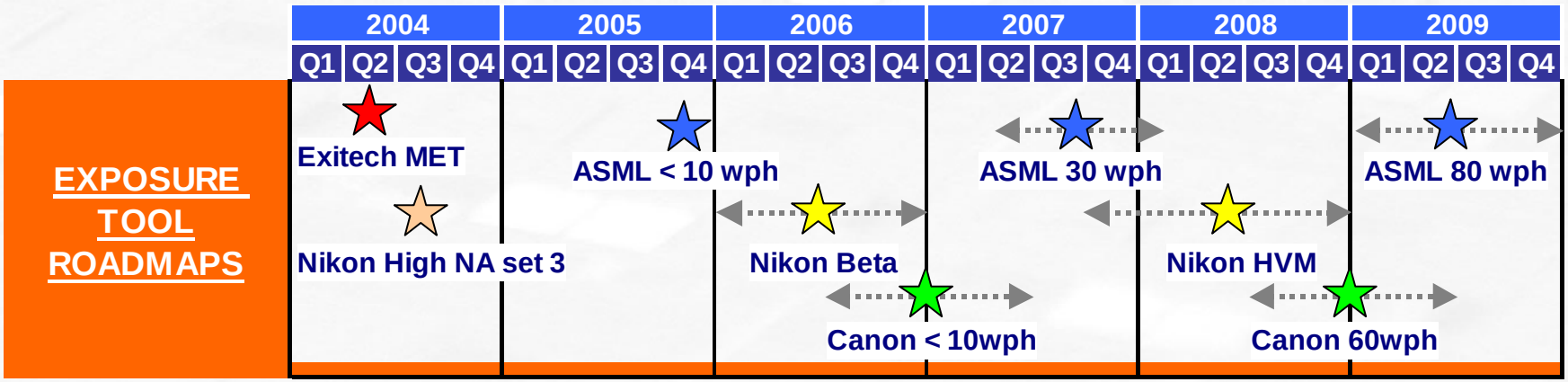
Immersion and EUV tool timing

193 immersion



EUV



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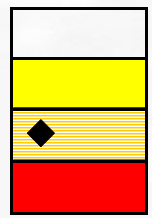
2004 ITRS lithography requirements are challenging

Year of Production	*2004*	*2007*	*2010*	*2013*	*2016*
Technology Node	*hp90*	*hp65*	*hp45*	*hp32*	*hp22*
DRAM ½ Pitch (nm)	90	65	45	32	22
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	107	76	54	38	27
MPU Gate in resist Length (nm)	53	35	25	18	13
MPU Gate Length after etch (nm)	37	25	18	13	9
Gate CD control (3 sigma) (nm)	3.3	2.2	1.6	1.2	0.8
Overlay	32	23	18	13	8.8
Mask CD uniformity (nm, 3 sigma) isolated lines (MPU gates), binary mask	3.8	2.2	2	1.3	0.5
Line Width Roughness (nm, 3 sigma) <8% of CD	4.2	2.8	2	1.4	1

- Gate CD control is intended to represent total CD variation
  - Is it possible to meet the desired gate CD control values?

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known



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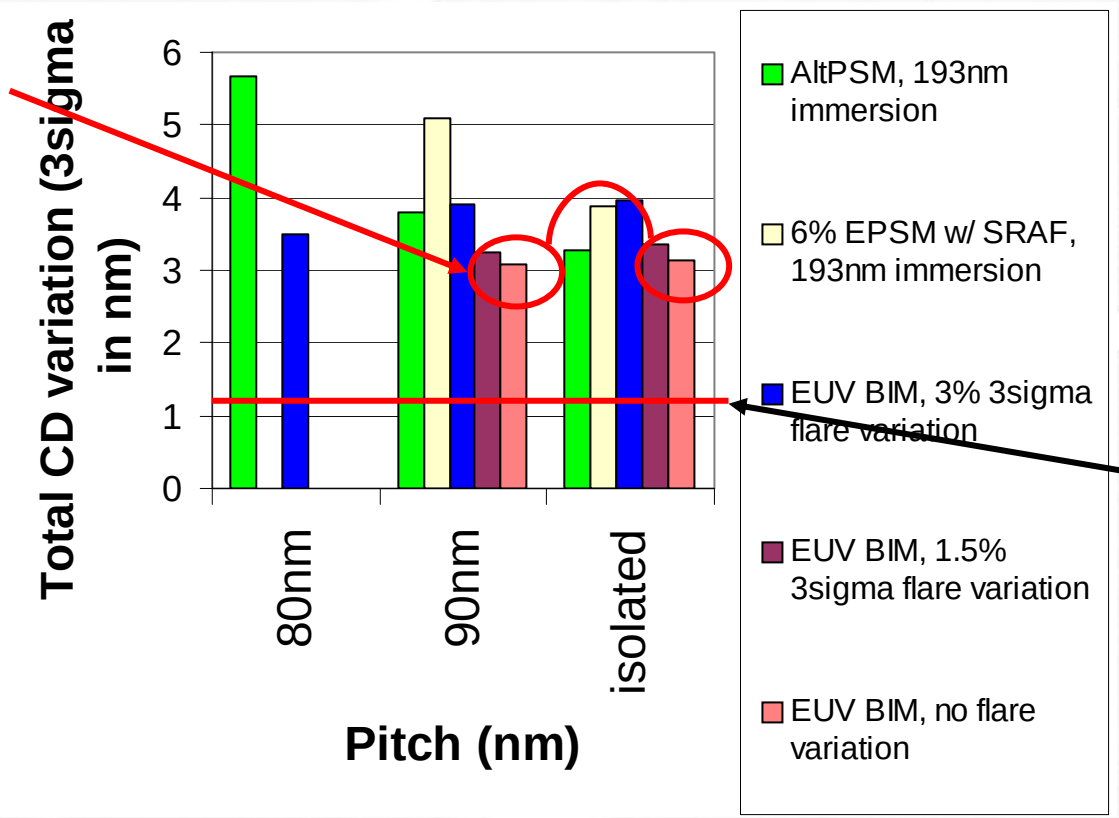
Major CD error sources

- Intrafield
  - Dose uniformity
  - Focus uniformity
  - Aberration variation within the field
  - Mask CD uniformity
  - Imperfect optical proximity correction (OPC)
  - Flare variation for EUV
- Interfield
  - PEB temperature variations
  - Dose variation
  - Mean focus variation

Metrology critical to identifying and reducing systematic errors

Calculated CD variation at 45nm half pitch

No flare variation



MEEF	
Dense	1.94
Iso	0.36
Dense	1.63
Iso	1.33
Dense	1.06
Iso	1.12

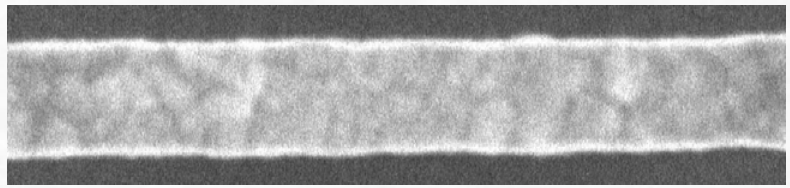
ITRS 2004: 1.2 nm 3σ

- Both 193nm immersion and EUV (k_1=0.83) will probably not meet ITRS requirements
- Under near ideal optical lithography conditions, 193nm immersion at near maximum NA with water (k_1=0.31) with AltPSM may provide better CD control if EUV flare variation is not fully compensated

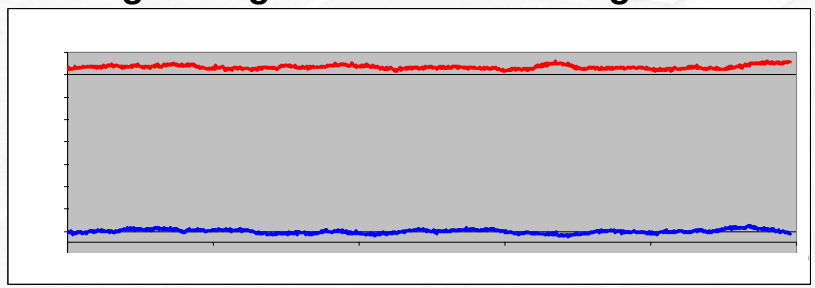
Importance of Line Edge and Width Roughness

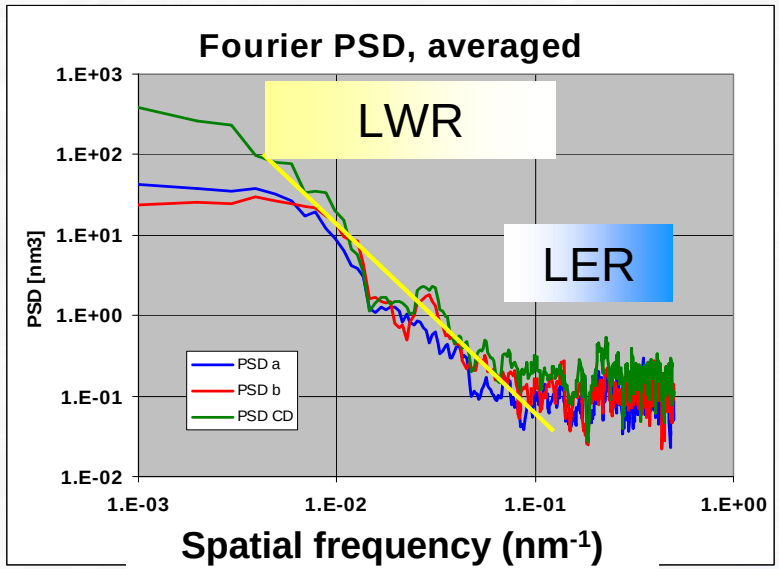
- Line Edge Roughness (LER)
  (High frequency roughness)
  - Can affect dopant concentration profiles
  - Probably affects interconnect resistance
- Line Width Roughness (LWR)
  (Mid-frequency roughness)
  - Leakage of transistors affected
  - Affects device speed of individual transistors
  - Leads to IC timing issues

Example: poly-silicon line

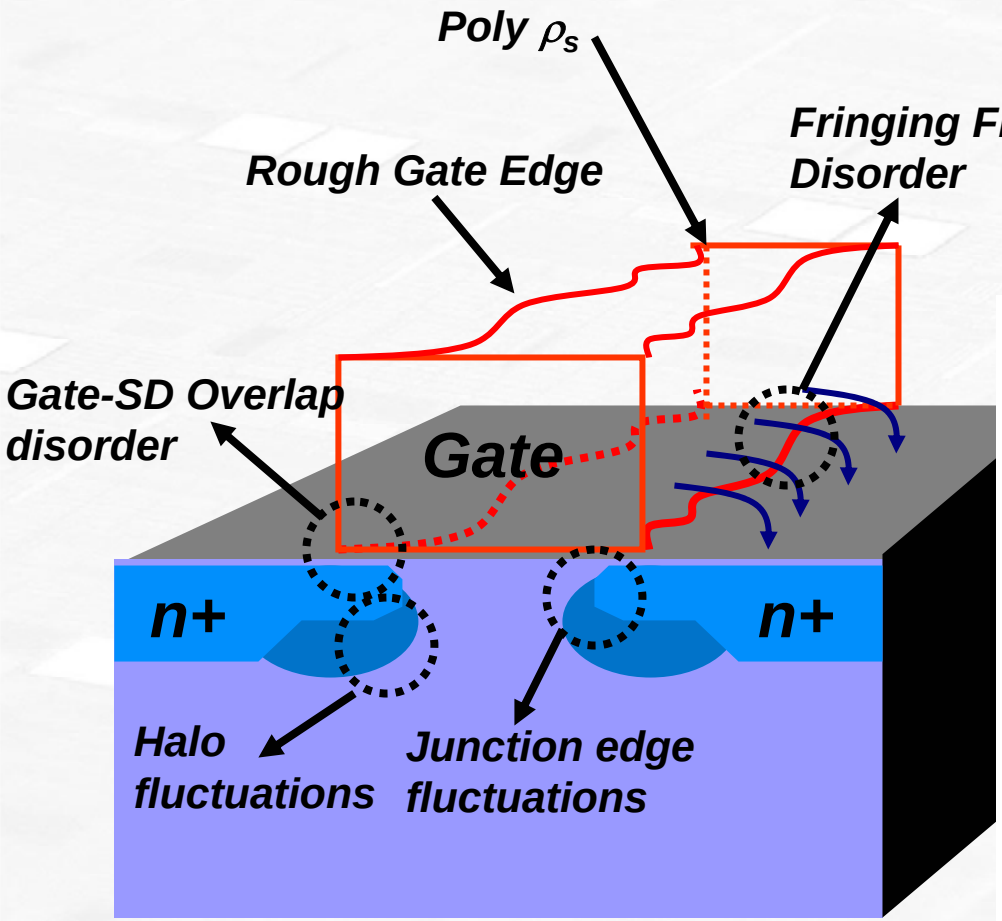


Edge assignment from SEM algorithm

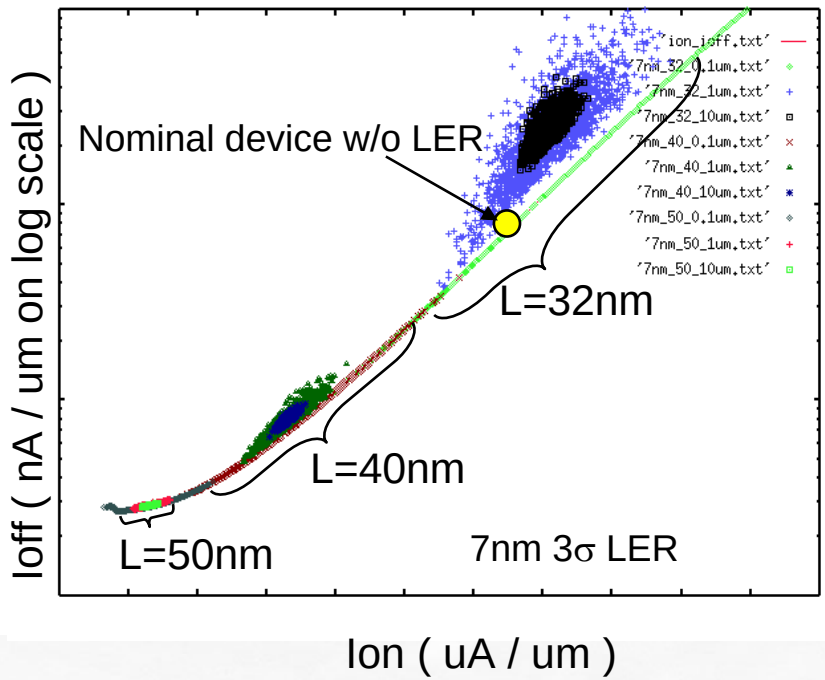




Areas of potential device impact



- Front end patterning
  - LWR after etch is what matters, not LWR in resist
  - LWR affects leakage current more strongly than drive current



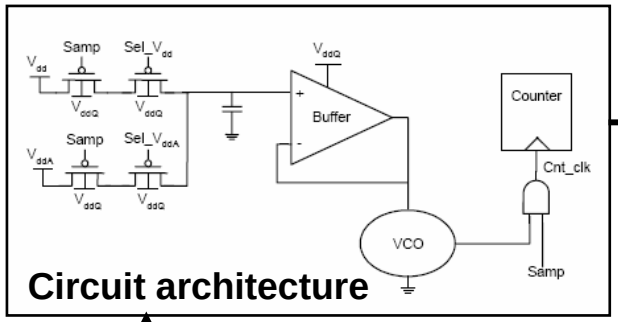
Eric Verret, Aaron Thean and Jonathan Cobb; Freescale Semiconductor

Trends to manage CD control and yield

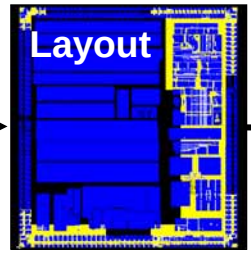
- Present approaches are not enough
  - More stringent design rule restrictions
  - Single orientation, pitch restrictions
  - Larger CD on resist
  - Relaxed minimum half pitch
  - Use of resolution enhancement technology (RET)
  - Field by field and within field dose corrections
- Further actions--DFM
  - Automation of software analysis of weak spots in design and feedback to physical layout of cells
    - RET applied to library cell layouts
  - Coordinates of weak points provided to mask and wafer CD metrology tools
    - Focus and exposure are optimized for printing hot spot regions with maximum process latitude rather than for CD of CD bars.
  - Identification of critical timing paths to locally specify CD control
  - Test programs optimized to detect electrical effects at weak points
  - Local corrections of mask to account for variations of scanner—mask specification to particular scanners
  - Software for reduction of slivers in design data is also being developed to reduce mask CD error and writing time.

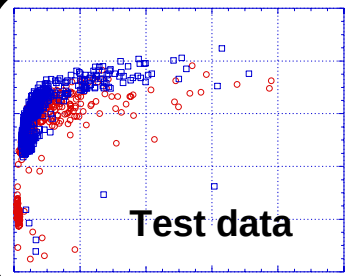
Based on IBM, Intel, ASML and Toshiba presentations at SPIE and PMJ

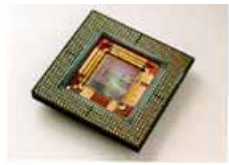
Present mode of operation for circuit design and fabrication



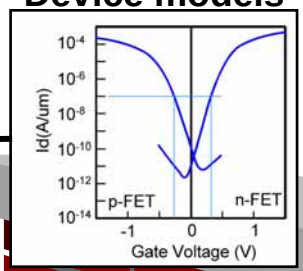
Circuit architecture



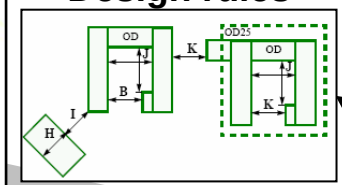


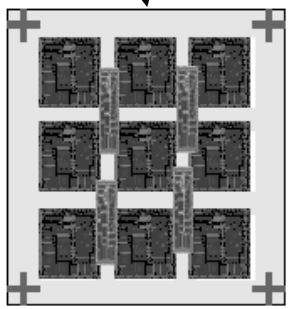

Packaged IC

Device models



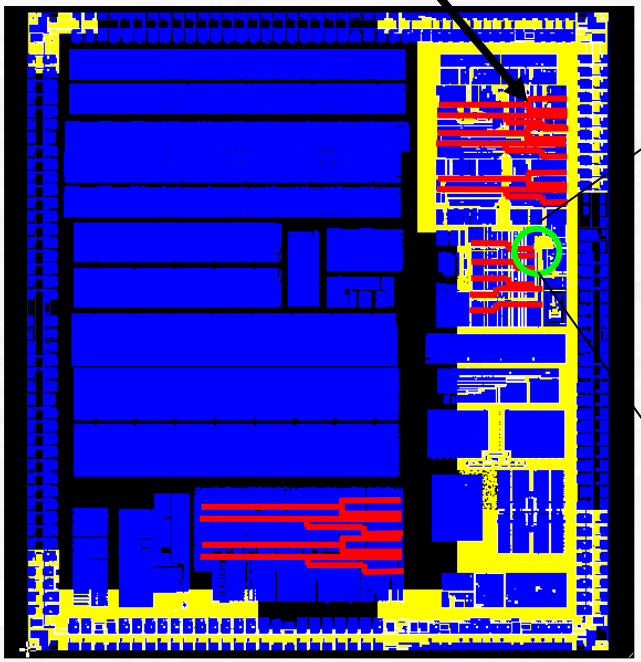
Design rules




Masks

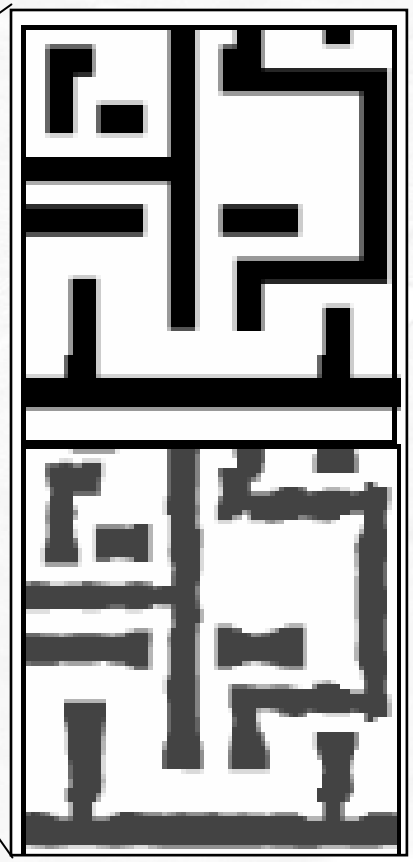
Incorporating design intent in new ways

Mark shapes in layout that affect critical circuit timing (shown in red)

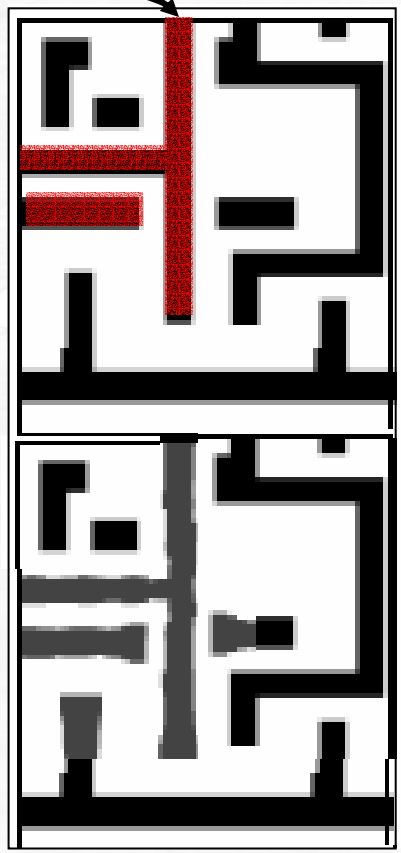


Layout from designer

Layout with RET



Without DFM (RET applied uniformly)



With DFM (RET applied where needed)

- **Vary intensity of RET based on location in circuit with respect to critical timing paths**
- **Increase metrology and decrease allowed tolerances where most needed**

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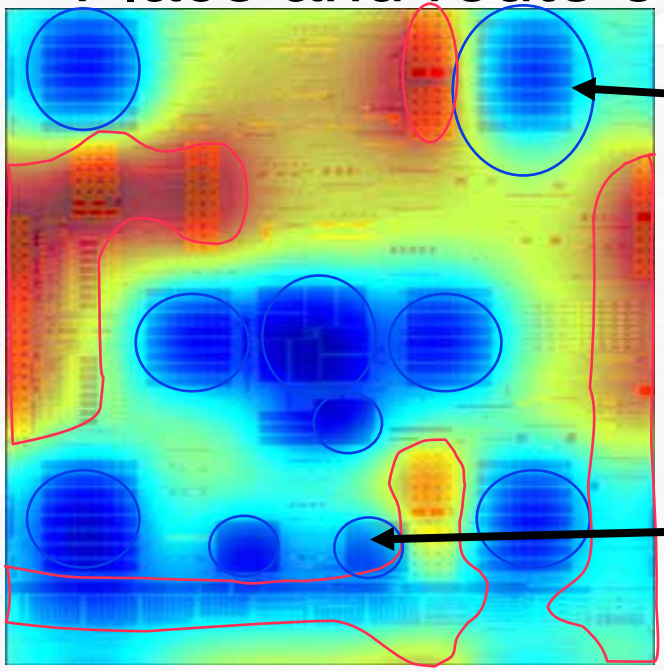
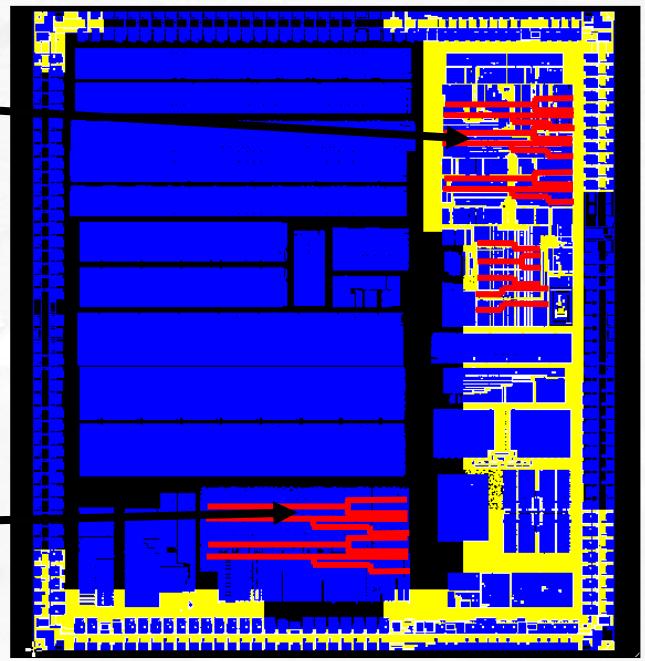
Incorporating design intent in new ways

- Optimize floor plan based on critical timing paths
- Place and route optimized based on critical



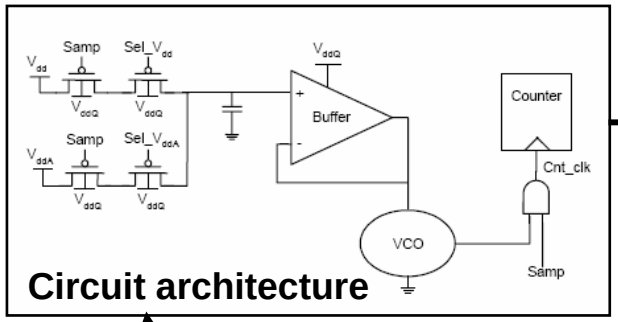
Potential problems areas marked where critical timing paths exist in regions with large variations



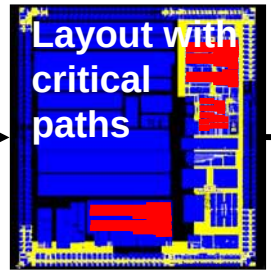
Known contours of CD, topography or overlay error with mfg. process

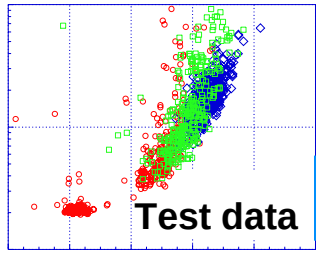
Change layout to move critical timing paths to areas without smallest errors

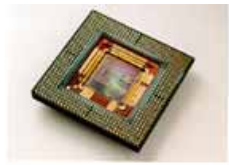
New mode of operation with design for manufacturing (DFM) practices

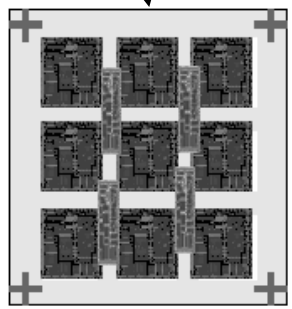


Circuit architecture

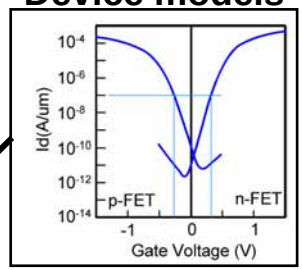



Test data


Packaged IC


Masks optimized based on design intent

Device models



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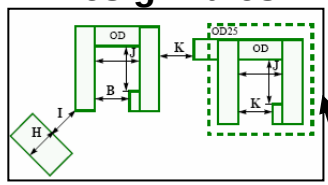
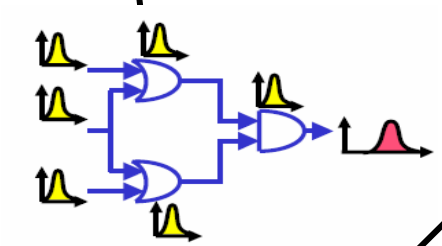
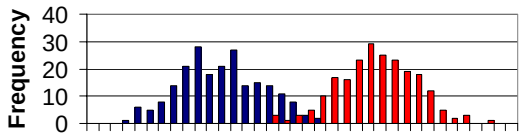
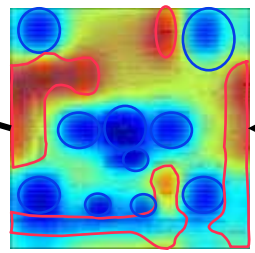



Statistical timing optimization



Process variation distributions


Known contours of CD, topography or overlay error with mfg. process

Conclusions

- 193nm immersion and EUV lithography are promising candidate technologies for 45-nm and 32-nm half-pitch patterning
  - Significant challenges remain in developing either technology to provide a timely, economical manufacturing solution
- Maintaining ±10% CD control doesn't appear to be possible
  - Metrology precision improvements critical to reducing systematic errors
- Measuring and controlling LWR and LER becoming increasingly important
- Increasing integration of design, lithographic resolution enhancement techniques and extensive metrology will be needed to maintain expected circuit performance
  - DFM drives need for improved precision and throughput