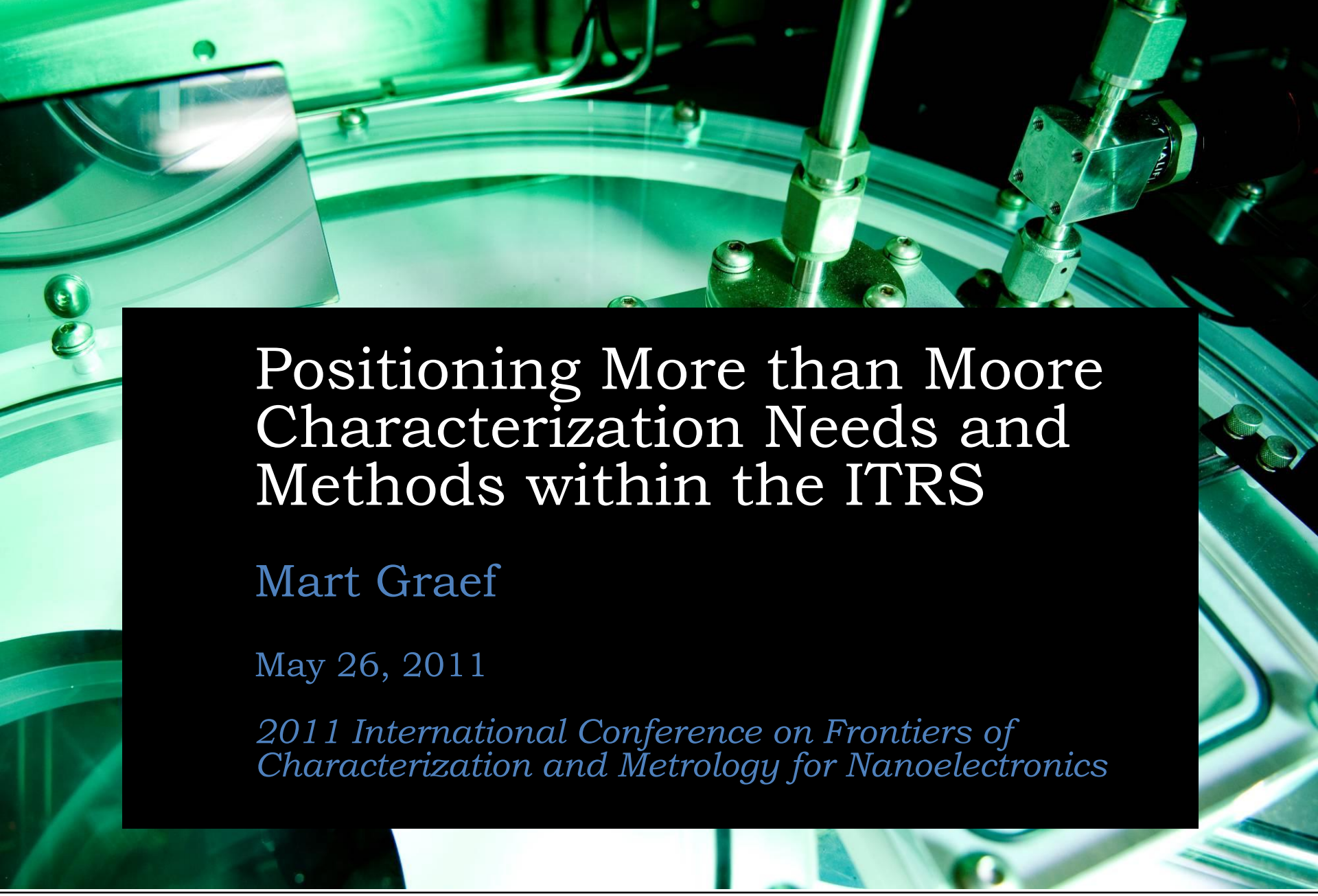


Positioning More than Moore Characterization Needs and Methods within the ITRS

Mart Graef

May 26, 2011

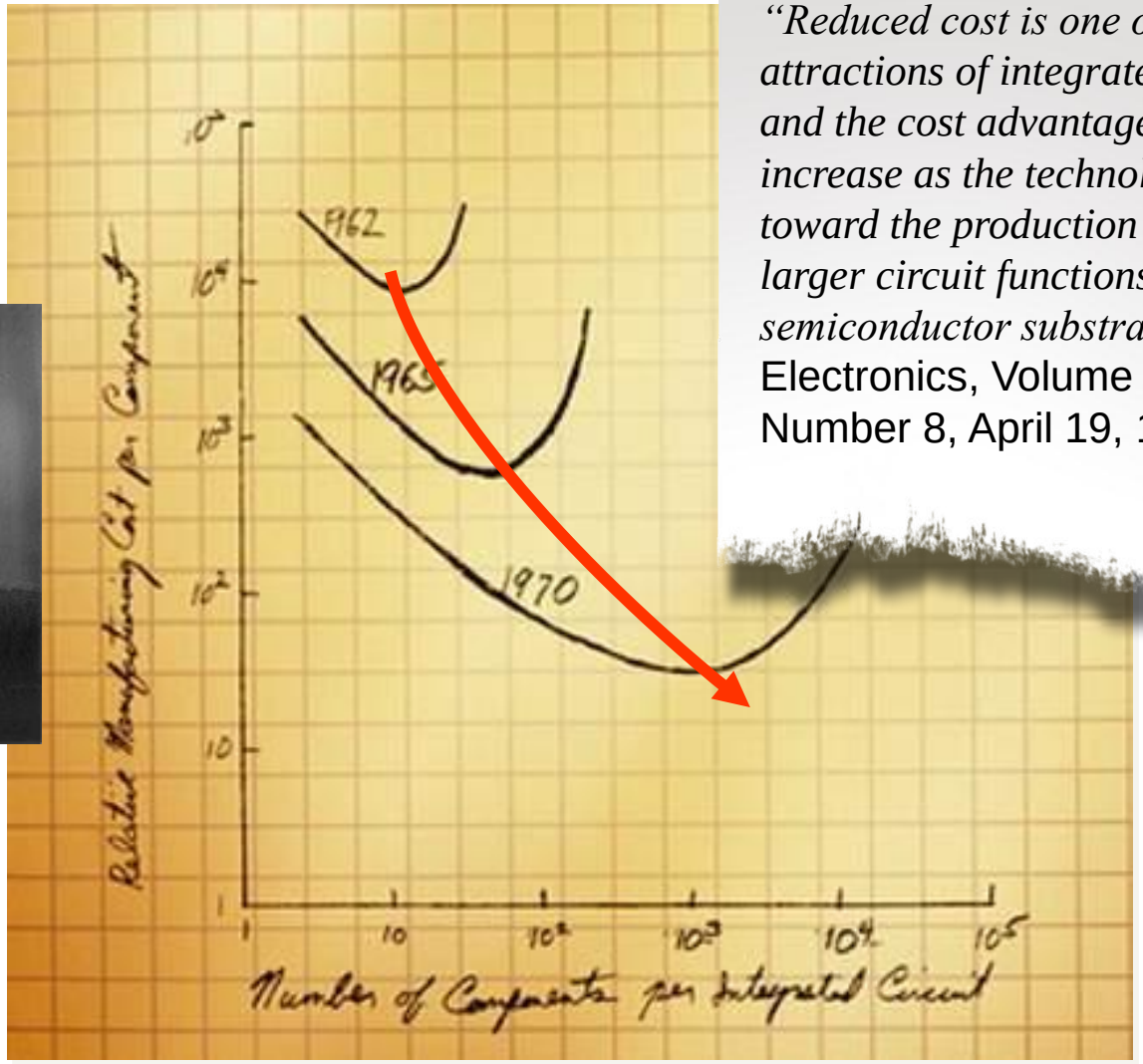
2011 International Conference on Frontiers of Characterization and Metrology for Nanoelectronics

Overview

- Miniaturization
- The ITRS roadmapping process
- New territory: More than Moore
- Characterizing More than Moore

Miniaturization

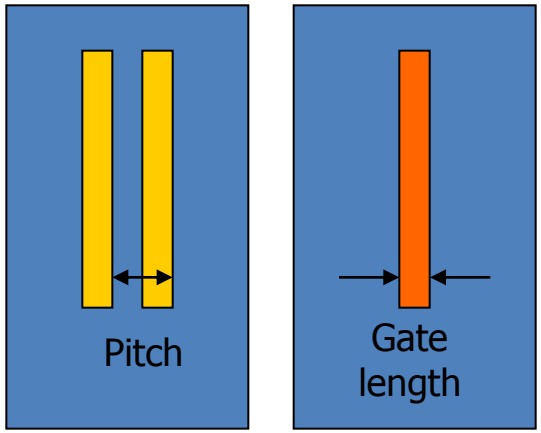
Gordon Moore, 1965



"Reduced cost is one of the big attractions of integrated electronics, and the cost advantage continues to increase as the technology evolves toward the production of larger and larger circuit functions on a single semiconductor substrate."
Electronics, Volume 38, Number 8, April 19, 1965

Courtesy Paolo Gargini, Intel

CMOS Transistor Scaling



Scaling S = ½√2 ≈ 0.7/cycle
(0.5x per 2 technology cycles)

Critical dimension (half pitch, gate length) [nm]:

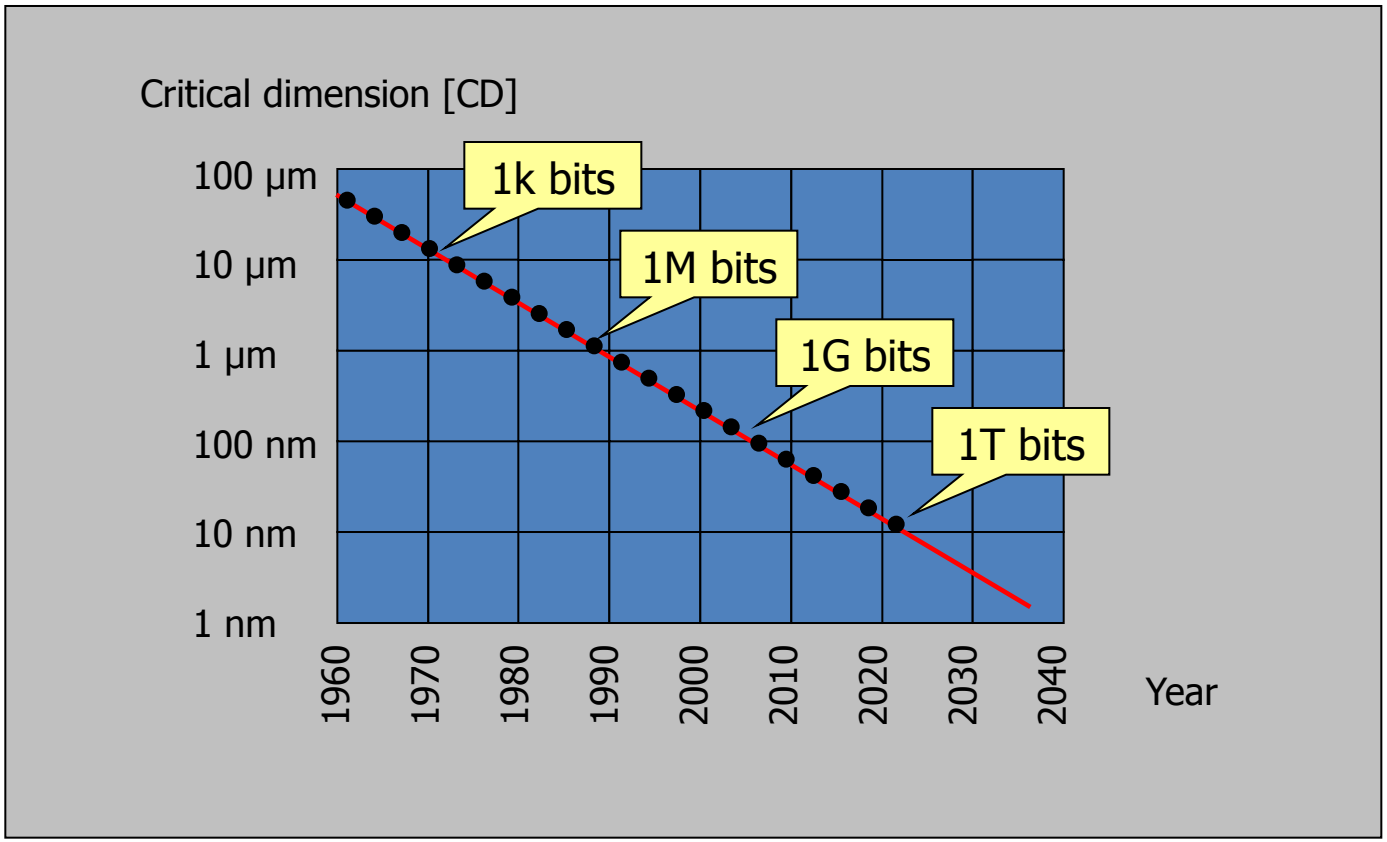
0.7x 0.7x

250 → 180 → 130 → 90 → 65 → 45 → 32 → 22 → 16

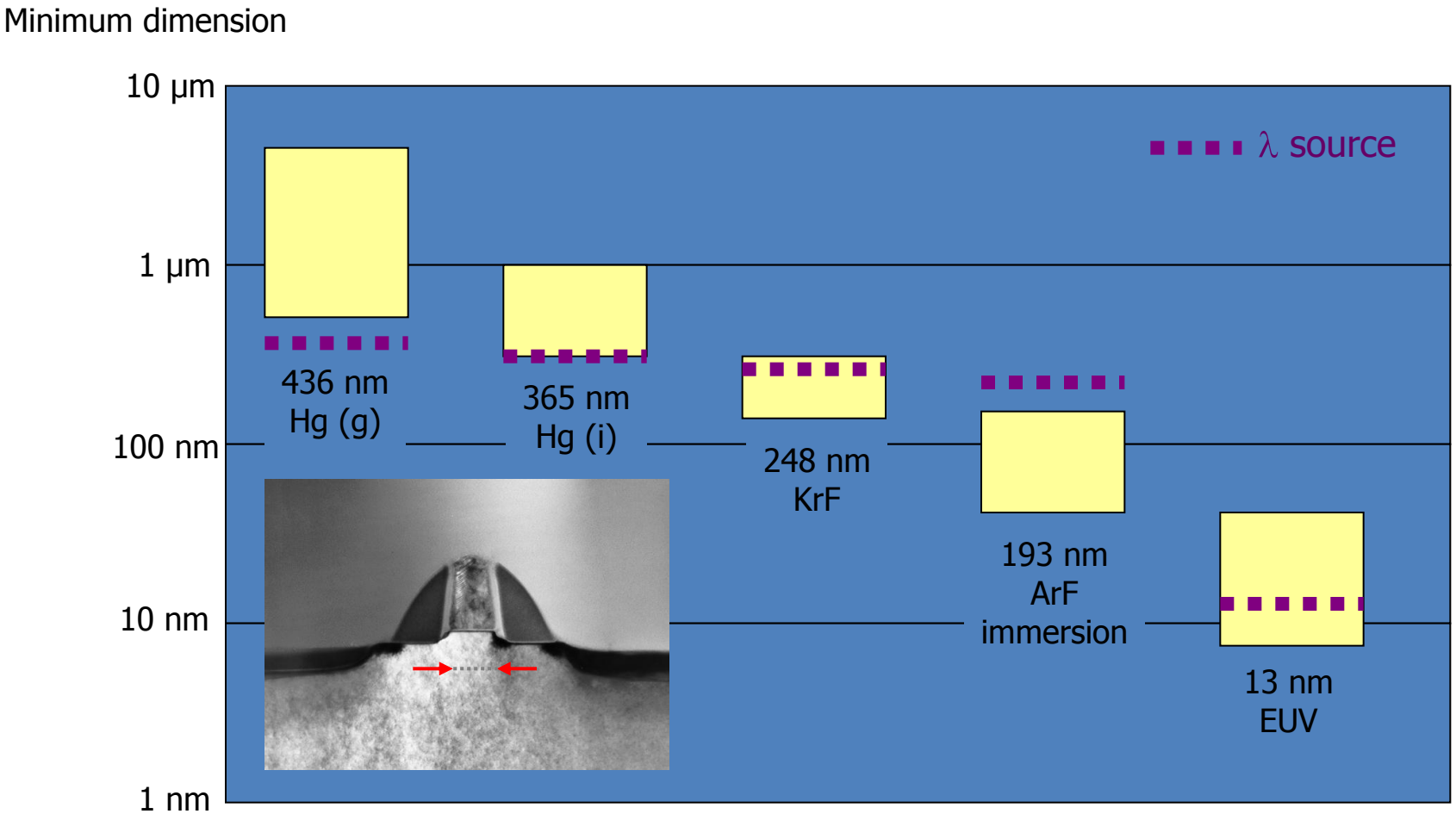
0.5x

1995 1998 2001 2004 2007 2010 2013 2016 2019

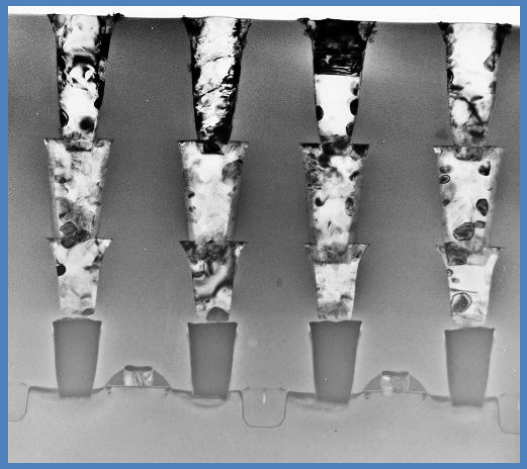
Moore's Law: Miniaturization

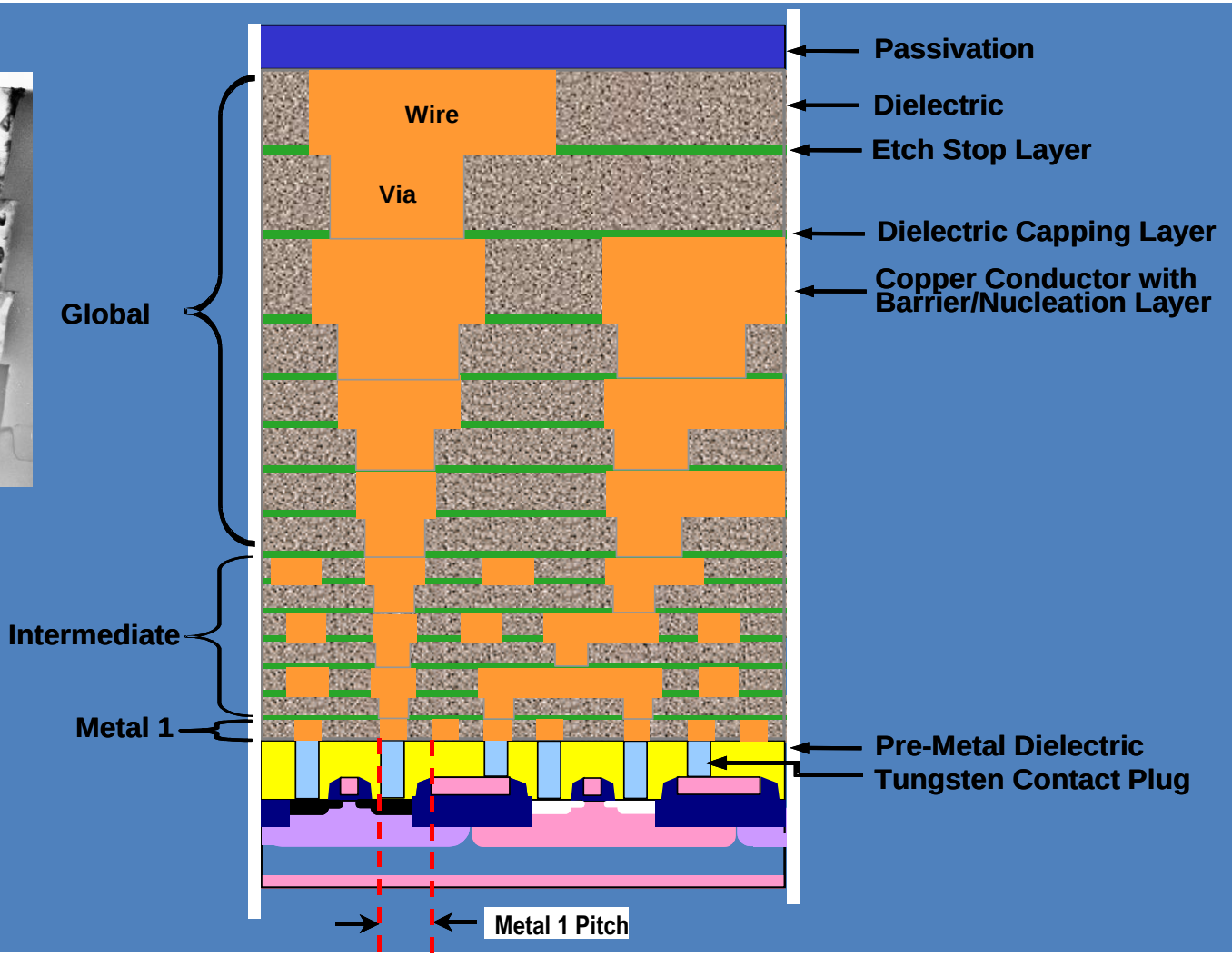


Scaling and Lithography



Typical Interconnect Stack



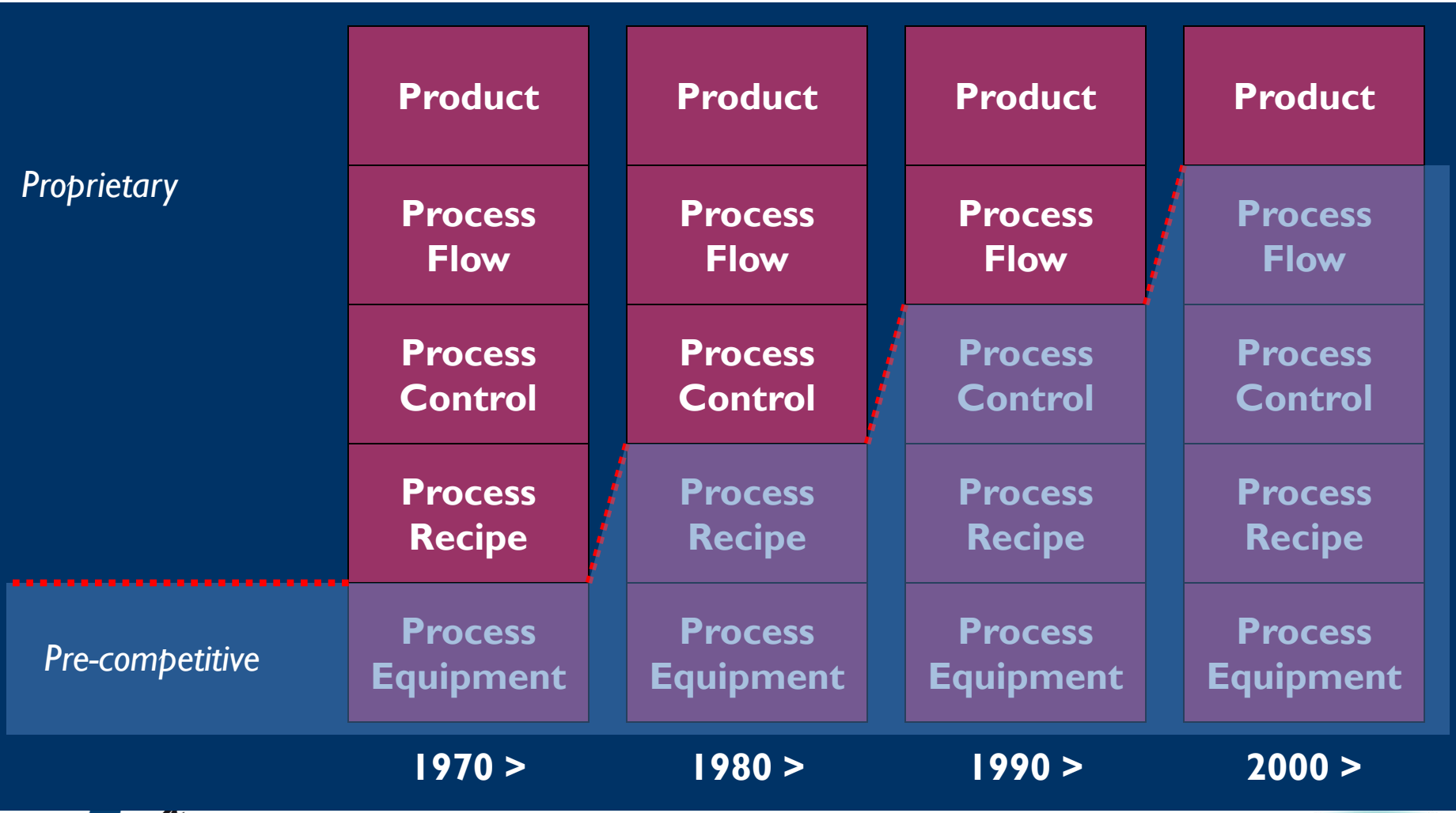


The ITRS roadmapping process

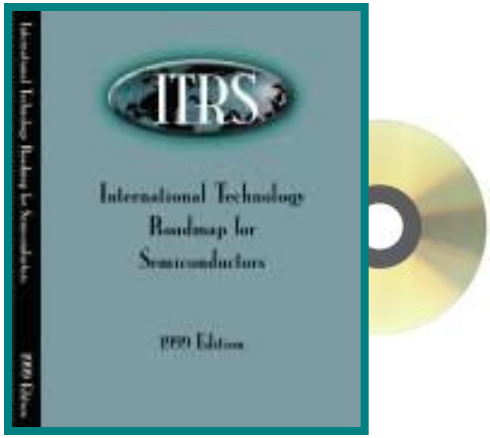
Why create a roadmap?

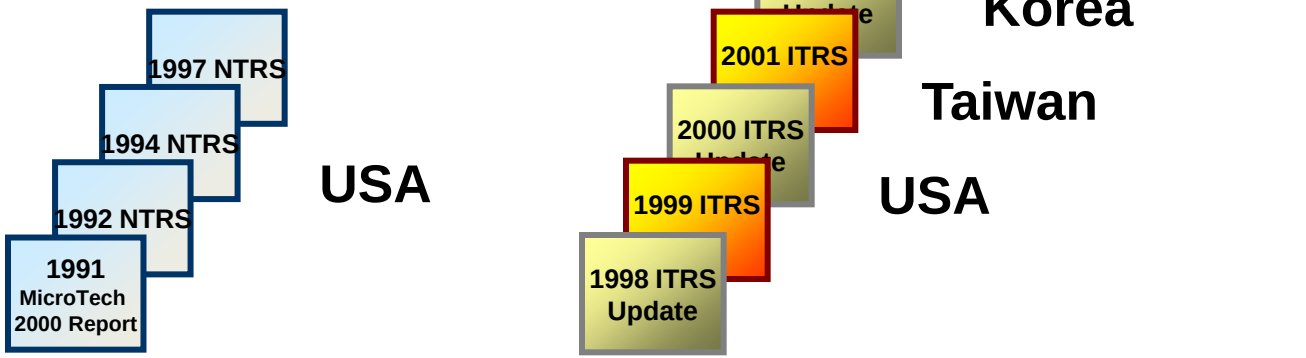
Cooperation:

The concept of 'pre-competitive' technology research



International Technology Roadmap for Semiconductors (ITRS) 1998 - now





http://www.itrs.net

ITRS Objective

- Provide guidance to the semiconductor industry by predicting technology trends in the industry, spanning 15 years (near-term 1-6 yrs; long-term 7-15 yrs)

Organization and implementation

- Organization
  - International Roadmap Committee (IRC)
  - 16 international technology working groups (ITWGs)
- ITRS release every 2 years
  - 16 chapters, ~1000 pages, >200 tables
  - >300 contributors, representing >50 companies ww
  - Update of tables every other year
- 3 Workshops/year
  - Europe (spring / Semicon Europa)
  - USA (summer / Semicon West)
  - Asia (winter / Semicon Japan)
- 2 Public symposia/year (incl. press conference)
  - ~130 participants

Technology Working Groups

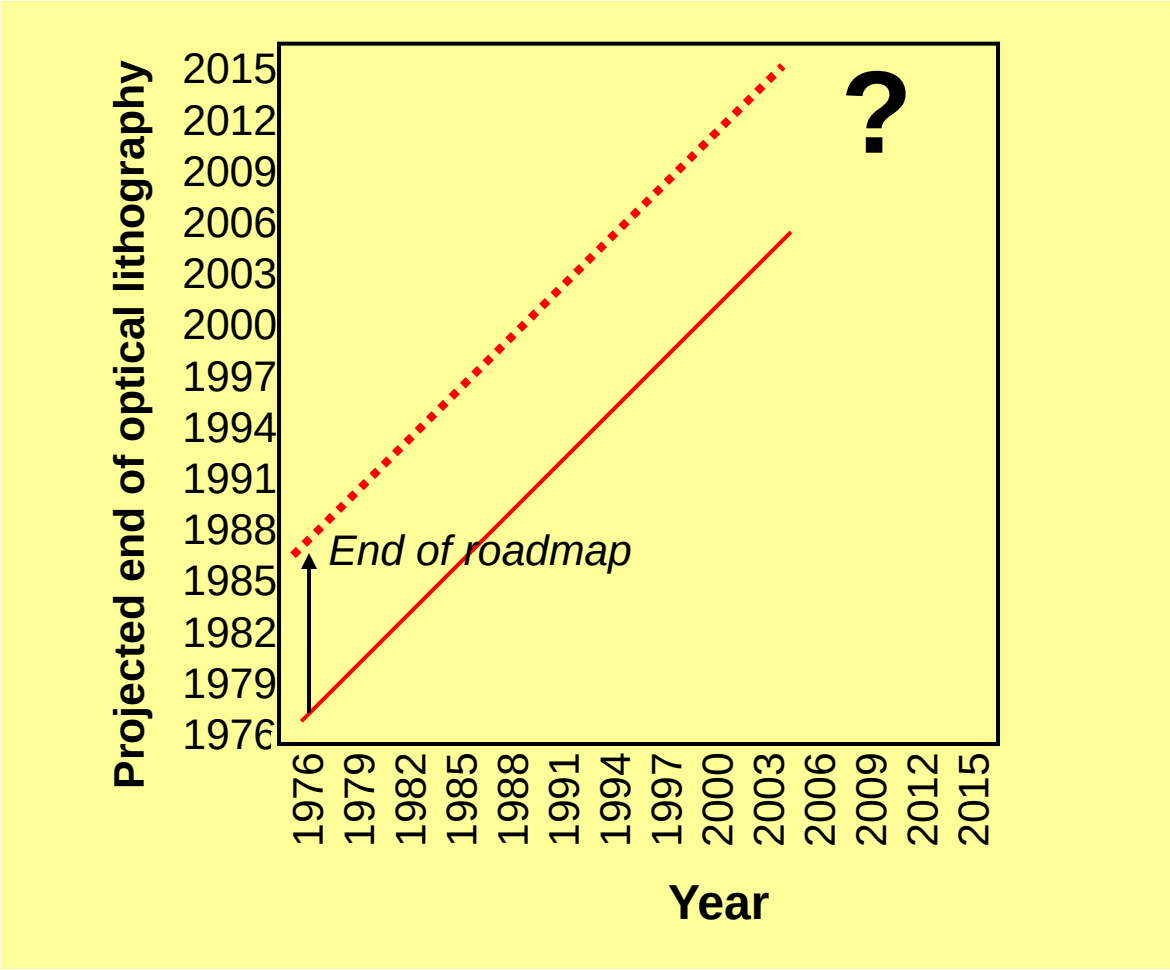
1. System Drivers
2. Design
3. Test & Test Equipment
4. Process Integration, Devices & Structures
5. RF and Analog/Mixed Signal
6. Emerging Research Devices
7. Emerging Research Materials
8. Front End Processes
9. Lithography
10. Interconnect
11. Factory Integration
12. Assembly & Packaging
13. Environment, Safety & Health
14. Yield Enhancement
15. Metrology
16. Modeling & Simulation

Impact of the ITRS

- Provides a benchmark for the semiconductor industry
- Identifies technology challenges
- Generates industrial research agenda
- Can be (mis)used for marketing purposes

When will the roadmap end?

The end of lithography?
The roadmap of the roadmap

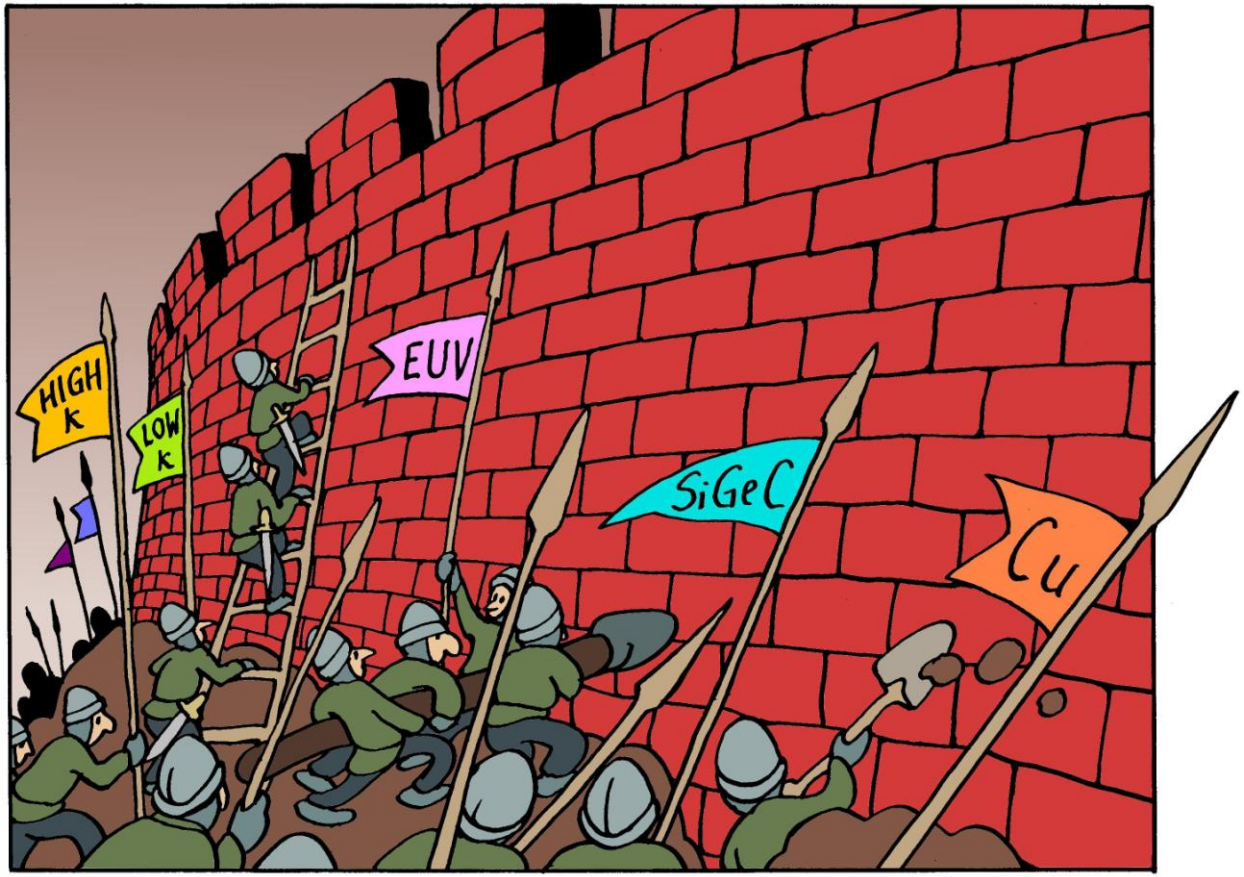


(John Sturtevant, Motorola)

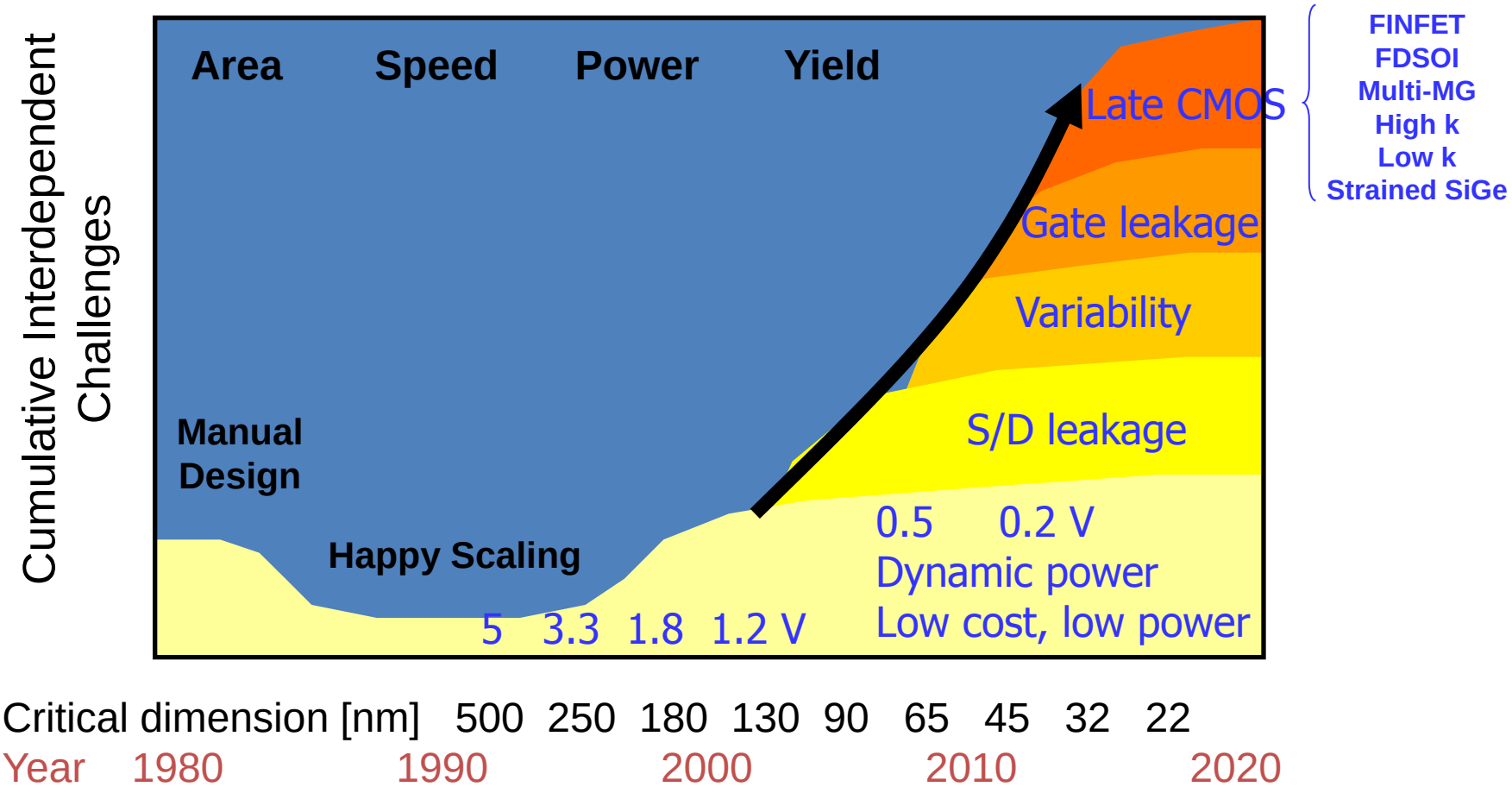
Lithography requirements

Year of Production	2009	2010	2011	2012	2013	2014	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024
DRAM ½ pitch (nm) (contacted)	52	45	40	36	32	28	25	23	20	18	16	14	13	11	10	9
DRAM																
DRAM ½ pitch (nm)	52	45	40	36	32	28	25	23	20	18	16	14	13	11	10	9
CD control (3 sigma) (nm) [B]	5	4,7	4,2	3,7	3,3	2,9	2,6	2,3	2,1	1,9	1,7	1,5	1,3	1,2	1,0	0,9
Contact in resist (nm)	57	50	44	39	35	31	28	25	22	20	18	16	14	12	11	10
Contact after etch (nm)	52	45	40	36	32	28	25	23	20	18	16	14	13	11	10	9
Overlay [A] (3 sigma) (nm)	10	9,0	8,0	7,1	6,4	5,7	5,1	4,5	4,0	3,6	3,2	2,8	2,5	2,3	2,0	1,8
k1 193 / 1.35NA	0,36	0,31	0,28	0,25	0,22	0,20	0,18	0,16	0,14	0,12	0,11	0,10	0,09	0,08	0,07	0,06
k1 EUVL		0,83	0,74	0,66	0,59	0,52	0,47	0,58	0,52	0,46	0,41	0,37	0,33	0,42	0,37	0,33
Flash																
Flash ½ pitch (nm) (un-contacted poly)	38	32	28	25	23	20	18	16	14	13	11	10	9	8	7	6
CD control (3 sigma) (nm) [B]	4	3,3	2,9	2,6	2,3	2,1	1,9	1,7	1,5	1,3	1,2	1,0	0,9	0,8	0,7	0,7
Contact Pitch (nm)	219	190	170	151	135	120	107	95	85	76	67	60	53	48	42	38
Contact after etch (nm)	52	45	40	36	32	28	25	23	20	18	16	14	13	11	10	9
Overlay [A] (3 sigma) (nm)	12	10,5	9,4	8,3	7,4	6,6	5,9	5,3	4,7	4,2	3,7	3,3	2,9	2,6	2,3	2,1
k1 193 / 1.35NA	0,26	0,22	0,20	0,18	0,16	0,14	0,12	0,11	0,10	0,09	0,08	0,07	0,06	0,06	0,05	0,04
k1 EUVL		0,61	0,55	0,49	0,43	0,39	0,33	0,41	0,37	0,33	0,29	0,26	0,23	0,29	0,26	0,23
MPU																
MPU/ASIC Metal 1 (M1) ½ pitch (nm)	54	45	38	32	27	24	21	19	17	15	13	12	11	9	8	8
MPU gate in resist (nm)	47	41	35	31	28	25	22	20	18	16	14	12	11	10	9	8
MPU physical gate length (nm) *	29	27	24	22	20	18	17	15	14	13	12	11	10	9	8	7
Gate CD control (3 sigma) (nm) [B] **	3,0	2,8	2,5	2,3	2,1	1,9	1,7	1,6	1,5	1,3	1,2	1,1	1,0	0,9	0,8	0,8
Contact in resist (nm)	66	56	47	39	33	29	26	23	21	19	17	15	13	12	10	9
Contact after etch (nm)	60	51	43	36	30	27	24	21	19	17	15	13	12	11	9	8
Overlay [A] (3 sigma) (nm)	13	11	9,5	8,0	6,7	6,0	5,3	4,7	4,2	3,8	3,3	3,0	2,7	2,4	2,1	1,9
k1 193 / 1.35NA	0,37	0,31	0,26	0,22	0,19	0,17	0,15	0,13	0,12	0,11	0,09	0,08	0,07	0,07	0,06	0,05
k1 EUVL		0,83	0,70	0,59	0,50	0,44	0,39	0,49	0,44	0,39	0,35	0,31	0,28	0,35	0,31	0,28
Chip size (mm^2)																
Maximum exposure field height (mm)	26	26	26	26	26	26	26	26	26	26	26	26	26	26	26	26
Maximum exposure field length (mm)	33	33	33	33	33	33	33	33	33	33	33	33	33	33	33	33
Maximum field area printed by exposure tool (mm^2)	858	858	858	858	858	858	858	858	858	858	858	858	858	858	858	858
Wafer site flatness at exposure step (nm) [C]	48	42	37	33	29	26	23	20	18	16	14	12	11	10	9	8
Number of mask levels MPU	35	35	35	35	37	37	37	37	39	39	39	39	39	39	0	0
Number of mask levels DRAM	24	26	26	26	26	26	26	26	26	26	26	26	26	26	0	0
Wafer size (diameter, mm)	300	300	300	300	300	450	450	450	450	450	450	450	450	450	450	450
NA required for Flash (single exposure)	NA															
NA required for logic (single exposure)	1,16	1,38	1,64	1,94	2,31											
NA required for double exposure (Flash)	1,02	1,22	1,36	1,53	1,72	1,93	2,17									
NA required for double exposure (logic)	0,80	0,95	1,12	1,34	1,59	1,78	2,00									
EUV NA minimum		0,25	0,25	0,25	0,25	0,25	0,25	0,35	0,35	0,35	0,35	0,35	0,35	0,5	0,5	0,5

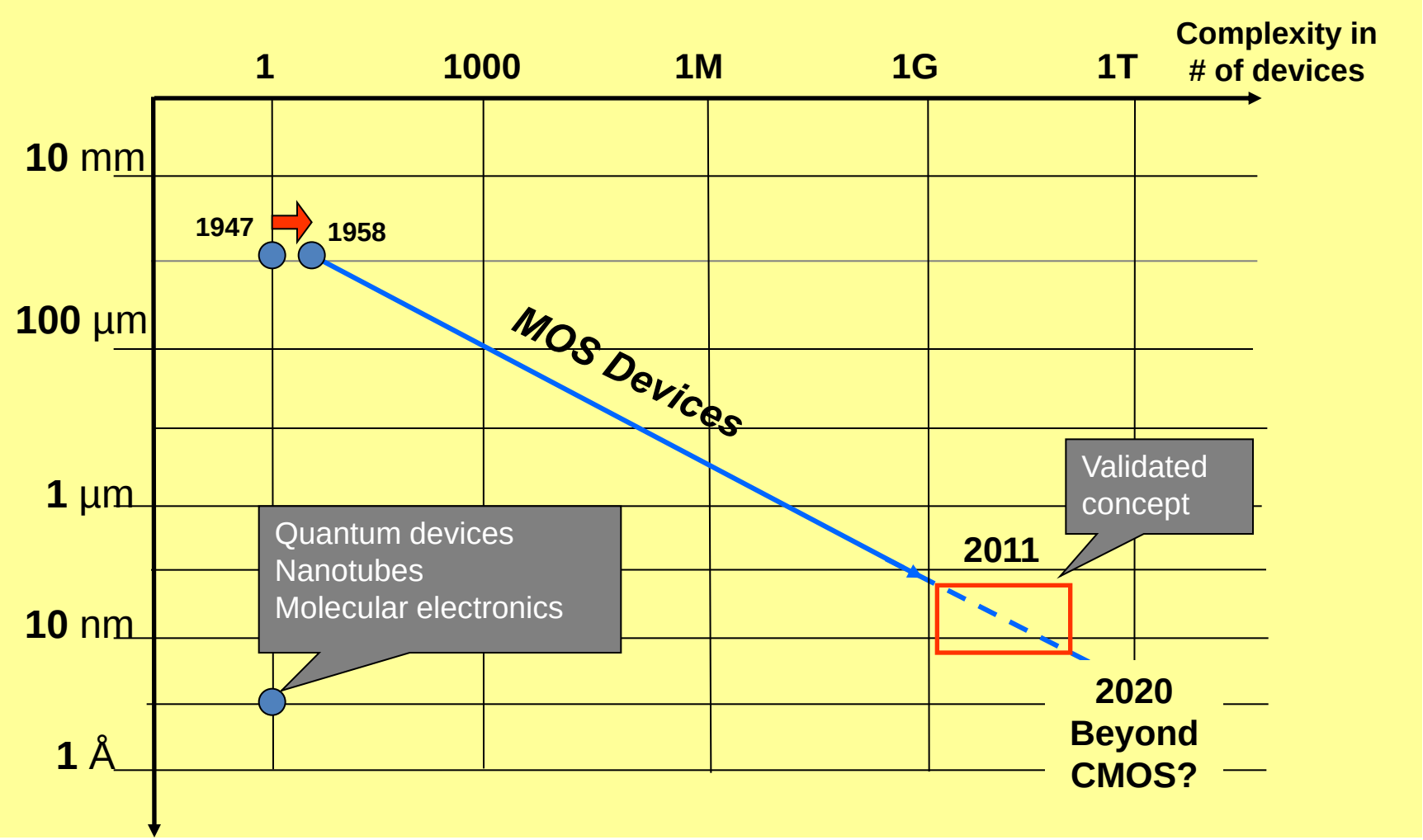
“The Red Brick Wall”



More Moore: Increasing complexity



Reaching dimension/complexity limits

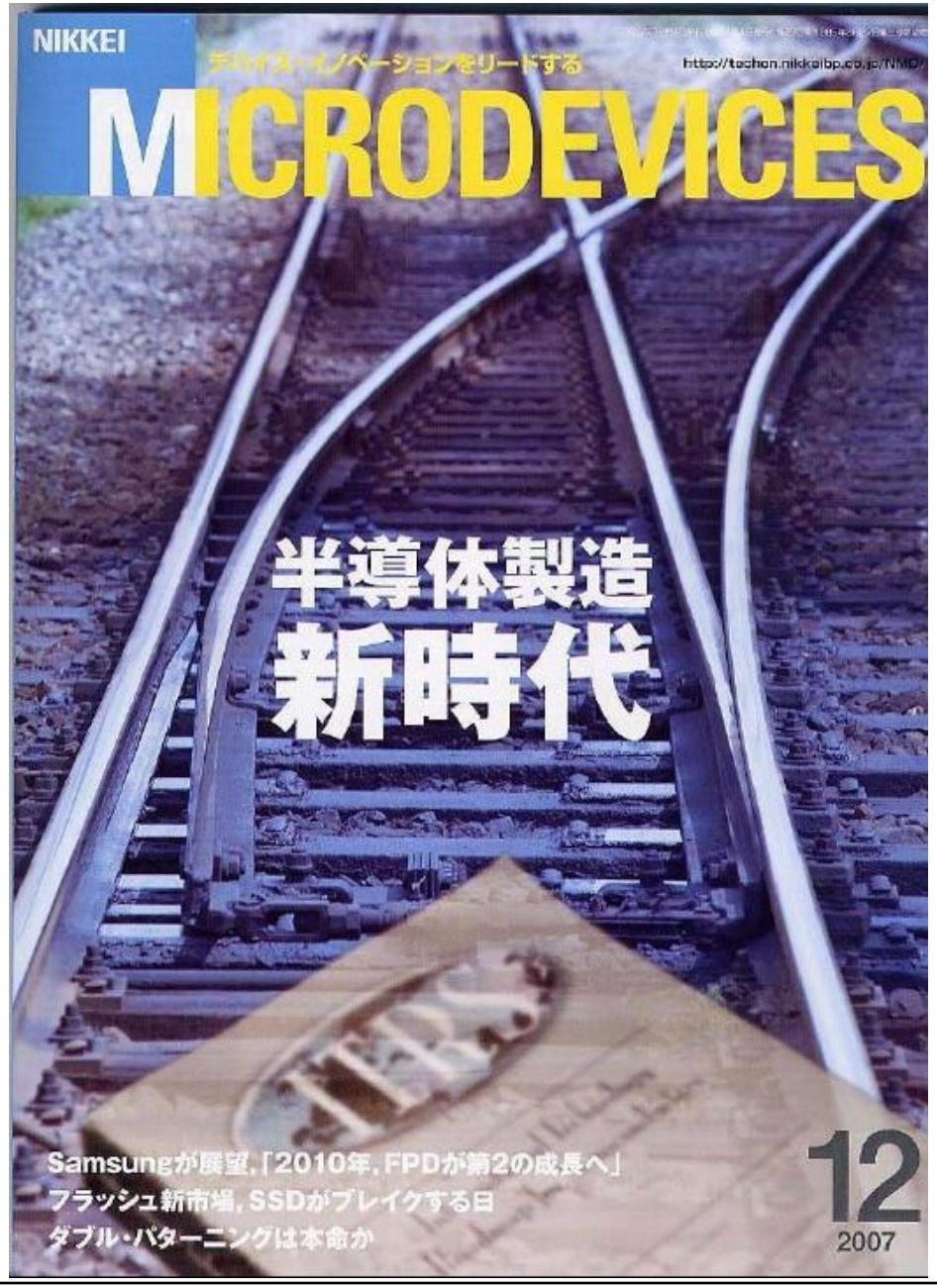


Source: STMicroelectronics

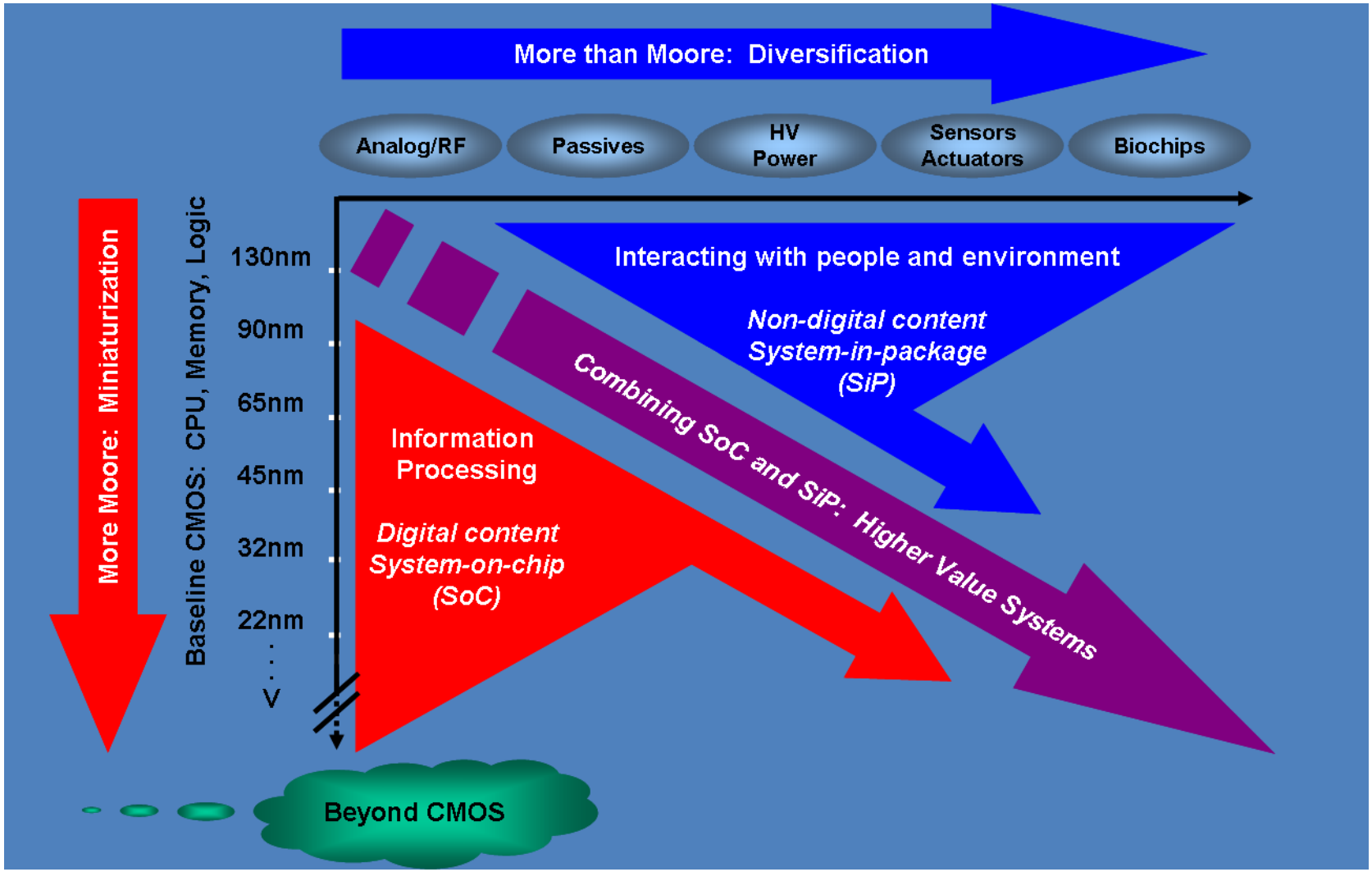
New territory:
More than Moore

Roadmap at the crossroads

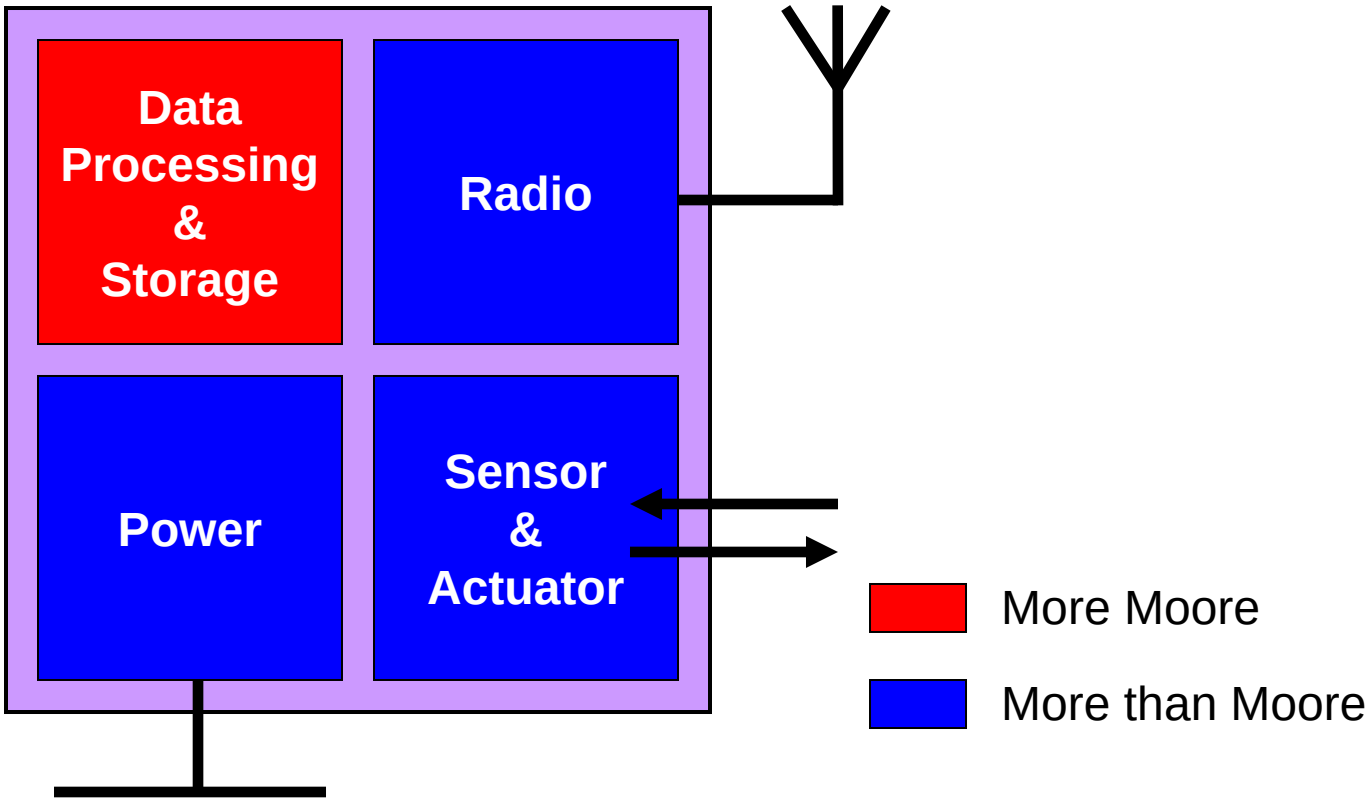
ITRS 2005



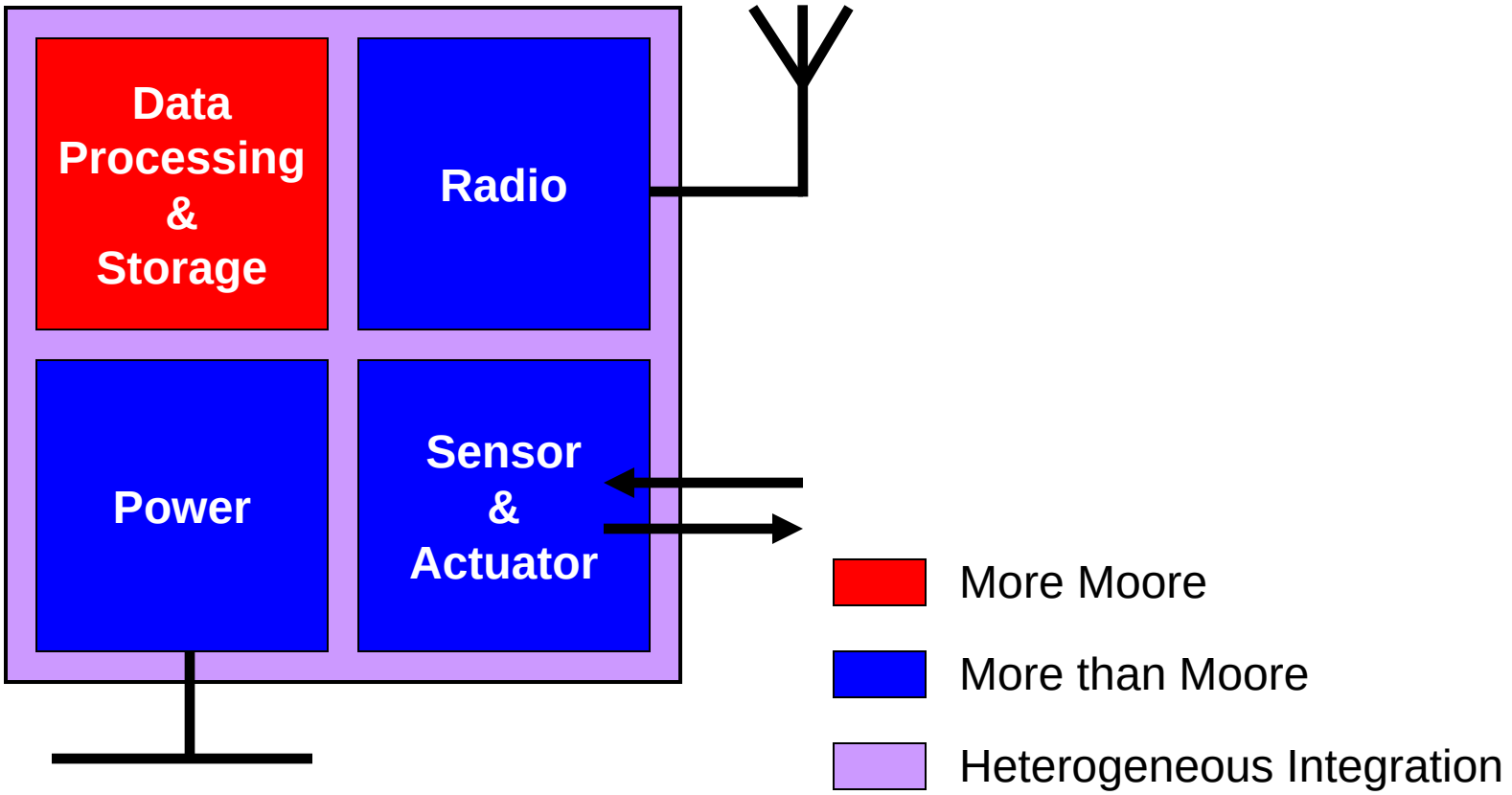
“More Moore” & “More than Moore”



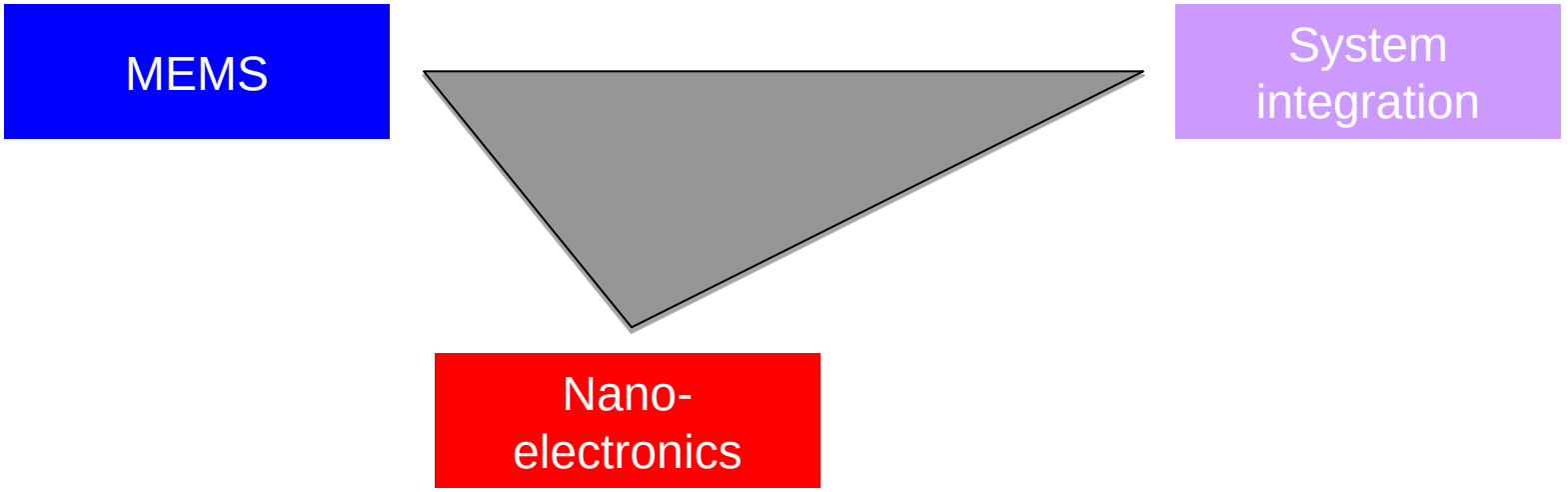
Smart microsystems: More Moore & More than Moore



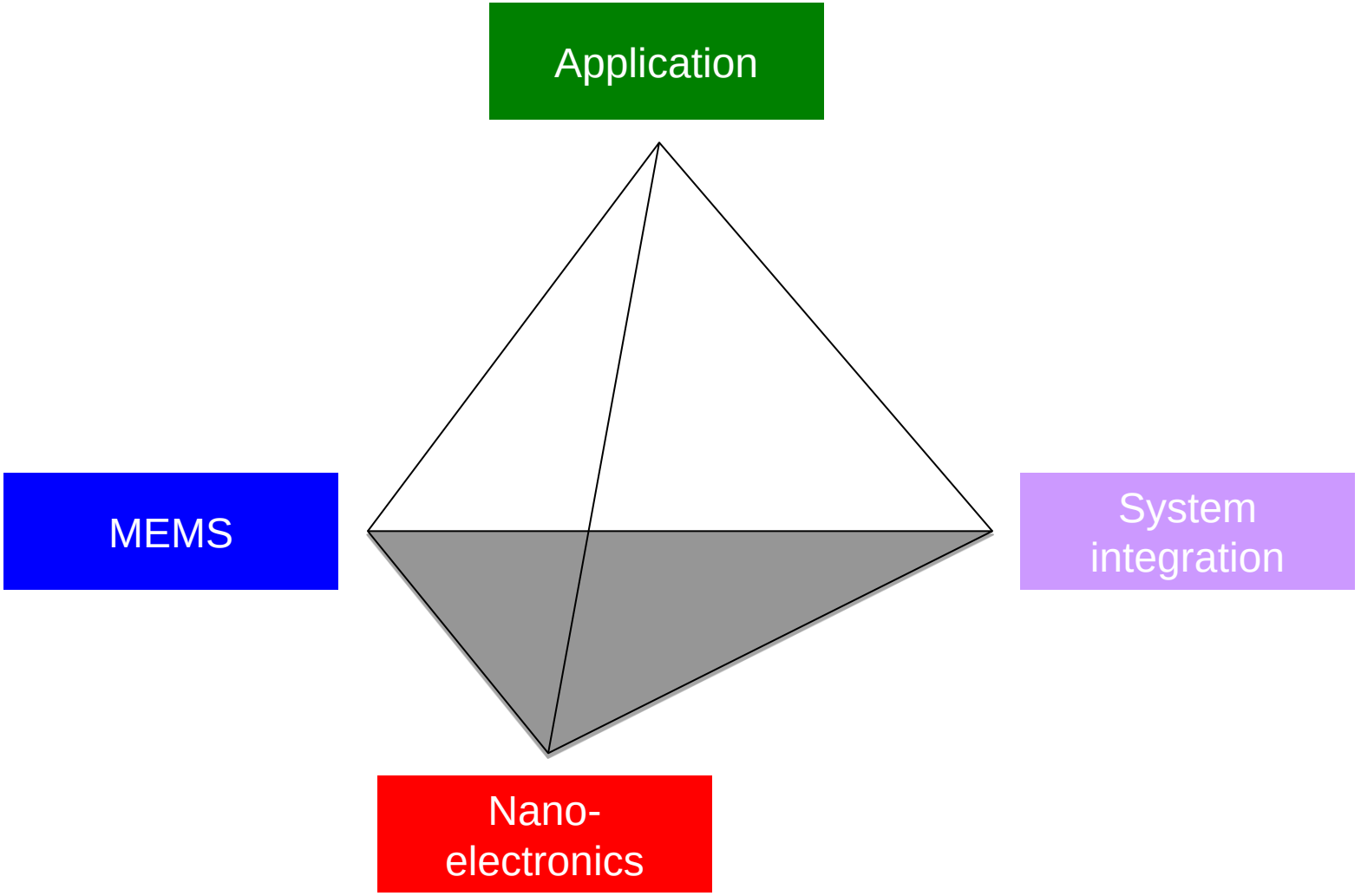
Smart microsystems: More Moore & More than Moore



Technology Framework

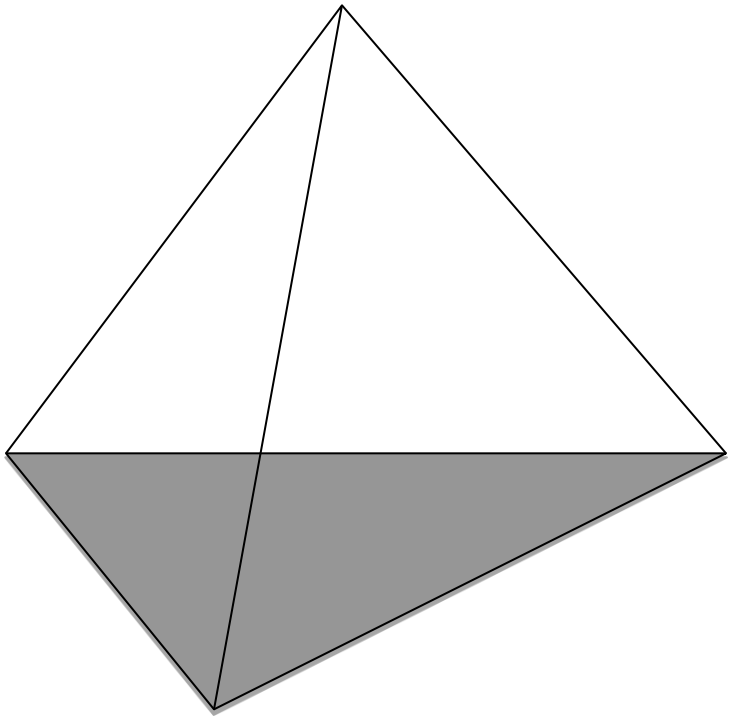


Technology-Application Framework



Example: healthcare domain

Radiotracer- & fluorescence-guided surgery, biopsy, diagnostics



Single-photon sensitive Si photon detectors

Compact probe

Time stamping electronics

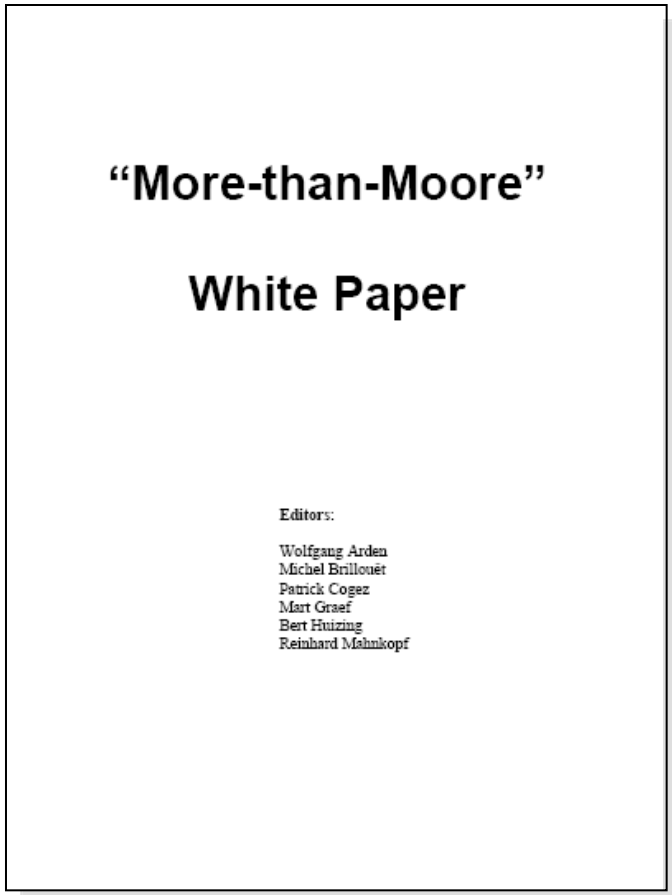
Courtesy Edoardo Charbon, TUDelft

Characterizing More than Moore

Why a More than Moore roadmap ?

- ITRS has demonstrated value of roadmapping for CMOS
  - Identify pre-competitive research domains, enabling cooperation between industries, institutes and universities.
    - Sharing of R&D efforts
    - Increase resource efficiency through focus
    - Reduction of development costs and time
  - Synchronization of the equipment & materials community with the semiconductor manufacturing community
- More than Moore roadmapping offers a similar but more challenging opportunity
  - Need to propose a roadmapping methodology
    - White paper

More than Moore White Paper Roadmapping Methodology



Published by the ITRS in 2010
http://www.itrs.net/papers.html

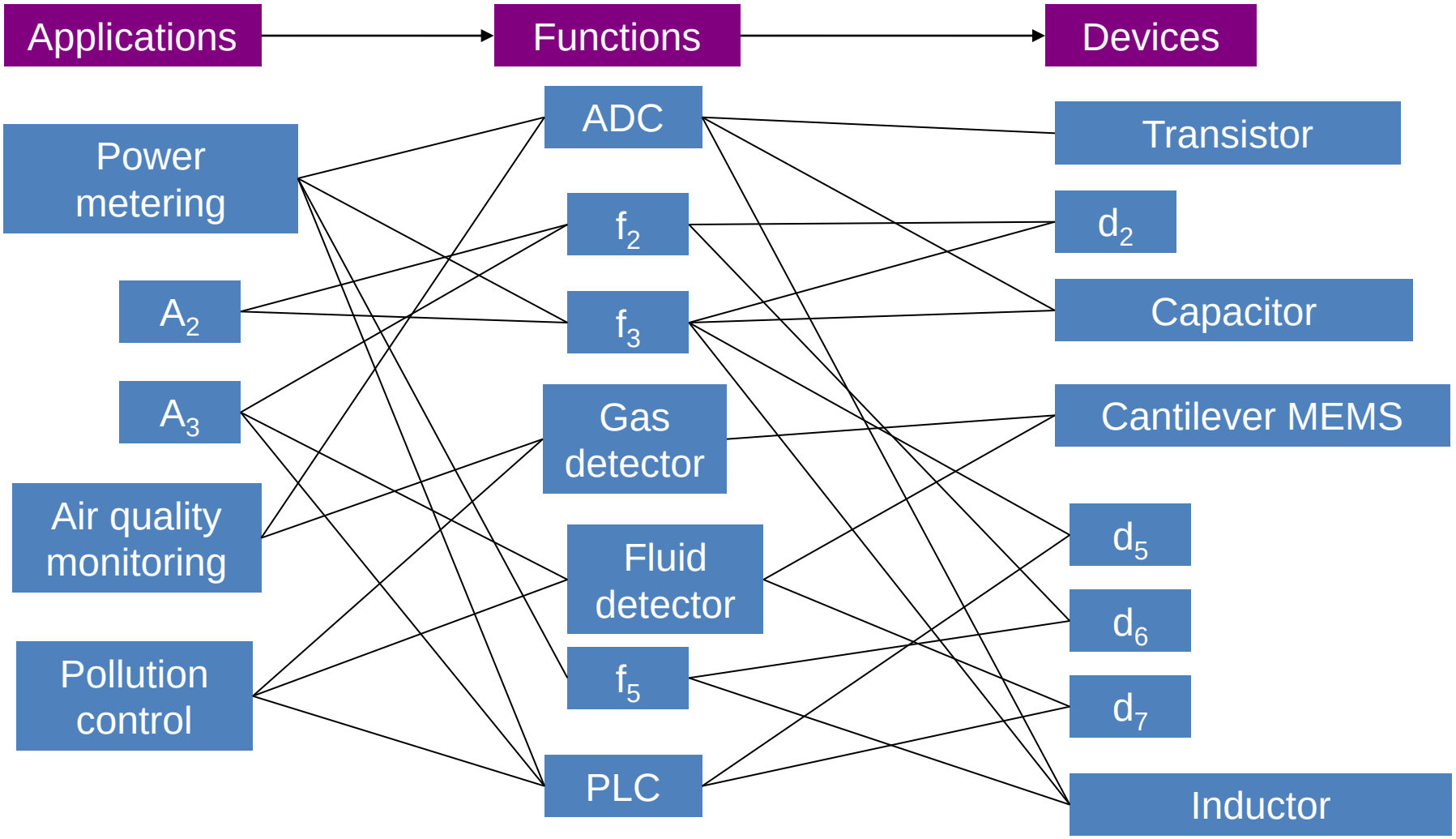
Necessary conditions for an industry-wide technical roadmap effort

- Restricted set of figures of merits (FOM)
- Convergence of opinion among a majority of the key players on the progress trends that these figures of merit are expected to follow (LEP)
- Potential market of significant size inducing a wide applicability of the roadmap (WAT)
- Willingness to share information (SHR)
- Existence of a community of players (ECO)

MtM Technology Assessment

	FOM *Figure of merit*	LEP *Law of expected progress*	SHR *Willing-ness to share*	WAT *Wide applica-bility*	ECO *Existing community*	In ITRS today?
RF	++	++	+	+/++	+	Yes
Power	+	+	?	=	?	No
Imaging	+	+	?	=	?	No
Sensors / actuators	--	?	?	++	--	i.s.n.
Biochips	--	?	--	?	--	No
…						

From applications to functions to devices



1st More than Moore Workshop
April 13, 2011 Potsdam

MtM ITRS Workshop

Agenda

08:30 – 08:50	ITRS White Paper & on-going actions	M. Graef
08:50 – 10:15	Update ITRS ITWG activities on MtM	
	Wireless	J. Pekarik (20mn)
	A&P	B. Bottoms (20mn)
	MEMS (+iNEMI MtM roadmap)	M. Gaitan (20mn)
	CATRENE WG summary	M. Brillouët (25mn)
10:15 – 10:30	*break*	
10:30 – 12:00	Parallel sessions:	
	Automotive (chair: P. Cogez)	
	Energy / Integr. power (chairs: M. Graef & B. Huizing)	
	Lighting (chairs: M. Brillouët & R. Mahnkopf)	
12:00 – 13:00	*lunch*	
13:00 – 13:30	Overview sensors for security & healthcare	M. Brillouët
13:30 – 14:00	3x10' summary of the discussion	rapporteurs
14:00 – 14:10	Wrap-up	M. Brillouët

ITRS TWGs
- Wireless
- Assembly & Packaging
- MEMS

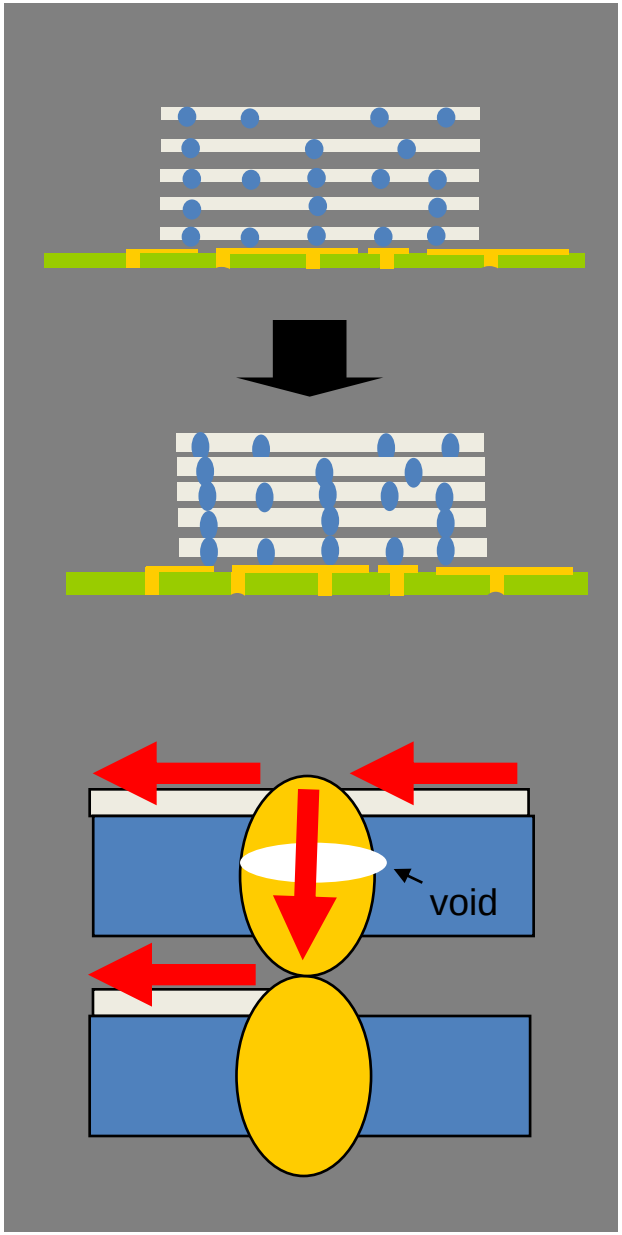
Application domains
- Automotive
- Energy & Power
- Lighting
- Security
- Healthcare

What we talk about when we talk about 'More than Moore'

- **System-in-Package:**
  Integration of digital and non-digital functions in one module
  - Power, RF, passives, sensors, fluidics, lighting,…
  - Packaging is a functional element
- **High diversity of technologies:**
  Heterogeneity of materials and designs
  - Modular platforms in a structured design environment
  - Integration of new materials: interfaces!
- **Builds on existing CMOS infrastructure**
  - Lithographic scaling capability controls Moore's law

Testing 3D Devices

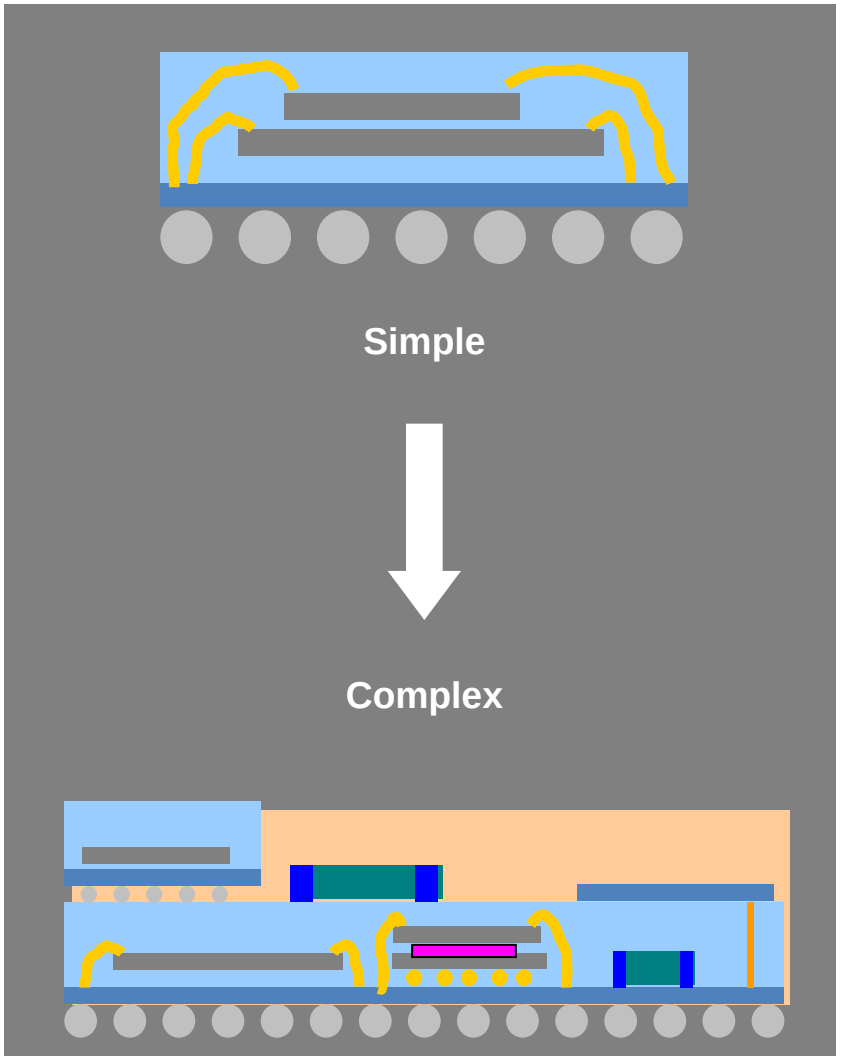
- Multiple die system
  - Sub-systems designed to operate and be assembled together
  - Process optimized for contents of each die
    - Logic, DRAM, NVM, Analog
  - Connection by potentially 1000s of TSVs
- Design, interconnect, assembly and test problem
- Design for Test requirements
  - Testability of each die
  - Via continuity checks
    - For signal and non-signal vias
    - 3-5 µm via cannot be probed! ESD!
  - N+ die test methodology as die added
  - Final “system” test



Source: Roger Barth, ITRS 2009

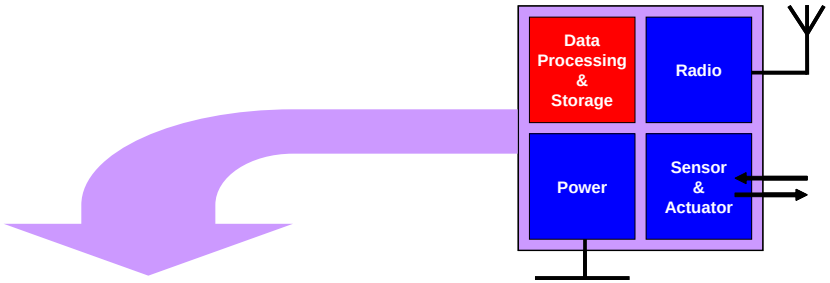
Testing System in Package (SiP)

- Challenges
  - High yield with low test cost
  - Standardized test strategy for mini-systems
- Potential test solutions
  - Design for die, debug and system test
  - Per die built in system test (BIST)
  - ‘Known good die’ (KGD) with minimal post test



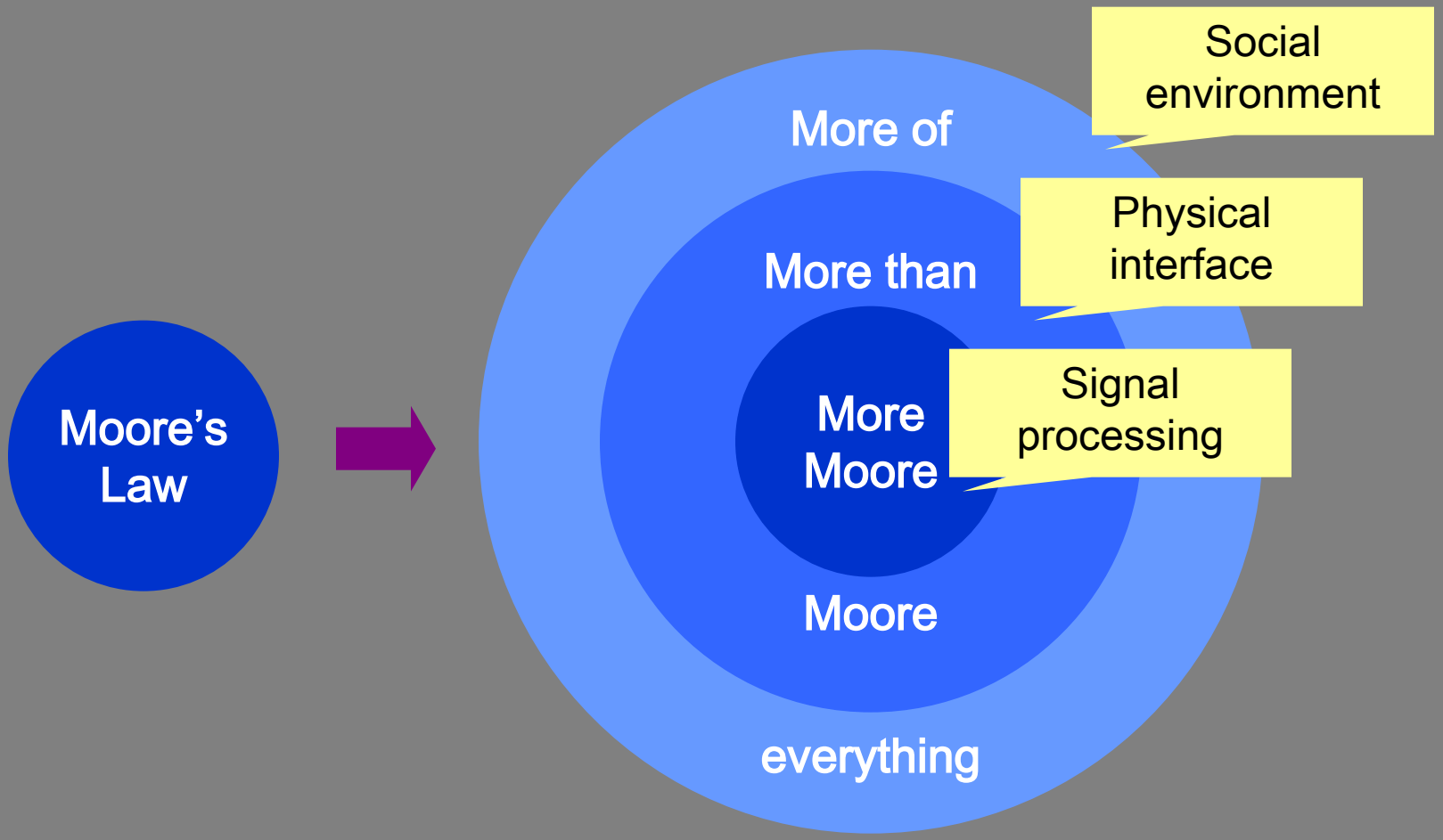
Source: Roger Barth, ITRS 2009

Characterization needs for More than Moore: Key terms



- **Multidisciplinarity**
  - Multifunctionality: device characterization requires methodologies from electrical engineering plus…
    (micro)mechanics, thermomechanics, materials science, optics, chemistry, biology, medical science,…
- **Heterogeneity**
  - 3D structures, multiscale characterization, new interfaces
- **Complexity**
  - Multi-variability
  - Merging of subsystems (new ‘middle end’)
- **Reliability**
  - Packaging is enabling functional component

From Microelectronics to Nanoelectronics



From miniaturization… to function integration

Thank you!

Acknowledgements:
International Roadmap Committee ITRS,
in particular Patrick Cogez, Bert Huizing, Reinhard Mahnkopf
& Michel Brillouët