IAC R&D Gaps Working Group

February 7 Update to IAC

Industrial Advisory Committee (IAC) – R&D Gaps Working Group

Daniel Armbrust
Silicon Catalyst

James Ang
Pacific Northwest National Laboratory

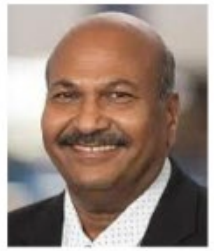
Susie Armstrong
Qualcomm

Ahmad Bahai
Texas Instruments

Carol Handwerker
Purdue University

Rajarao Jammy
MITRE Engenuity

Mukesh Khare
IBM Research



Om Nalamasu
Applied Materials

Debo Olaosebikan
Kepler Computing

H.S. Philip Wong
Stanford University

Ann Kelleher
Intel Corporation

Added 12/8

Charles Gray
Ford Motor Company

Added 12/2

Todd Younkin
SRC

invited, R&D Gaps WG only

Supporting: Ben Davis, Tamiko Ford, David LaVan

IAC Working Groups

#1 R&D Gaps	*The charter of this working group is to look at the long term research needs of the semiconductor industry. The working group will then need to understand what is being funded by other initiatives, where the gaps are, and then suggest priorities to the IAC as to where the focus areas should be for CHIPS funding and the NSTC that provide the best opportunities to sustain US leadership in semiconductor innovation. (Chair: Dan Armbrust)*
#2 Org & PPP	*This working group will review and examine all the various funding sources for semiconductor R&D and map out the relationships between these entities to ensure spending efficiency and eliminate any overlaps. In addition, this working group will review the essential functions of the NSTC. Finally, this committee will review PPP proposals for both R&D partnerships, the value proposition for industry participation in PPPs, as well investment. (Chair: Deirdre Hanford)*
#3 Workforce	*This working group will look at the workforce needs across the industry from high level R&D personnel to factory workers. They should review programs that will increase the interest and availability of the necessary skills for the US to lead the world in semiconductor R&D and manufacturing. (Chair: Tsu Jae King Liu)*

R&D Gaps WG work plan – 90 day sprint

• Nov 15	1st meeting	Charter and expectations
• Nov 22	2nd meeting	Speakers and member homework
• Nov 29	3rd meeting	Grand Challenges and Gaps Part 1
• Dec 1	4th meeting	Grand Challenges and Gaps Part 2
• Dec 8	5th meeting	IAC Meeting #1 and Breakout team discussions
• Dec 13	6th meeting	Breakout team updates
• Jan 3	7th meeting	Breakout team updates
• Jan 10	8th meeting	Breakout team updates
• Jan 17	9th meeting	Breakout team updates
• Jan 24	10th meeting	Draft of WG recommendations to IAC
• Jan 31	11th meeting	Finalize WG recommendations to IAC
• Feb 7		IAC Meeting #2

Sources for semiconductor R&D landscape and priorities

DOE	Nov ’19	Basic Research Needs for Microelectronics
	Oct ’22	OSTP RFI Response
SRC	Jan ‘21	Decadal Plan for Semiconductors (Grand challenges)
MITRE	Nov ’21	American Innovation, American Growth: A Vision for the NSTC
	Mar ’22	NSTC RFI Response
ASIC	Feb ’22	Accelerating Semiconductor Research, Accelerating America
	Mar ’22	NSTC RFI Response
NIST	Sep ’22	Incentives, Infrastructure, and R&D Needs for Semiconductor Ind. (RFI response summary)
	Aug ’22	Metrology and Measurements
PCAST	Sep ’22	Revitalizing the U.S. Semiconductor Ecosystem
DOC	Sep ’22	A Strategy for the CHIPS for America Fund, and Briefing
	Oct ’22	CHIPS for America R&D Program briefing
OSTP	Oct ’22	Draft National Strategy on Microelectronics Research
SIA	Oct ‘22	Advancing Semiconductor Research Report
DOD	Nov ‘22	Future Directions – Microelectronics

Invited Speakers for IAC R&D Gaps working group

Speaker	***Affiliation***	***Topic***
Mark Rosker	DARPA	3DHI
Steve Pawlowski	Micron	Memory
Alex Pothen	Purdue	Algorithms
Karen Willcox	UT Austin	Modeling and Simulation
John Shalf	LBNL	Accelerators for HPC
Bill Dally	Nvidia	Accelerated Computing
David Patterson	Alphabet	Accelerators, Chiplets, and Sustainability
Ravi Mahajan	Intel	Packaging and Heterogeneous Integration
Markus Kuhn	Rigaku	Metrology
David Su	Former TSMC	Metrology
Rick Gottscho	LAM	Equipment and Digital Twins
Regina Freed	Applied Materials	Digital Twins
Shankar Krishnamoorthy	Synopsys	EDA and Co-design
John Damoulakis	Cadence	EDA and Co-design and Simulation
David Pan	UT Austin	EDA and Co-design
Edith Beigne	Meta	VR and AR
Eli Harari	Sunrise	Memory Startup
Gregg Lowe	Wolfspeed	Power Electronics and SiC
Tom Edman	TTM Tech	PCB, Interposers
Keren Bergman	Columbia	Photonics and Opto-electronics Systems

Key questions to answer

The charter of this working group is to look at the long-term research needs of the semiconductor industry. The working group will then need to understand what is being funded by other initiatives, where the gaps are, and then suggest priorities to the IAC as to where the focus areas should be for CHIPS funding and the NSTC that provide the best opportunities to sustain US leadership in semiconductor innovation.

1) How to establish research grand challenges, and refresh periodically?

2) What are the research grand challenges (that impact long term needs)?

3) What are the most important R&D gaps to these challenges?

4) What role should the CHIPS Act entities and funding play?

R&D Gaps WG breakout teams

#1	What are the R&D grand challenges and gaps?	Debo, Philip, Om, Chuck
#2	How to establish research grand challenges, and refresh periodically?	Ahmad, James, Todd, Raj
#3	How should the CHIPS Act entities address R&D grand challenges and gaps?	Carol, Mukesh, Susie, Ann

Summary of R&D Gaps WG progress

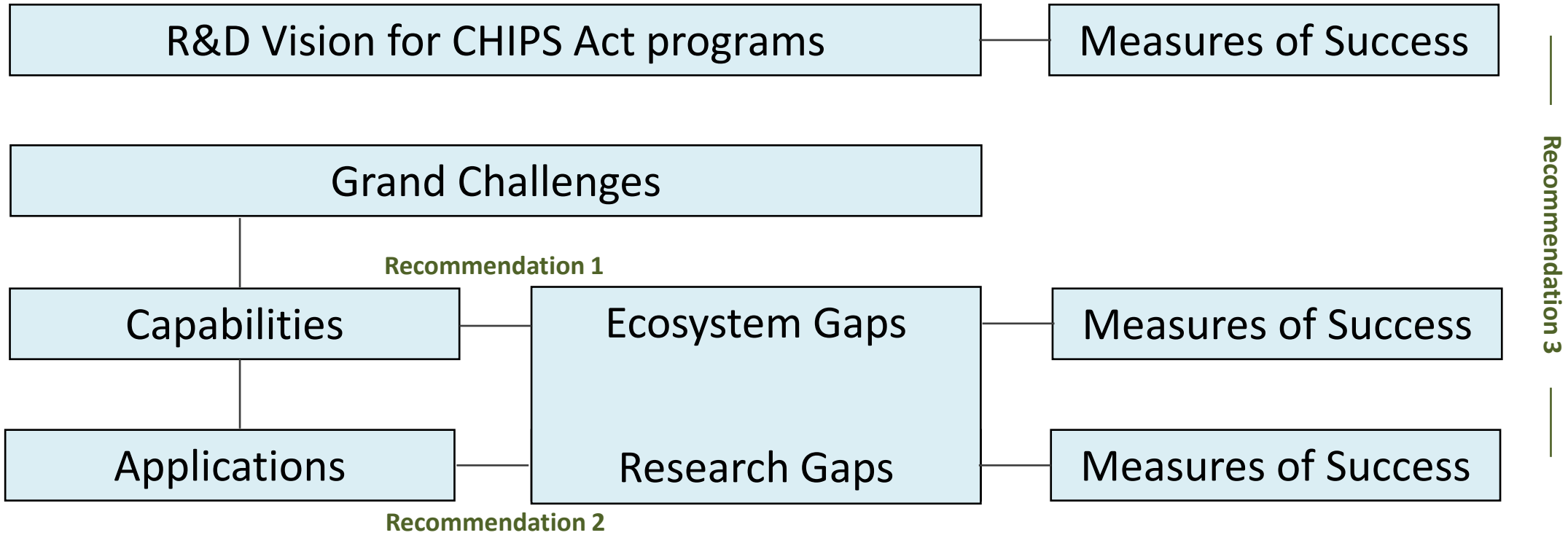
Focus of 90-day sprint:

- Reviewed 15 R&D reports and invited 20 experts to record their POV
- Created an overarching R&D vision
- Achieved consensus on capabilities and application grand challenges
- Defined ecosystem and research gaps for each challenge
- Identified measures of success overall, and for grand challenges
- Prepared recommendations by Feb 7 IAC meeting

Mostly deferred to subsequent sprints (overlaps with WG#2 scope):

- How to prioritize among grand challenges (emphasis, timing, scope)
- How to execute overall mission in NSTC / NAPMP / Mfg USA

R&D Gaps WG framework



R&D Gaps WG vision

1) Drive semiconductor innovation for energy efficiency and a sustainable planet

2) Democratize access to the semiconductor innovation engine

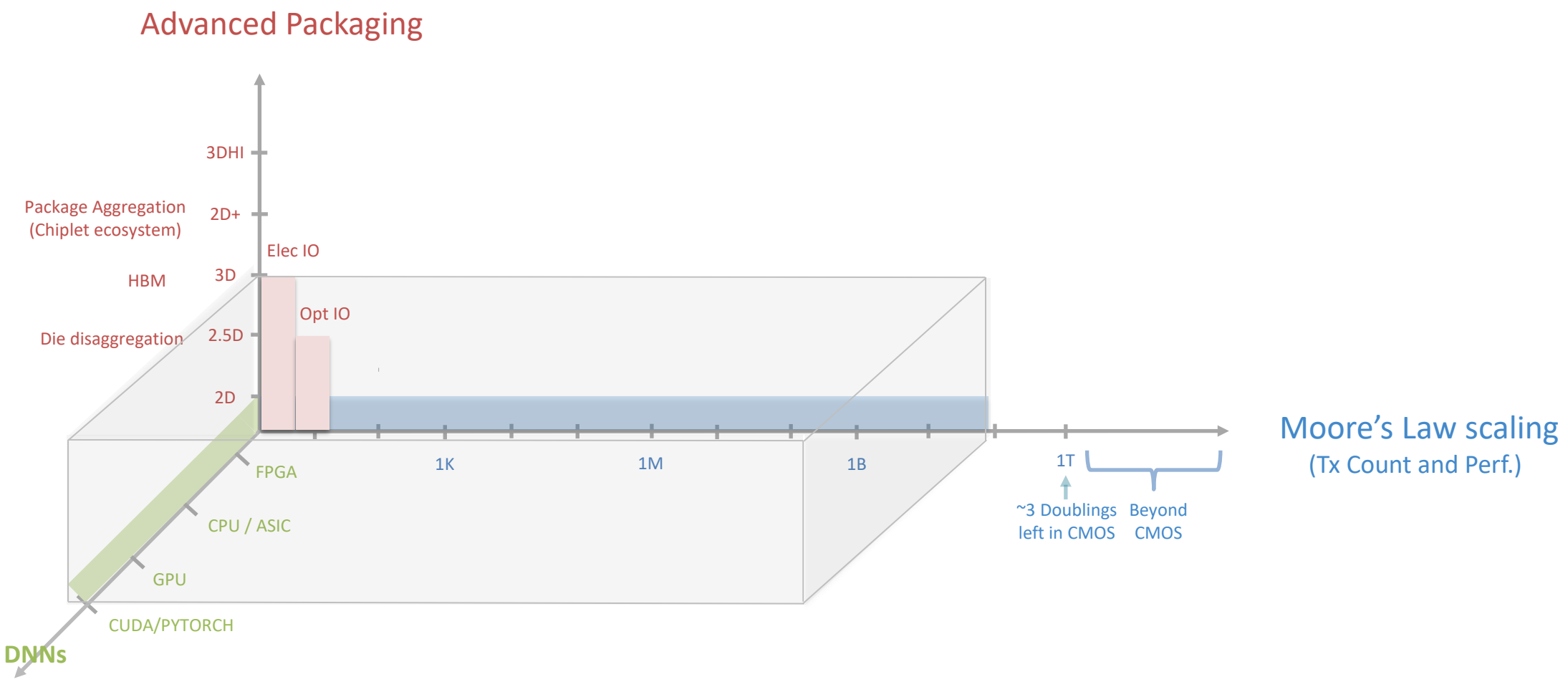
3) Supercharge semiconductor system innovation through an open chiplet platform

4) Regain undisputed US technology leadership through fundamental R&D which will revolutionize applications

5) Grow semiconductor industry through start-up incubation and acceleration

6) Cultivate a knowledgeable talent pool

Context: Expanding the computing volume drives economics



Application driven systems with specialized architectures/algorithms
w/ software stack

R&D Gaps Working Group recommendations

Recommendation 1:

Establish a set of five key capabilities aimed to lower the barriers to entry and success for innovators. These capabilities will rely on a network of physical and virtual facilities with a digital backbone to reduce design and experimentation cycle time. These capabilities should benefit the *entire community of stakeholders and it should be of primary importance to increase access to and reduce the effective cost of accessing these capabilities over time.*

Recommendation 2:

Identify a small number of application driven grand challenges to inspire innovation across the computing stack and spans fundamental materials, equipment and process R&D, design, and manufacturing. The grand challenges should be at the system level, integrating hardware and software considerations, and necessarily require contributions across several layers of the compute and system hierarchy.

Recommendation 3:

CHIPS Act R&D programs must demonstrate their relevance through support and contributions from all stakeholders, and especially industry, as the ultimate measure of success – by periodic assessment of quantified metrics that are endorsed by appropriate advisory and governance bodies.

R&D Gaps Working Group recommendations

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1) Establish easily accessible prototyping capabilities in multiple facilities and enact the ability to rapidly try out CMOS+X at a scale that is relevant to industry

2) Create a semiverse digital twin

3) Establish chiplets ecosystem and 3D heterogeneous integration platform for chiplet innovation and advanced packaging

4) Build an accessible platform for chip design and enable new EDA tools that treat 3D (monolithic or stacked) as an intrinsic assumption

5) Create a nurturing ecosystem for promising startups

R&D Gaps Working Group recommendations

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1) Improve computing energy efficiency by 1,000X in a decade including leveraging domain specific accelerators and architectures, and innovation in materials, process and equipment technologies.

2) Develop and implement next-generation semiconductor manufacturing that is 10X more capital and human resource efficient and achieve net zero emissions with minimum waste and demonstrated sustainable materials in the next decade.

3) CHIPS Act R&D programs to prioritize additional application grand challenges with advice from stakeholders (see next page).

R&D Gaps Working Group recommendations

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CHIPS Act R&D programs to prioritize additional application grand challenges with advice from stakeholders.

Candidates include:

- AR/VR performative solutions that enable mobile and interactive computing and communication access for training, education and life
- Next generation wireless communication building blocks at 10x energy efficiency, 10x capacity and 10x reduction in latency compared to today's state of the art
- High voltage intelligent power solutions for grid/distribution control and sensing at 10X higher power density and at >90+% efficiency
- Life science health monitoring, diagnostics and therapeutic wearable and implantable solutions
- Life science brain-like information interface via multi-modal neuroscience solutions
- Autonomous systems via multi-modal and "intelligent" sensing to action with integrated decision making 100x lower energy and cost for ubiquitous application.

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Capabilities

1.Cost, cycle time and utilization of prototyping capabilities against benchmarks. Projects enabled via CHIPS Act R&D programs should show a significant improvement over the status quo. Startups and researchers should constitute an impactful proportion. Included should be measuring the progress of projects to higher readiness levels.

2.Utilization and integration of semiverse and co-design capabilities with leadership capabilities

3.Utilization of an accessible platform for chip design and new 3D EDA tools

4.A functioning ecosystem of standards, for example, for chiplets that are increasingly integrated in 3D, with supporting packaging and test prototyping capabilities

5.Quantity of startups, quality of outcomes and transition to CVC and VC supported funding rounds

Applications:

1.Ecosystem participation and satisfaction of all stakeholders in standards, roadmaps, capabilities, program prioritization and execution.

2.Achievement of fundamental breakthroughs that lead to advances towards achieving application grand challenges

3.Achievement of quantified and time-based intermediate milestones of demonstrations

Overall R&D programs:

1.Obtaining membership fees and program matching contributions from stakeholders, both amount and variety of sources

2.Obtainment of US manufacturing outcomes for CHIPS Act R&D that emerge ready for translation to commercialization, showing the connection between R&D and mfg.

3.Recognition by stakeholders that the CHIPS Act R&D programs are widely viewed as neutral and trusted.

4.Cancellation of some programs due to failure or change in support – its absence would indicate a lack of robust feedback and risk taking.

5.Generation of revenue streams as a percentage of funding, including fees for utilization of capabilities, licensing of IP developed by the CHIPS Act R&D programs and valuations (non-cash) and returns from investment capital for startup portfolio.

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