Organization / PPP Working Group Update and Deliberation

DoC Industrial Advisory Committee

Deirdre Hanford and Org/PPP WG Hosted by: Ben Davis, Designated Federal Officer February 7, 2023

Agenda

- Recap of Organization/PPP focus and activities
- Recommendations
- Deliberation

IAC Organization / PPP Working Group



Bill Chappell Microsoft



Scott DeBoer Micron



Michael Fritze

Potomac Institute for Policy Studies



Deirdre Hanford Synopsys

Ken Joyce Brewer Science



Alex Oscilowski TEL America

Composition

- Hyperscaler
- Semiconductor
- Think tank
- Packaging
- SME
- Academia
- EDA & IP

Supported by DoC staff

- Ben Davis, DFO
- Tamiko Ford, DFO
- Lisa Ng





Willy Shih Harvard Business School



Anthony Yen ASML Technology Development Center

Aligning with Commerce



IAC Organization / PPP Working Group – February 7, 2023 IAC meeting

At present, the Department is engaged in four high-priority tasks:

- Evaluating potential gaps in research and engineering that could be filled by the NSTC. As part
 of the whole-of-government effort, the NSTC will
 complement the many excellent centers already
 established by industry, academia, allies, and other
 governmental agencies. The Department will create
 a preliminary landscape analysis with the benefit
 of recommendations developed by the CHIPS
 Industrial Advisory Committee. Ultimately, the NSTC
 itself will finalize the focus areas, but this early work
 will inform further decisions.
- Evaluating and defining a structure and governance model that fulfills the CHIPS for America goals of promoting U.S. economic and national security and protecting taxpayer investments while ensuring technical excellence and leadership.
- Creating a preliminary operating, business, and financial model that will serve as a road map for near-term investment informed by an understanding of what will be required for long-term sustainability.
- Identifying a slate of candidates for the NSTC chief executive.

The Department will release a white paper in the first quarter of 2023 that will summarize the results of the landscape analysis, governance structure, and preliminary operating and financial model. At that time, the Department will issue guidance on when to expect requests for proposals.

Organization / PPP Working Group Charge

01

This working group will review and examine all the various funding sources for semiconductor R&D and map out the relationships between these entities to ensure spending efficiency and eliminate any overlaps. 02

In addition, this working group will review the essential functions and governance of the NSTC and NAPMP.

03

Finally, this committee will review PPP proposals for both R&D partnerships, the value proposition for industry participation in PPPs, as well as investment funds and support of start ups

Briefings

Organization	Торіс	Guest
NIST	CHIPS Overview and program mapping	Dr. Jason Boehm, Chief of Staff, NIST
Semiconductor Alliance	NSTC/NAPMP	Dr. Raj Jammy, CTO and Chief Technologist, MITRE-ENGENUITY
DoD Undersecretary of Defense for Research & Engineering	DoD Microelectronics Commons	Dr. Dev Shenoy, DoD, PD Microelectronics, OUSD (R&E) Microelectronics Modernization
NIST	Interagency perspective on R&D programs	Dr. Ronald Jones, CHIPS R&D Interagency Coordinator, NIST
Intel Corporation	NAPMP	Dr. Babak Sabi. SrVP and GM of Assembly/Test Development Dr. Tom Rucker, VP Technology and Development
Department of Commerce	NSTC Governance	Ms. Donna Dubinsky, Senior Counselor for CHIPS Implementation
IMEC	Best practices on PPP's and IMEC governance structure	Dr. Luc Van den hove, President and CEO, IMEC
American Semiconductor Innovation Coalition	NSTC / NAPMP	Dr. Mukesh Khare, Vice President Hybrid Cloud Dr. Douglas Grose, Advisor
	Lessons learned	Dr. Paolo Gargini

Org / PPP Working Group

- Focus of January Sprint Charge 2 NSTC Governance
 - NSTC entity structure and type of governance board
 - NSTC CEO profile
 - NSTC capabilities and value proposition
 - NSTC's interface with CHIPS R&D program office and industry

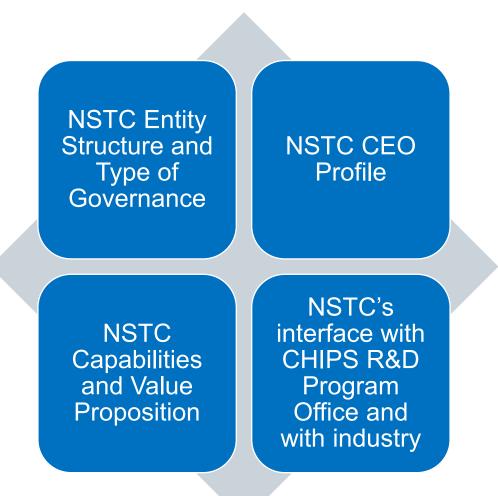
- Deferred to subsequent sprints
 - NSTC/NAPMP
 - Early Wins for NSTC
 - Important role of academia
 - Composition of governance board
 - IP rights
 - Charge 1: examine all the various funding sources for semiconductor R&D and map out the relationships between these entities to ensure spending efficiency and eliminate any overlaps
 - Charge 3: review PPP proposals for both R&D partnerships, the value proposition for industry participation in PPPs, as well as investment funds and support of start ups

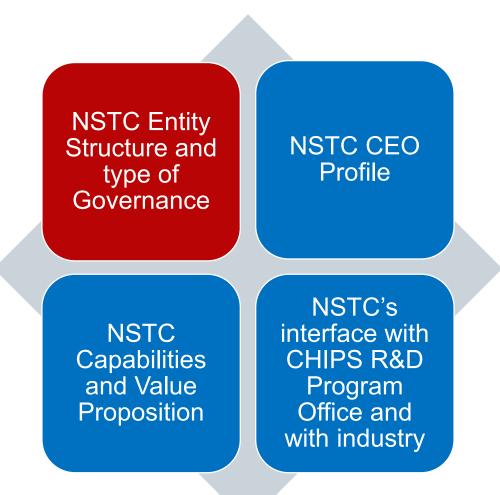
Agenda

• Recap of Org/PPP working group focus and activities

Recommendations

- 1 NSTC entity structure and type of governance board
- 2 NSTC CEO profile
- 4 NSTC capabilities and value proposition
- 5 NSTC's interface with CHIPS R&D program office and industry
- Deliberation





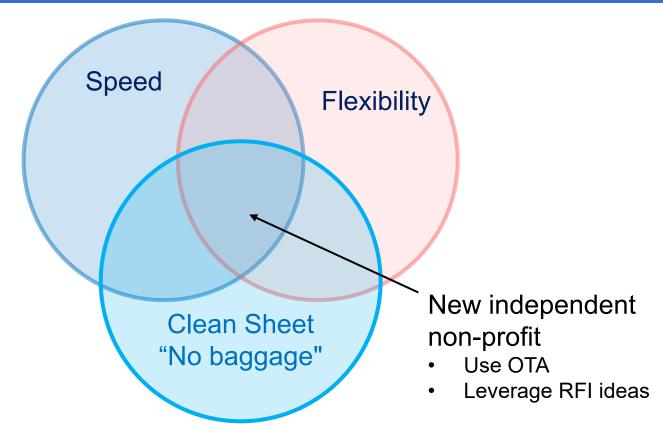
Questions

Principles



NSTC Entity Structure

Recommendation 1-1: The subcommittee recommends that the Department of Commerce structure the NSTC as a new and independent non-profit utilizing the Department's Other Transaction Authority (OTA), leveraging many of the ideas that have been proposed in RFI responses but unencumbered by established agendas



We considered:

- Government corporations
- Partnership with or independent new non-profit
 - New likely using Other Transaction Authority
 - Existing
- Speed via Other Transaction Authority (OTA)

NSTC Board Structure

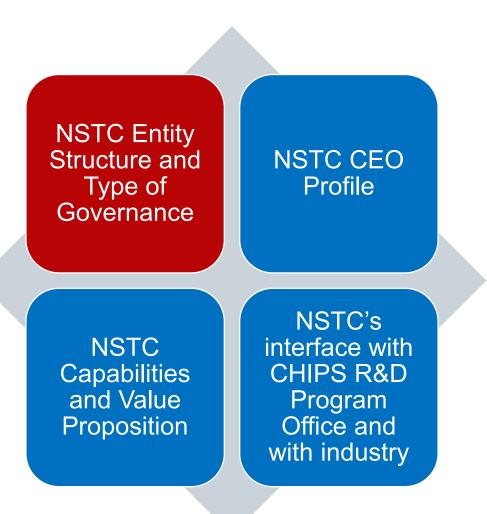
Recommendation 1-2: The subcommittee recommends a <u>fiduciary board</u> for oversight of the NTSC

- Fiduciary board
 - Requires members with appropriate experience/expertise to exercise due diligence and oversight to ensure that the organization is well managed
 - Does not necessarily direct the CEO and organization to make individual investments or take specific actions. Rather its roles is to ensure a solid decision-making process and a financially sound strategy
 - Independent and free of member company representation
 - Note: have not yet deliberated on specific fiduciary board composition
- Governance structure fosters independence of the CEO
 - Streamlined governance, simplicity and agility
- Technical Advisory Board (TAB) provides the CEO with technical and program guidance, bringing deep industry and technical knowledge
 - Member companies represented on the TAB

We considered:

- Fiduciary and Representative Boards
- Governance structures including:
 - Independent versus government entity
 - IMEC, DARPA, NSF, SRC, and SEMATECH, public company boards

- Independent, nimble and new non-profit
- Leverage input from RFI teams
- OTA (vs. solicitation)
- Fiduciary board (vs. member board)
- Members participate in TAB



NSTC CEO Profile

Recommendation 2-1: The subcommittee recommends recruiting a highly respected executive with deep technical expertise and senior level leadership experience in the semiconductor industry to serve as the CEO of NSTC

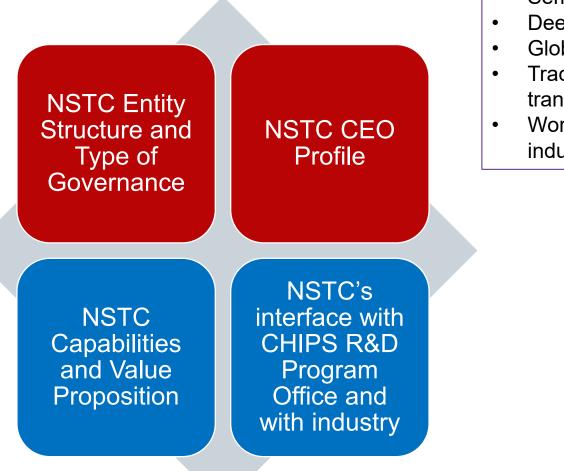
CRITICAL CAPABILITIES:

- Deep technical expertise and experience in semiconductor industry
- Visionary: willing to initiate high-risk/high-reward programs to enable critical technologies
- Bold thinking: Open to new leverageable ideas proposed by responders to Commerce RFIs
- Ability to work smoothly with USG Program Offices and Technical Advisory Board
- Skillful in designing organizational structures and business processes
- **Track record**: running global organization with significant operational scale
- Experience Leading Technology based organization: Technology & Product Roadmaps
- **Thinks** and **acts creatively** non-traditional alternatives: collaborations/partnerships
- Suitable CEO tenure to enable establishment of a sustainable NSTC

Considerations:

- Archetypes
- Has created businesses and/or industry technical achievements during career
- Track record of transitioning technologies and bringing them to market
- Can consider an academic with strong industry experience
- Career runway
- Appointment process
- CEO authority and reporting

- Independent, nimble and new non-profit
- Leverage input from RFI teams
- OTA (vs. solicitation)
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Semiconductor industry

- Deep technical experience
- Global, Bold, Creative
- Track record of technology transition to market
- Works with partners, USG, industry and academia

NSTC Vision

- Robust U.S electronics ecosystem to assure economic competitiveness and microelectronics R&D leadership
- An NSTC that **brings together** industry, academia, and government
- Attract the most motivated students to the field, as well as the most skilled scientists, engineers and technology practitioners
- Support small entities so they can successfully create new value



NSTC Mission

- Coordinating function to encourage ecosystem growth
- Strengthen core domestic semiconductor R&D, development, and manufacturing
- Attract industry participation and private capital
- Grow skills pipeline
- Guide mid- and long-term R&D
 directions
- Facilitate transition of R&D into domestic and allied production
- Attract aligned foreign investments

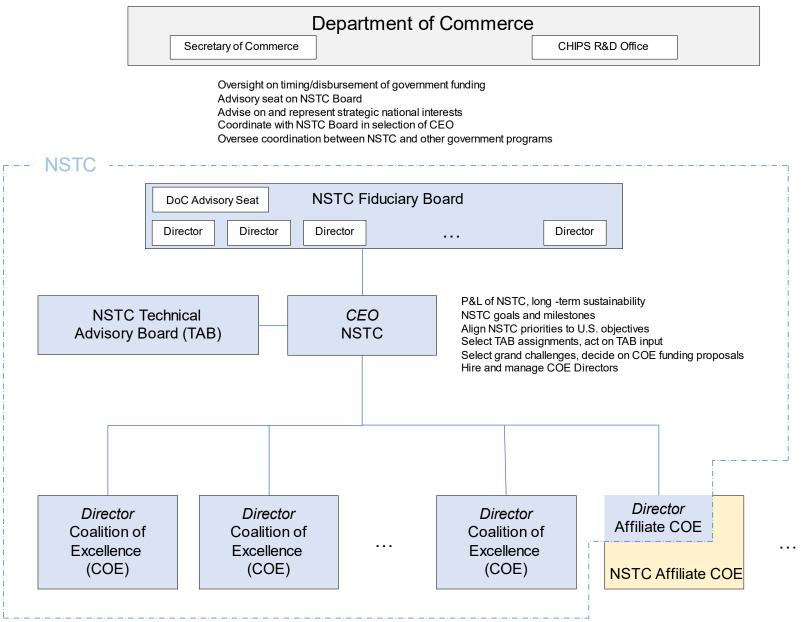
NSTC PPP Organization

Recommendation 4-1: The NSTC should be a leading and convening public private partnership, led by an independent CEO reporting to a fiduciary board, with the advice of a Technical Advisory Board (TAB).

The CEO oversees Multiple Coalitions of Excellence (COEs), each with an Executive Director who oversees specific work sectors

Considerations:

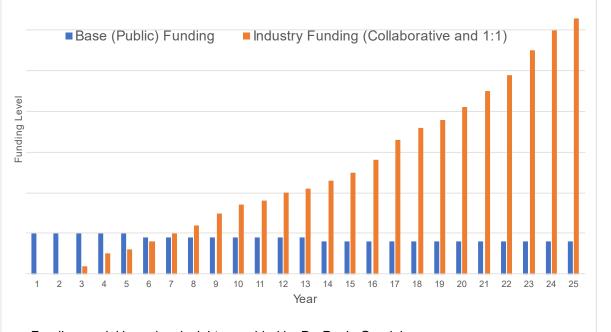
- CEO appointment process
- CEO authority & reporting structure
- COE specialization areas



NSTC Sustainable Business Model

Recommendation 4-2: The NSTC should develop a sustainable business model, with increased funding by industry over time. Government funding should provide risk capital to facilitate broad participation of firms and research institutions of all sizes and means

 Industry and Government must co-invest for the long term to ensure sustainability and ongoing success



Considerations:

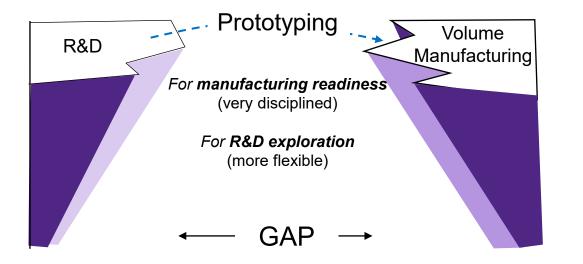
- Successful PPPs strike a good balance between Industry and Government investment
- Sustained government investment ensures **broad access** (start-ups, universities, small businesses) and increased **risk tolerance**
- Sustained Industry investment ensures relevance and evergreen capabilities
- Compared organizational models
- IMEC, SRC, SEMATECH, etc.

Funding model based on insights provided by Dr. Paolo Gargini

From Prototypes \rightarrow Domestic Volume Manufacturing

Recommendation 4-3: The NSTC should offer prototyping enablement with a translation path to multiple domestic volume production sources, encompassing the spectrum from pre-competitive to private research program types. It should lower barriers to innovation and enable smaller entities to participate

 NSTC should leverage COE capabilities and U.S. Shared Resource Network to facilitate transition to domestic manufacturing

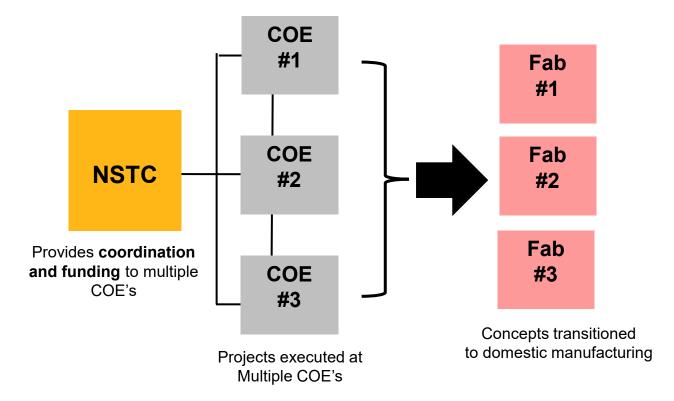


Considerations:

- Baseline flows/PDKs to enable execution
- Provides value to large entities
- Accessible to small/mid size entities, start-ups
- Provides a pathway to volume manufacturing

Vital Role of COEs

Recommendation 4-4: NSTC should be a funding mechanism for Coalitions of Excellence and for projects executed within and across COEs



Considerations:

- NSTC coordinates projects at multiple COE's
- CEO decides COE areas and leadership for each
- COEs prototype R&D concepts for domestic production

Have not yet addressed:

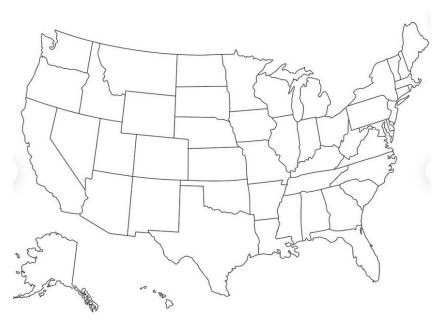
 How will NSTC work with other entities

 ME Commons, NSF, SRC, DARPA, et al.

Partner with and complement existing centers, rather than build from scratch

Recommendation 4-5: NSTC should partner with and be complementary to existing centers, and emphasize build-out of the ecosystem and enabling infrastructure

• Building a **sustainable domestic infrastructure** that leverages existing US & global capabilities.



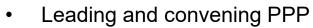
COE's located across the US

COE's leverage existing domestic infrastructure

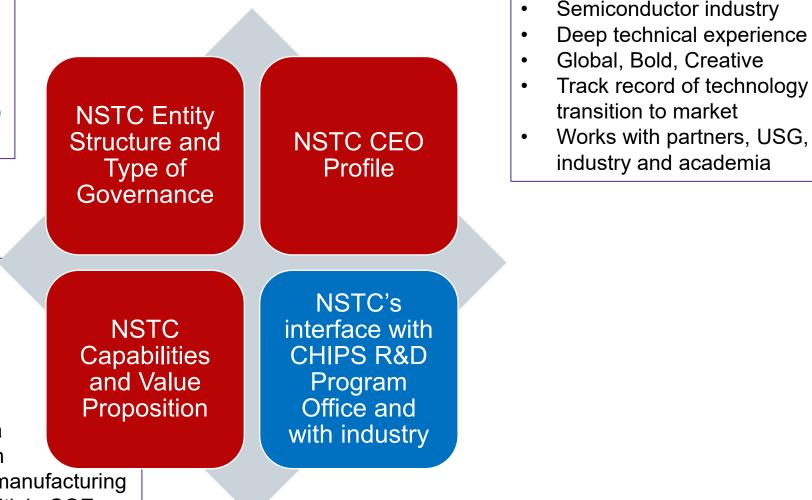
Also engage with overseas organizations w/ domestic footprints **Considerations:**

- Need for early "wins" with new organization
- Leverage existing US infrastructure
- Enable new domestic capabilities
- Engage global capabilities within the US
- Provide technical and financial leverage

- Independent, nimble and new non-profit
- Leverage input from RFI teams
- OTA (vs. solicitation)
- Fiduciary board (vs. member board)
- Members participate in TAB



- Empowered CEO oversees
 multiple COEs
- Sustainable business model with increasing industry funding and ongoing USG investment in order support small entities and academia
- Offering prototyping capabilities with transition path to domestic volume manufacturing
- NSTC is funding mechanism for multiple COEs
- Leverage existing facilities



Questions

NSTC Principles

What is the interaction between the NSTC CEO and the DoC CHIPS R&D Director?

Where do the Executive Directors of the COEs reside and what are the expectations of them?

What is the role of competition?

Promote Competition of Ideas

Avoid conflicts of interest

Establish clear **joint goals and success metrics** aligned with NSTC mission

Structure of goals drives competition
 of ideas

Enable the emergence of disruptive innovations by allowing **exploration of** "out-of-the-box" insights

Ability to **accept technical risks and make hard decisions**, including cutting poor performance or stopping programs Recommendations

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Recommendation 5b-1: A strong centralized NSTC CEO office that emphasizes personal responsibility and avoids committee group think. The CEO should be given broad autonomy on how the organization's goals are executed

Department of Commerce				
Secretary of Commerce	CHIPS R&D Office			
Oversight on timing/disbursement of government funding Advisory seat on NSTC Board Advise on and represent strategic national interests Coordinate with NSTC Board in selection of CEO Oversee coordination between NSTC and other government programs				
DoC Advisory Seat NSTC Fiduciary Board				
Director Director	Director			
ISTC Technical CEO NSTC goals and Align NSTC priori Select TAB assig	ng -term sustainability milestones ities to U.S. objectives Inments, act on TAB input Ilenges, decide on COE funding proposals			

Adv

NSTC CEO

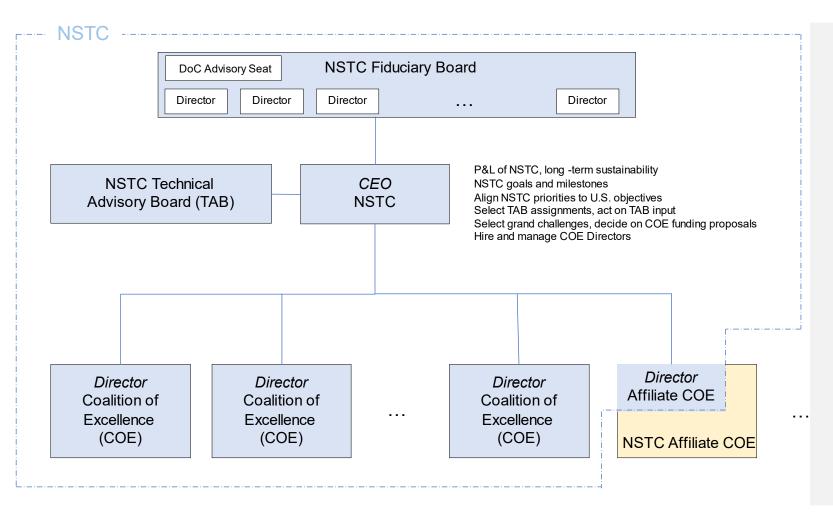
- Strong centralized CEO office essential
- Broad authority and autonomy
- Politically shielded

Department of Commerce CHIPS R&D Office

- Oversight on timing and disbursement of funding
- Represent strategic national interests
- Coordination between government entities
- Translation from PCAST

Hire and manage COE Directors

Recommendation 5b-2: The structure of the NSTC must foster healthy competition at its foundation. This competition must apply to entities who are eligible for funding and who meet publicly stated criteria



Executive Directors of the COEs

- Oversee COE operations
- Manage budgets
- Make funding and program recommendations to CEO
- Run project solicitations and execute with public decision criteria that will pass external review
- See proposals from multiple industry participants and be able to shield IP between competing entities
- Be hired by CEO and reside within NSTC

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Recommendation 5b-3: The CEO should be responsible for items delineated below

- Clear <u>understanding of current gaps in U.S. semiconductor technology industry leadership</u>
- <u>Aligning mission</u> to enable the future technology required for U.S. leadership over the next decade
- Technical Advisory Board (<u>TAB</u>) assignments and process
- Meeting objectives and acting on recommendations from the TAB
- <u>Selecting grand challenges</u> and approving and executing the associated proposals
- Setting yearly goals and milestones
- Selection of Coalition of Excellence (COE) focus areas and expected outcomes in conjunction with the CHIPS R&D
 office
- <u>Managing P&L</u> with eye towards long term <u>sustainability</u>, including target mix of government and industry funding and how it evolves over time
- <u>Hiring and managing Executive Directors of Coalitions of Excellence</u>
- Being the *source selection authority* for Coalition of Excellence decisions and arbitrating competitions
- <u>Coordinate</u> with the execution of <u>other government funded programs</u>
- Protect Executive Directors of the COEs and the TAB from outside influence and <u>allow for unbiased technical decisions</u>
- <u>Identify new revenue sources including direct U.S. industry engagement and use of facilities</u>

This is not a complete list – other areas like workforce, investment fund, convening, etc. will also be part of CEO responsibilities

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- Independent, nimble and new non-profit
- Leverage input from RFI teams
- OTA (vs. solicitation)
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NSTC Entity

Structure and

Type of

Governance

• Semiconductor industry

- Deep technical experience
- Global, Bold, Creative
- Track record of technology transition to market
- Works with partners, USG, industry and academia

- Leading and convening PPP
- CEO oversees multiple COEs
- Sustainable business model with increasing industry funding and ongoing USG investment in order support small entities and academia
- Offering prototyping capabilities with transition path to domestic volume mfng
- NSTC is funding mechanism for multiple COEs
- Leverage existing facilities

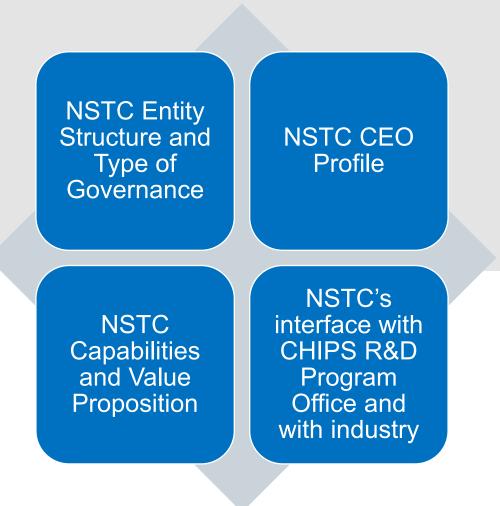
NSTC's interface with CHIPS R&D Program Office and with industry

NSTC CEO

Profile

- Strong empowered CEO with broad autonomy on setting strategy and driving execution
- CEO reports to NSTC Board
- Important relationship with Secretary of Commerce and CHIPS R&D Office
- Competition at its core at NSTC level and at COEs
- Avoids conflicts of interest
- List of responsibilities

Questions and Deliberation



Voting

NSTC entity structure and type of governance board

- Recommendation 1-1: The subcommittee recommends that the Department of Commerce structure the NSTC as a new and independent non-profit utilizing the Department's Other Transaction Authority (OTA), leveraging many of the ideas that have been proposed in RFI responses but unencumbered by established agendas
- Recommendation 1-2: The subcommittee recommends a fiduciary board for oversight of the NTSC

NSTC CEO profile

Recommendation 2-1: The subcommittee recommends recruiting a highly respected executive with deep technical expertise and senior level leadership experience in the semiconductor industry to serve as the CEO of NSTC

Vision and Mission of NSTC Recommended Organizational Form

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 oversees Multiple Coalitions of Excellence (COEs), each with an Executive Director who oversees specific work
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- Recommendation 4-2: The NSTC should develop a sustainable business model, with increased funding by industry over time. Government funding should provide risk capital to facilitate broad participation of firms and research institutions of all sizes and means
- **Recommendation 4-3:** The NSTC should offer prototyping enablement with a translation path to multiple domestic volume production sources, encompassing the spectrum from pre-competitive to private research program types. It should lower barriers to innovation and enable smaller entities to participate
- **Recommendation 4-4:** NSTC should be a funding mechanism for Coalitions of Excellence and for projects executed within and across COEs
- **Recommendation 4-5:** NSTC should partner with and be complementary to existing centers, and emphasize build-out of the ecosystem and enabling infrastructure

Interface between the NSTC, the DoC CHIPS Program Office and Industry

- Recommendation 5b-1: A strong centralized NSTC CEO office that emphasizes personal responsibility and avoids committee group think. The CEO should be given broad autonomy on how the organization's goals are executed
- **Recommendation 5b-2:** The structure of the NSTC must foster healthy competition at its foundation. This competition must apply to entities who are eligible for funding and who meet publicly stated criteria
- Recommendation 5b-3: The CEO should be responsible for items as described in presentation

Thank You

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