A 3D stacked nanowire technology - Applications in advanced CMOS and beyond

T. Ernst, L. Duraffourg, C. Dupré, K. Tachi, E. Bernard, P. Andreucci, V. Maffini-Alvaro, S. Bécu, E. Ollier, E. Colinet, P. Cherns, A. Hubert, C. Halté, C. Vizioz, S. Barnola, J. Buckley, O. Thomas, G. Delapierre, V. Delaye, J.-M. Hartmann, M. Cassé, P. Rivallin, M. A. Jaud, E. Saracco, M. Jublot, B. de Salvo, J.P. Colonna, S .Deleonibus and O. Faynot

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Outline

- Introduction
- Stacking nanowires for MOSFETs and memories
- Sensors
- Conclusion

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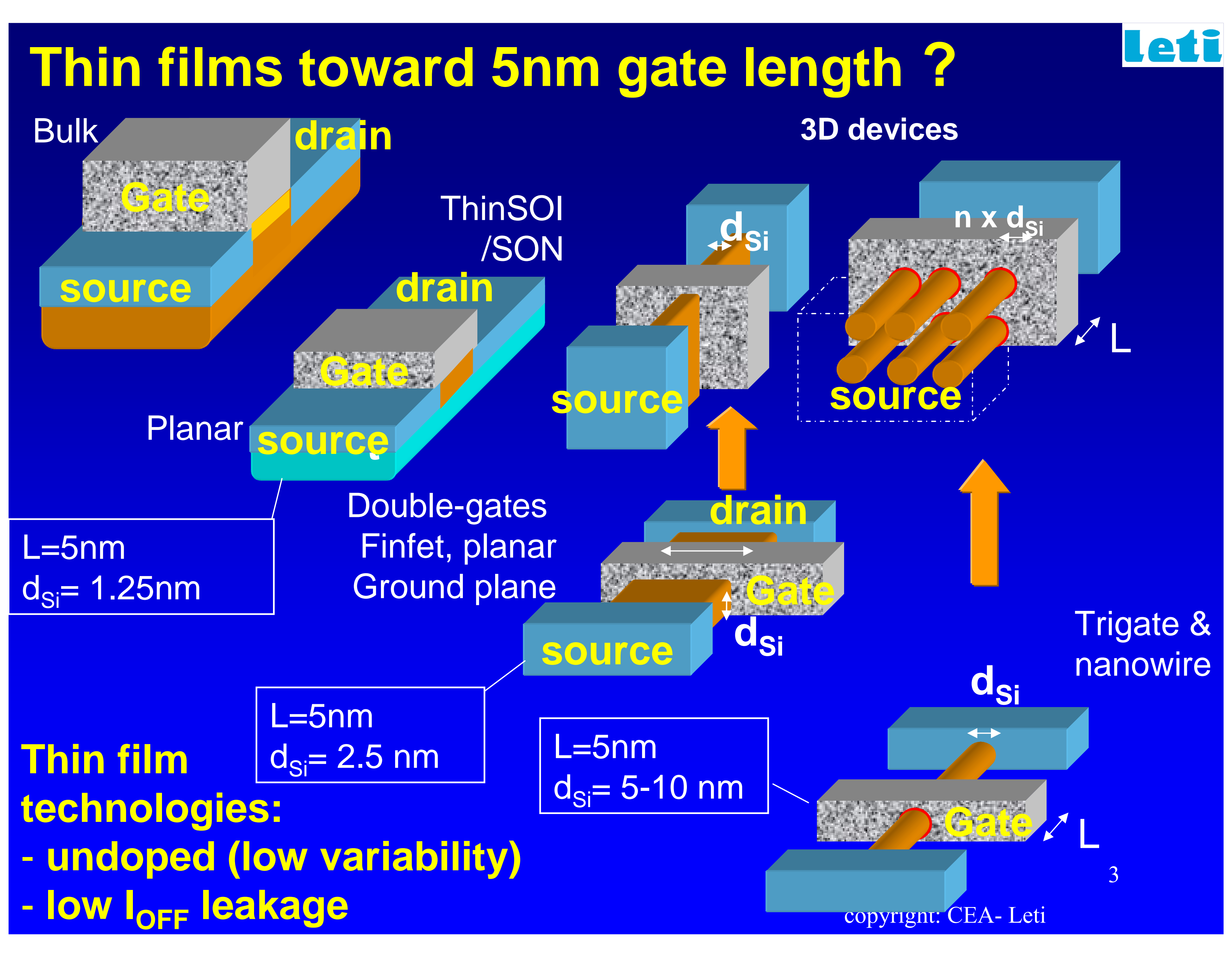
Thin films toward 5nm gate length ?
Leti
Bulk
drain
Gate
source
ThinSOI
/SON
drain
Gate
Planar
source
L=5nm
d_Si= 1.25nm
Double-gates
Finfet, planar
Ground plane
3D devices
d_Si
source
n x d_Si
L
source
drain
Gate
source
d_Si
L=5nm
d_Si= 2.5 nm
L=5nm
d_Si= 5-10 nm
Trigate &
nanowire
d_Si
Gate
L
Thin film
technologies:
- undoped (low variability)
- low I_OFF leakage
3
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Nanowire for sub 22nm nodes ?

CVD nanowires > above IC ?

Si

SiGe

T. Ernst et al. , IEDM06

N. Singh et al. , IEDM06

More than Moore

3D Nanowires

3D Memories

3D

3D stacked devices

Bio detection - NEMS

3D

Mono electronic

Logic

FDSOI

Std SOI

UTBOX

Nanowire

More Moore

22nm

16nm

11nm

<11nm

2009 2010 2012 2013 2014 2015 2016

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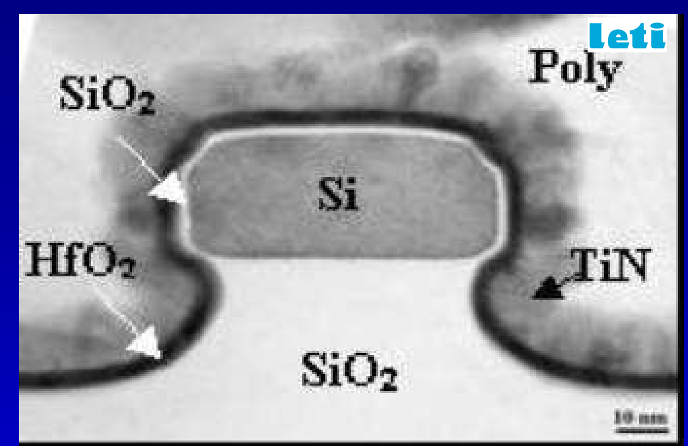
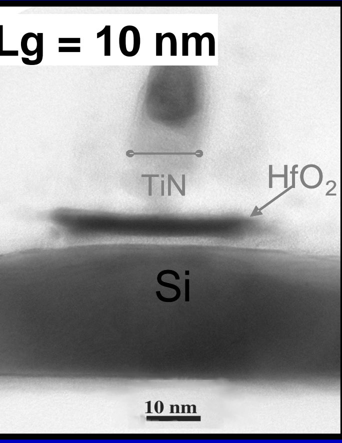
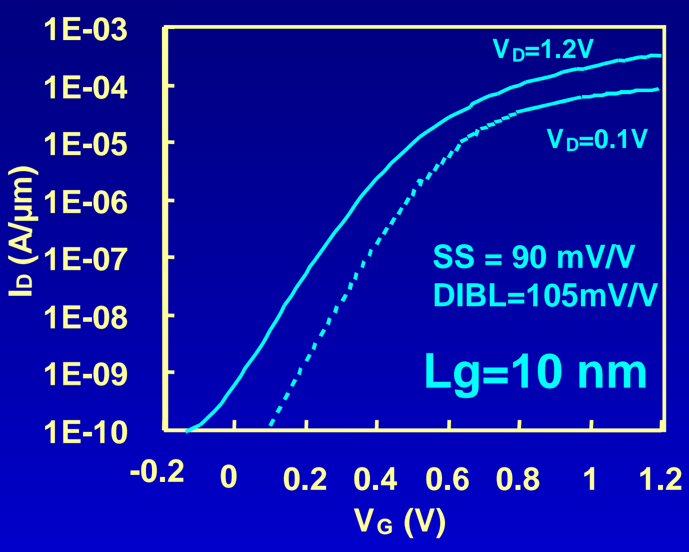
NanowireFET scalability - state of the art

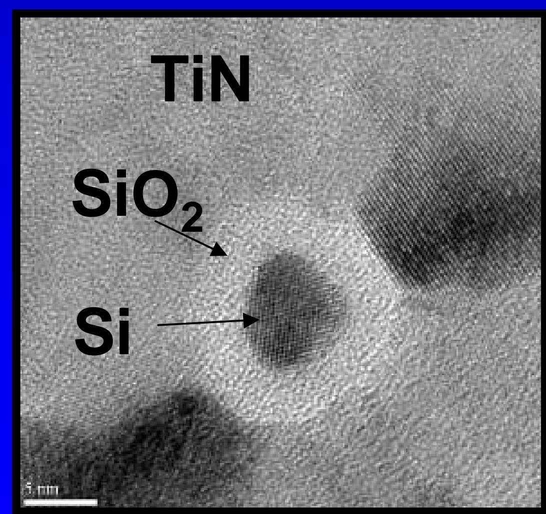
C. Jahan et al, VLSI'05 – 20 x 50 nm trigate

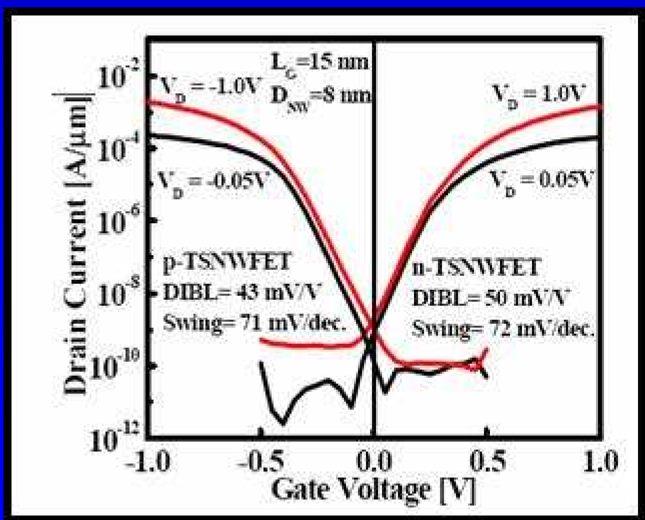






K. H. Suk et al. IEDM'06 8x8 nm GAA nanowire





Functional 10nm (I_{OFF}<1nA/µm) gate length ΩFETs with good electrostatic control, even with relaxed diameter and trigate configuration

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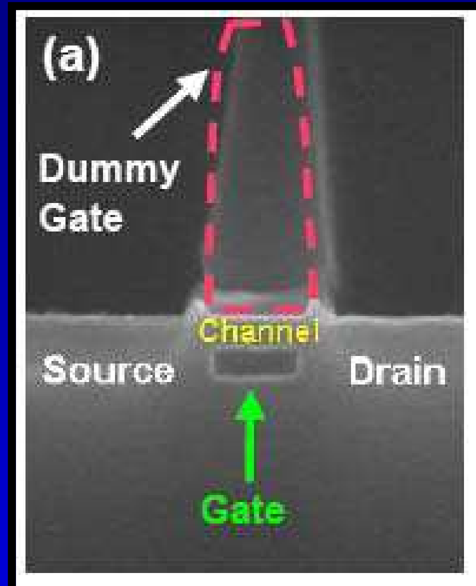
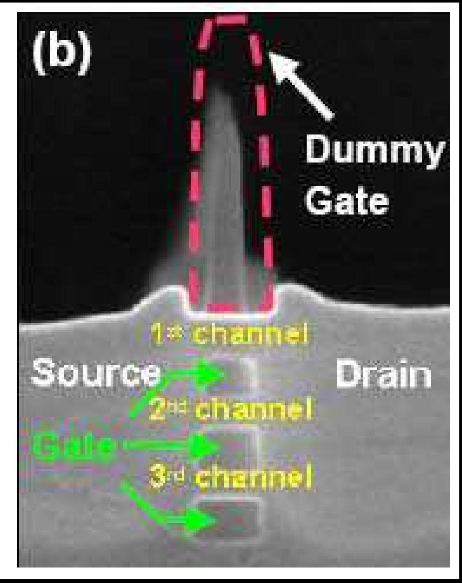
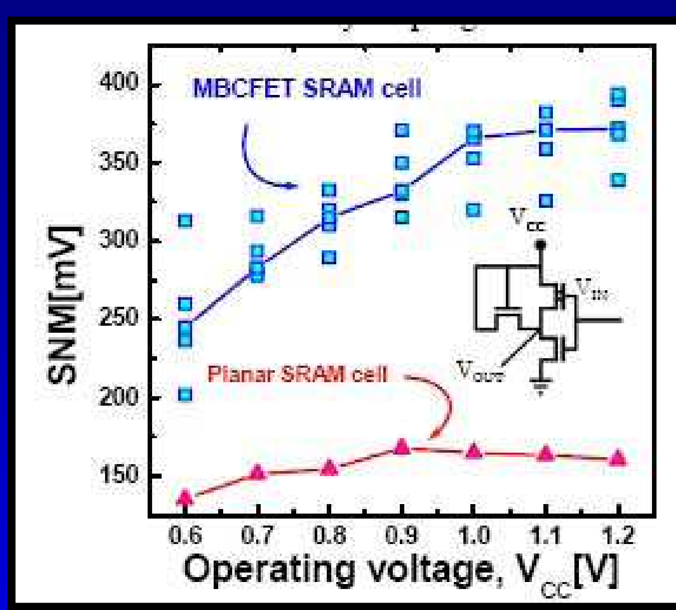
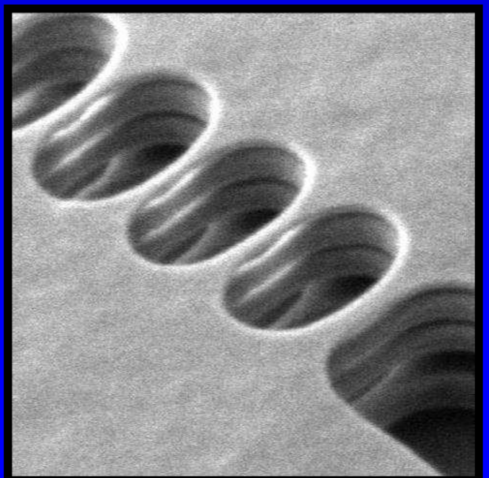
Multi-Channel FET - state of the art







M.S. Kim et al. , VLSI 06



Excellent static noise margin

Several technologies for levels separation:

- **=> Preferential oxidation**
- **=> Wet etching**
- **=> Dry plasma etching or HCl**

N. Singh et al. , IEDM06

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Outline

Leti

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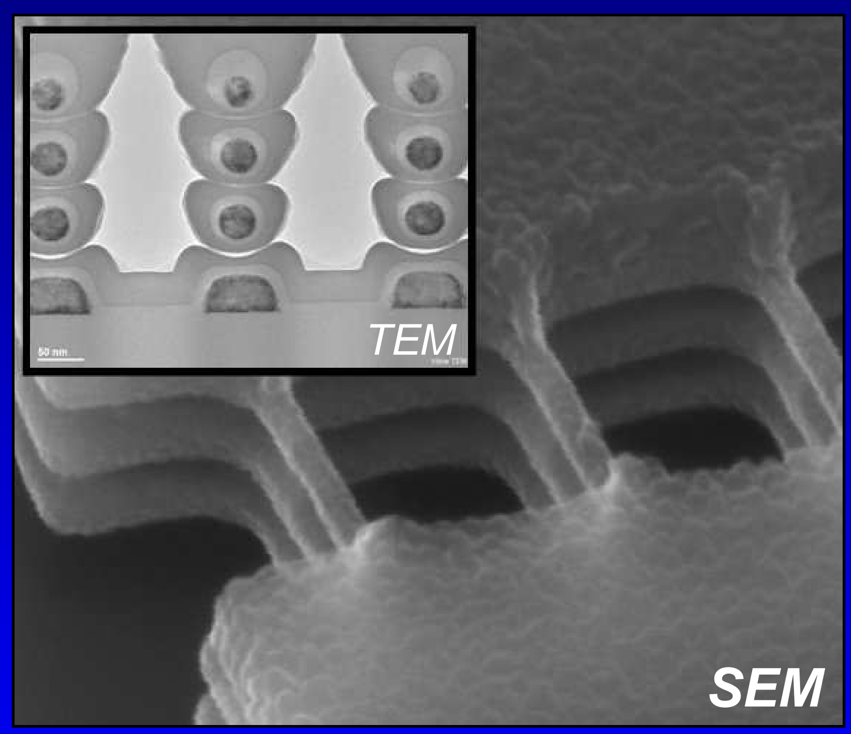
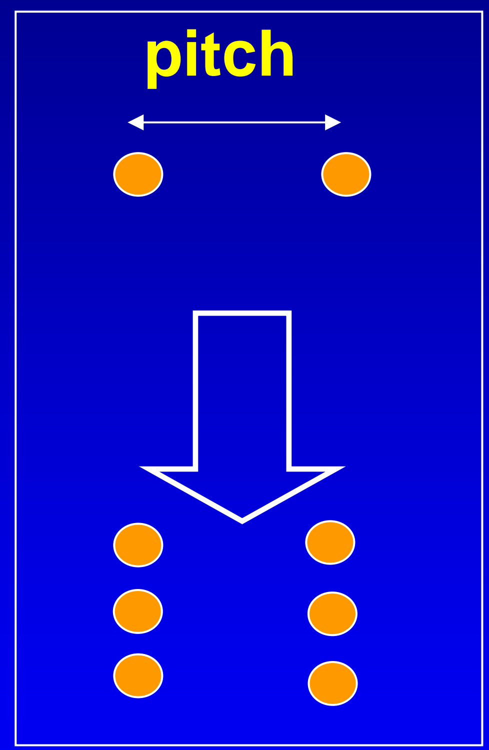
Building stacked nanowires ... pitch limitation 3D overbalanced





- Use of nanowires limits the available Si surface for conduction
- 3D Multi-channels: a very efficient approach to increase available surface
- Open tunable width and tunable shape possibilities

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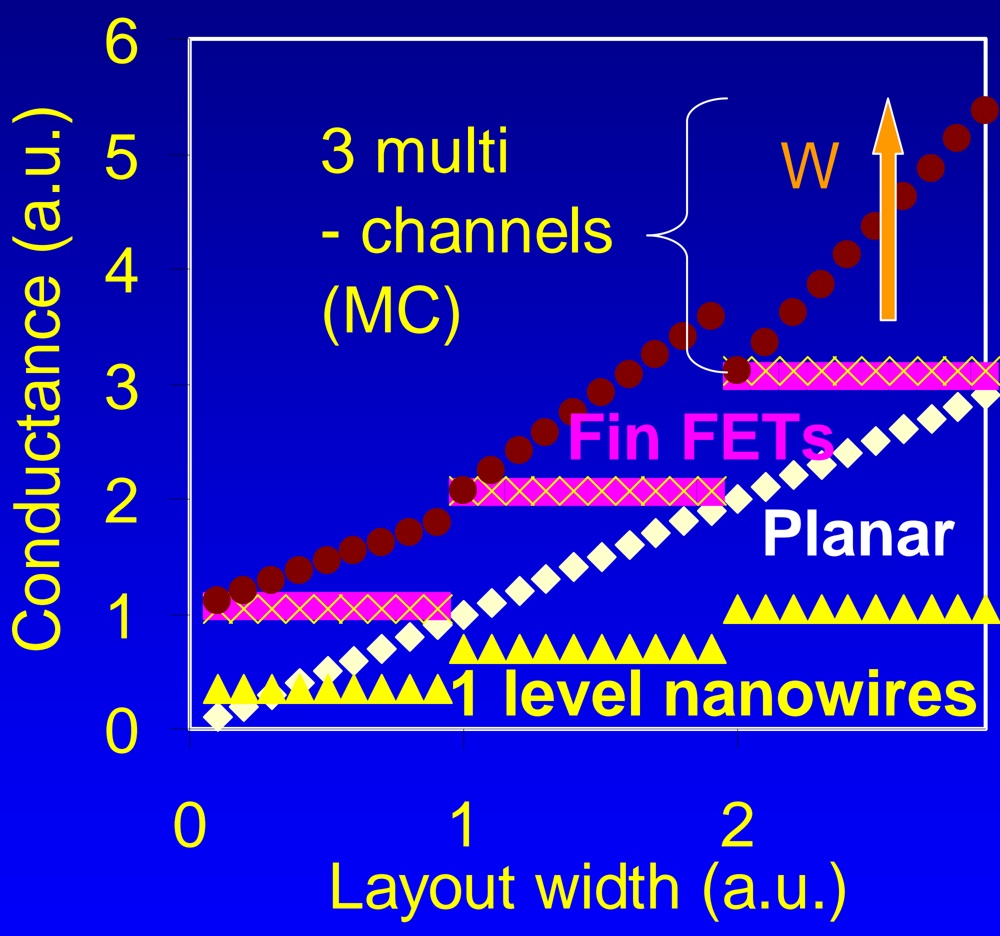
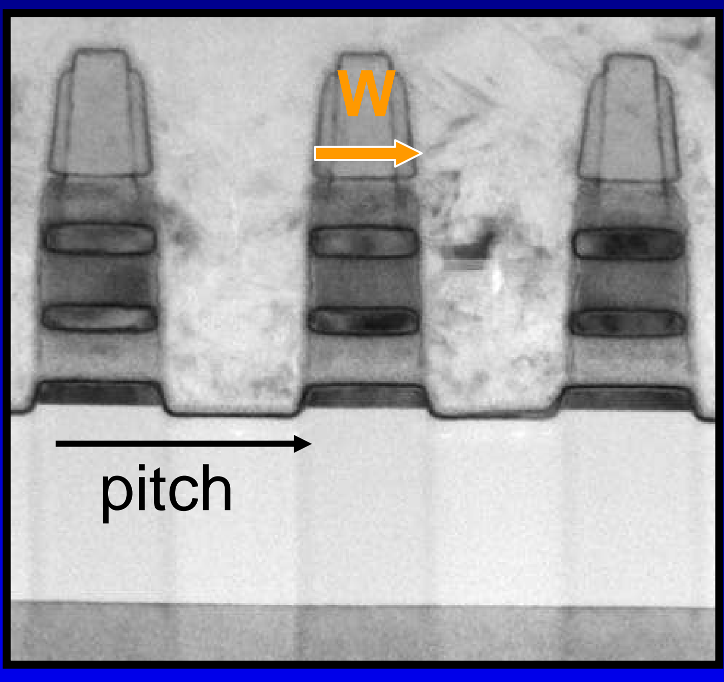
Tunable width





See for details:
T. Ernst et al, IEDM'06,'08 SSDM'07, ICIDT'08
E. Bernard et al. VLSI'08, ESSDER'07
C. Dupré et al, IEEE SOI Conference 07

Design flexibility to tune the conductance

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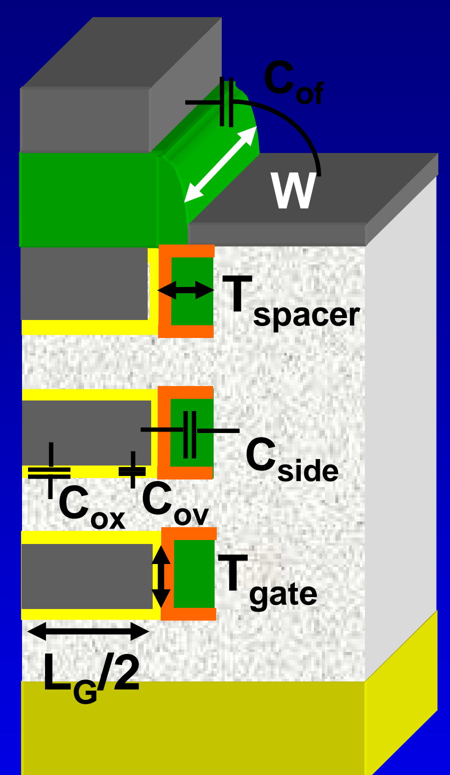
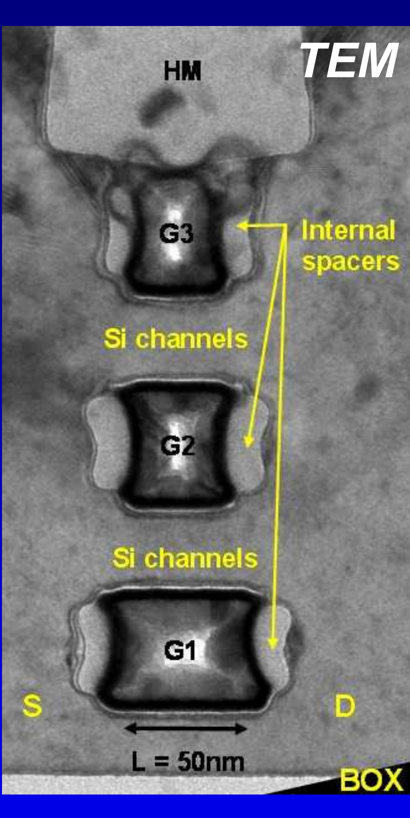
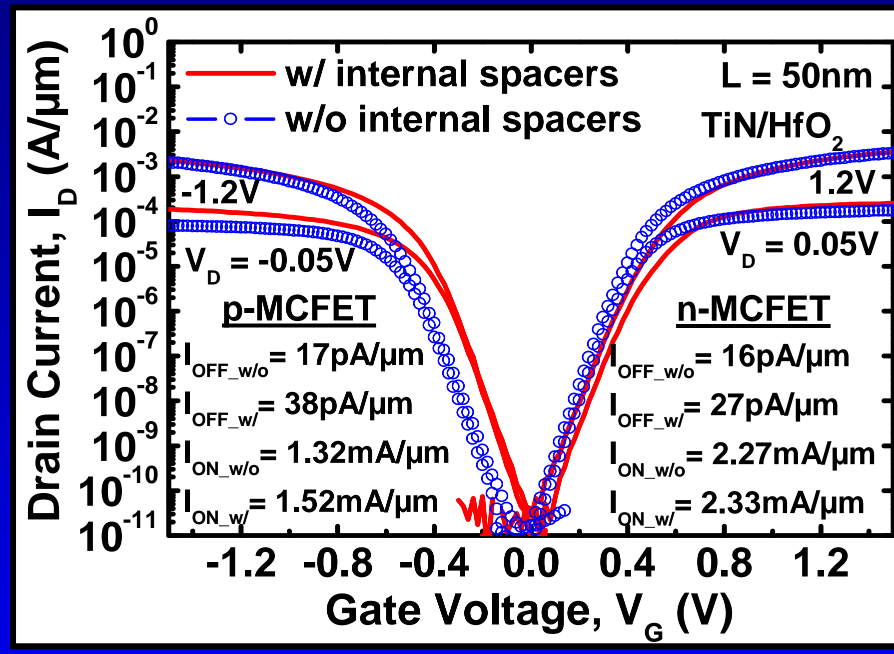
Internal spacers





L=50nm W=50nm



E. Bernard, N. Vulliet, B. Guillaumot, T. Ernst et al.
VLSI 2008 & Electron Device Letters Feb. 2009

CEA/LETI & STMicroelectronics collaboration on GAA/SON technology

Internal spacers reduce capacitances without impacting I_{ON}/I_{OFF} current

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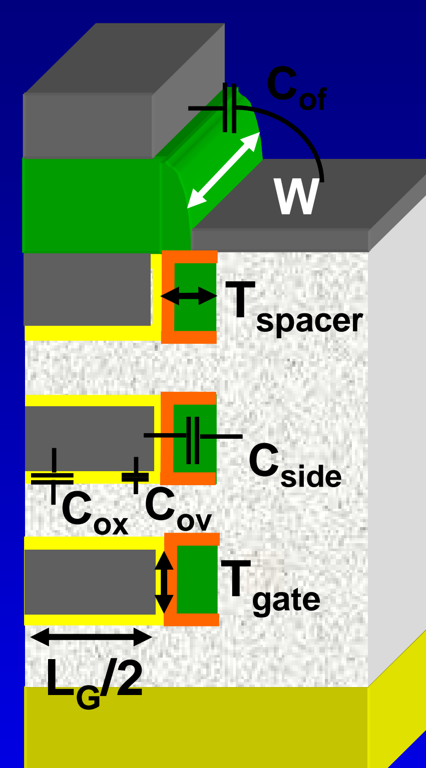
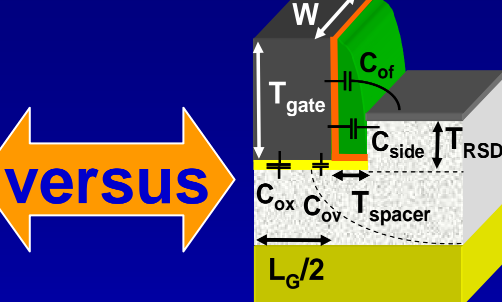
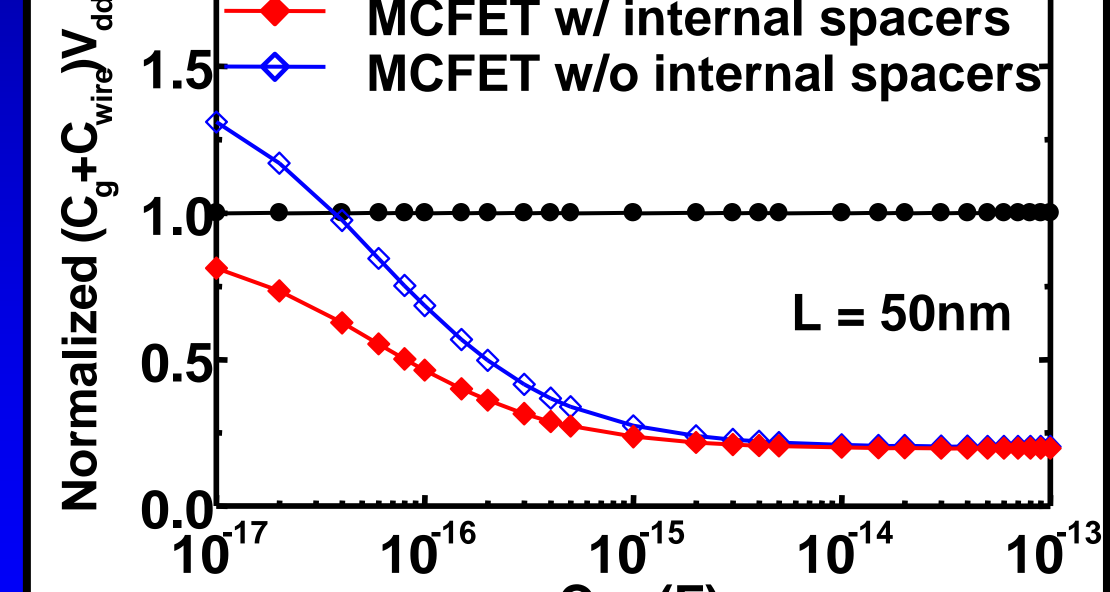
CV/I : 3D versus planar



versus





E. Bernard et al.
IEEE Trans. Elec. Device
t.b.p., June 2009

Multi-Chanels CV/I outperform planar in a loaded environment

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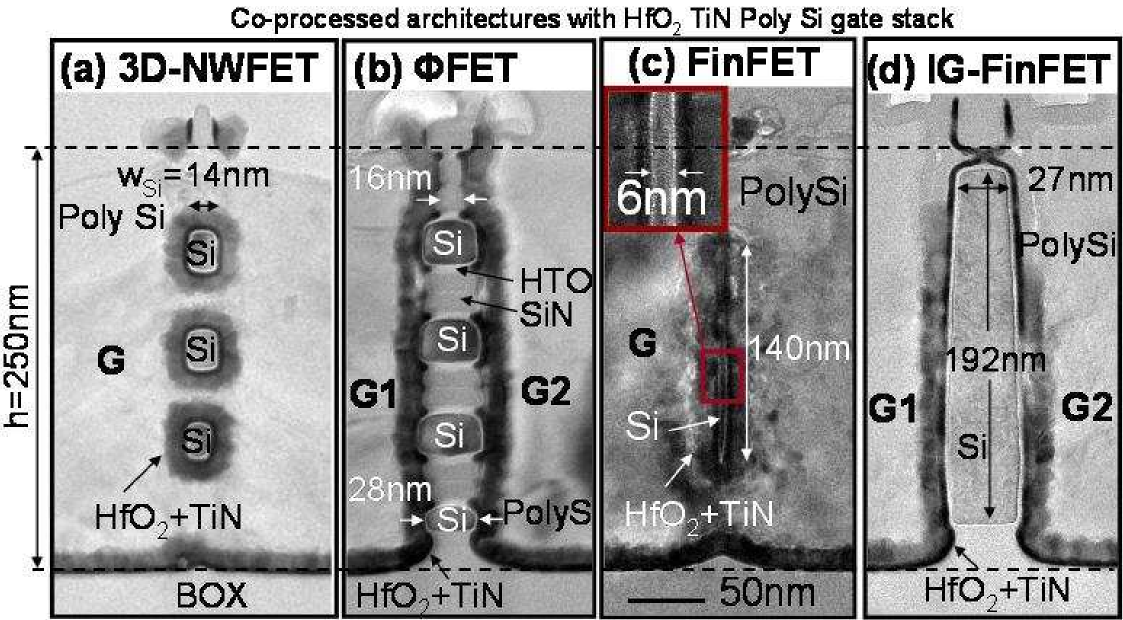
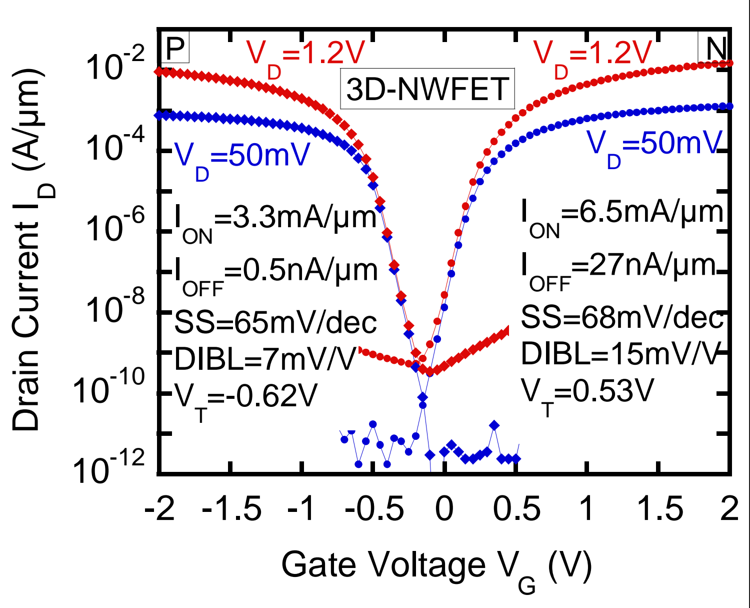
Tunable shape for flexible designs



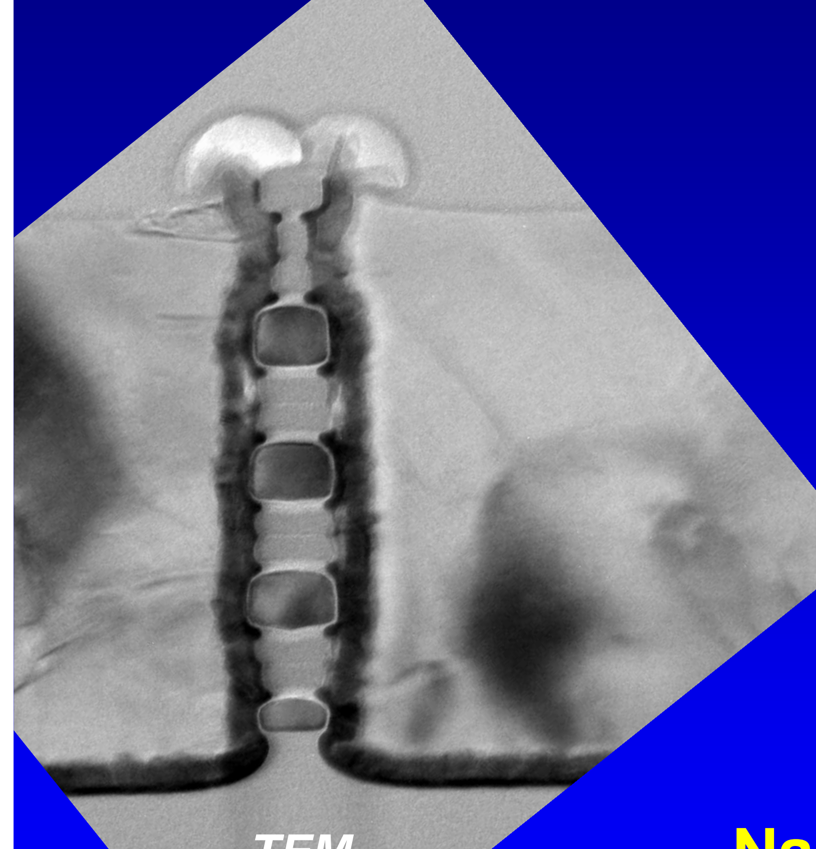


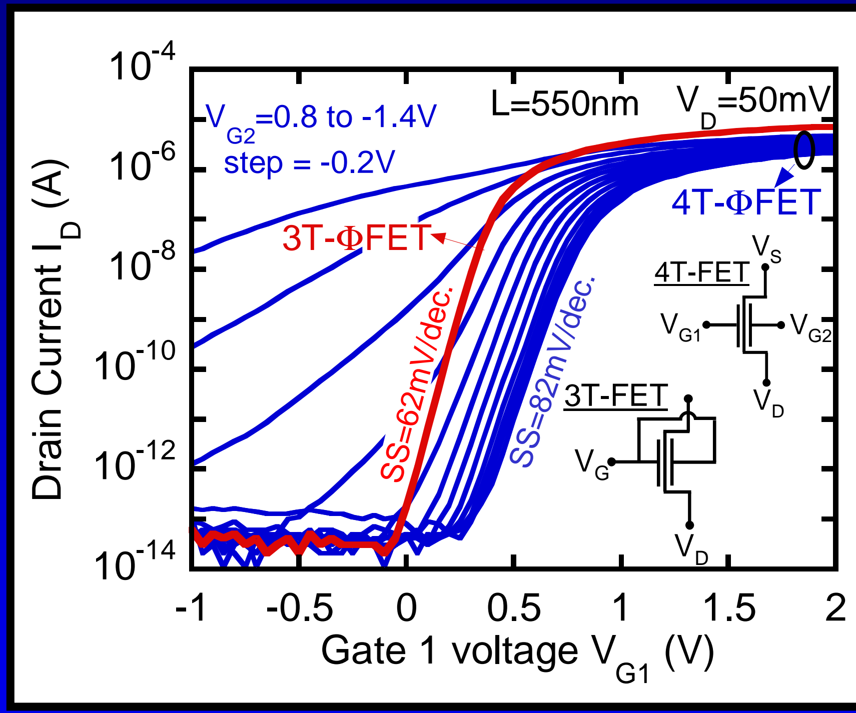
Flexible process :

- Reduced gate capacitance (spacers)
- Independent gate nanowire (PhiFet)
- Finfet compatible
- Excellent current drivability due to 3D: 6.5 mA/µm !

copyright: CEA- Leti

Nanowires with independent gates (Φ-Fet) electrical results

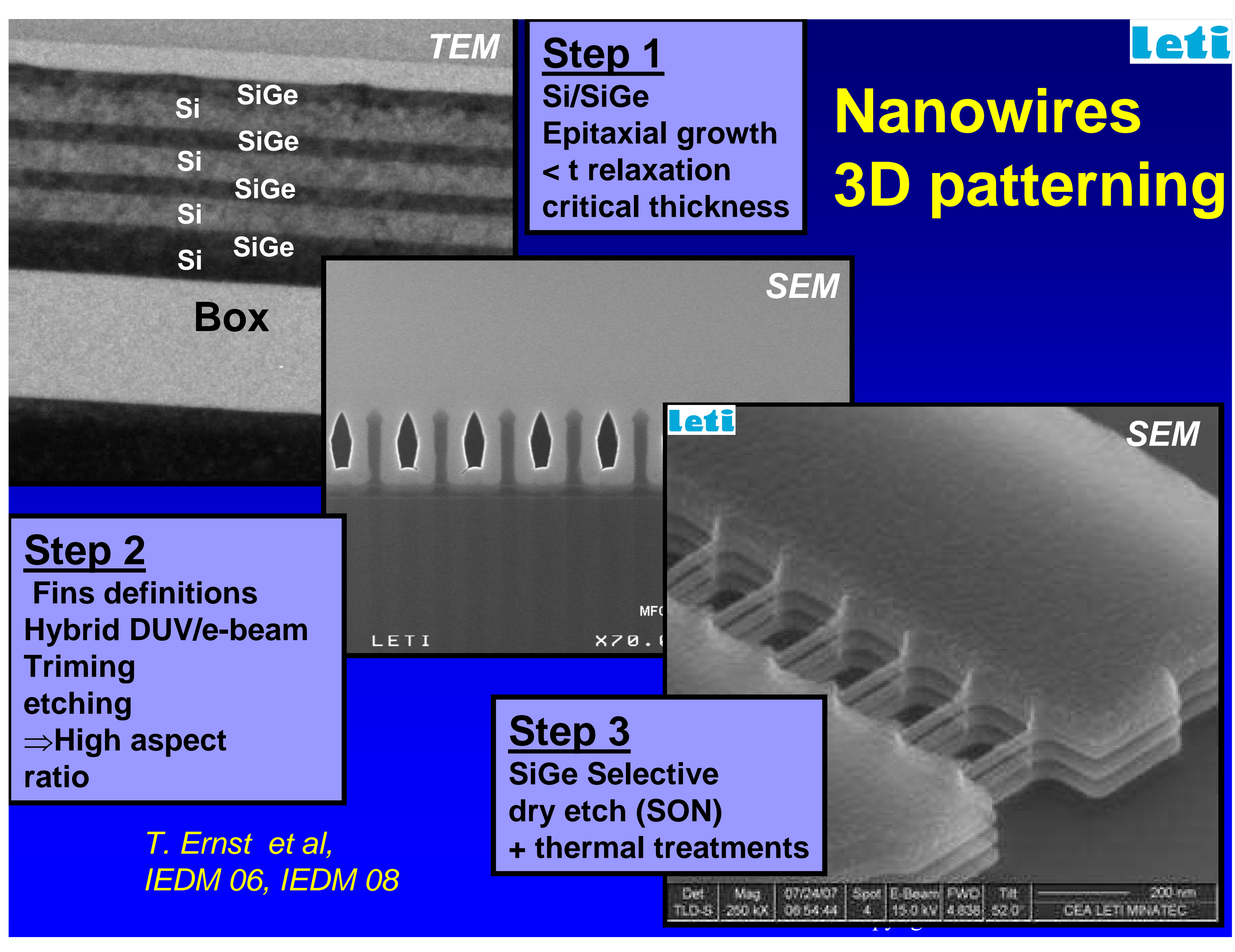




Nanowires with independent gates allows ultra-low power management

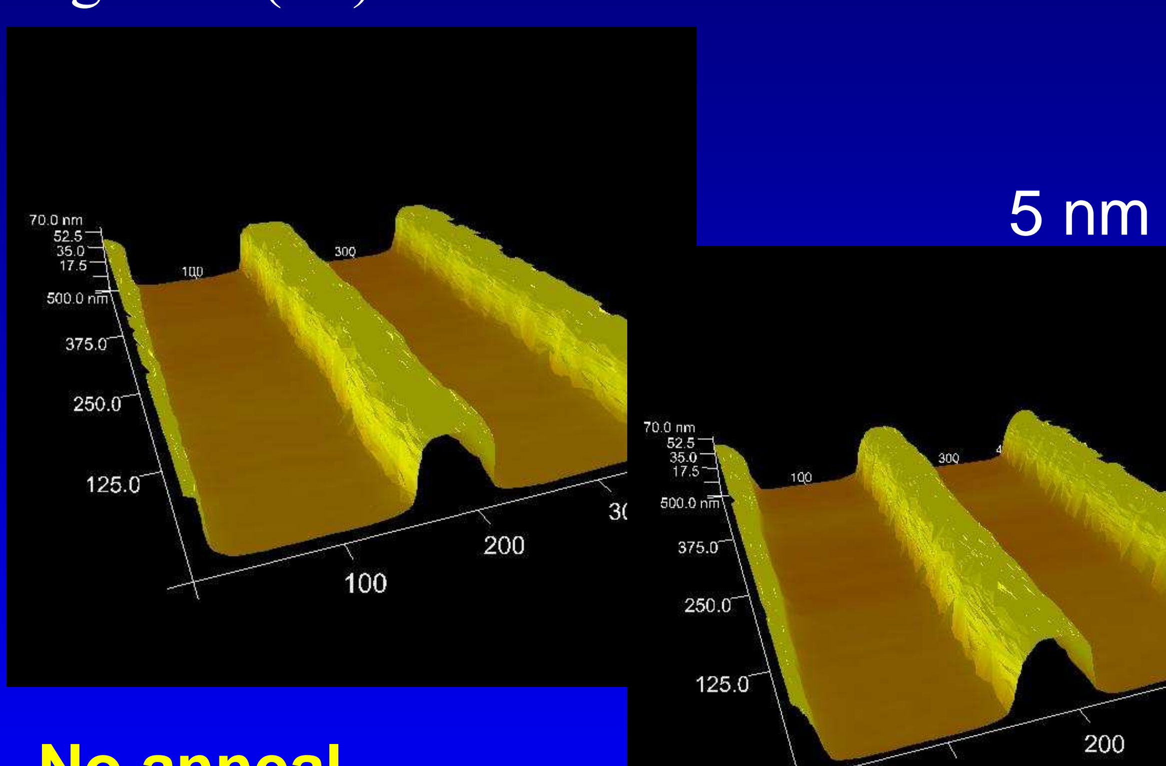
C. Dupré et al, IEDM 08

copyright: CEA- Leti


TEM
Si
SiGe
Si
SiGe
Si
SiGe
Si
SiGe
Box
Step 1
Si/SiGe
Epitaxial growth
< t relaxation
critical thickness
Nanowires
3D patterning
leti
SEM
LETI
SEM
leti
Step 2
Fins definitions
Hybrid DUV/e-beam
Triming
etching
⇒High aspect
ratio
Step 3
SiGe Selective
dry etch (SON)
+ thermal treatments
T. Ernst et al,
IEDM 06, IEDM 08

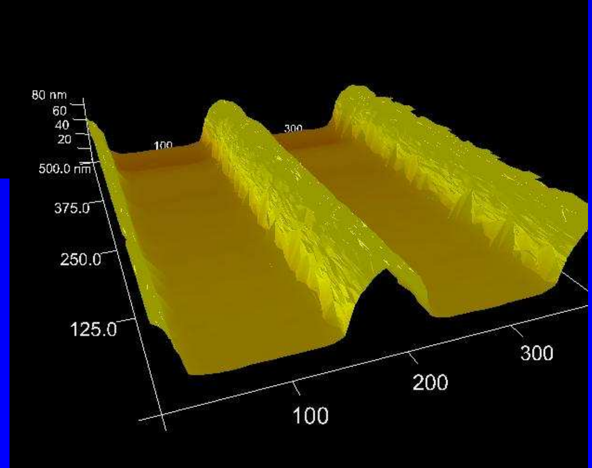
Rounding by hydrogen annealing

Line roughness (3σ) 6.5 nm



5 nm

3.5 nm



No anneal

800℃ anneal

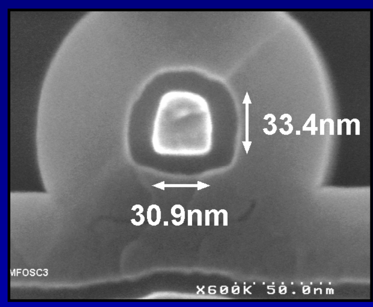
850℃ anneal

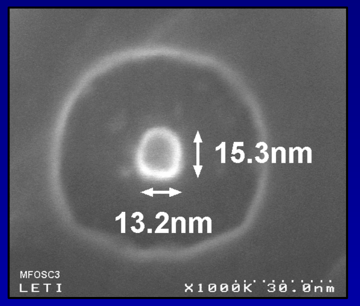
3D Atomic Force Microscopy
J. Fouchet, CEA-LETI

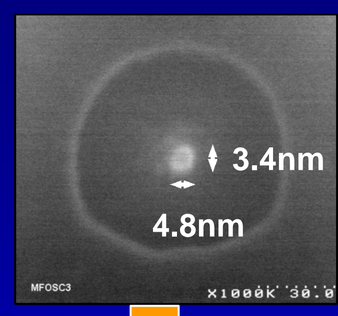
E. Dornel et al , Appl. Phys. Lett. 91, 233502 (2007)

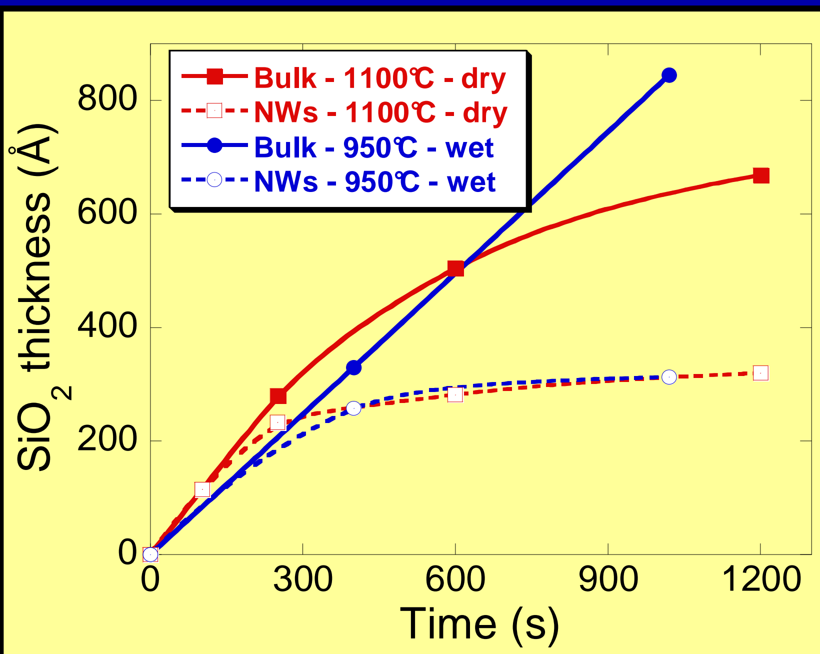
Nanowires oxidation kinetics

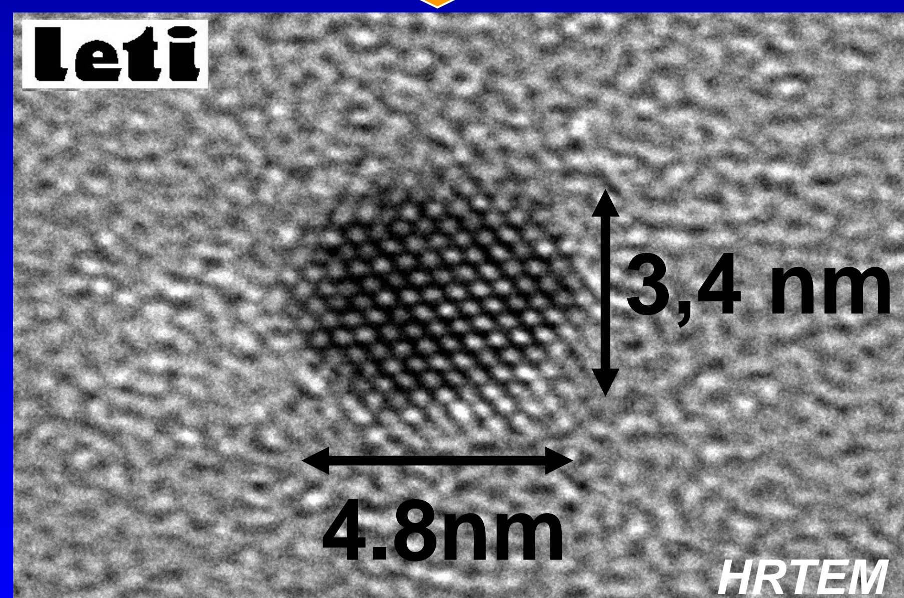
SEM











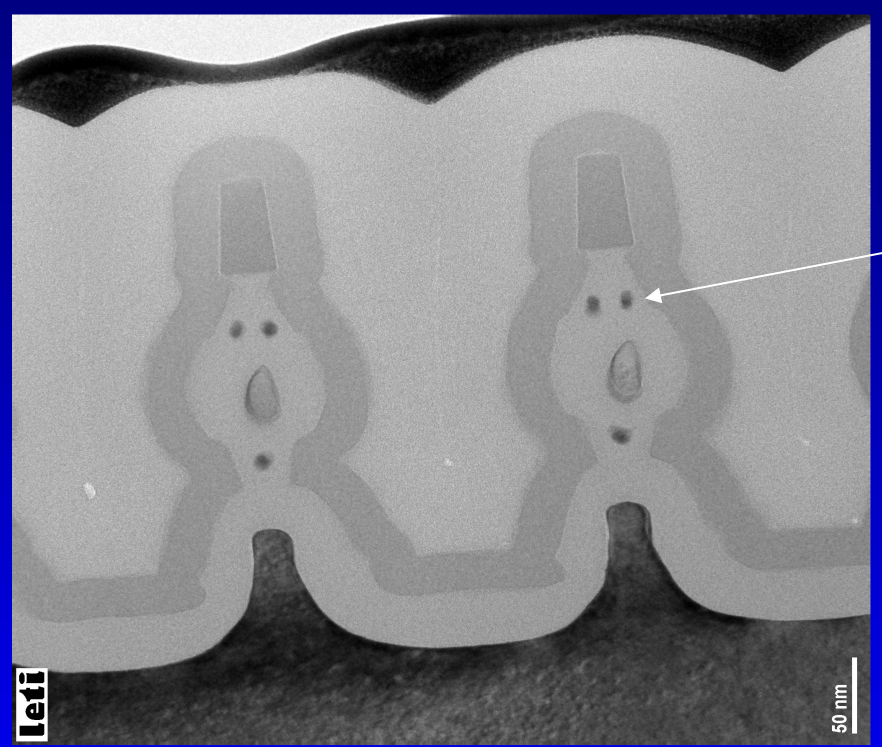
⇒ Self-limited oxidation is used for

small diameter control and variability reduction

A. Hubert et al., ECS Trans. 2008

copyright: CEA- Leti

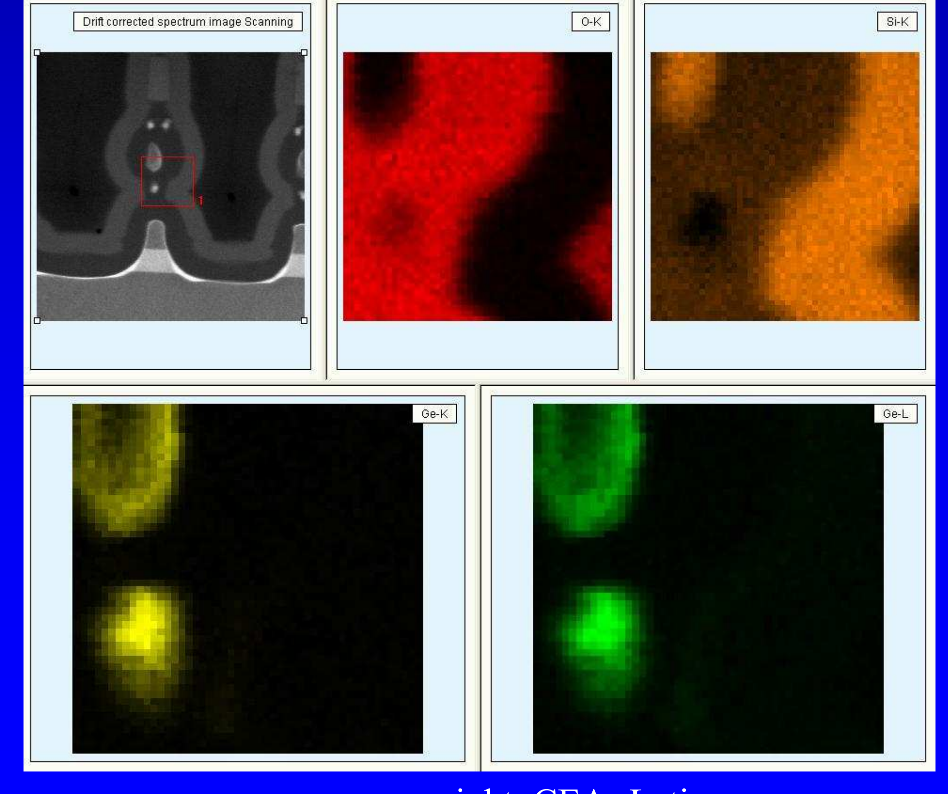
Nanostructuration by oxidation



5nm Ge nanowires

JP Colonna et al. To be published

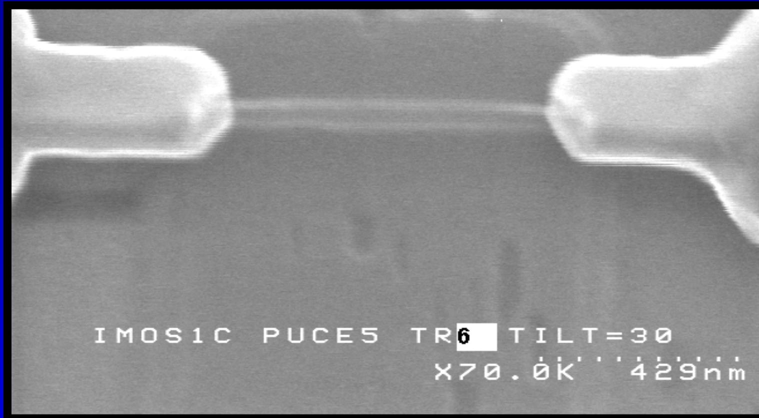
EFTEM (V. Delaye/M. Jublot)

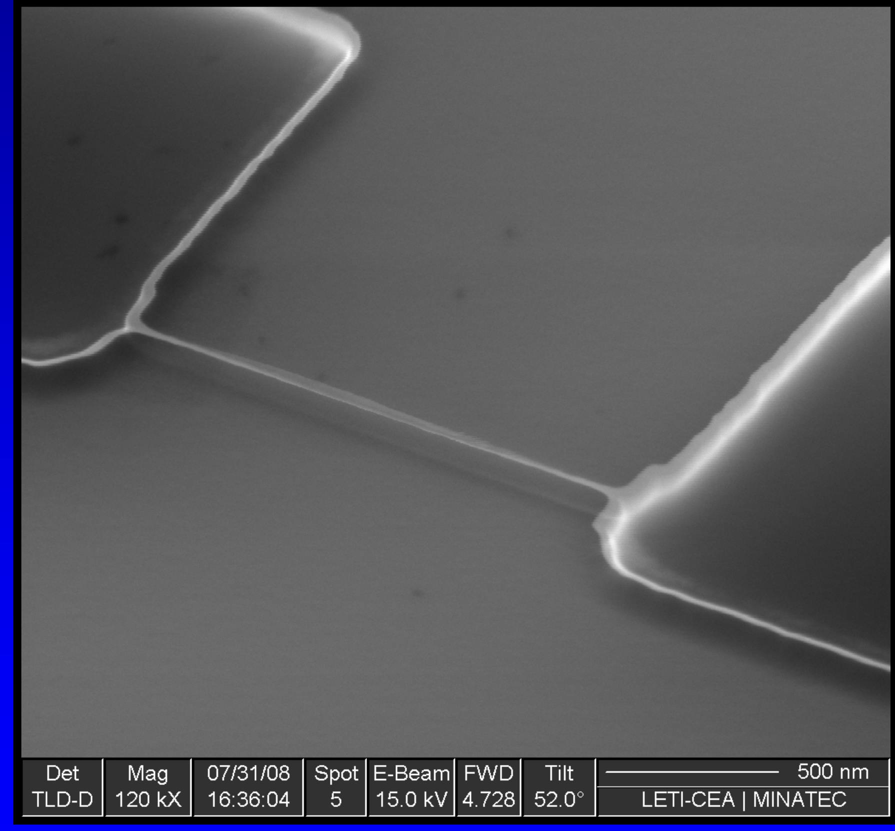


Complex 3D sub-10 nm structures can be designed by $(Si/SiGe)_n$ lateral oxidation

copyright: CEA- Leti

Standard on-line SEM of 10nm suspended nanowire ...





Accurate in-line metrology for sub 10 nm 3D structures is needed

copyright: CEA- Leti

3D Atomic Force Microscopy

[J. Foucher et al. SPIE 08]

Before epitaxy

After epitaxy

Height (nm)

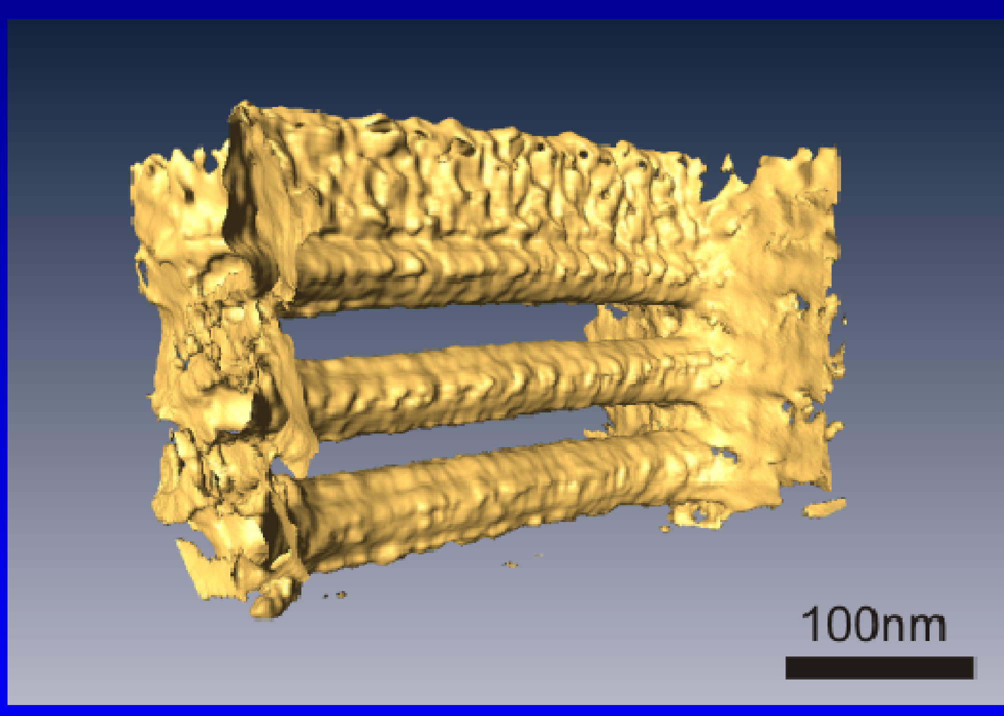
Width (nm)

Systematic and non destructive accurate in line method

copyright: CEA- Leti

3D nanowires TEM tomography

Rough SiGe nanowires



[P. Cherns al. EMC 08]

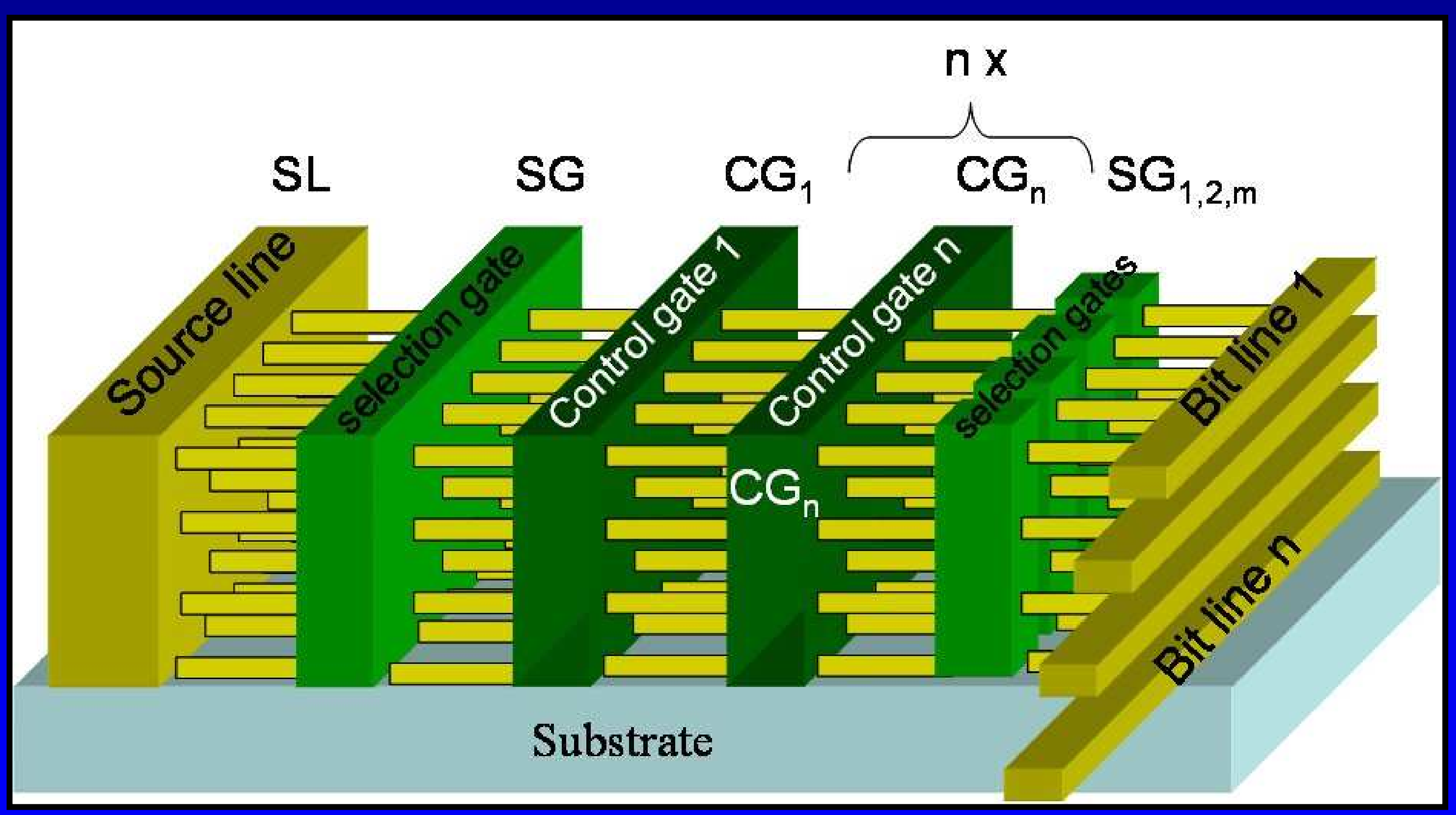
This conference:
P. Cherns al., **POSTER THO21**
A. Chabli et al, **invited**

3D accurate description along the wire, including roughness

copyright: CEA- Leti

3D Flash memories (concept)

TEM



T. Ernst et al. , IEDM'08

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Leti

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- **Sensors and hybrid CMOS**
- Conclusion

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Nanowires are introduced for very sensitive mass measurement

	Sensitivity	Resolution	
	$\Re = -\frac{\delta f}{\delta m} = \frac{f_0}{2M_{eff}} \propto l^{-4}$	$\delta m = \frac{M_{eff}}{Q} 10^{-\frac{DR}{20}} \propto l^3$	
10^{-9}g	Quartz microbalance		M_{eff}~1 mg ω_0~10 MHz
10^{-12}g	Surface Acoustic Waves resonator		M_{eff}~1 mg – 1 µg ω_0~10 MHz – 1 GHz
10^{-15}g	MEMS		M_{eff}~1 µg – 1 ng ω_0~10 kHz
$10^{-18...-21}$g	NEMS	500 nm	M_{eff}~1 ng – 10 fg ω_0~100 MHz
$10^{-18...-21}$ g	Nanowire		M_{eff}~10 fg – 10 ag ω_0~100 MHz – 1GHz

Few molecules sensitivity can be achieved => 1zg

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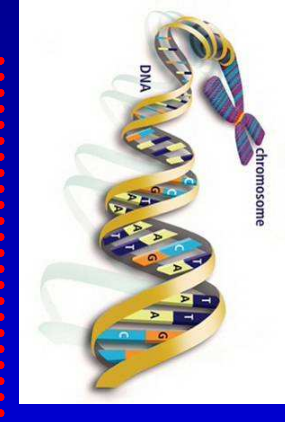
Mass units in biology

Atomic mass unity = 1Da = 1 u ≈ $1.66053886 \times 10^{-27}$kg
1zg = 10^{-21}g = 602 Da ≈ a nucleotides pair (DNA)

Nanowires

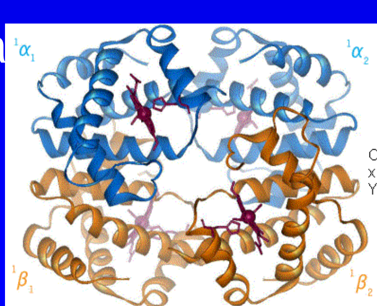
NEMS



A-T — 613.4 Da

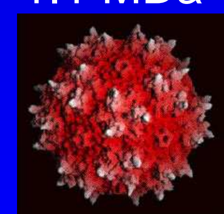
G-C — 616.4 Da

Hemoglobine A molecule — 66.2 kDa



Protein PrP (Prion) — 150 kDa

Parvoviridae viruses: Hepatitis B — 1.1 MDa



E. Coli bacteria — 4.2×10^{11} Da

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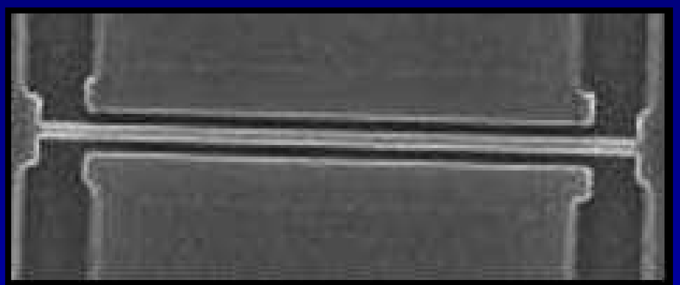
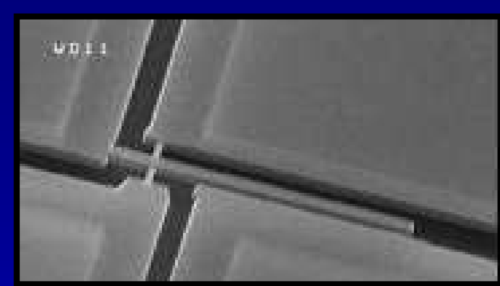
Nanowire used for mass detection

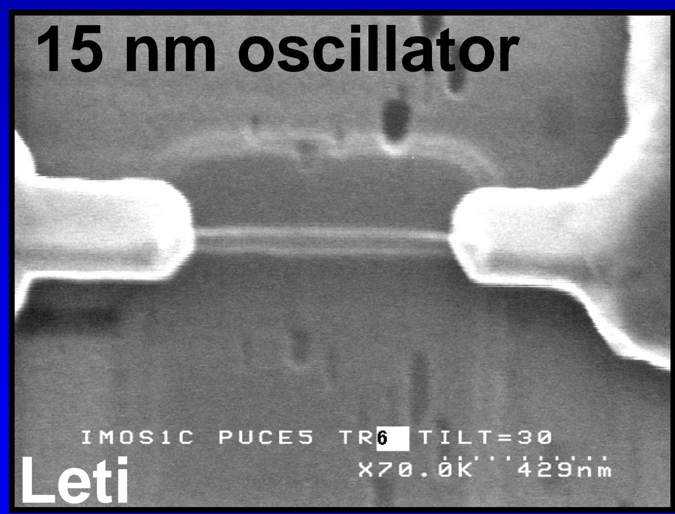


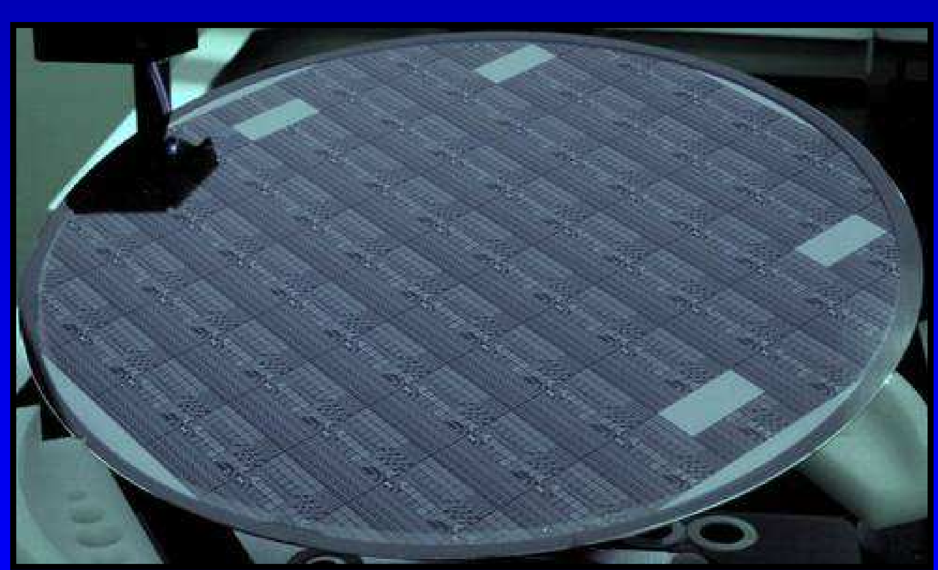
Capacitive actuation & detection



Capacitive actuation & piezo-resistive detection with nanowires

Thermo-elastic actuation & piezo-resistive detection.





First 200 mm wafers with 3.5 millions NEMS

CALTECH & LETI VLSI NEMS Alliance

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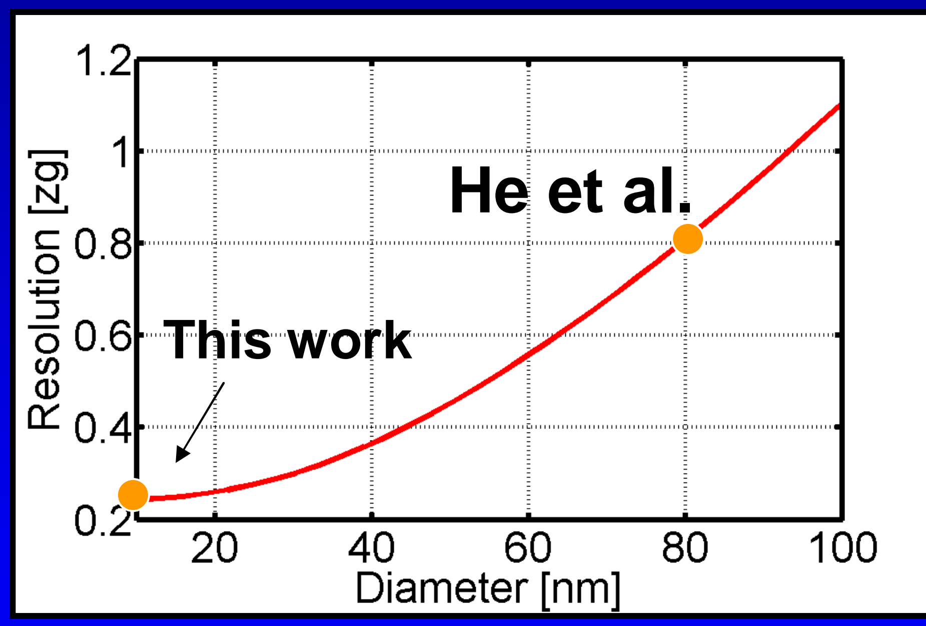
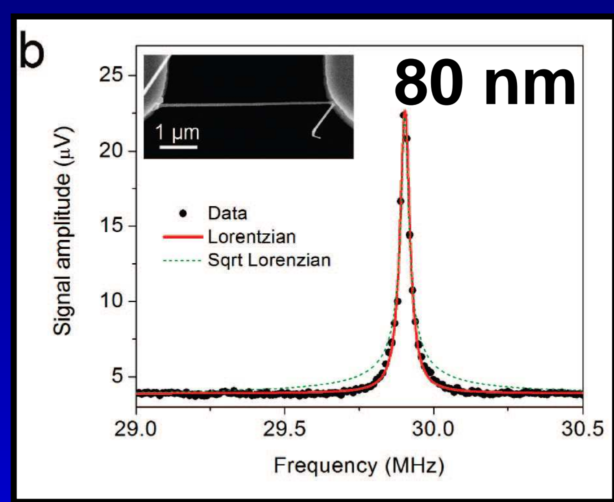
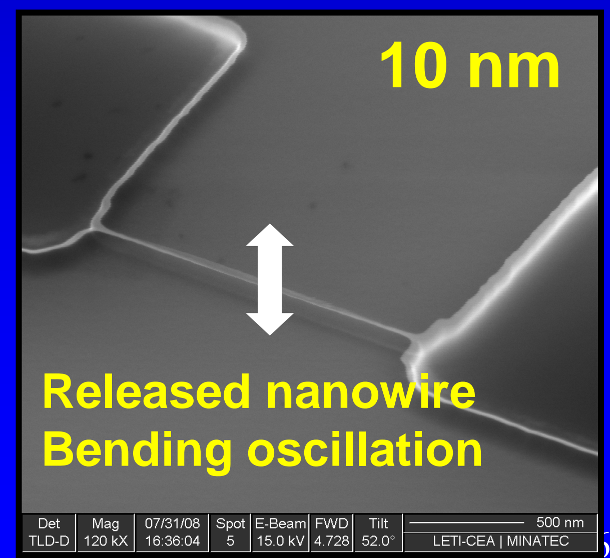
Mass resolution with nanowire





R. He, M. Roukes et al. Nanoletters 12/08



Mass resolution according to the diameter

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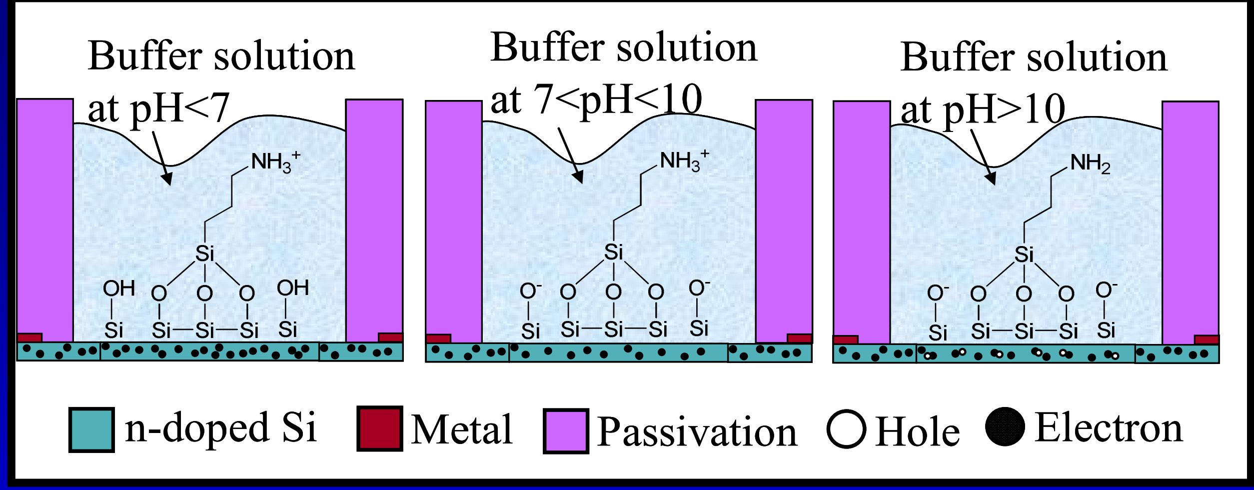
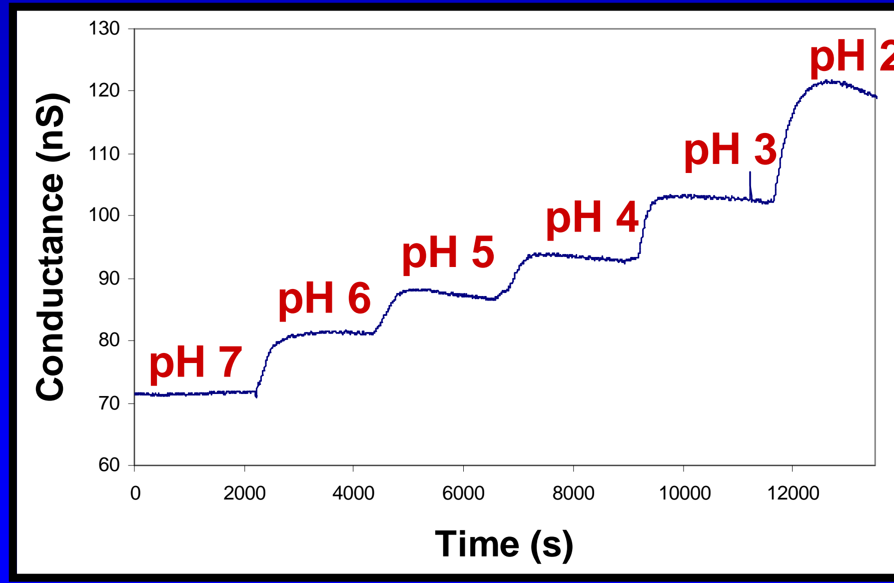
Nanowire for chemical detection





Change of Si nanowire conductance according to pH

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Summary

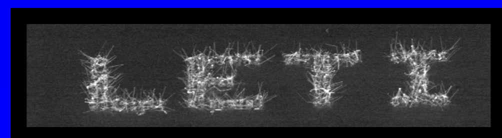
- Several methods were presented to overcome some difficulties linked to 3D structures:

  - self-gate alignment
  - internal spacers
  - diameter control (oxidation …)
  - V_T modulation/power management (by independent gates…)

- Nanowire should be seen as a natural scaling of thin film technologies and not as a one “ever ultimate” node or technology.

- New 3D nanowires matrices offer an original solution for lithography pitch limitation => possible applications to memories and CMOS

- There is a convergence between thin film nanowire CMOS and sensors technologies which open new applications opportunities.



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