International Technology Roadmap for Semiconductors
Metrology Roadmap
2012

Metrology Technical Working Group

Alain Diebold (CNSE)
Christina Hacker (NIST)

College of Nanoscale Science & Engineering
University at Albany State University of New York

NIST
National Institute of Standards and Technology
Technology Administration
U.S. Department of Commerce

Metrology Roadmap 2012
Spring and Summer Attendance

Europe	Carlos Beitia (*CEA LETI MINATEC*) Philippe Maillot (ST)
Japan	Masahiko Ikeno (Hitachi High-Tech) Yuichiro Yamazaki (Toshiba)
Korea Taiwan	
North America	Alain Diebold (CNSE) -Chair Christina Hacker (NIST) – co Chair George Orji (NIST) – 2013 co Chair David Seiler (NIST) Yaw Obeng (NIST) Benjamin Bunday (SEMATECH) Karey Holland (FEI) Scott List (Intel)

ITRS Process
www.itrs.net

Overall Roadmap Characteristics

Gbits, CD, Speed

Focused Roadmaps

Litho, FEP, Interconnect, PIDS, Packaging, Test, Design, Wireless, ERM, ERD

Metrology
ESH
Yield Enhancement
Modeling and Simulation

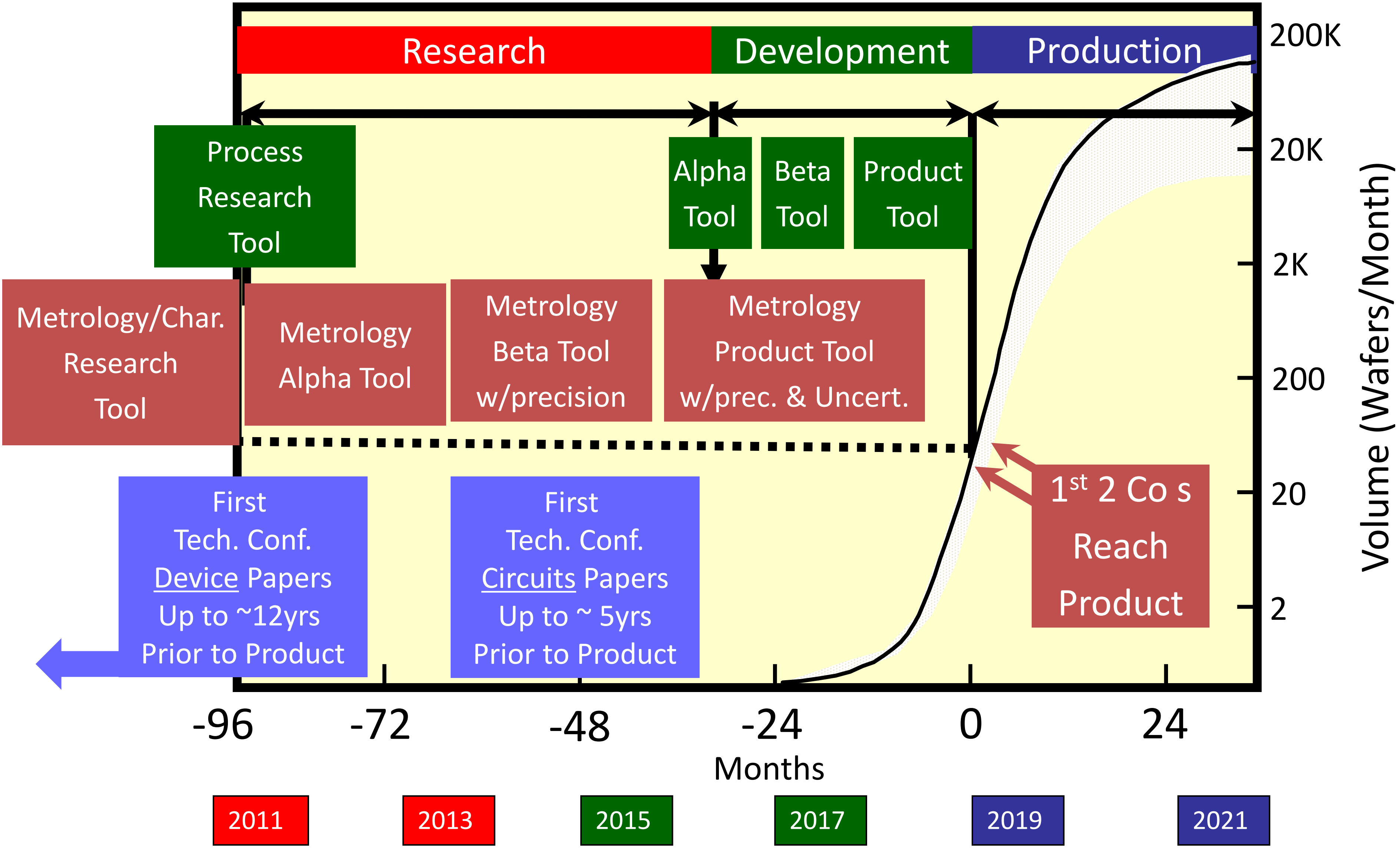
2011 – Text & Requirements Update

2012 – Requirements Update

3 Meetings/year

- Spring Europe
- Summer US – Semicon West
- Winter – Japan/Taiwan/ Korea

Metrology Timing Model w/Technology Cycle Timing



Source: 2009 ITRS - Executive Summary Fig 2b

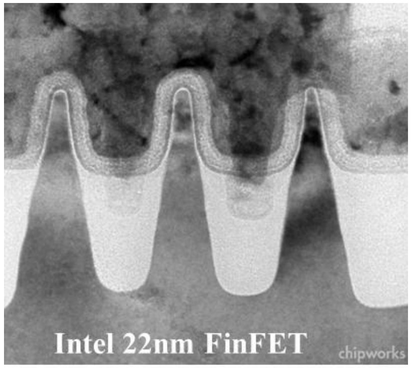
AGENDA

- Metrology for Extreme CMOS – 15 Year Horizon?
  - FEP Metrology
  - Lithography Metrology
  - Interconnect Metrology
- Metrology for Beyond CMOS
  - Graphene Devices
  - Other Devices
- Key Message about the Future

NanoElectronics – NanoTechnology – NanoScale Science

15 year Horizon
Non-classical CMOS ITRS shows
Bulk Si CMOS stopping in 2017 ?
And only Multi Gate (i.e., Fins) after 2020 ?

Fins are the Future



AGENDA

- Metrology for Extreme CMOS – 15 Year Horizon?
  - **FEP Metrology**
  - Lithography Metrology
  - Interconnect Metrology
- Metrology for Beyond CMOS
  - Graphene Devices
  - Other Devices
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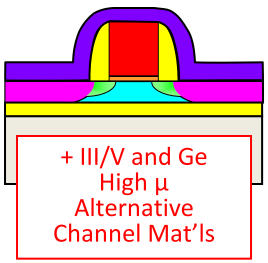
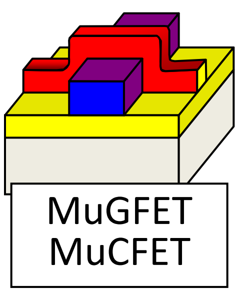
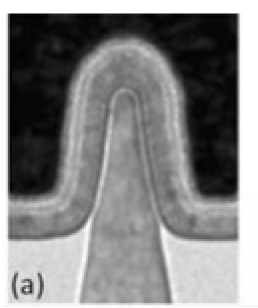
Metrology for 3D Transistors and Memory

EOT & Defects for
New Channel Materials for high μ

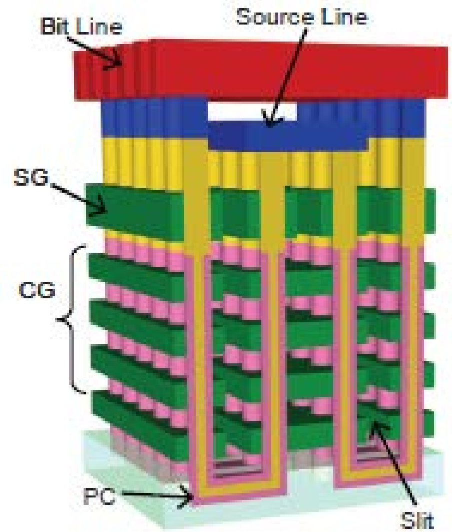


CD/Sidewall/Height/Stress/Dopant Metrology for 3D Devices



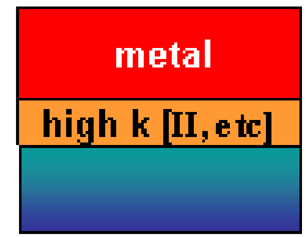


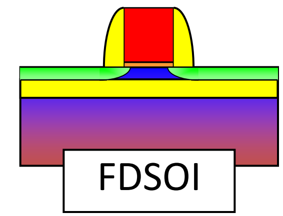
3D Metrology
for Advanced Memory



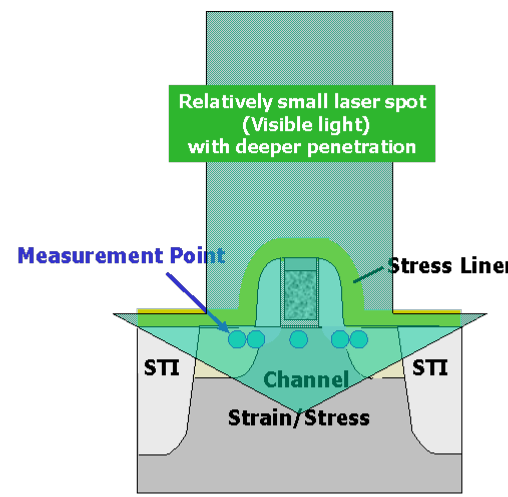
New Memory Materials
Phase Change Memory

Metrology for Next Generation
Metal Gate/High k stacks





Nano-topography &
Local Stress measurements

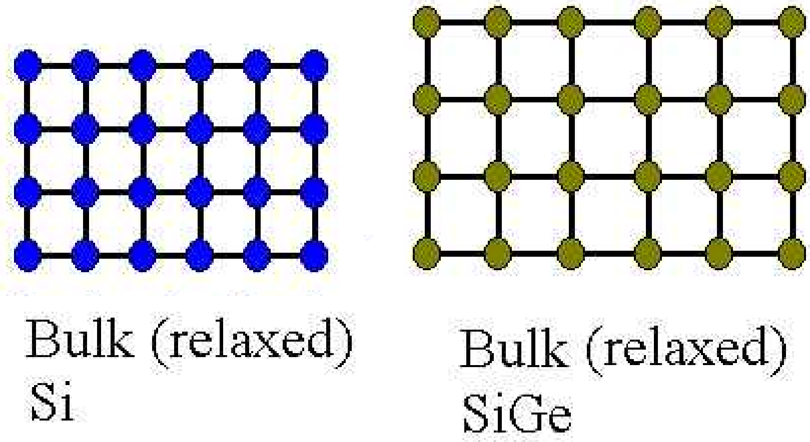


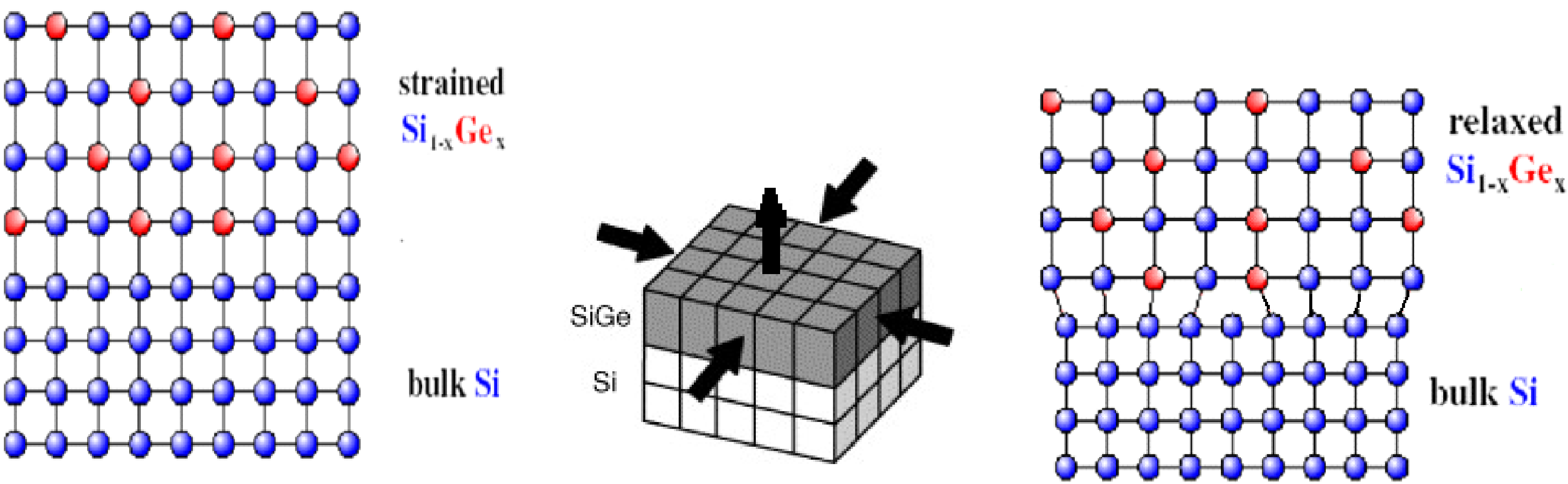
Metrology for New Channel Materials

Silicon and Germanium lattice constants differ by more than 4 %.

$Si_{1-x}Ge_x$ has a larger lattice than that of Silicon

$Si_{1-x}Ge_x$ undergoes bi-axial stress to match Silicon's in-plane lattice.

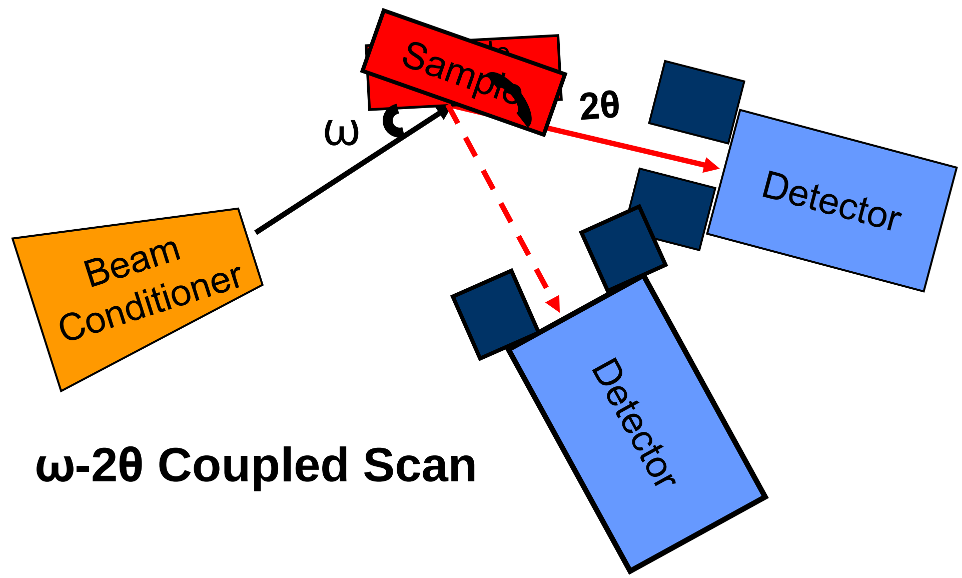




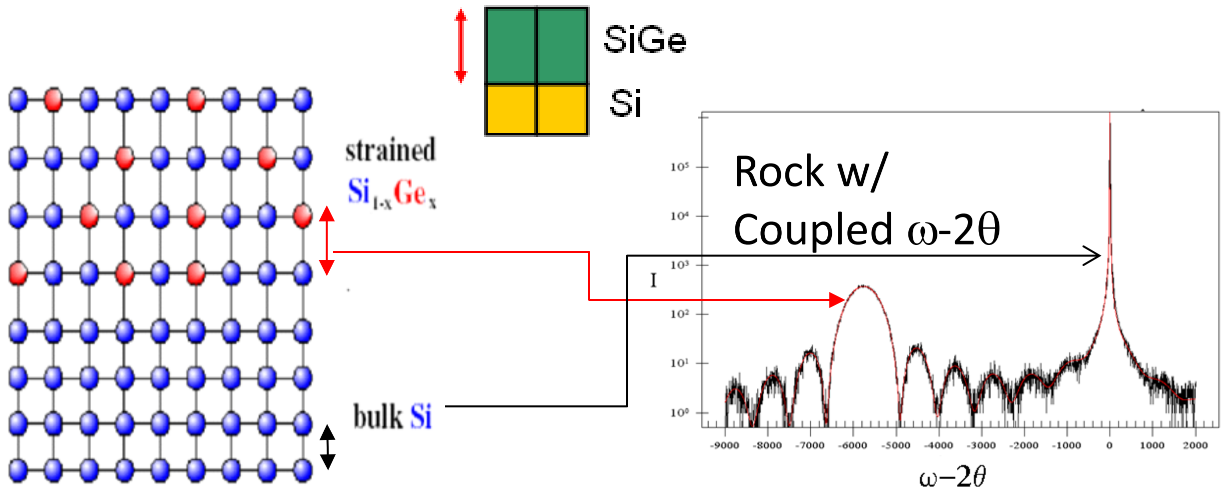
http://www.aip.org/tip/INPHFA/vol-8/iss-3/p22.pdf
http://ars.sciencedirect.com/content/image/1-s2.0-S0167572905000464-gr4.jpg
D.J. Paul, *Physics World* 13, pp27-32 (February 2000)

004 Scan Measures SiGe lattice planes parallel to Si substrate

- Record Si Peak at the respective ω and 2θ combination.
- Vary ω to find the SiGe peak with the detector angle 2θ varying twice as fast as ω.
- Results in having data only for perfectly parallel planes.

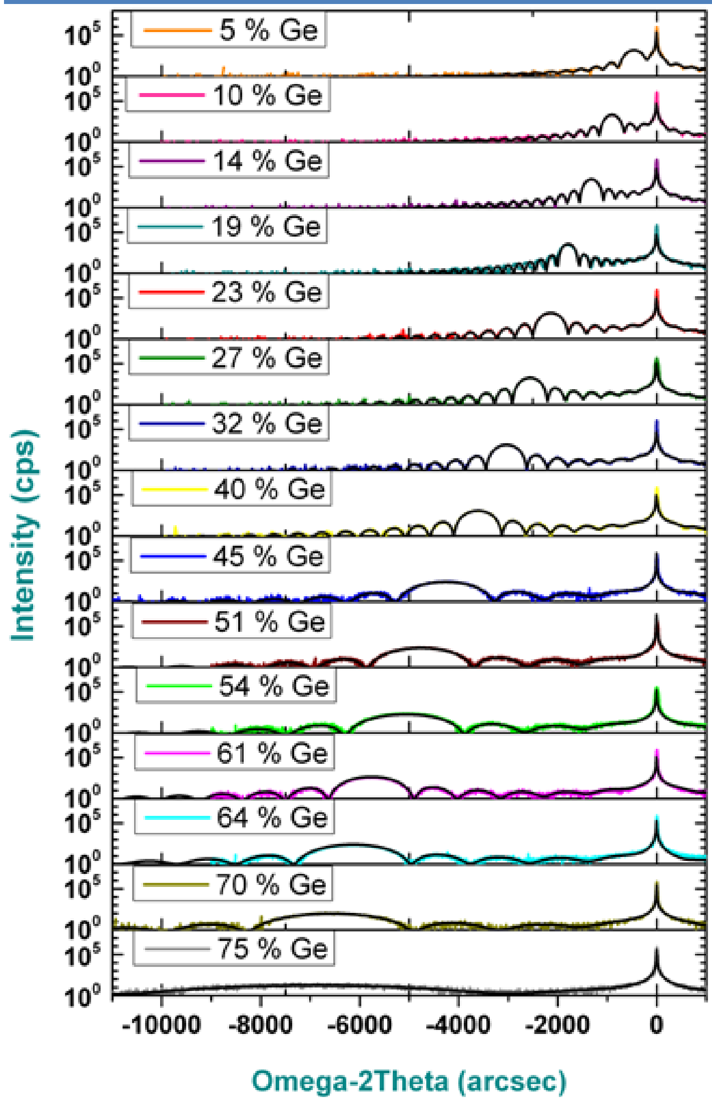


- 004 ω-2θ coupled scans.



Metrology for New Channel Materials

004 HR XRD ω-2θ plots



S.No.	Ge Concentration (x)	$Si_{1-x}Ge_x$ Thickness (Angstroms)
1	0.05	638 A°
2	0.10	752 A°
3	0.14	790 A°
4	0.19	870 A°
5	0.23	529 A°
6	0.27	534 A°
7	0.32	460 A°
8	0.40	374 A°
9	0.45	188 A°
10	0.46	191 A°
11	0.51	175 A°
12	0.54	158 A°
13	0.61	219 A°
14	0.64	145 A°
15	0.70	115 A°
16	0.75	46 A°

$Si_{(1-x)}Ge_x$ from x = 0.05 to x = 0.75

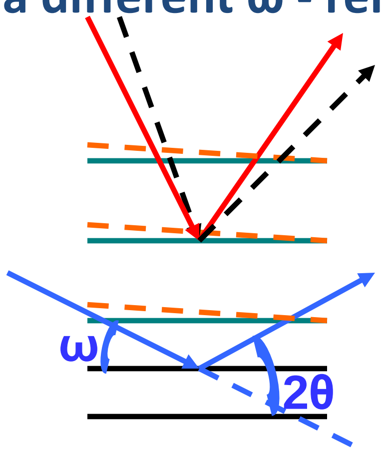
Metrology for New Channel Materials

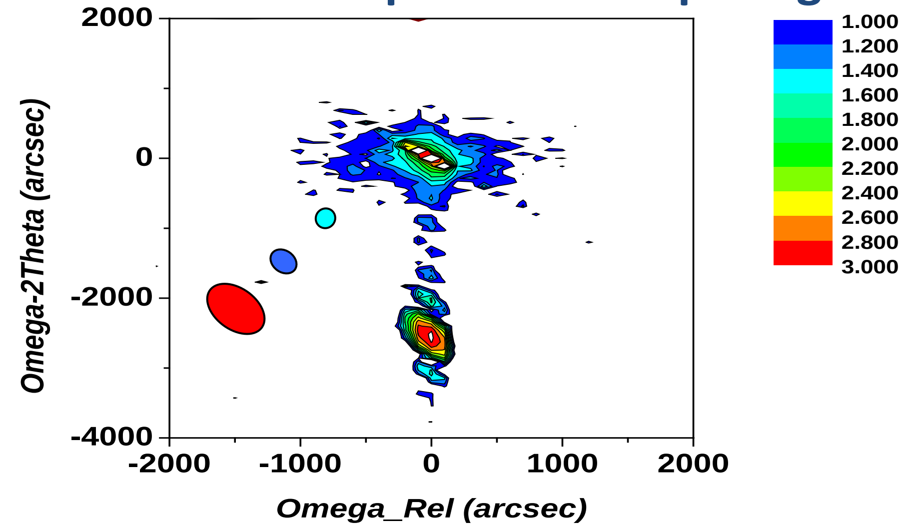
We record ω - 2θ coupled scan intensities for varying ω angles.

- **Start with ω - 2θ coupled scans.**
- **Fixing 2θ, slightly vary ω → ω-rel.**
- **We get a Si Peak at a Particular ω - 2θ ➔ $[\omega\text{-rel}]_a$ and a SiGe peak at another ω - 2θ ➔ $[\omega\text{-rel}]_b$.**

If there is no tilt -- SiGe peak at the same ω-rel angle as Silicon's.

A tilted layer gives the SiGe peak at a different ω - 2θ for that particular d-spacing and at a different ω - rel angle.

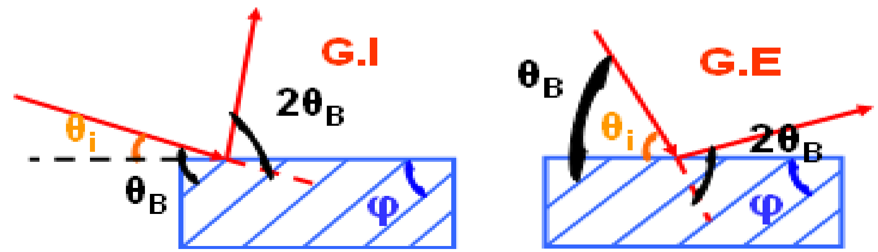


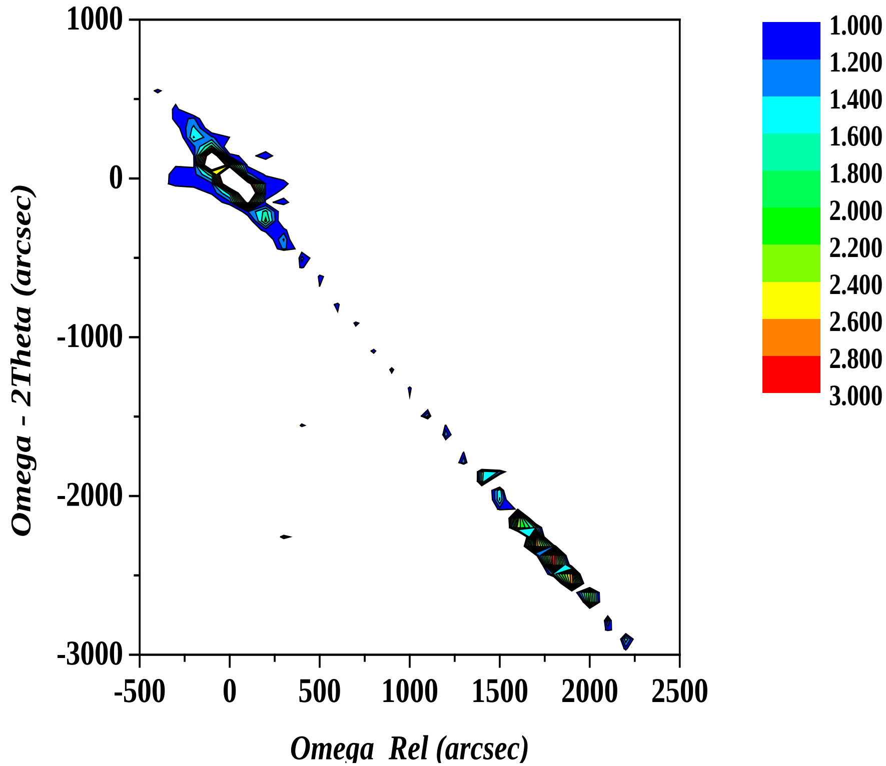


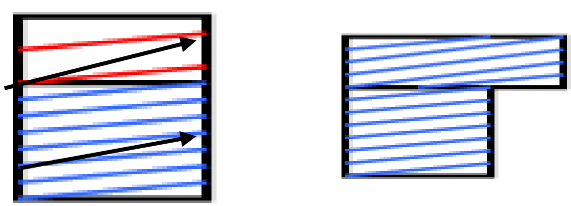
004 Reciprocal Space Maps

Metrology for New Channel Materials

- An asymmetric scan – Grazing incidence or Grazing exit.
- Grazing Incidence $\theta_i = \theta_B - \phi$
- Grazing Exit $\theta_i = \theta_B + \phi$
- We record ω - 2θ coupled scan intensities for varying ω angles.
  - Start with ω - 2θ coupled scans.
  - Fixing 2θ, slightly vary ω → ω-rel.
  - We get a Si Peak at a Particular ω - 2θ - ω-rel and a SiGe peak at another ω - 2θ - ω-rel .
- A relaxed layer gives the SiGe peak at a different ω - 2θ but at the same ω - rel angle.

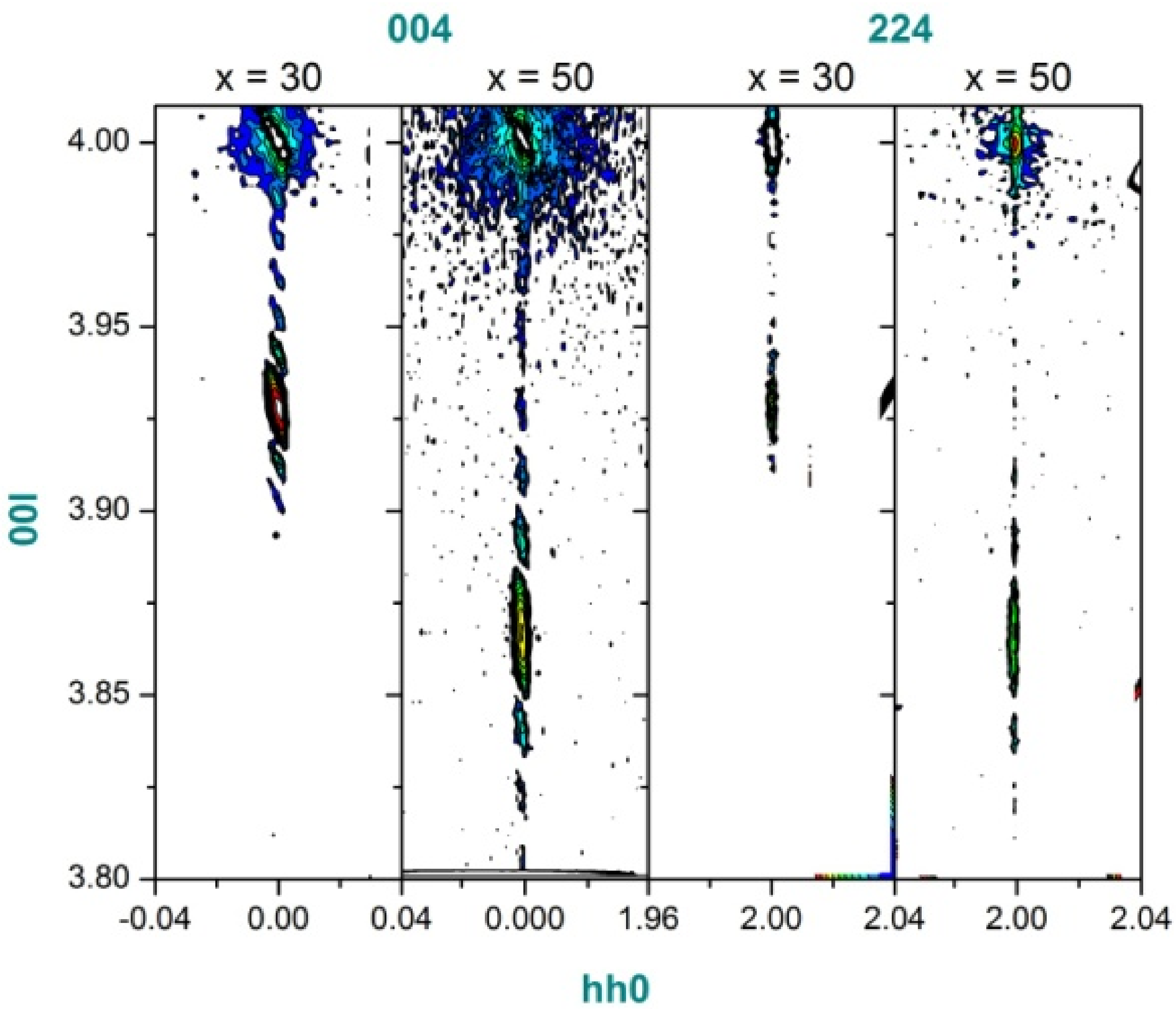






224 Reciprocal Space Maps

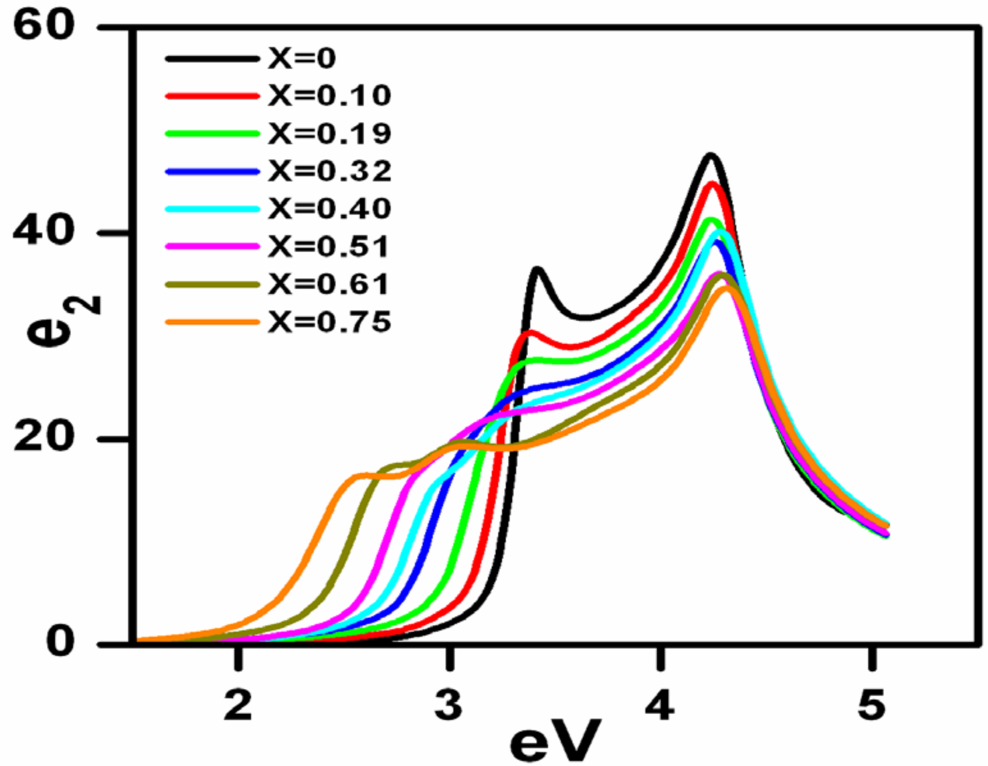
Metrology for New Channel Materials



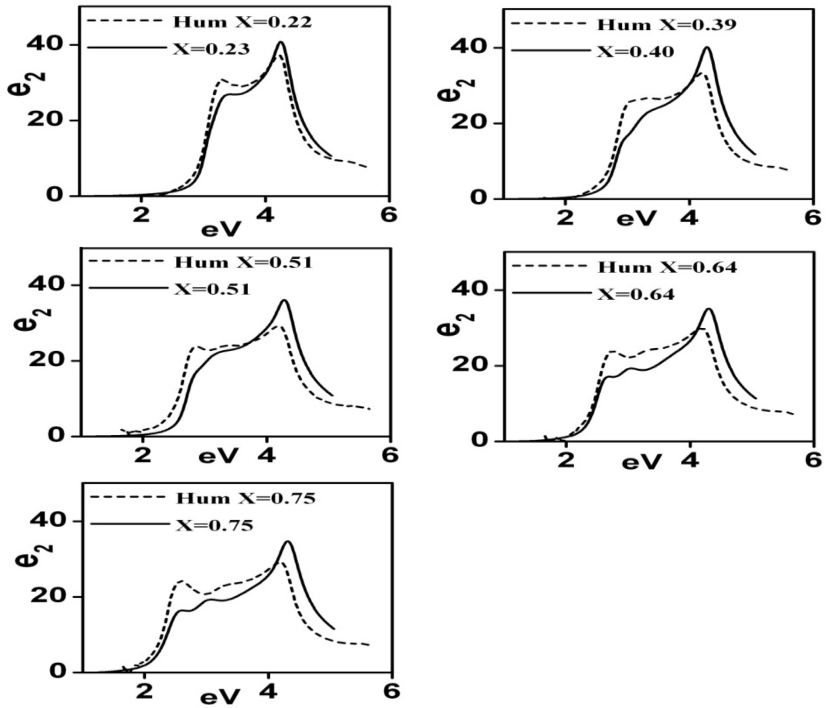
RSM's of Si(1-x)Gex, x = 0.30, x = 0.50

Metrology for New Channel Materials

Fully Stressed



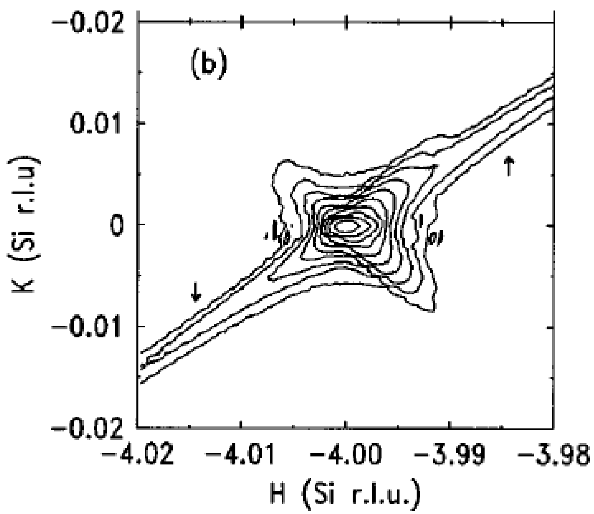
Fully Stressed vs Relaxed



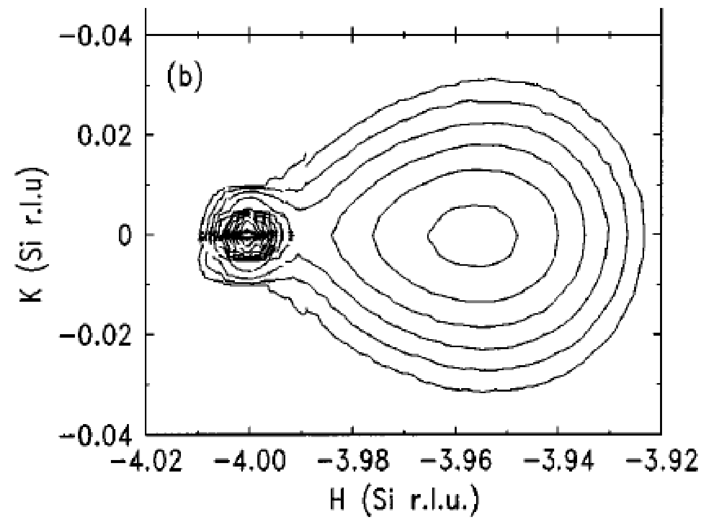
e_2 of Si(1-x)Gex

Defect Metrology – in line method needed?

GI-I-XRD H-K Reciprocal Space Maps



X-Pattern observed for films that relax with the Modified Frank-Reed Mechanism



Pattern for relaxation via "roughening mechanism"

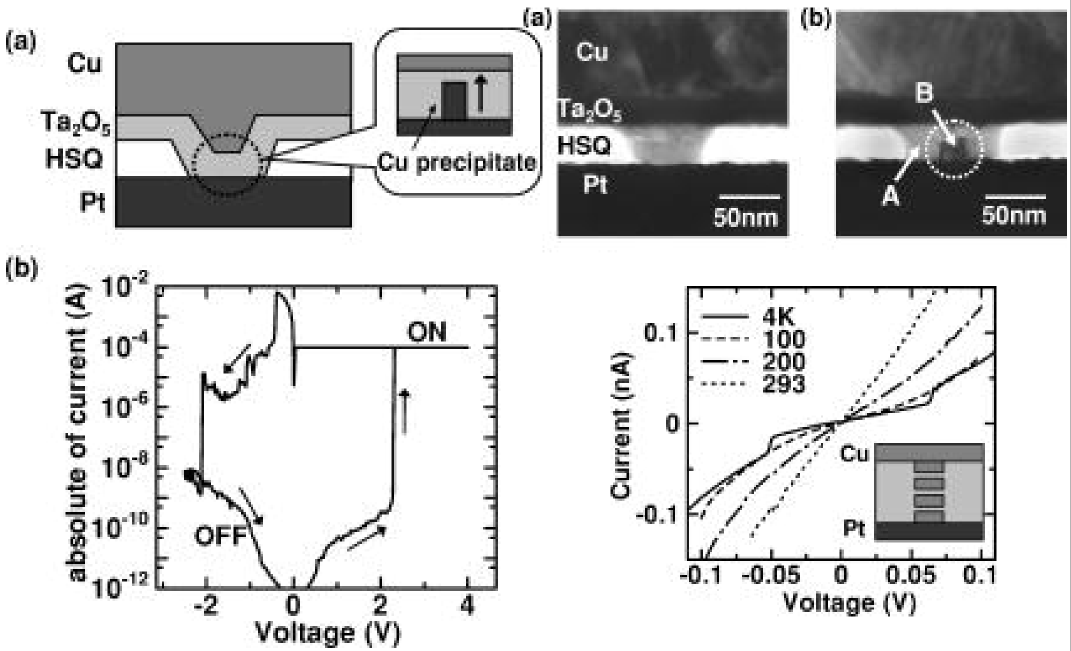
J-L Jordan-Sweet, et al, J. Appl. Phys. 80, (1996), p89.

Metrology for New FEP Memory

Resolving Redox Memory

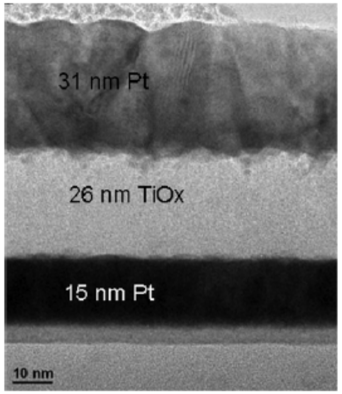
- What is the switching mechanism(s)?
- How does it form? Can we see filaments?
- Is it reversible?

Proposed mechanism: Reversible Metal Filament



Sakamoto et al., APL **91** 092110 (2007)

Proposed mechanism: Mobile Oxygen Vacancies



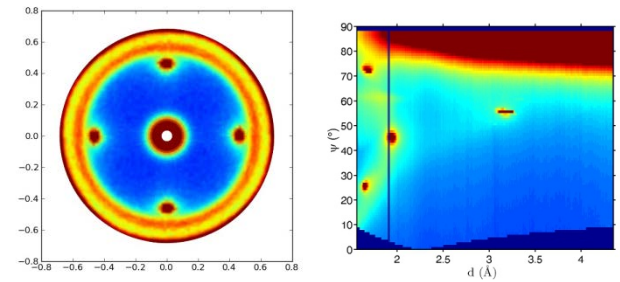
Tong, et al, IEEE Transactions on Nuclear Science, 57,(2010), p 1640

Properties of next Gen High k stacks

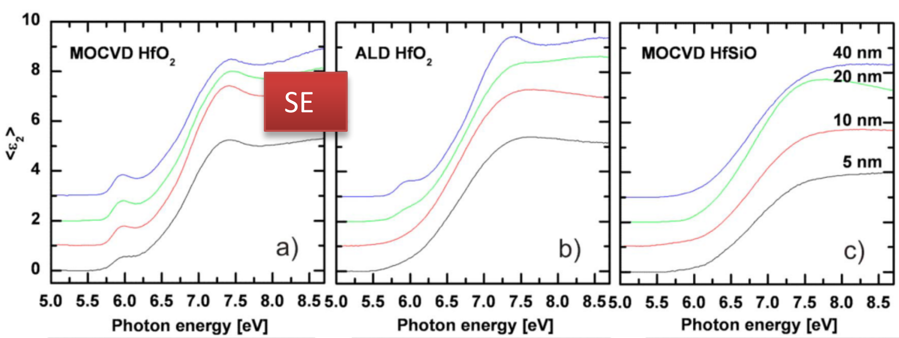
Resolving New Materials and Processes

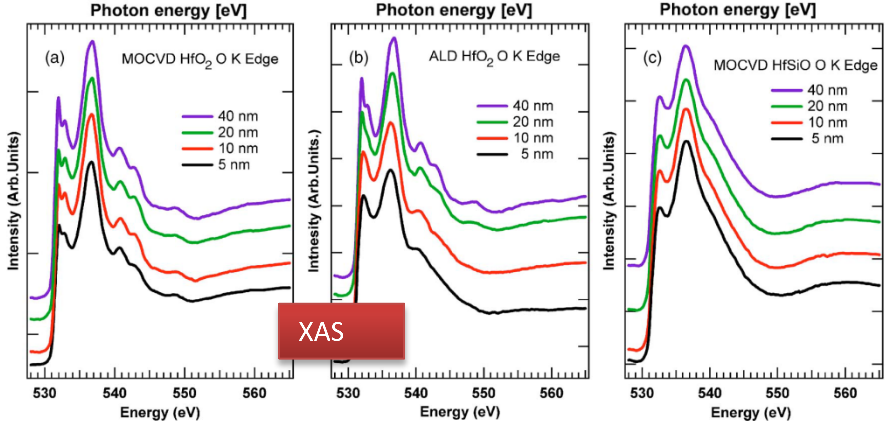
- What is the crystal structure?
- What is the correlation between electrical properties & materials structure?
- How can interfaces be engineered?

XRD



GI-I- XRD & Texture



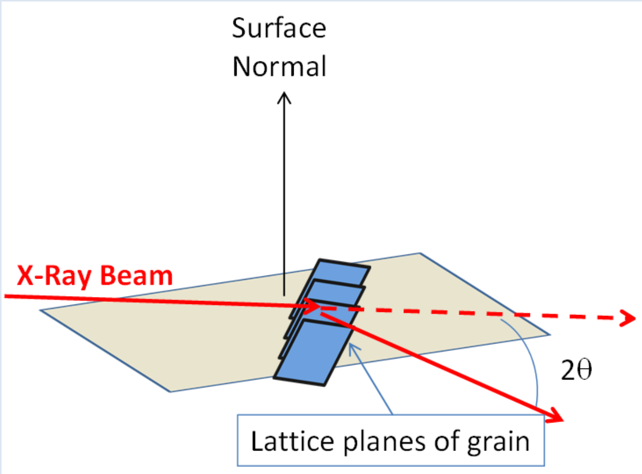


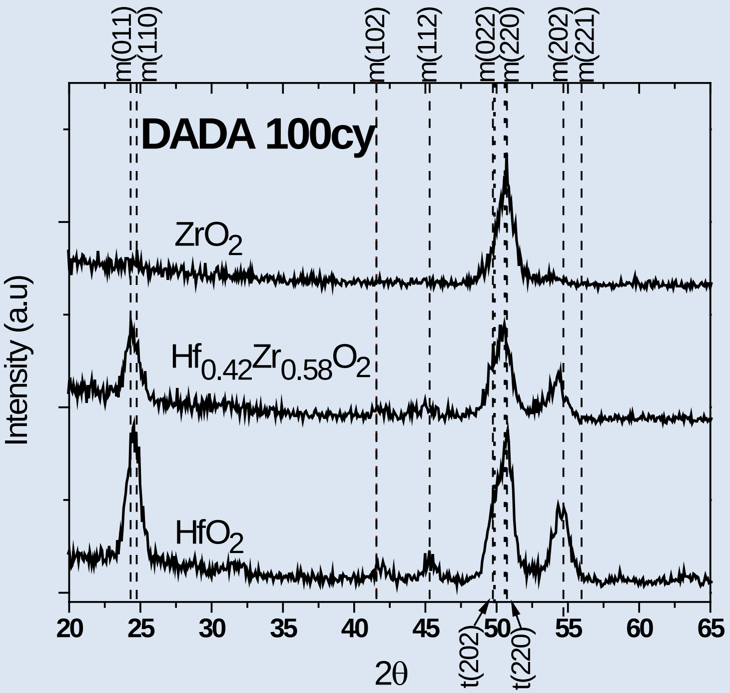
Theoretically determined k values

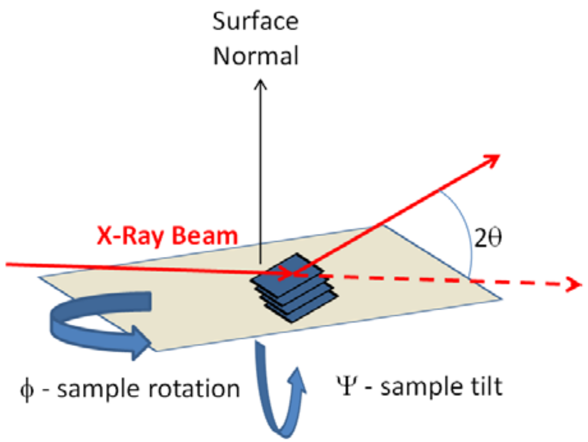
X. Zhao and D. Vanderbilt, *Phys. Rev. B.*, 233106 (2002)

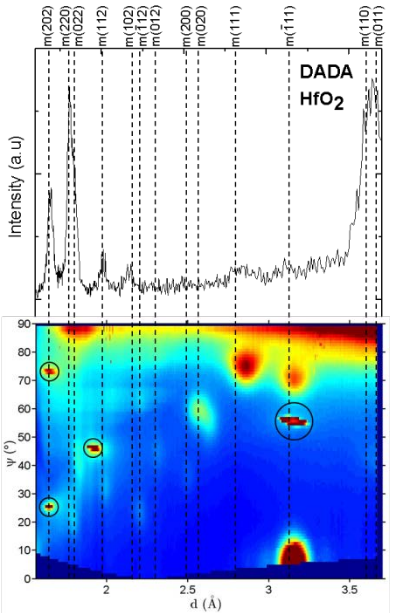
	monoclinic high-k	cubic	tetragonal
		higher-k	
k (HfO_2)*	16	29	70
k (ZrO_2)†	20	37	47

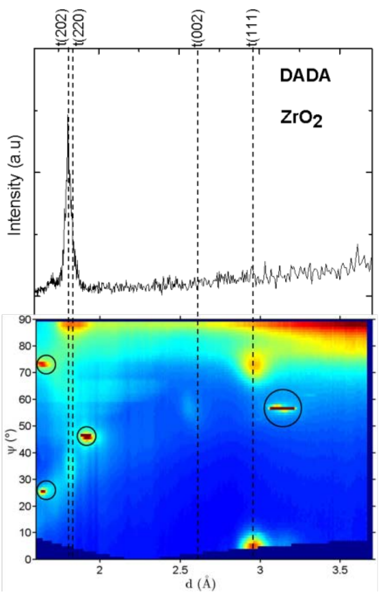
Metrology for New High K











High K texture – tetragonal phase via ZrO_2

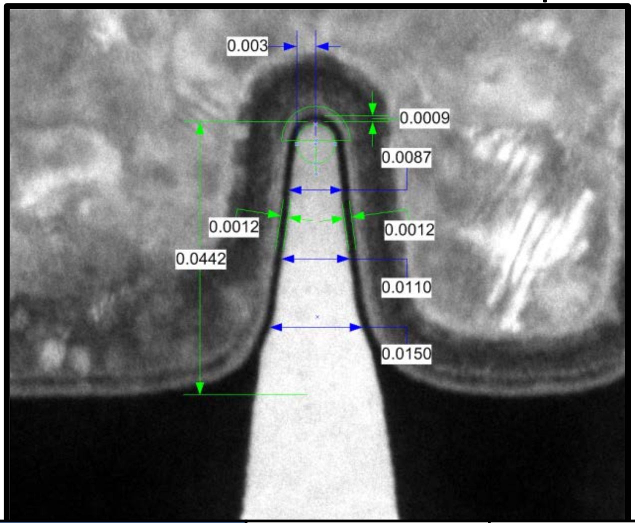
STEM/TEM High Volume Process Monitoring

Future S/TEM High Sample → Data Rates

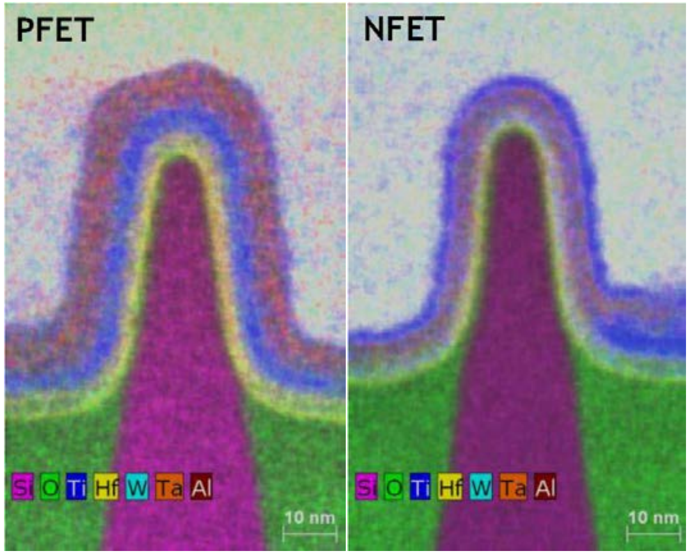
High throughput sample prep/measure 15,000 images/month/tool

Data Acquisition & Analysis

Automated: 30% Better Repeatability



Fast Elemental Analysis
5 min EDS Mapping



Feature	(Automated) Average CD (nm)	(Automated) Dynamic Precision (nm 3-σ)	(Manual) Dynamic Precision (nm 3-σ)
Fin width at 75%	8.48	0.16	0.19
Fin width at 25%	15.23	0.14	0.24
Fin Height	45.10	0.16	0.46
Tip Radius	2.50	0.17	0.31

Image thanks to Karey Holland

Low Voltage Imaging to avoid Damage

30kV STEM Imaging

BF+DF1+DF3

Simultaneous acquisition of 3-channels (pseudo-colored for segmentation)

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  - FEP Metrology
  - **Lithography Metrology**
  - Interconnect Metrology
- Metrology for Beyond CMOS
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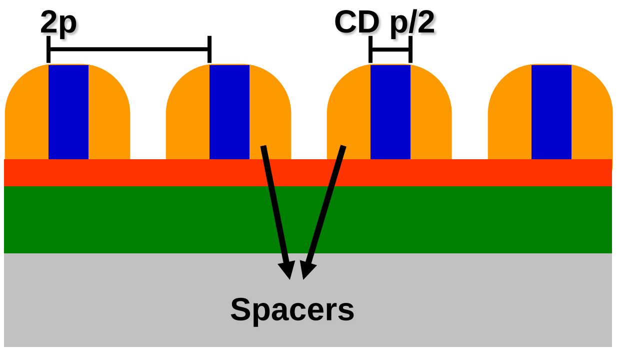
- Key Message about the Future

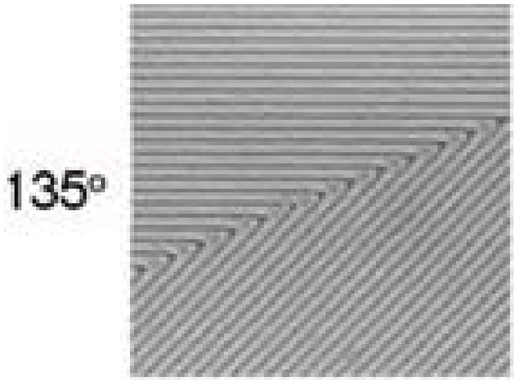
Metrology for Lithography

Challenges for Critical Dimensional Metrology

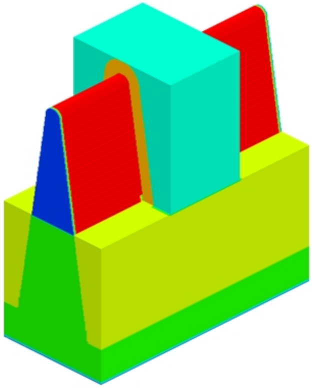
Multiple Patterning Issues:
Two sets of CD's
Pitch Walking



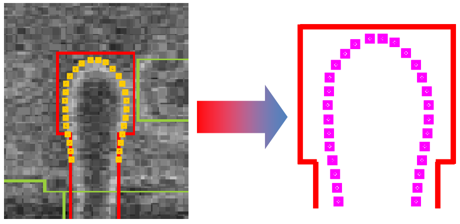
Directed Self Assembly with Block co-polymers



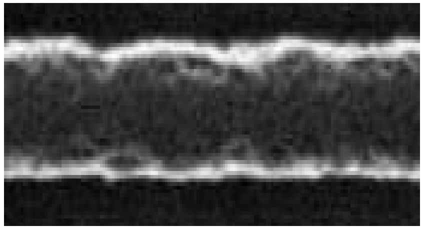
CD Metrology for 3D Transistors and Interconnect



CD Metrology for Optical and EUV Masks



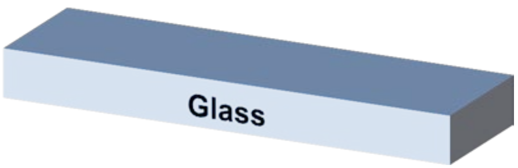
Line Edge Roughness



Peter Clark ee Times 5-17-12

Area of Great Industry Interest

Mask Substrate Defect Inspection

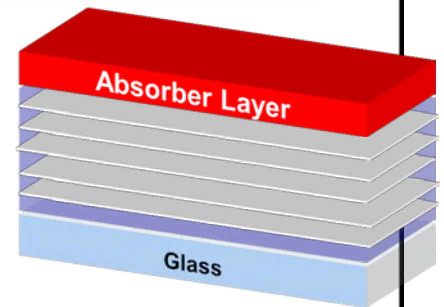


Mask Blank Inspection

Absorber Layer

Mo-Si Multi Layer

Glass

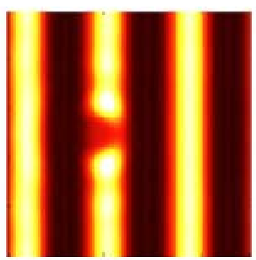


2 defect types: phase and amplitude defects

Actinic AIMS

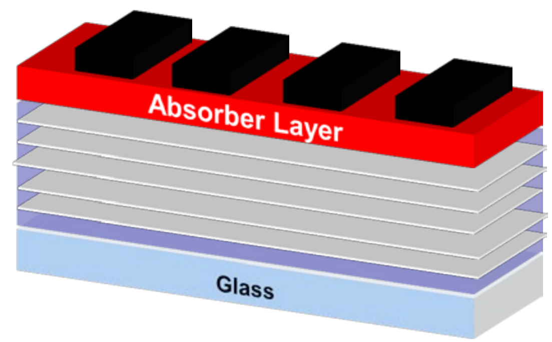
Aerial imaging measurement system

Project what mask will print onto a CCD detector

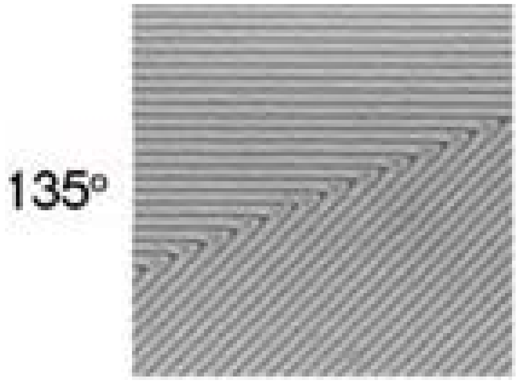


Aerial Image

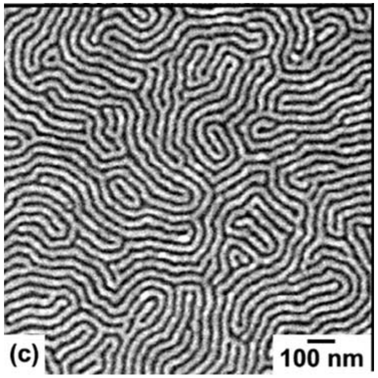
Patterned Mask Inspection

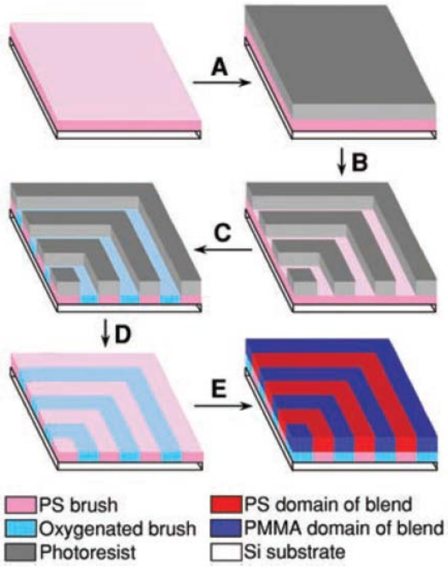


Metrology for DSA Lithography



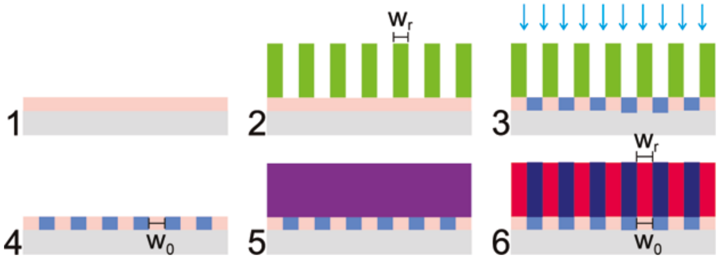
Directed Self Assembly with Block co-polymers
ERM survey indicated "in-production" with
2018 insertion dates for Flash and Logic
(one unofficial claim of 2015)



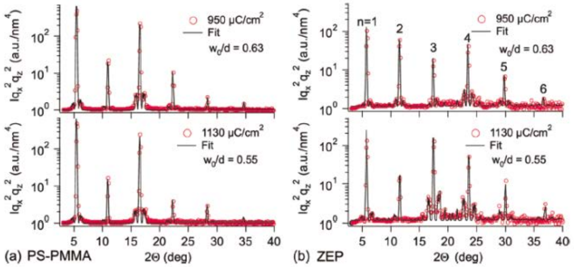


CD Metrology before and after removal of co-polymer

Need Method to Detect Defects below Surface



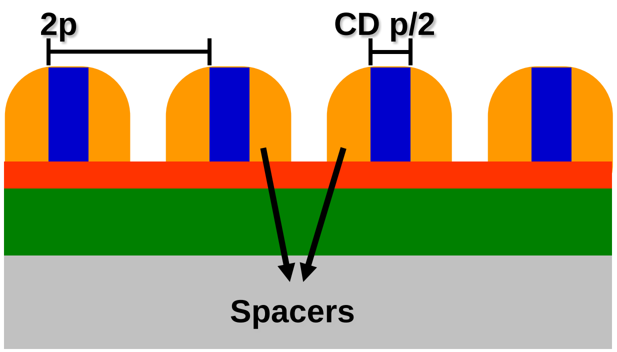
Transmission soft X-Ray Diffraction CD-SAXS



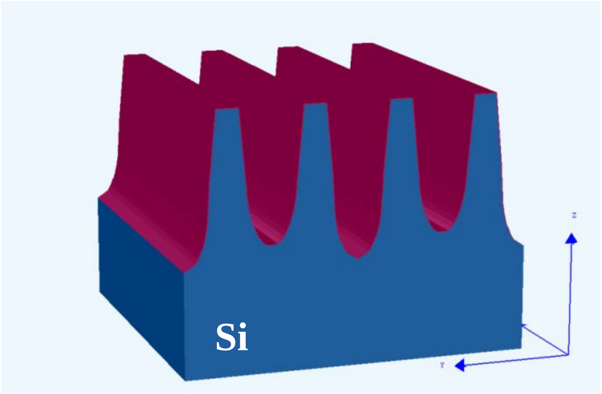
Stein, Liddle, Aquila, Gullikson, (NIST, Berkeley, U. Houston) Macromolecules 2010, 43, 433–441

Metrology for Double Patterning Lithography

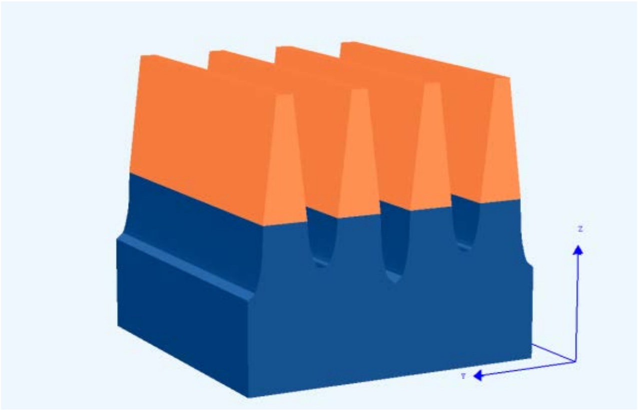
Multiple Patterning Issues:
Two sets of CD's
Three sets of CD's
Four sets of CD's



Pitch Walking



Stress Induced Anisotropic Optical Properties



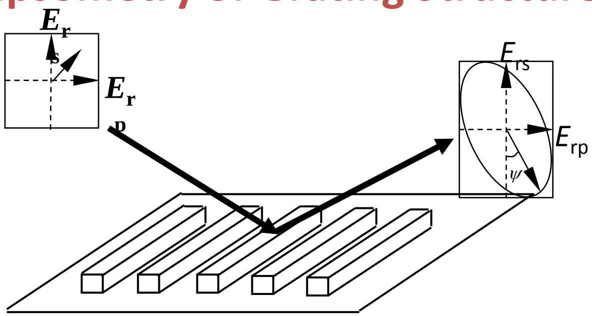
ITRS Litho - Triple Patterning by 2013 and Quad by 2017

CD Metrology for Lithography

Critical Dimensional Metrology Methods

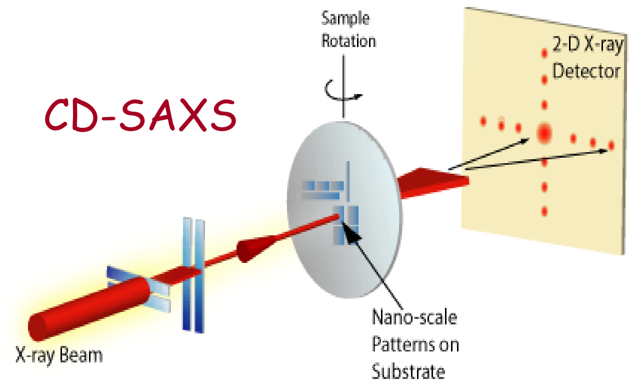
Scatterometry – AKA OCD

Ellipsometry of Grating Structures



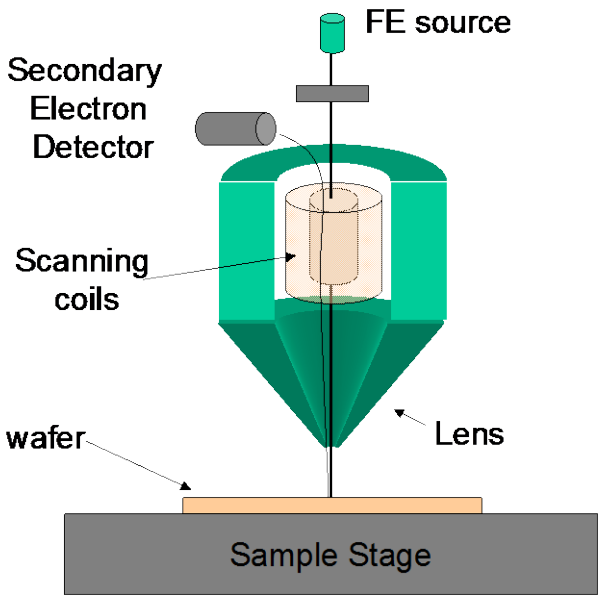
CD Metrology Extendibility Potential Solutions

CD-SAXS

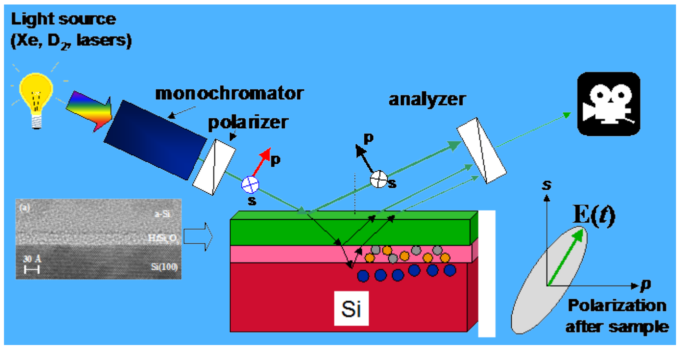


Joe Kline + Wen li Wu (NIST)

CD SEM – State of the art uses energy filtered imaging



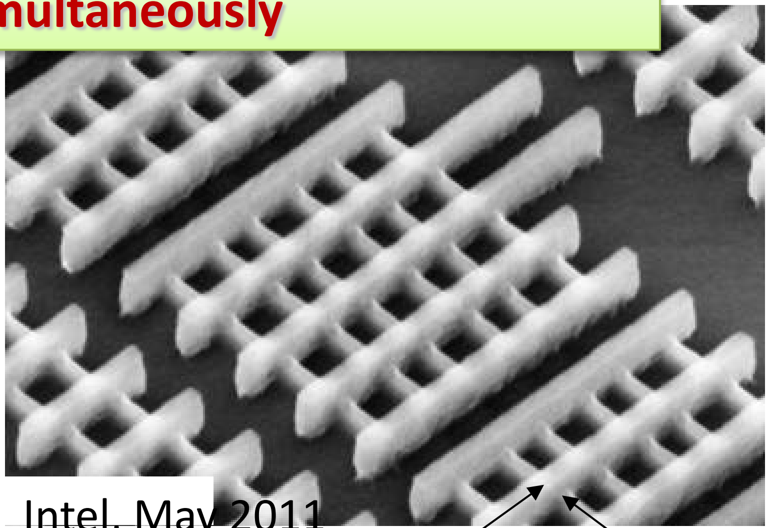
Scatterometry - Mueller Matrix Ellipsometry



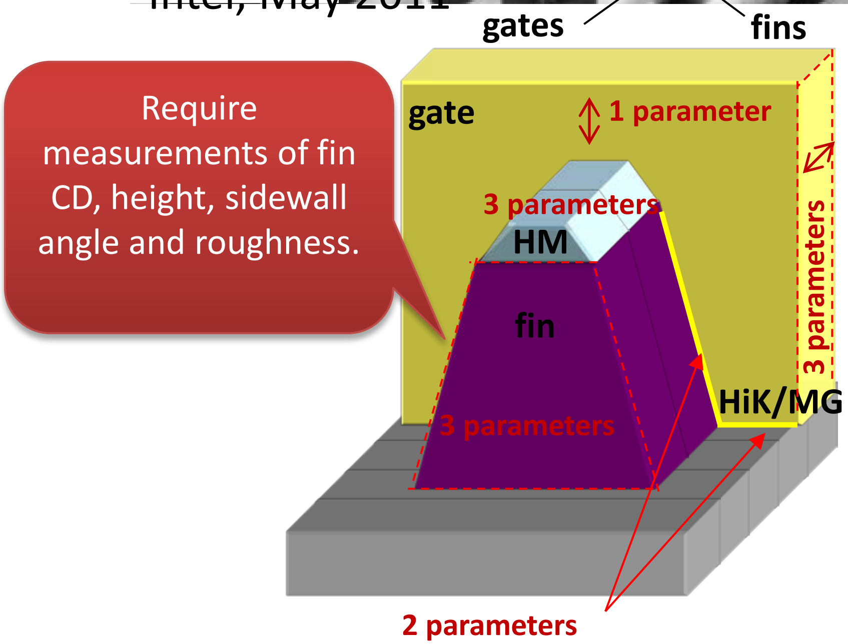
3D Transistor Dimensional Metrology

Challenge: Dimensional metrology on complex 3D structures requires many parameters to be measured simultaneously

- Complex structures such as FinFETs require 3D metrology
  - Many parameter (see diagram), not counting top corner rounding, footing, or etch recess under fin.
  - Gate spacer would increase number of parameters.
- One example from 2011 SPIE: Fin is measured by CD-SEM or AFM and results fed forward
  - OCD (scatterometry) then simultaneously measures fewer parameters with improved measurement uncertainty and higher speed.
- All methods are advancing :
  →Complementary metrology delivers better solution



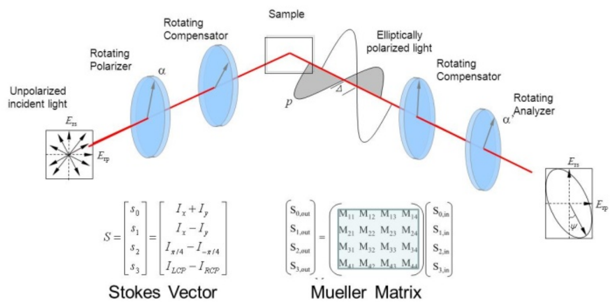
Intel, May 2011



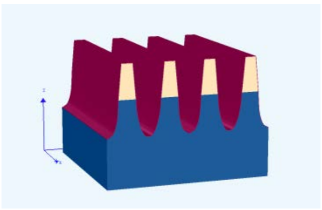
3D Transistor Dimensional Metrology
Mueller Matrix Ellipsometry

COLLEGE OF NANOSCALE SCIENCE & ENGINEERING
UNIVERSITY AT ALBANY State University of New York

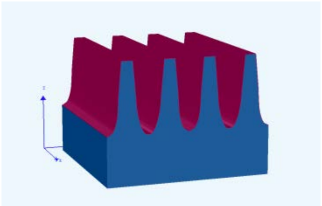
Laboratory Ellipsometer
Great for All Types of Samples

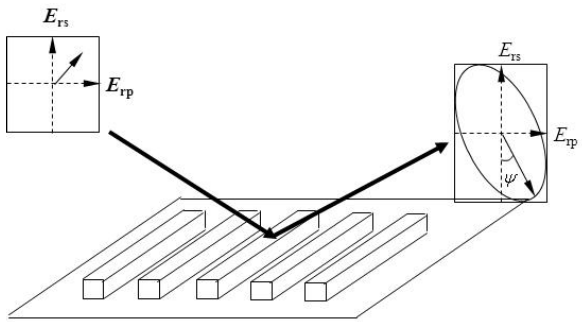


SiGe Grating

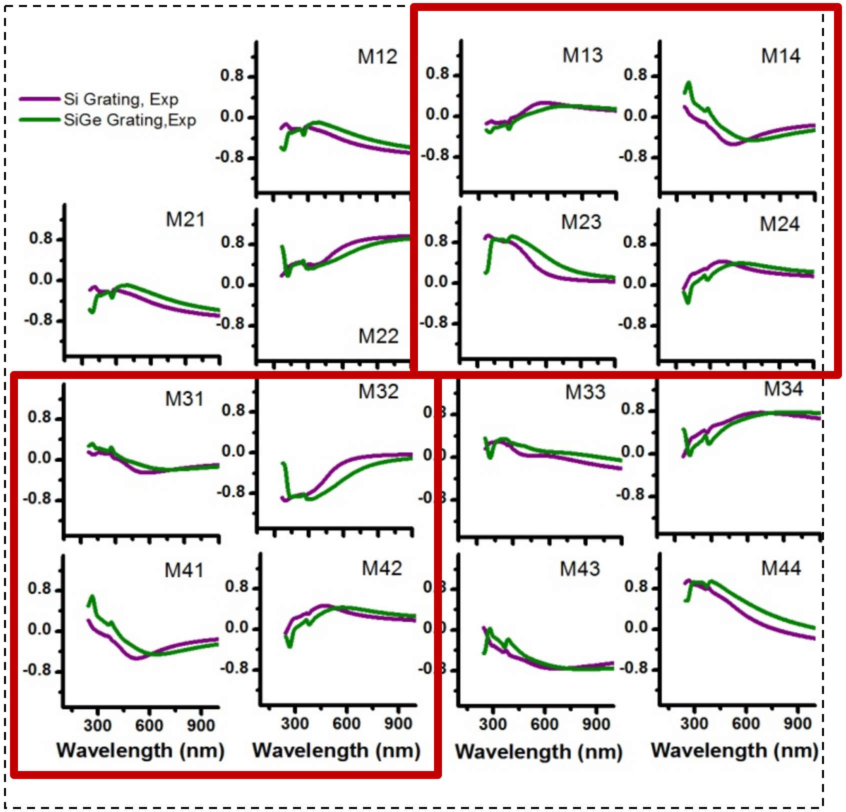


Si Grating



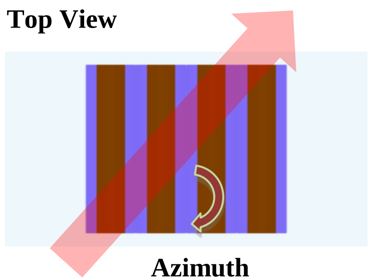


Ellipsometry of Grating Structures



Azimuth = 45^0

Top View

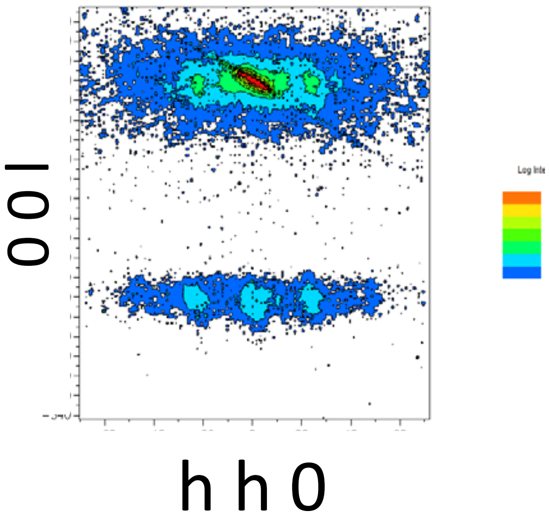


$$S = \begin{bmatrix} I_x + I_y \\ I_x - I_y \\ I_{45} - I_{-45} \\ I_L - I_R \end{bmatrix} \qquad \begin{pmatrix} S_{0,out} \\ S_{1,out} \\ S_{2,out} \\ S_{3,out} \end{pmatrix} = \begin{pmatrix} M_{11} & M_{12} & M_{13} & M_{14} \\ M_{21} & M_{22} & M_{23} & M_{24} \\ M_{31} & M_{32} & M_{33} & M_{34} \\ M_{41} & M_{42} & M_{43} & M_{44} \end{pmatrix} \begin{pmatrix} S_{0,in} \\ S_{1,in} \\ S_{2,in} \\ S_{3,in} \end{pmatrix}$$

Non-zero off-diagonal Mueller response

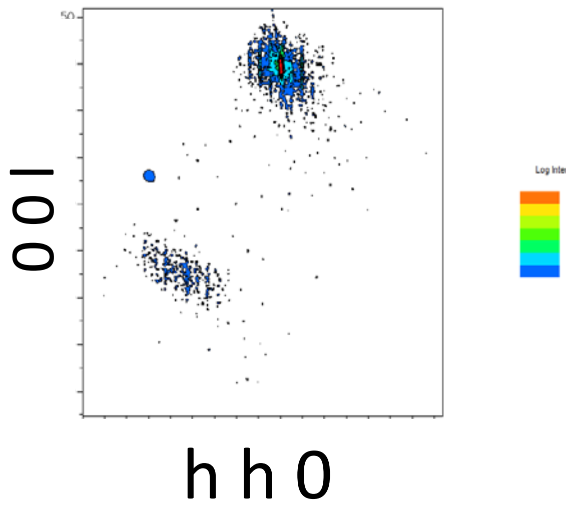
3D Transistor Dimensional Metrology

(004) RSM



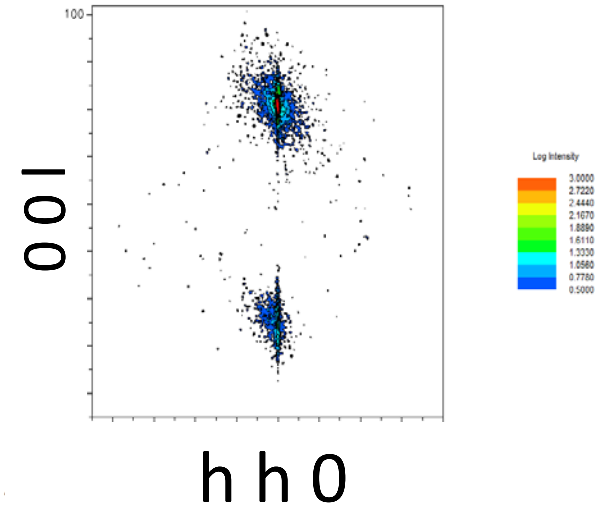
Phi Perpendicular to Fins

(224) RSM



Phi Perpendicular to Fins

(224) RSM

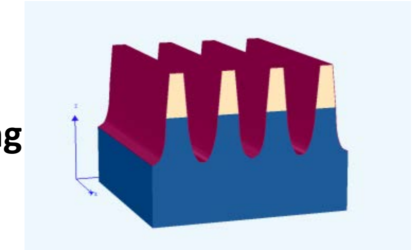


Phi Parallel to Fins

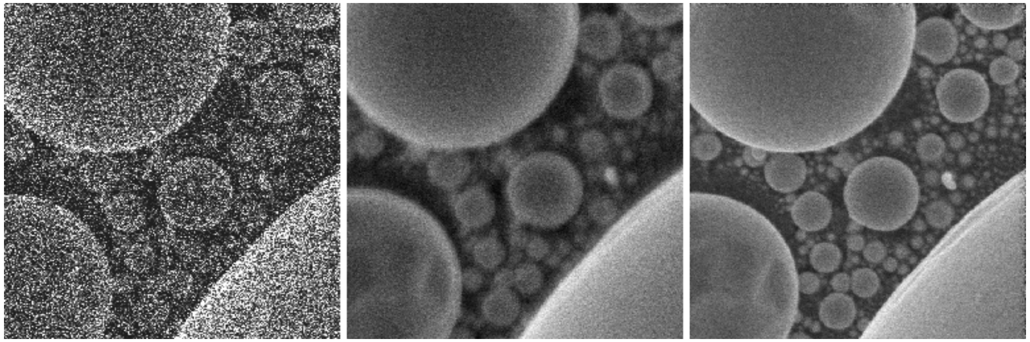
SiGe layer strained along the length of the fin and partially relaxed perpendicular to it.

$$\boldsymbol{\varepsilon} = \mathbf{A}\begin{bmatrix} \varepsilon_{x'} & 0 & 0 \\ 0 & \varepsilon_{y'} & 0 \\ 0 & 0 & \varepsilon_{z'} \end{bmatrix}\mathbf{A}^{-1}$$

SiGe Grating



CD-SEM Extendability



Fast single frame

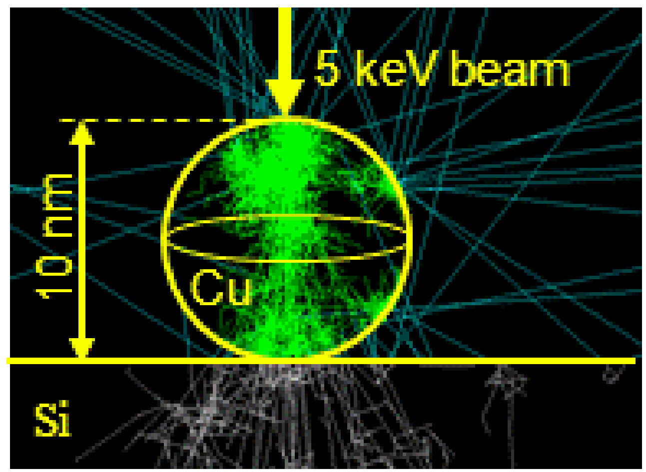
Traditional frame averaging

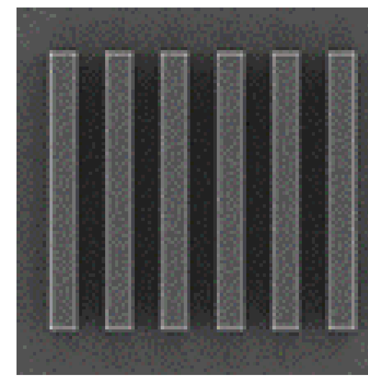
Drift-corrected frame averaging

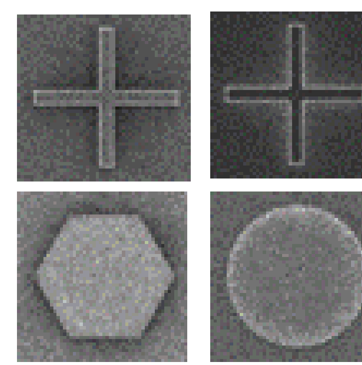
Aberration Corrected CD-SEM

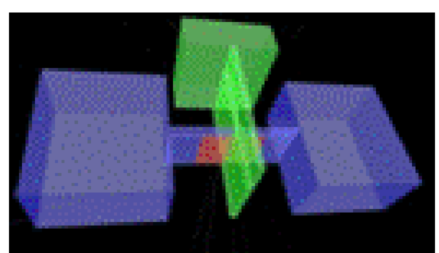
Better CD SEM Via better image acquisition

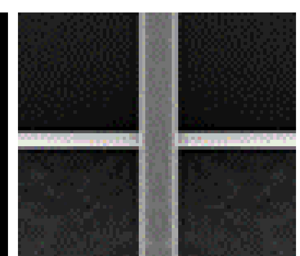
3D model determines all structure dimensions











Andras Vladar, NIST

2012 Metrology Roadmap

		2013	2016	2019	2024
	Flash 1/2 pitch (nm)	*18*	*14*	*11*	*8.0*
	DRAM ½ Pitch (nm)	28	20	14	8.0
	MPU Printed Gate Length (nm)	28	20	14.0	6.0
	MPU Physical Gate Length (nm)	20	15.0	12.0	7
	Wafer Overlay Control (nm) - 20% DRAM	6.0	4.0	2.8	1.3
	Wafer Overlay Control Double Patterning (nm)	4	2	1	?
	Lithography Metrology				
Gate	Physical CD Control (nm) Allowed Litho Variance = 3/4 Total Variance	2.1	1.6	1.2	0.7
Gate	Wafer CD metrology tool **uncertainty** (3σ, nm) at P/T = 0.2	0.42	0.31	0.25	0.15
Gate	Etched Gate Line Width Roughness (nm) <8% of CD	1.6	1.2	1.0	0.6
Dense Lines	Printed CD Control (nm) Allowed Litho Variance = 3/4 Total Variance	1.9	1.5	1.1	0.8
Dense Lines	Wafer CD metrology tool **uncertainty** (3s, nm) at P/T = 0.2	0.4	0.3	0.3	0.2
DP	***Double Patterning Metrology Requirements, Generic Spacer Patterning - Driven By Flash***				
DP	Metr0logy Uncertainty for Core Gap (Carrier line)	0.4	0.3	0.2	0.1
Fin	***Fin Metrology***				
Fin	Metrology Uncertainty for fin top corner rounding radius (nm)	1.5	1.1	0.9	0.64

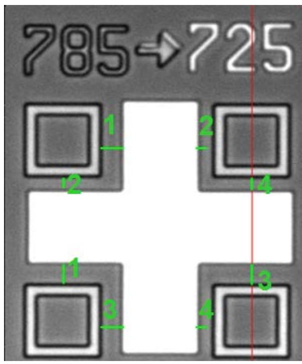
AGENDA

- Metrology for Extreme CMOS – 15 Year Horizon?
  - FEP Metrology
  - Lithography Metrology
  - **Interconnect Metrology**
- Metrology for Beyond CMOS
  - Graphene Devices
  - Other Devices
- Key Message about the Future

Metrology for 3D Interconnect

New subchapter for 3D Interconnects introduced in 2011

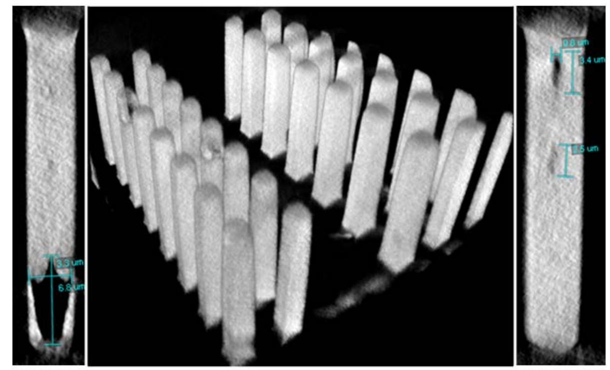
Overlay Through Silicon Substrate – IR Microscopy



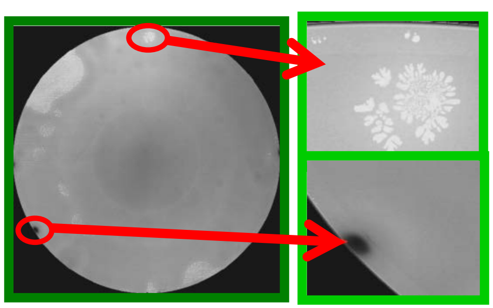
# X	Width[µm]
1	4.3603
2	2.2896
4	4.368
3	2.3057

# Y	Width[µm]
1	4.1033
2	2.2913
3	4.1334
4	2.3796

TSV Metrology and Inspection: X-Ray Microscopy

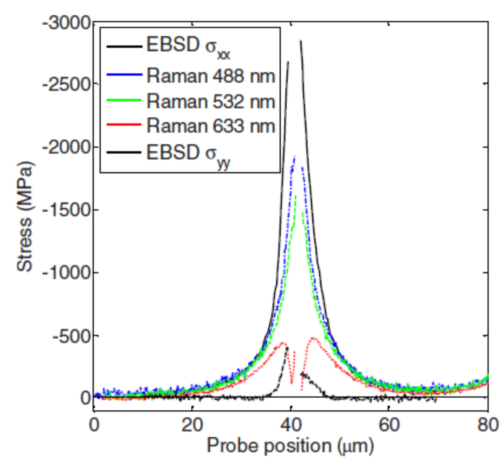


Bonding Defects – SAM Scanning Acoustic Microscopy



Voids and Delamination

Stress Metrology around TSVs Raman Microscopy



AGENDA

- Metrology for Extreme CMOS – 15 Year Horizon?
  - Lithography Metrology
  - FEP Metrology
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- **Metrology for Beyond CMOS**
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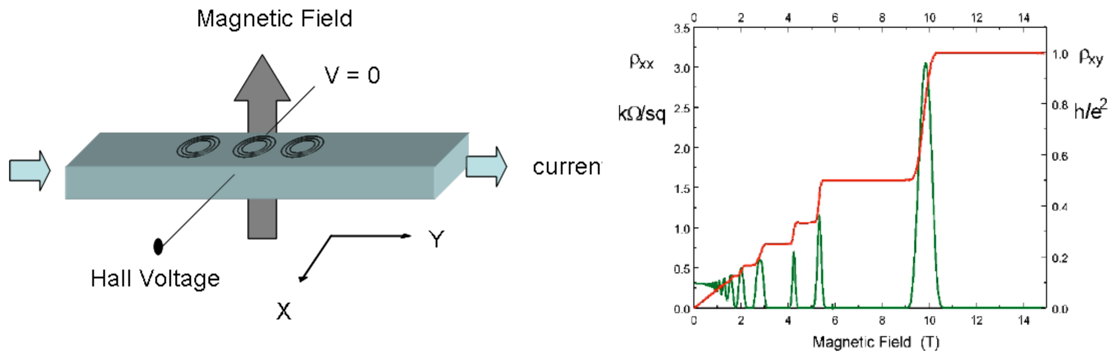
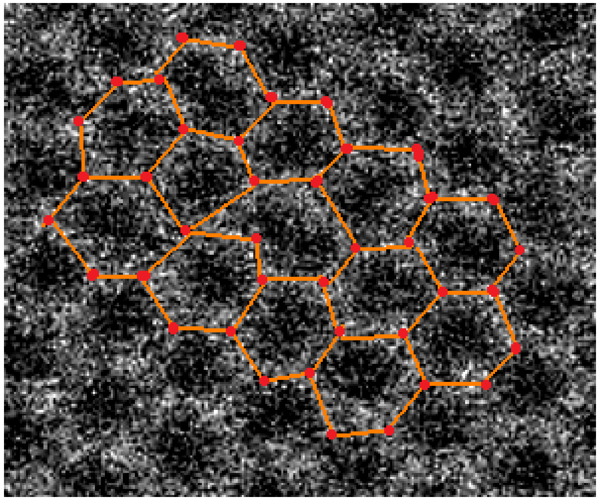
- Key Message about the Future

High carrier mobility and structural robustness have driven a considerable effort in Graphene research

Quantum Hall Effect observes the Berry Phase



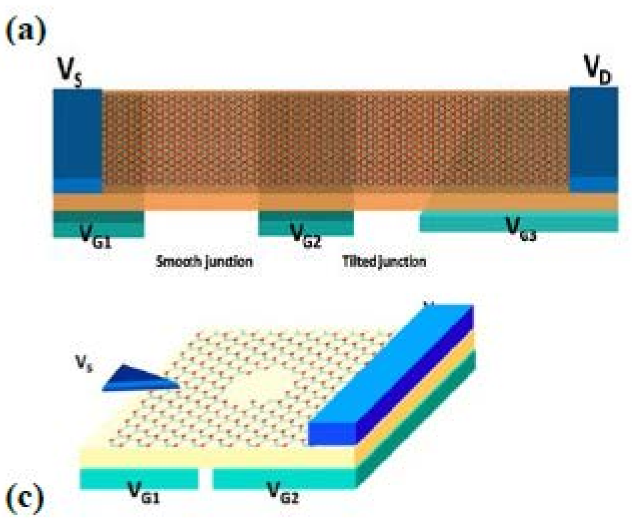
Defects in CVD Graphene

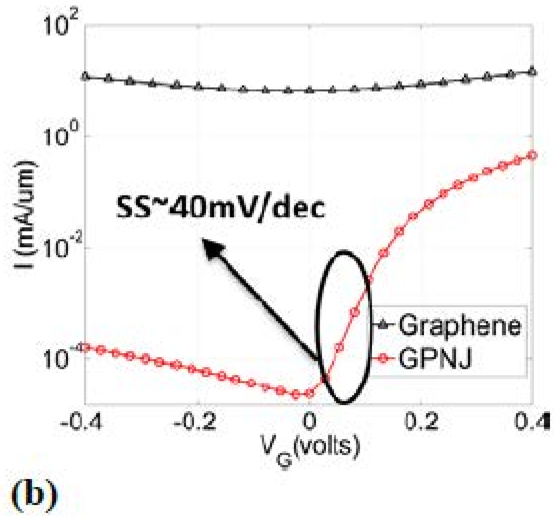


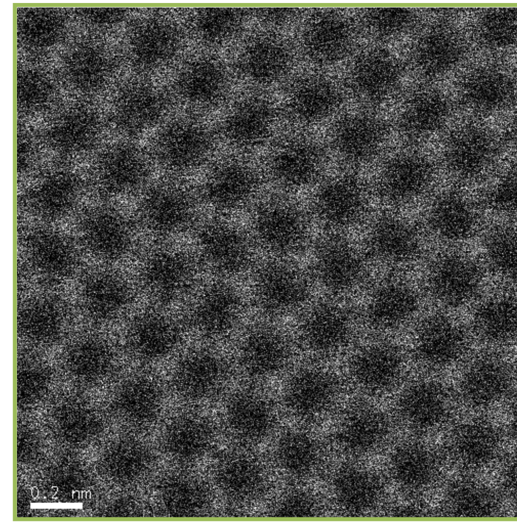
Newly Recognized Gaps

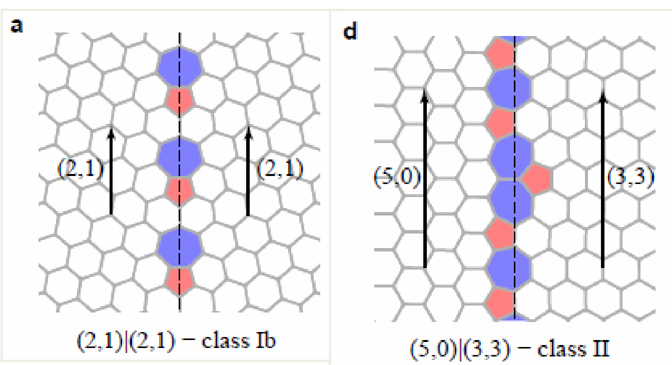
- Measurement of Contact Resistance for Nanostructures
- ESH measurement requirements for new materials and nanomaterials

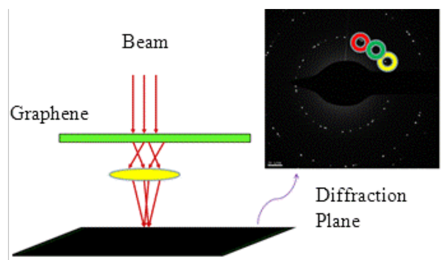
Metrology for ERM / ERD



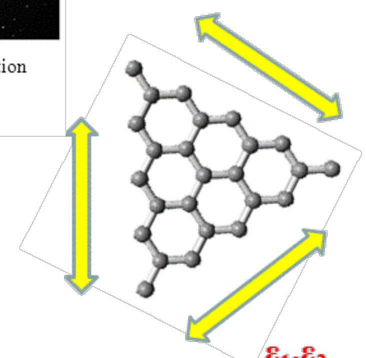




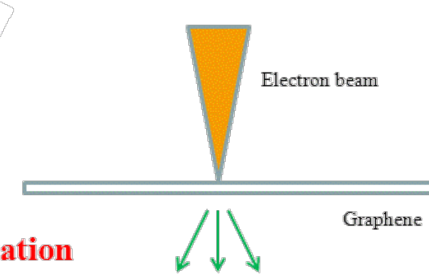




Grain-boundary structural/electronic characterization

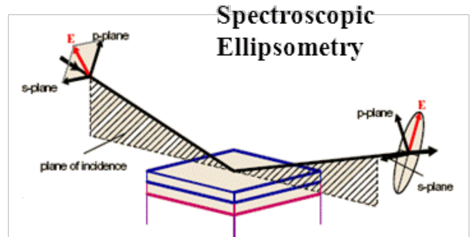


Electron Energy Loss Spectroscopy (EELS)



Grain-size dependent optical properties

Spectroscopic Ellipsometry



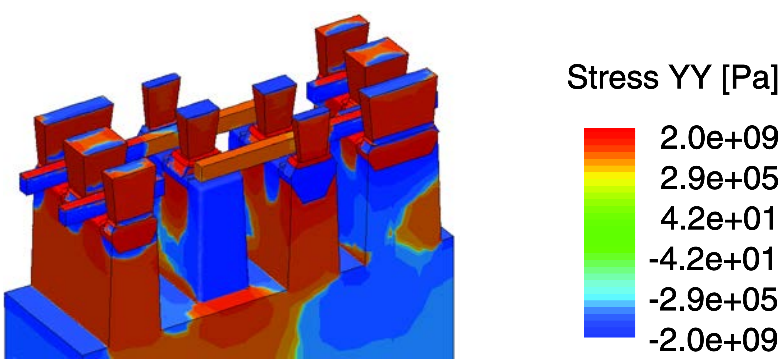
$\varepsilon_1, \varepsilon_2$ Characterization

ShaRE
Shared Research Equipment User Facility
an Office of Science User Facility

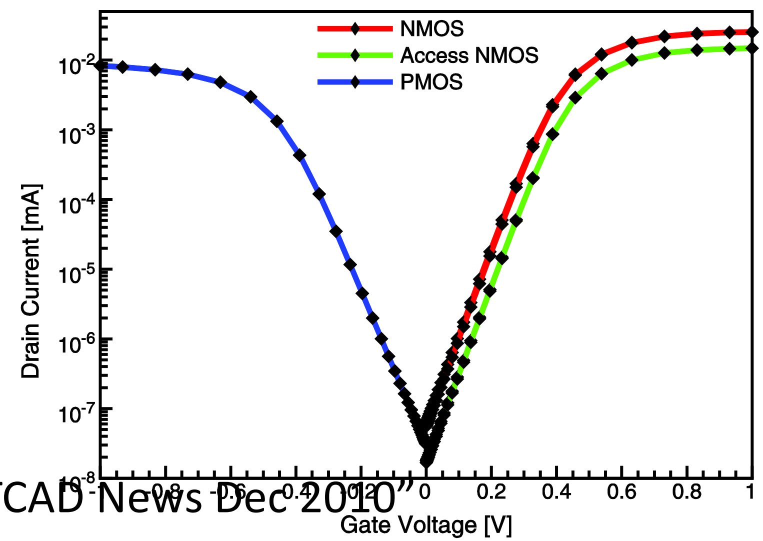
Modeling, Simulation, and Metrology

- Need to connect multiple measurements/methods at nanoscale to properties in a large area using modeling and simulation
- Example : Simulations of SRAM cell show that each transistor experiences a different stress field – measuring one transistor does not represent the entire SRAM Cell

Final Stress in SRAM Cell



I - V

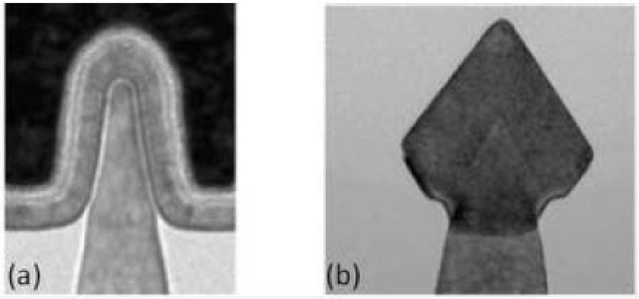


Sentaurus TCAD simulations from Synopsys – TCAD News Dec 2010”

Metrology Summary

- **Litho**
  - **Litho Metrology Now 3D**
  - **Fin, Double Patterning Requirements**
- **FEP**
  - **USJ Metrology Gap (profile and dose)**
  - **Defects in new channel materials**
    Ge and III-V 's
- **Interconnect**
  - **Void Characterization now R&D**
  - **K values of patterned films**
- **ERD-ERM**
  - **Contact Resistance Measurement Gap**
- **ES&H**
  - **Many Measurement GAPS**

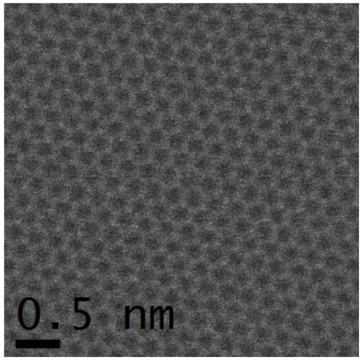
3D Metrology



TEM images of Intel 22-nm PMOS tri-gate transistor (a) and

From Dick James – Chip Works SST Blog

CVD Graphene F. Nelson CNSE



References

- Effects of stress on the dielectric function of strained pseudomorphic $Si_{1-x}Ge_x$ alloys from 0 to 75 % Ge grown on Si (001) G.R. Muthinti, M. Medikonda, T.N. Adam, A. Reznicek, and A.C. Diebold, **J. Appl. Phys. 112, (2012), 053519.**

- Fin Pitch and Stress Measurement using X-Ray Diffraction Reciprocal Space Maps and Optical Scatterometry, A.C. Diebold, M. Medikonda, G.R. Muthinti, V. Kamenini, J. Fronheiser, M. Wormington, B. Peterson, and J. Race, **Metrology, Inspection, and Process Control for Microlithography XXVII, SPIE Advanced Lithography, San Jose, Feb 24-March 1, 2013**.

- Mueller based scatterometry measurement of nanoscale structures with anisotropic in-plane optical properties,_G.R.Muthinti, M. Medikonda, J. Fronheiser, V.Kamineni, B. Peterson, J. Race, W.McGahan, S. Rabello, and A. C. Diebold, **Metrology, Inspection, and Process Control for Microlithography XXVII, SPIE Advanced Lithography, San Jose, Feb 24-March 1, 2013**.

- Mueller based scatterometry measurement of nanoscale structures with anisotropic in-plane optical properties,_G.R.Muthinti, M. Medikonda, J. Fronheiser, V.Kamineni, B. Peterson, J. Race, W.McGahan, S. Rabello, and A. C. Diebold, **Metrology, Inspection, and Process Control for Microlithography XXVII, San Jose, Feb 13-16, 2012.**

- Investigation of E-beam patterned nanostructures using Mueller Matrix based Scatterometry, G.R. Muthinti, B. Peterson, and A.C. Diebold, **Metrology, Inspection, and Process Control for Microlithography XXVI, SPIE Advanced Lithography, San Jose, Feb 13-16, 2012.**