Metrology for Nanoelectronics:

The Impact of Nano-Sized Dimensions on Characterization and Metrology

Alain C. Diebold

ITRS International Technology Roadmap for Semiconductors

AGENDA

- Evolution of Micro to Nanoelectronics
- Transistor (FEP) Metrology Challenges
- Nano Dimensions & Ultra Thin SOI
- Interconnect Metrology
- Patterning Metrology
- Trends & Conclusions

Transistor Metrology Evolution

Beyond CMOS

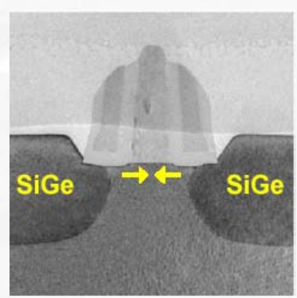
15 year Horizon
Non-classical CMOS

High κ/interface
& Metal Gate
Metrology

Strain
Metrology

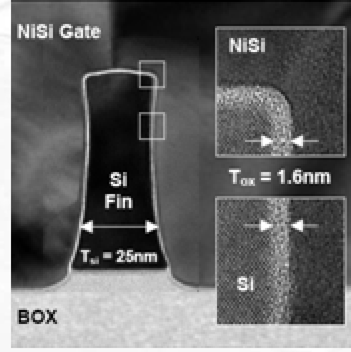
Today
45 nm ½ pitch

Yesterday
90 nm ½ Pitch



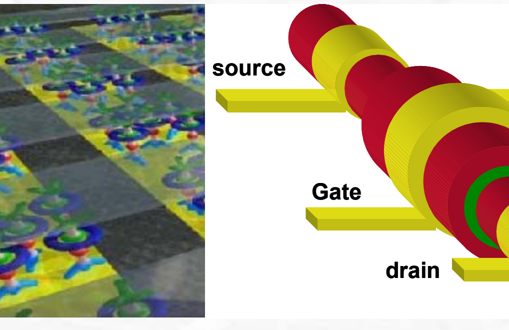
Strain
Enhanced Mobility

New Materials



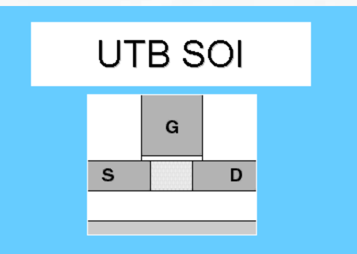
CMOS
pMOS FINFET

Metrology
For New
Structures



Molecular Switches ?
Nanowire Transistor ?

Metrology
For New
Switches



Metrology R&D Rule #1

- Figure out what the next devices are and something about how they will work
  - Know just enough to be Dangerous!
  - Have Friends that Know The Field

Switching Speed of Long Channel Transistor - The Old Days

$I_{dsat} \propto (1/Lg) \; (\mu_{Carrier\ Mobility}) (1/EOT)$

Transistor Gate Delay, τ, decreases as CD decreases but Gate Dielectric must also decrease in thickness.

Idsat ⇧ as Lg gate length ⇩

Sounds Easy

- Just decrease the Gate length &/or increase mobility

TROUBLE As dielectric thickness decreases leakage current increases

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General Rules for CMOS Scaling

$$\frac{Xj}{L} \cong \frac{1}{3}$$

$$\frac{T_{ox}}{L} \cong \frac{1}{30}$$

Today - All Scaling Rules are Violated

$$\frac{T_{depletion}}{L} \cong \frac{1}{3}$$

$$\frac{V_{th}}{V_{dd}} \cong \frac{1}{3}$$

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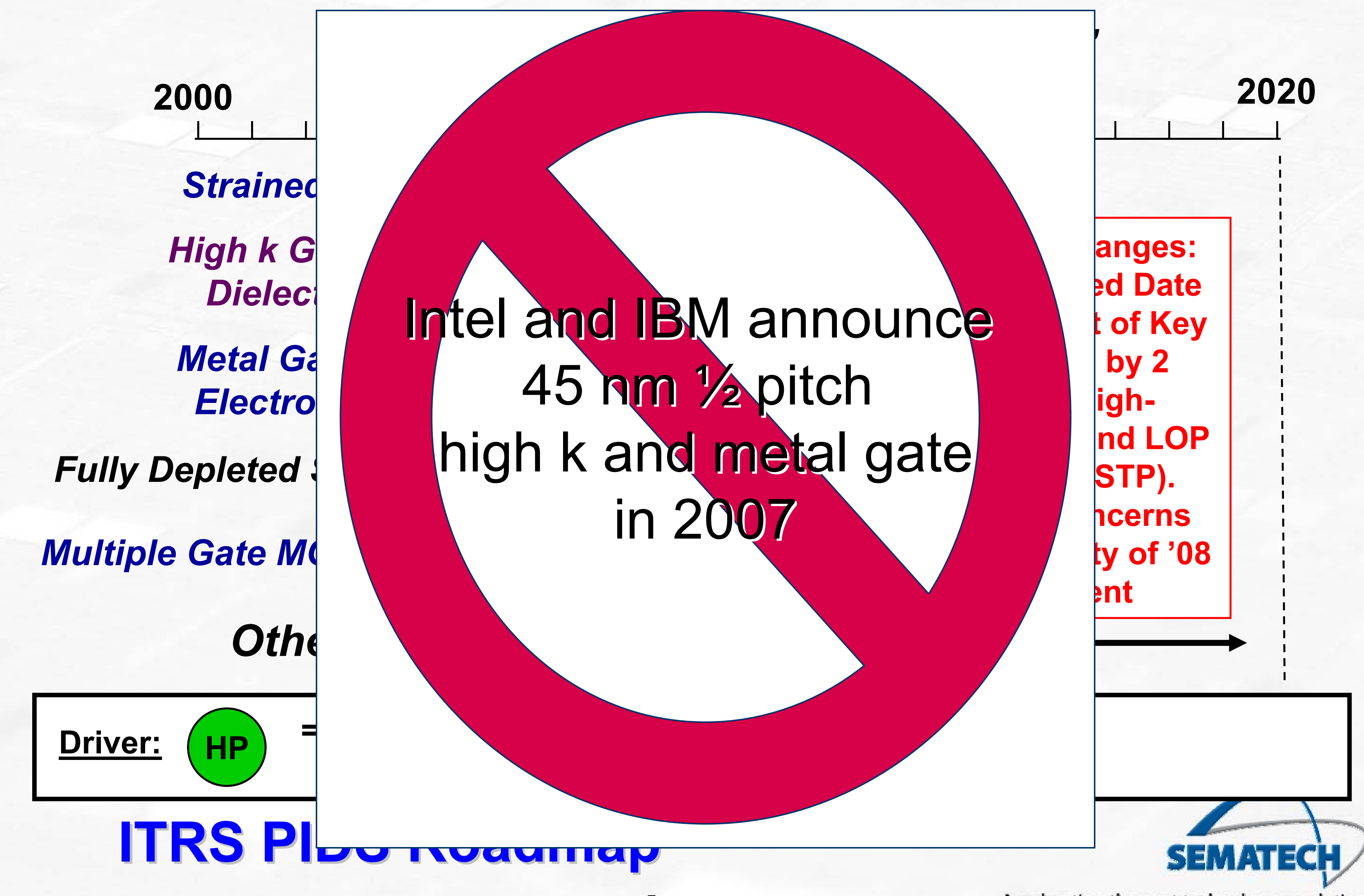
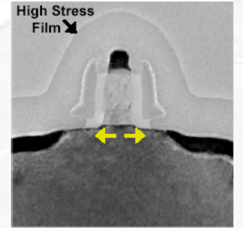
Planar CMOS Evolution

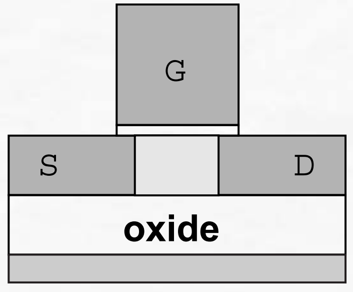


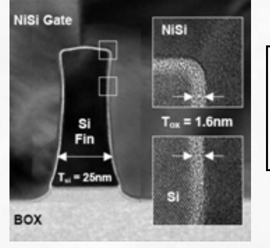
New Transistor Devices (2006 ITRS)

Year in Volume Production	2005	2007	2010	2013	2016	2020
DRAM 1/2 Pitch	80 nm	65 nm	45 nm	32 nm	22 nm	14 nm
Logic Gate Length	32	25	18	13	9	7



Planar Bulk CMOS





Dual Gate or Multiple-Gate

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The Future – the Ultimate NanoTransistor

Short Channel Behavior

$I_{dsat} \propto$ (1/Lg) ($\mu_{Carrier}$? bility) (1/EOT)

Nano Transistors

$$I_{dsat} \sim W\, C_{ox}\, (V_G - V_T)\, \nu_{sat}$$

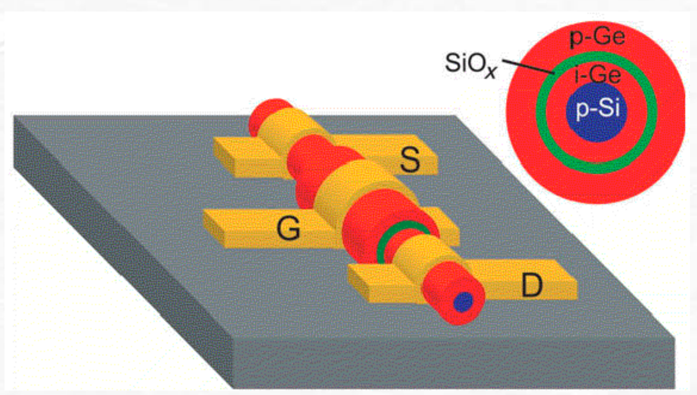
$$\tau = C_{load}\, V_{DD} / I_{dsat}$$

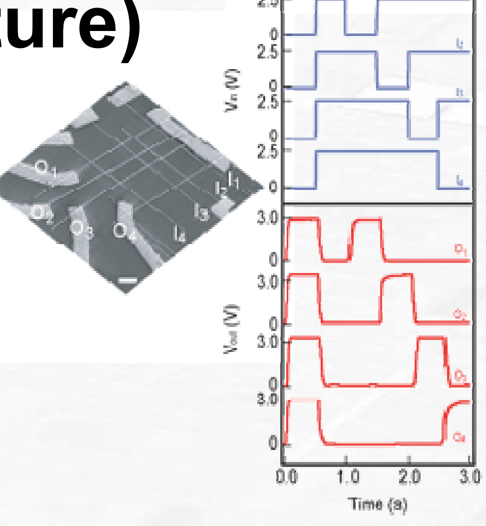
C dependence
A = Lg x W
Dopant Conc.

See Lundstrom's publications

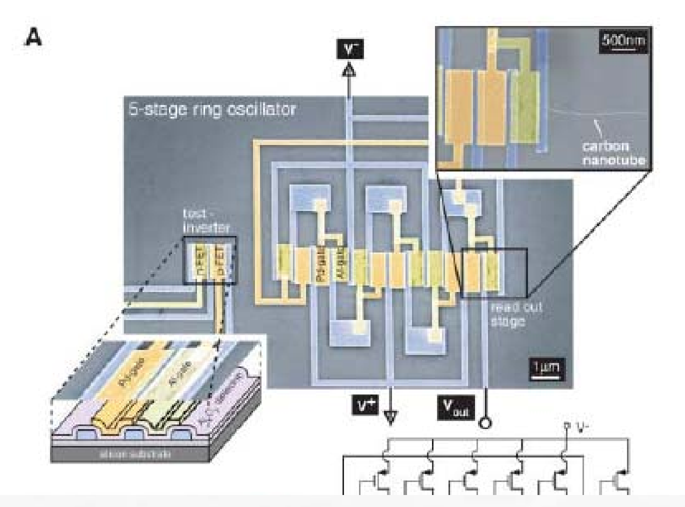
Transition to Beyond CMOS: Make CMOS from NanoMaterials

Nanowire Electronics (Lieber -Nature)





NanoTube Electronics (Avouris – Chen, Science)



18 um long
Carbon nanotube

Ring Oscillator
5 CMOS inverters
= 10 FETs

Nano-Sized Transistor Features require Materials Characterization

NiSi Gate

NiSi

Si Fin

T_{ox} = 1.6nm

T_{si} = 25nm

Si

BOX

SOI

Gate

Source

Drain

Buried Oxide

~ 5 nm

5 nm

[110]

Ge nanowire

Nanowire Sized Si or Ge channel

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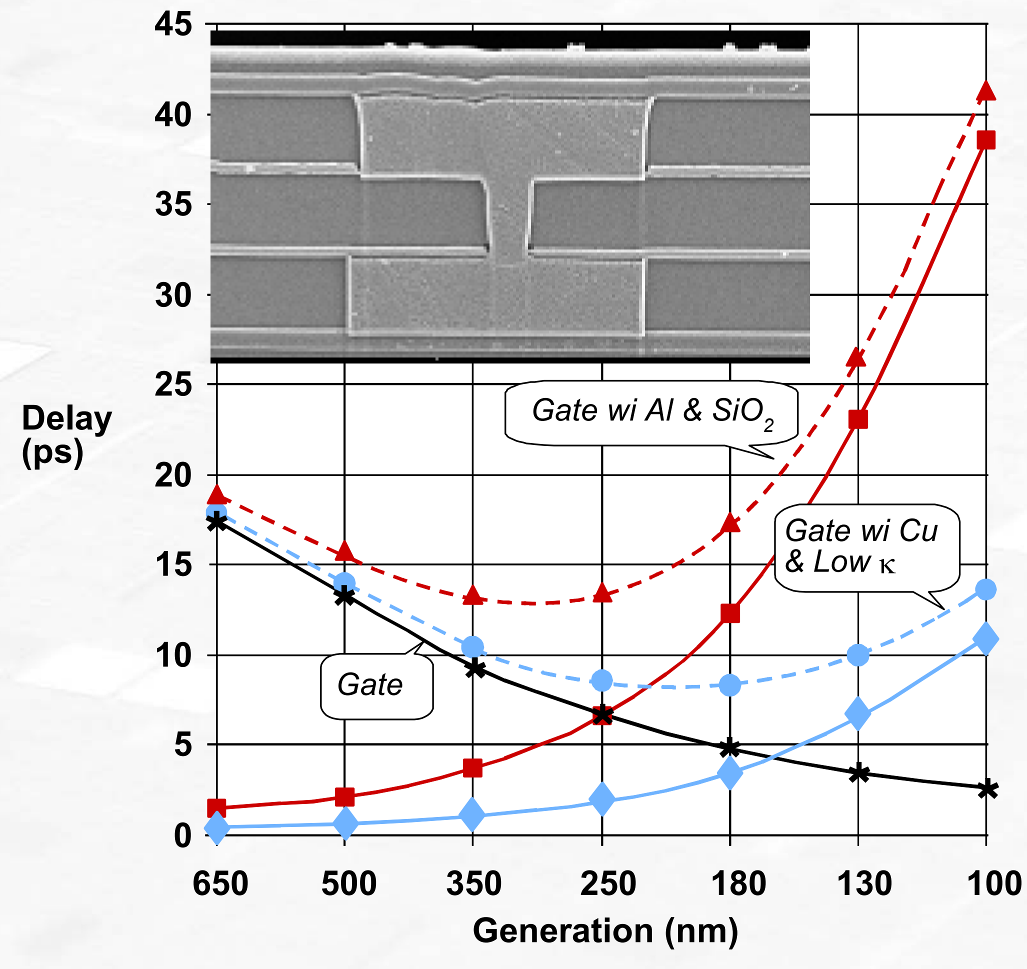
Transistor and Interconnect Delays

SPEED / PERFORMANCE ISSUE *The Technical Problem*



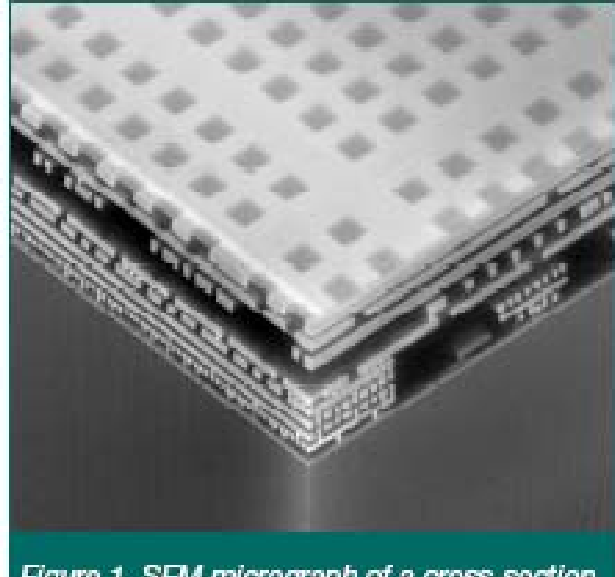


Figure 1. SEM micrograph of a cross-section of AMD's Opteron™ and AMD Athlon™64 microprocessors showing the 9-metal interconnect hierarchy [4].

From ITRS and Mark Bohr (Intel)
Figure from IBM

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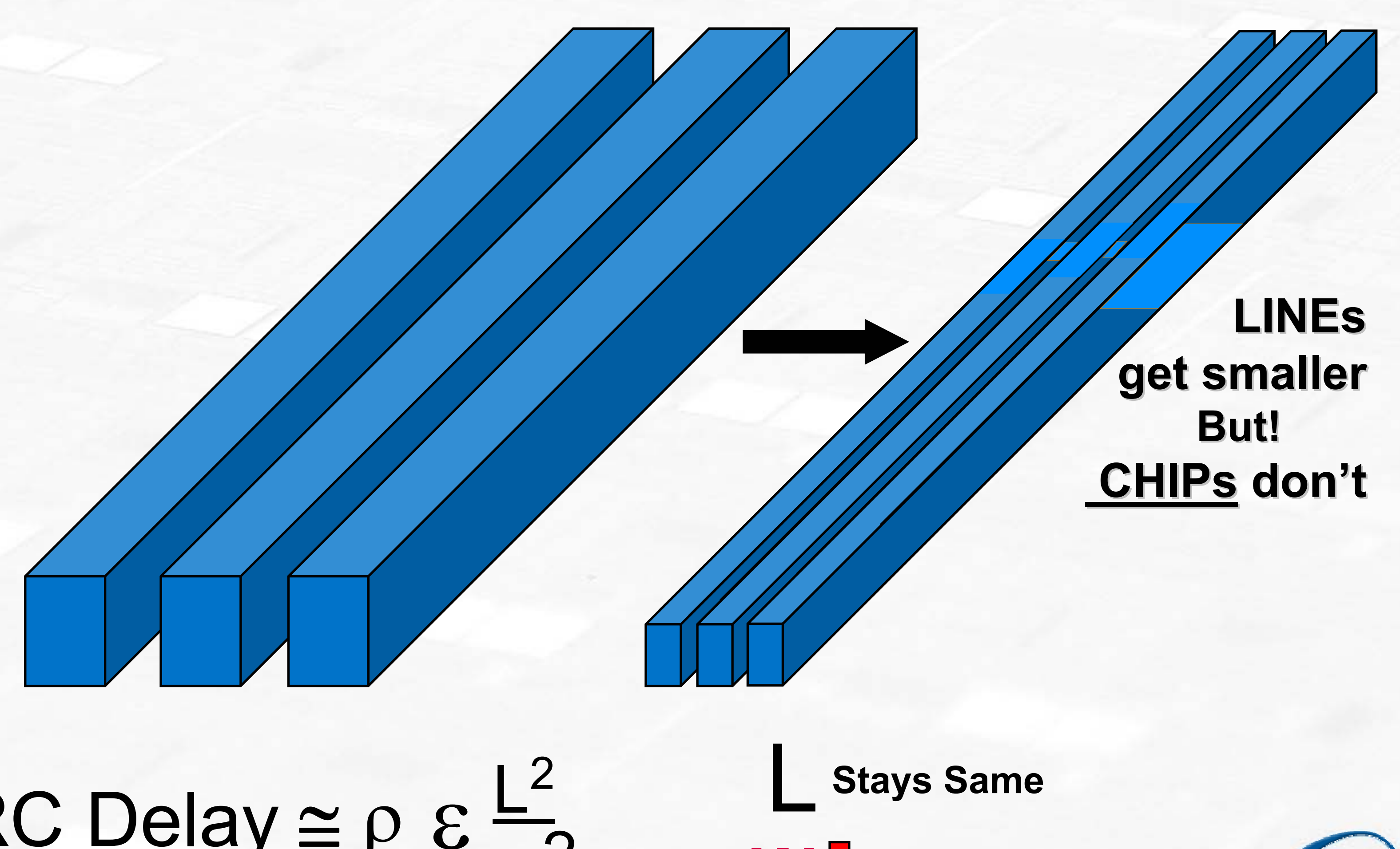
Interconnect Delay: GLOBAL LINE SCALING

Global conductor lines getting smaller in cross-section but *NOT* in length. Signal delay is growing exponentially!



$$\text{RC Delay} \cong \rho\ \varepsilon \frac{L^2}{w^2}$$

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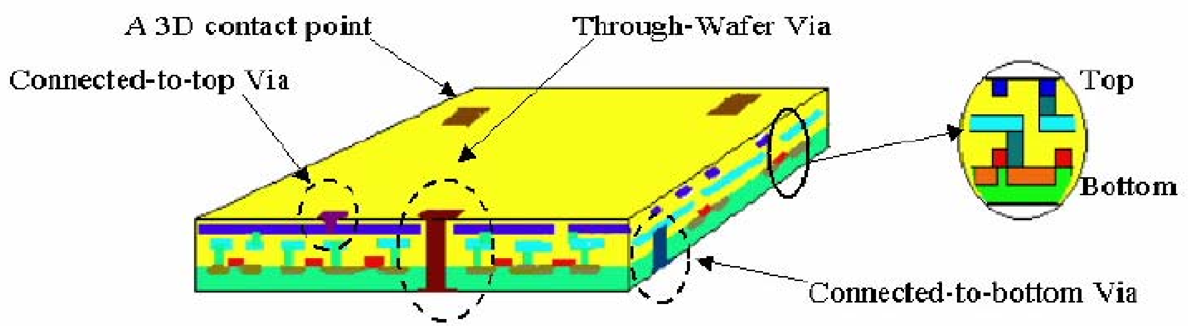
Future Interconnect (ITRS 2006)

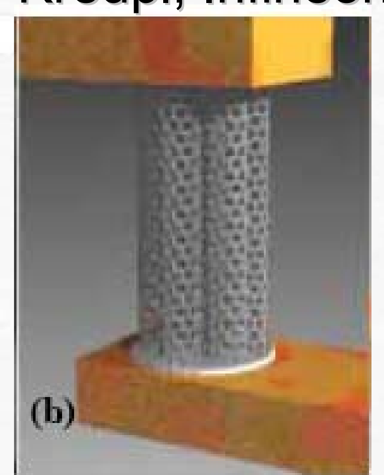


- 3D Interconnect ?

- Carbon Nanotubes ?

MARCO Center

Kreupl, Infineon



Intel

1) Light Source
2) Guide Light
3) Modulation
Waveguide devices
4) Photo-detection
5) Low Cost Assembly
6) Intelligence
Passive Align
CMOS
SiGe Photodetectors

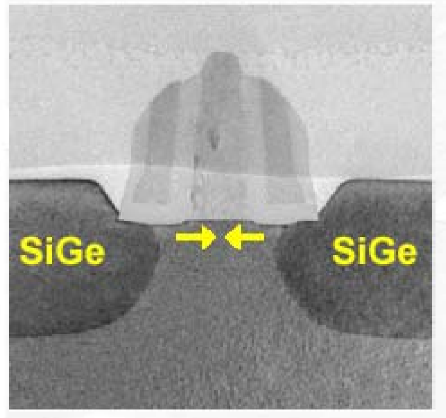
- Optical Interconnect ?

AGENDA

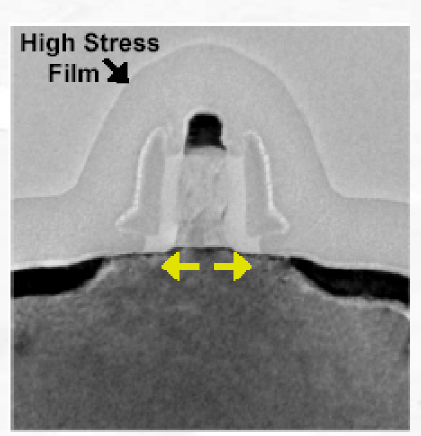
- Evolution of Micro to Nanoelectronics
- Transistor (FEP) Metrology Challenges
  Extending Planar CMOS & Introducing Non-Planar CMOS
  - Stress and Film Thickness (& Sidewall)
- Nano Dimensions & Ultra Thin SOI
- Interconnect Metrology
- Patterning Metrology
- Trends & Conclusions

Today - ICs use Locally Strained Si
Considerable Process Diversity

NMOS – SiN Stress Liner
PMOS SiGe in Source & Drain



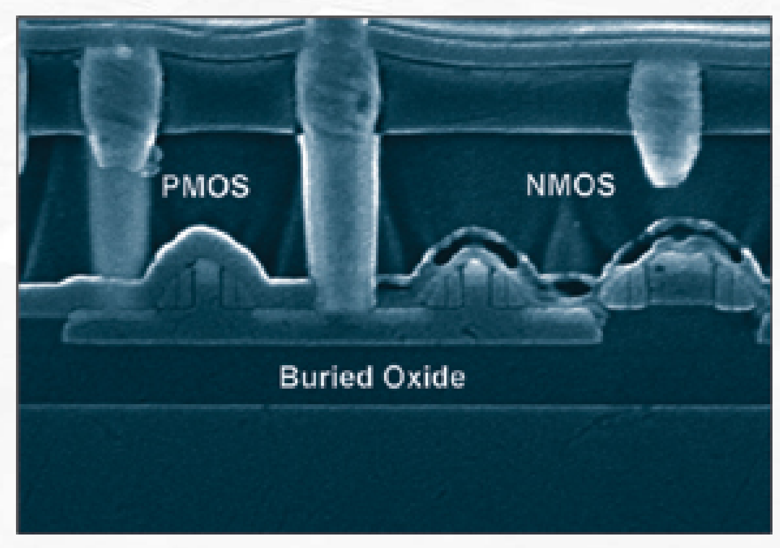
PMOS
Compressive Strain
increased hole mobility



NMOS
Tensile Stress SiN Layer
increased electron mobility

From T. Ghani, et al., IEDM 2003, p 978.
Courtesy Intel

Dual Stress Liner
NMOS – Tensile SiN
PMOS – Compressive SiN



AMD Athelon™ 350 Venice
Micro - Chipworks Corner
Dick James

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Diversity in Dual Stress Liner Process Drives unique Metrology Solutions

AMD Athelon™ 350 Venice
Micro - Chipworks Corner
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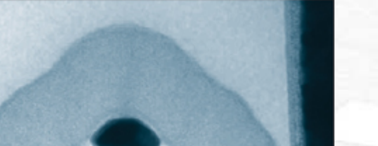
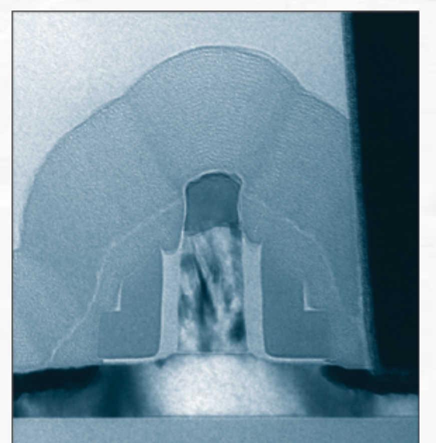
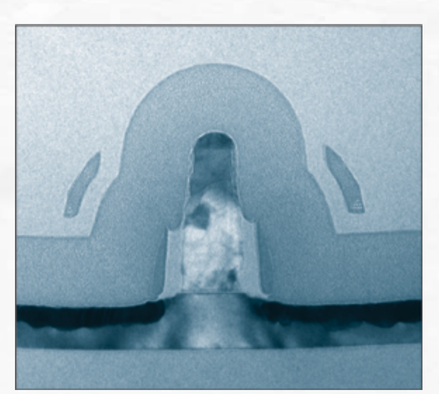
PMOS **NMOS**



IBM –MP from Xbox 360
Micro - Chipworks Corner
Dick James

PMOS **NMOS**

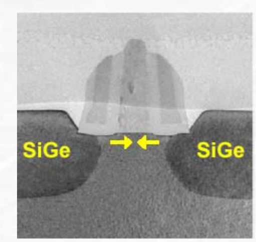


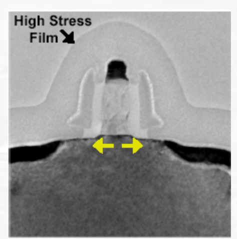


Reported AMD Process
N&P MOS Compressive Si Nitride layer
Oxygen Implanted in NMOS area
& Nitride becomes tensile OxyNitride

Reported IBM Process
NMOS Spacer reduced
PMOS Multilayer Compressive Nitride

Survey of Stress(Strain) Measurement Methods



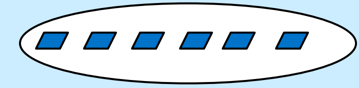


Nano-Raman and CBED

Transistor Level Stress

Micro-Raman, XRD
Photoreflectance Spectroscopy

Micro-Area Level Stress



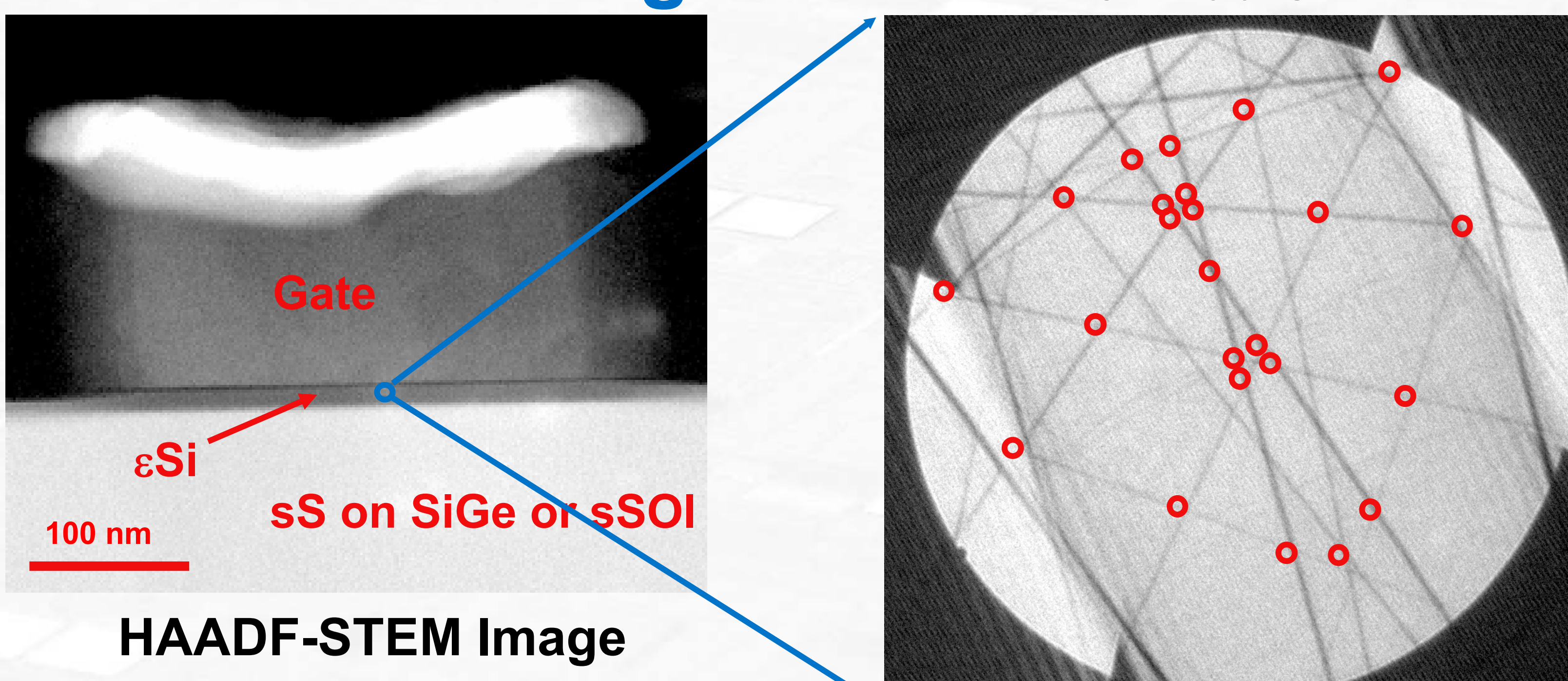
Die Level Stress

Laser Interferometry
Oraxion Method

Wafer Bow

Laser Interferometry, Oraxion Method

Strain measurement
Convergent Beam Electron Diffraction (CBED)
HOLZ Line Fitting



Lattice constants determined by least-squares (χ^2) fitting of experimental to simulated HOLZ line patterns for [340] zone.

ASACS™ software by Soft Imaging Systems Inc (from "STREAM" project).

3-D lattice fitting under constraints of plane strain approximation.

Armigliato, et al., Appl. Phys. Lett. 82, 2172 (2003).
J. M. Zuo, Ultramicroscopy 41, 211 (1992)

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TEM sampling will not be easy

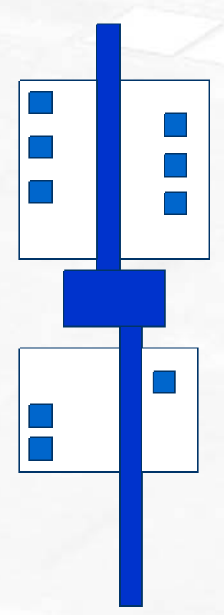
Differences in PMOS and NMOS mobility: iso vs Dense

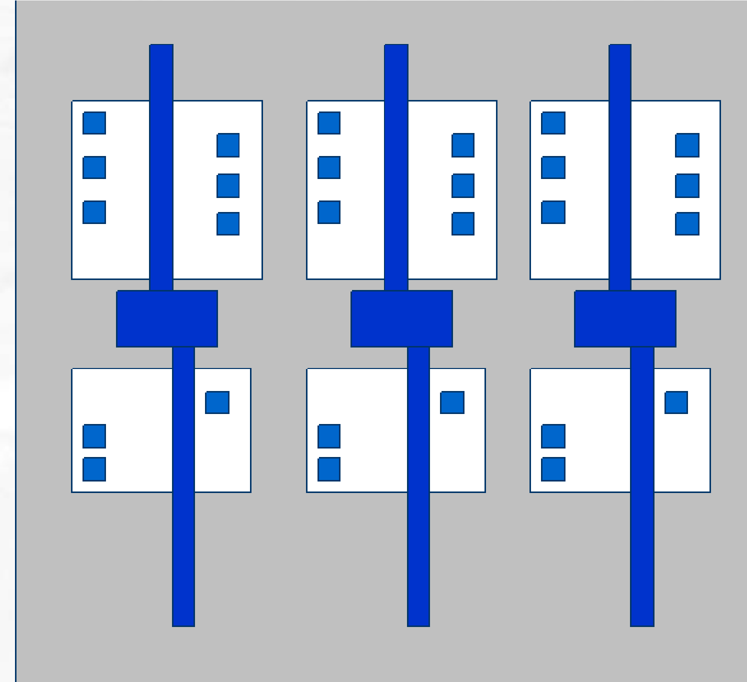
pMOS difference 14%

nMOS difference 8%

nMOS to pMOS difference ratio 22%

Much more complicated for real design

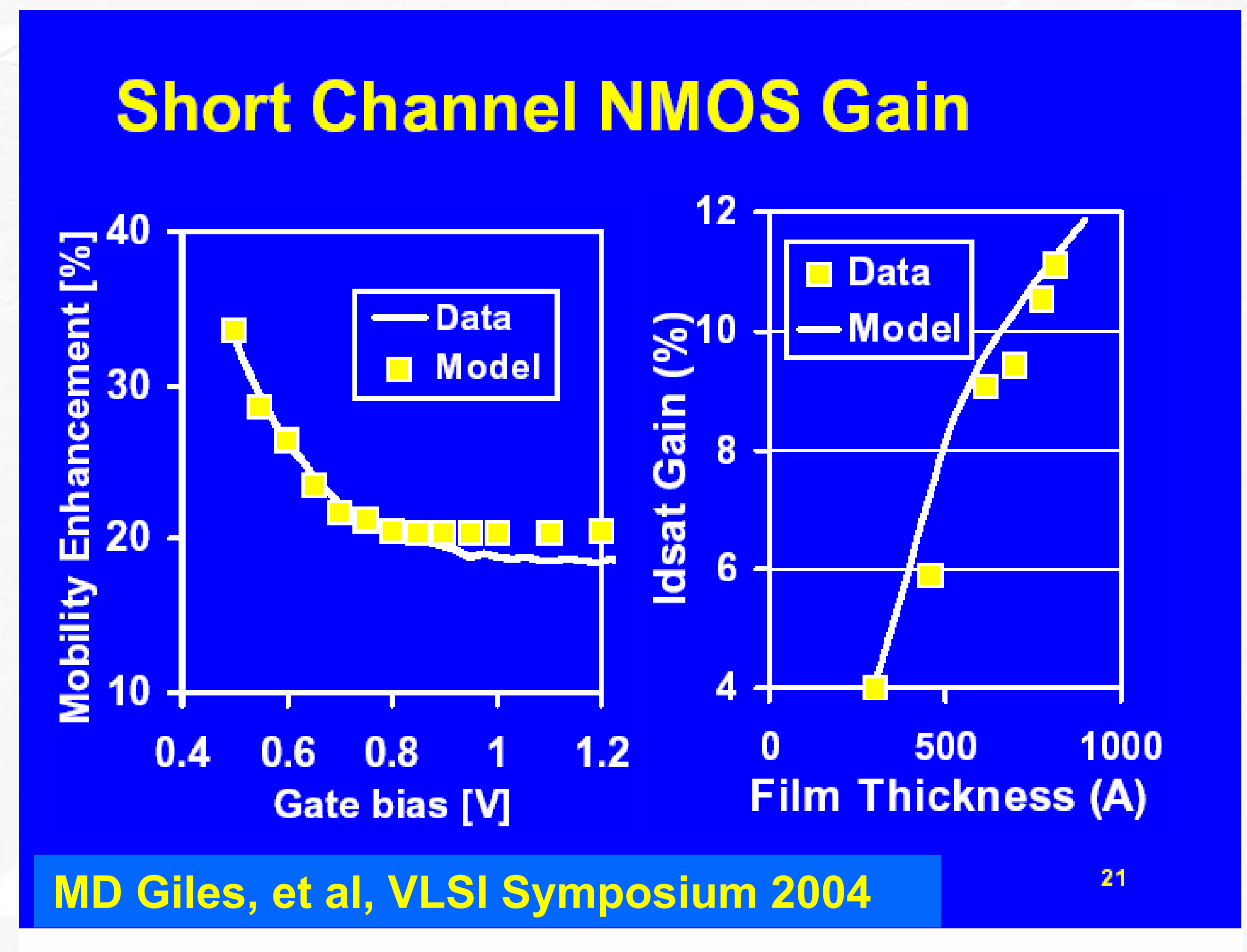




Fichtner –at 2005 Nano Transistor Conference

Trend : Use Modeling to connect what you want to measure with what you need to know

Example: Metrology of Strained Channel Devices



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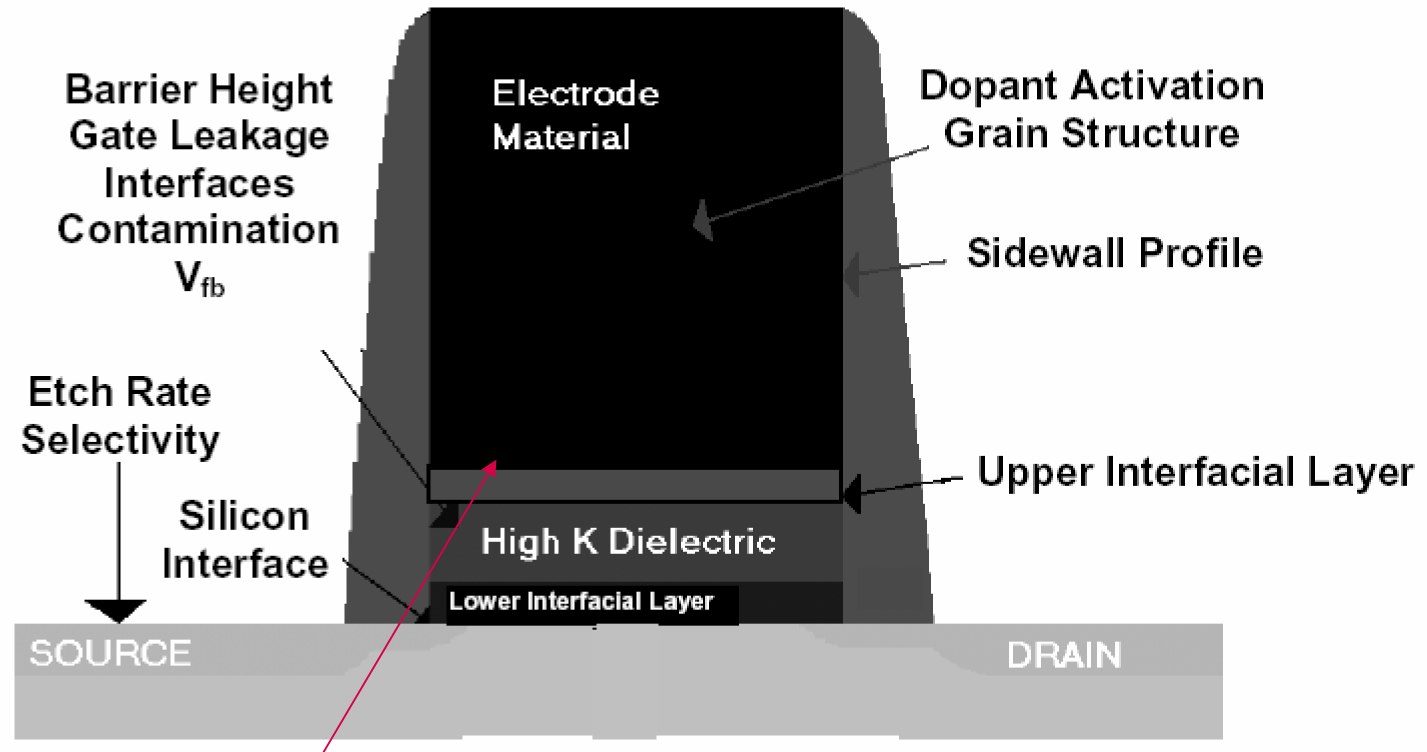
Film Thickness at Nano-Dimensions

- Transistor Gate Dielectric
  - Complicated Dielectric Stack with SiO_2 Interface



- Metal Gate
  - Thin Metal Layer with Dual Work Functions for NMOS vs PMOS

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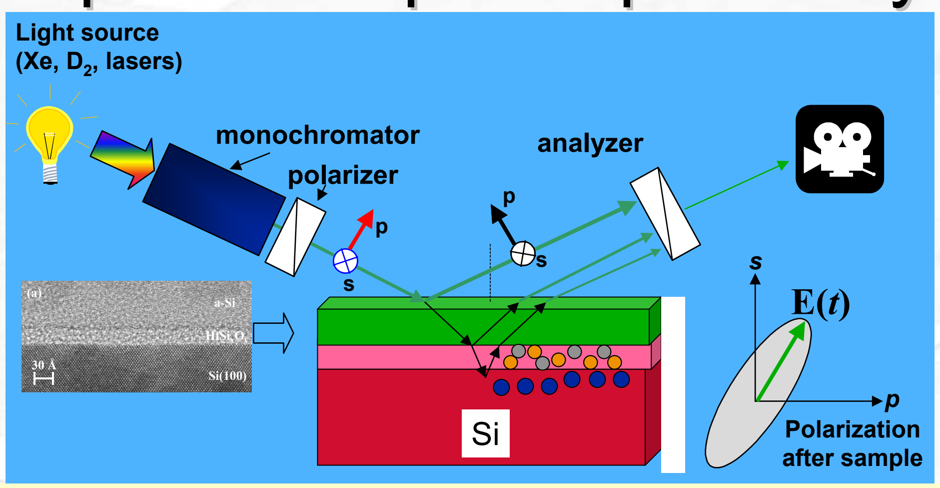
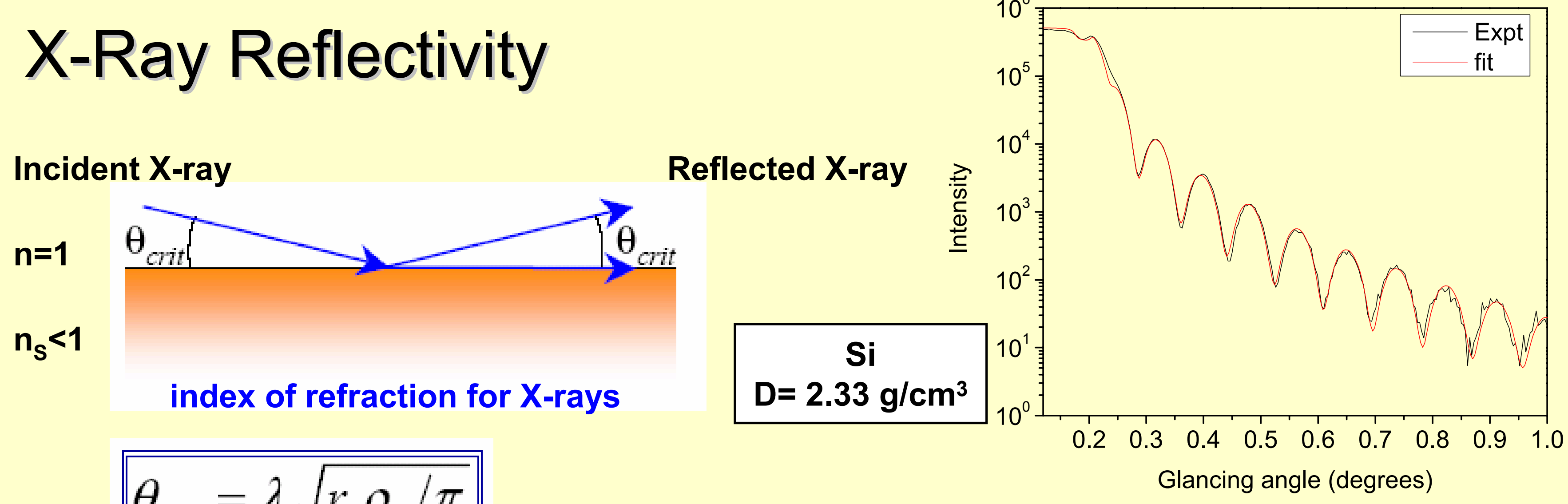
Physical Film Thickness Metrology

Spectroscopic Ellipsometry



X-Ray Reflectivity



$$\theta_{crit} = \lambda\sqrt{r_o \rho_e / \pi}$$

Optical/X-ray vs Electrical Measurement

C-V Structures receive Further Processing
Optical thickness vs electrical EOT
Capacitance of a very thin interface can have big effect

$EOT = t_{int} + (3.9/\kappa)t_{high\ \kappa}$

$t_{optical} = t_{int} + t_{high\ \kappa}$

$t_{ox.}$

$t_{int.}$

poly-Si

dielectric

Si-substrate

V_{gate}

$V_{poly\ depletion}$

$C_{ox.}$

$C_{interface}$

QM charge

Optical ⟺ Physical ⟺ Traditional Electrical

(Process Monitoring) (Performance/Reliability)

See also : C Richter (NIST) in Char & Met for ULSI 2000

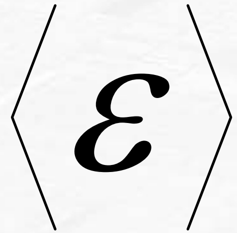
Traditional High Precision SiO2 Thickness

- Single Wavelength Ellipsometry
- Optical constant at one wavelength – only n needed - k close to zero in visible wavelength range
- Oxynitrides – same principle works for thickness - nitrogen concentration not easy to pin down to 0.1 atomic % optically even with SE

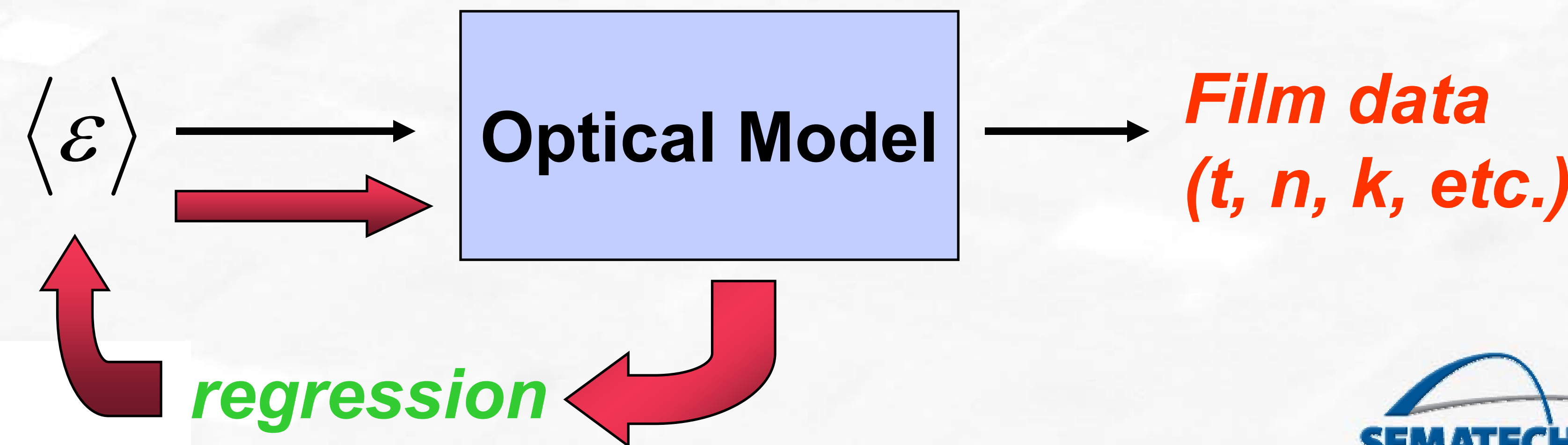
Spectroscopic Ellipsometry

Lab – Far IR to VUV

In-line – Near IR to VUV



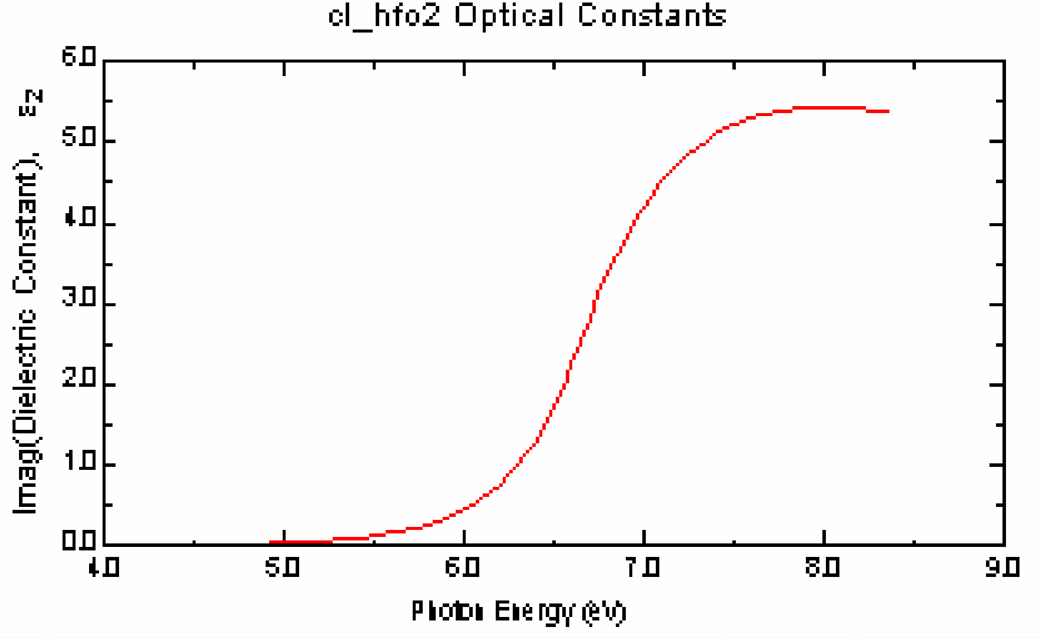
Dielectric Properties are a function of wavelength of light



Cody-Lorentz* optical model used for parametric modeling of gate dielectrics.

$$\varepsilon_2 \propto Exp\left[\frac{(E - E_t)}{\beta}\right], for E \le E_g.$$

$$\varepsilon_2 \propto (E - E_g)^2, for E > E_g.$$



* A.S. Ferlauto, et. al., J. Appl. Phys., 92, 2424 (2002).

J. Price, et. al, Appl. Phys. Letters, 85, 1701 (2004).

New Optical Models
Variability with Composition and Process
See Jimmy Price's talk for SE of defects in High K

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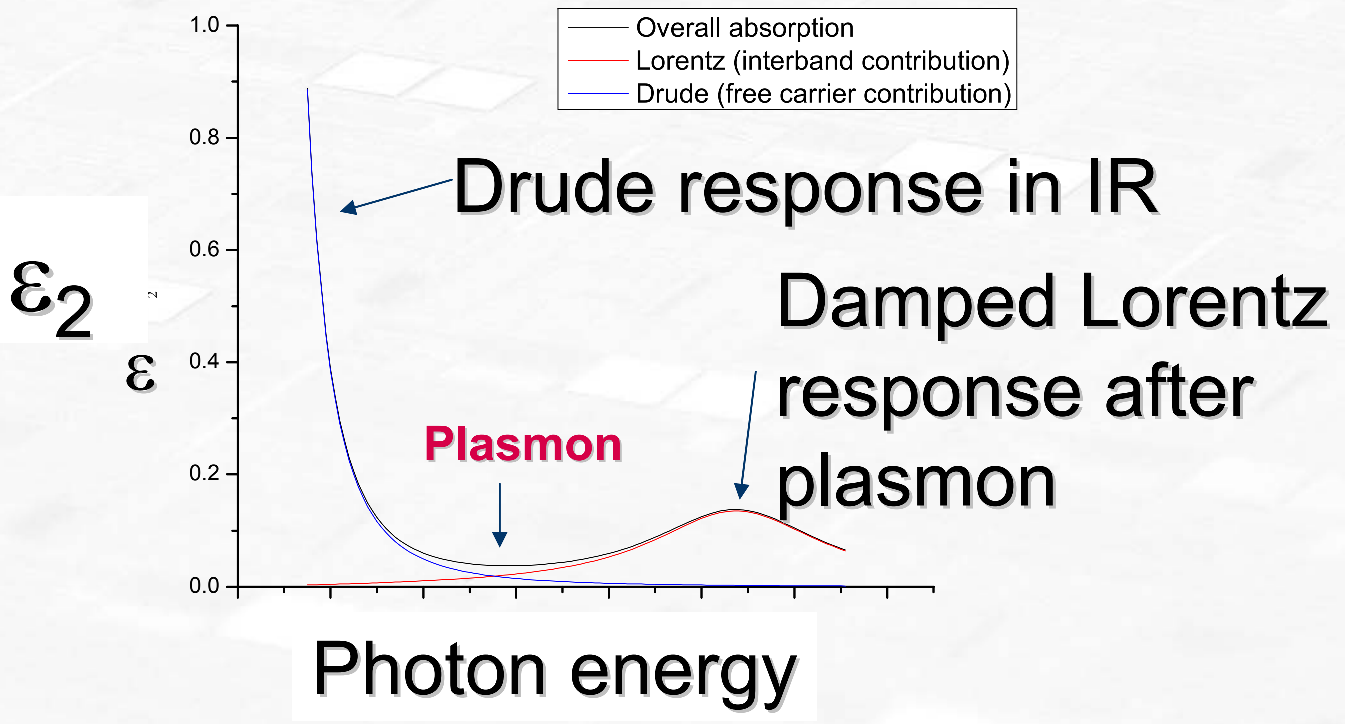
Thin Metal film metrology

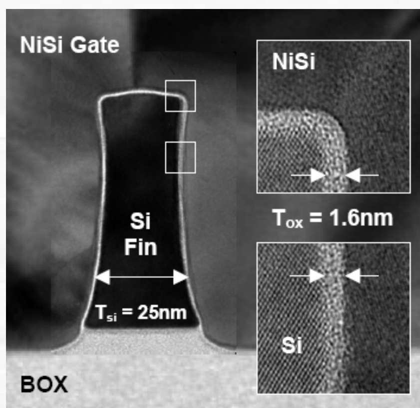
Dielectric function of a Metal film



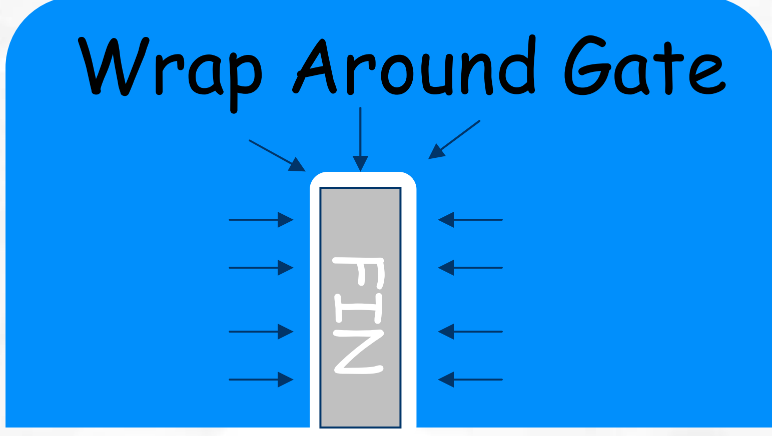
Challenge : Stable Recipe over wide range of thickness

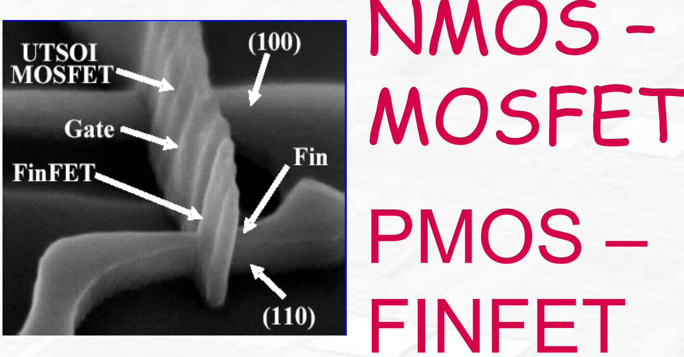
Wrap Around Gate Metrology

FINFET (IBM)



Side Wall and Top Dielectric Thickness and Composition

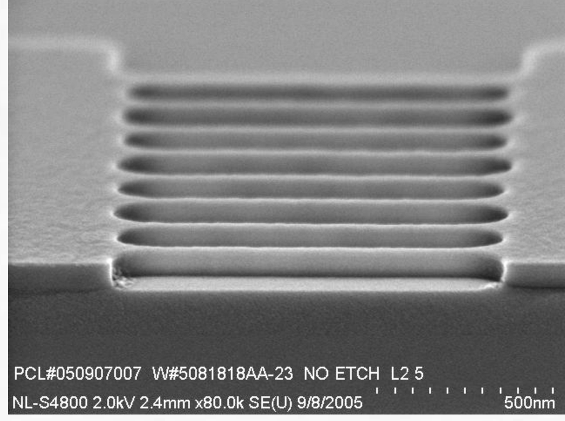




NMOS - MOSFET

PMOS – FINFET

MUGFET



- **Fin line edge roughness,**
- **Fin thickness uniformity**

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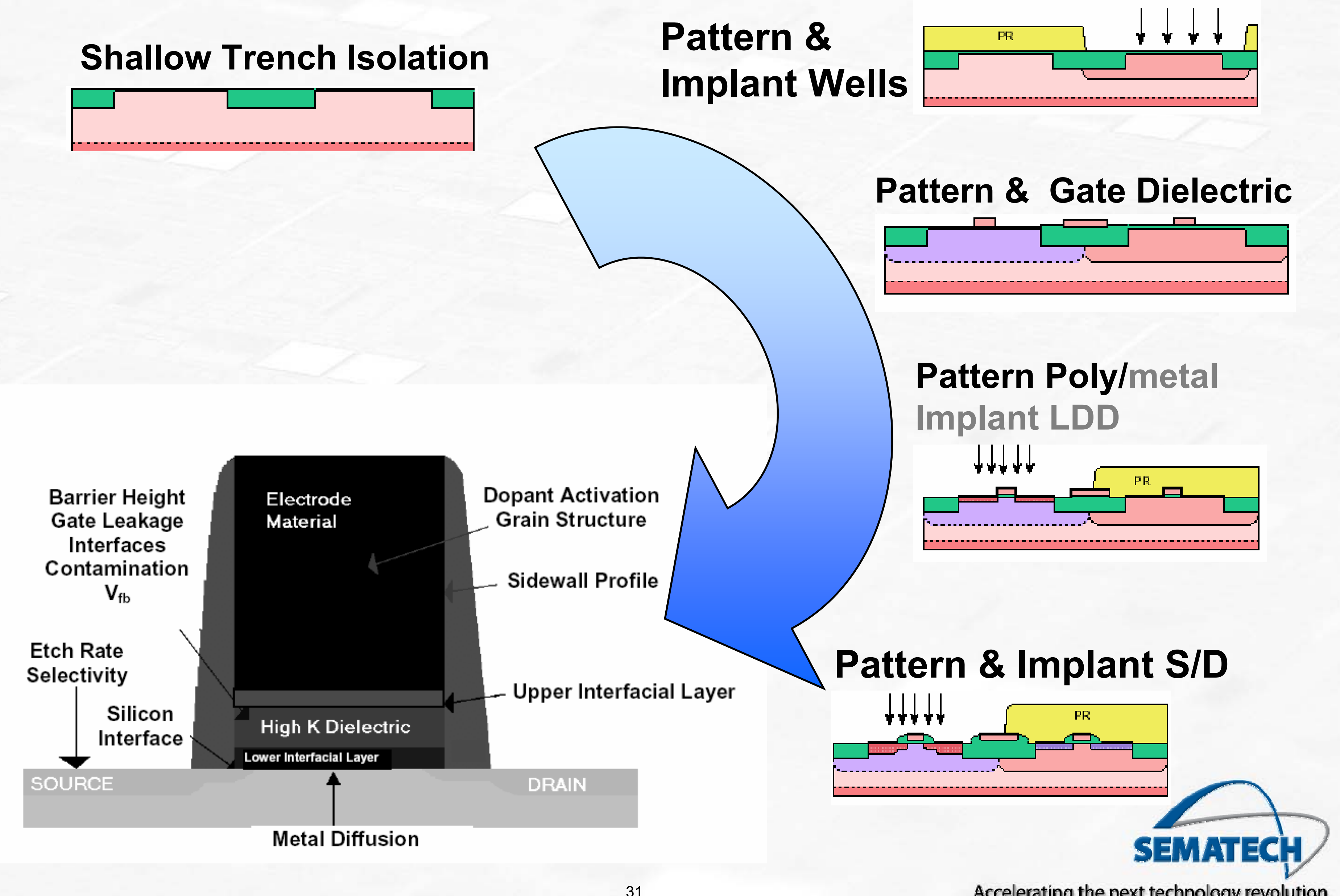
Front End Metrology Other Measurements



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- Evolution of Micro to Nanoelectronics
- Transistor (FEP) Metrology Challenges
- Nano Dimensions & Ultra Thin SOI
    - Example of SEMATECH Work (Price & Diebold)
- The Future of Materials Characterization
- Interconnect Metrology
- Patterning Metrology
- Nano - Characterization and Metrology
- Trends & Conclusions

Optical ~~Constants~~ Properties:

- **Bulk Si optical properties are well known**
- **Optical properties of nano-scale materials are not well known.**
- **Shifts in nano-scale SOI films can be observed at room temperature**

Data Proves the Problem is Real:

3	native oxide	15.166 Å
2	bulk soi	101.78 Å
1	buried oxide layer (box)	1606.4 Å
0	silicon substrate	1 mm

Difference between optical model & data.

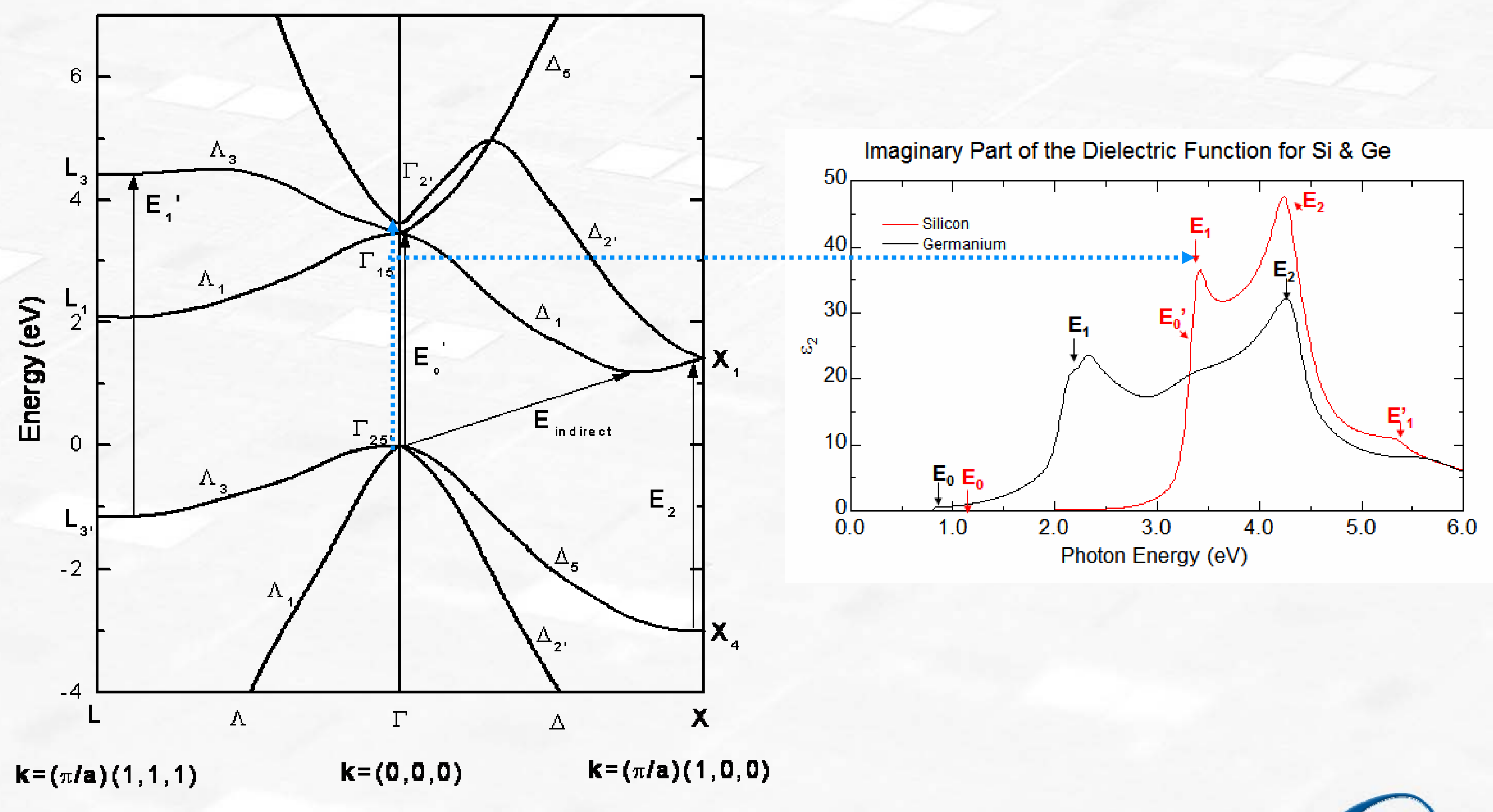
10 nm SOI **6.7 % Δ TEM**

8 nm SOI **15.1 % Δ TEM**

4 nm SOI **18.5 % Δ TEM**

2 nm SOI **19.8 % Δ TEM**

Optical Absorption at Critical Points



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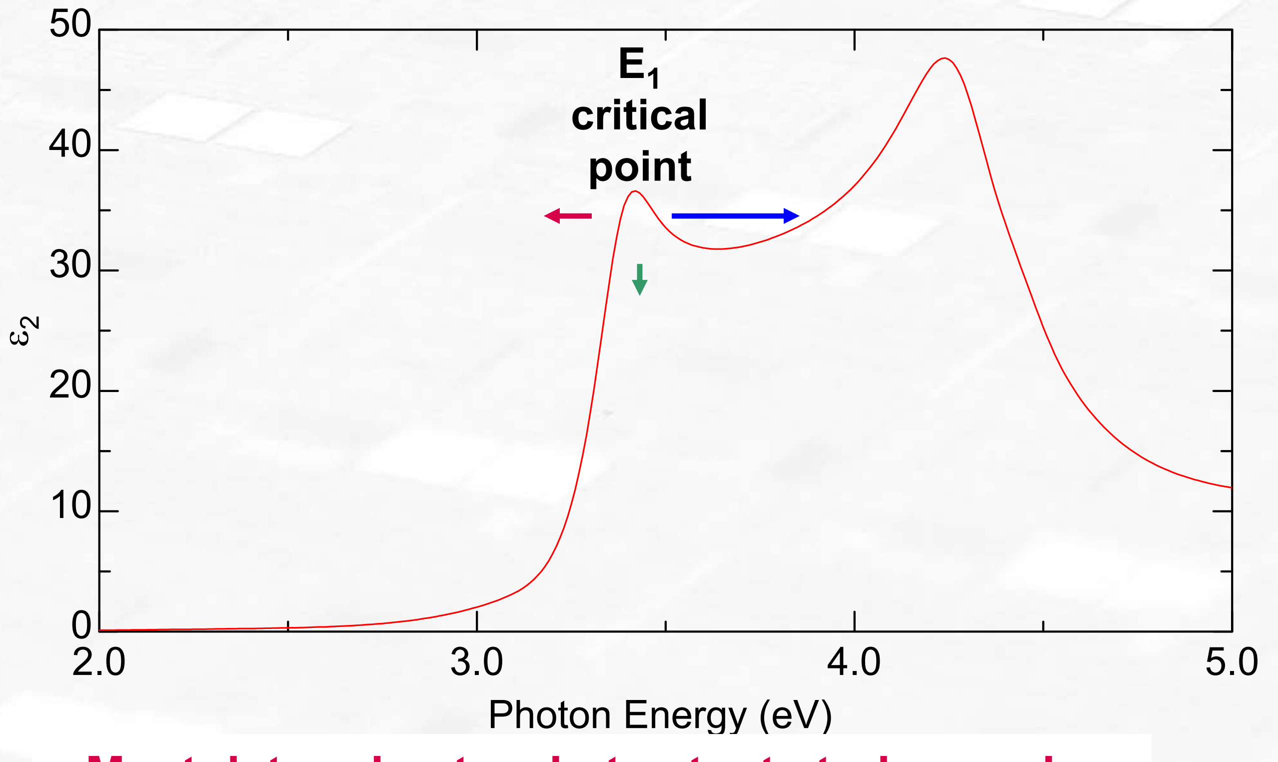
Summary of techniques:

- Crystallinity → no effect.
- P composition → possible E_1 amplitude decrease for high P concentration.
- Strain → Red shift for E_1 transition.
- Quantum confinement → Blue shift for E_1 transition.



Must determine to what extent strain may be impairing the critical point energy shift!

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Other sources of shifts in the optical properties?

Shows Importance of cross-method characterization

1. Confirmed Crystallinity → TEM

2. Dopant Profiles → SIMS

   (No Oxidation induced P Buildup at Interface)

3. No Strain Observed → Raman and XRD

4. Quantum Confinement Observation → SE

SE results for UTB-SOI films:

Blue shift for E1 transition.

~ 50nm SOI
~10nm SOI
~7nm SOI
~4nm SOI
~2nm SOI

1. Energy Shift
2. Shape change (i.e. JDOS)

ε_2

50
40
30
20
10
0
-10

2.0
3.0
4.0
5.0

Photon Energy (eV)

•Clearly, quantum confinement effects are observed with decreasing thickness of the silicon layer.

•Provided the thickness values are fixed by independent means (eg. TEM), data inversion method is able to extract optical constants for quantum confined silicon.

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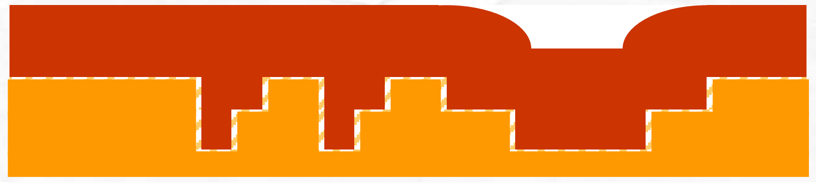
Interconnect Metrology

Pattern Low κ

Control Film Stack Thickness, Line width/depth and shape

Deposit barrier and copper

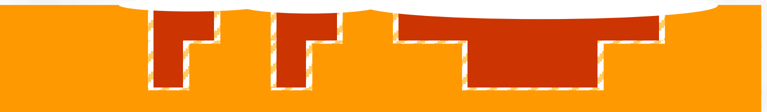
Control barrier/copper & voiding



Low k / barrier etch stop / low k

Chemical Mechanical Polishing

Control Flatness



Modeled Effective Dielectric Constants

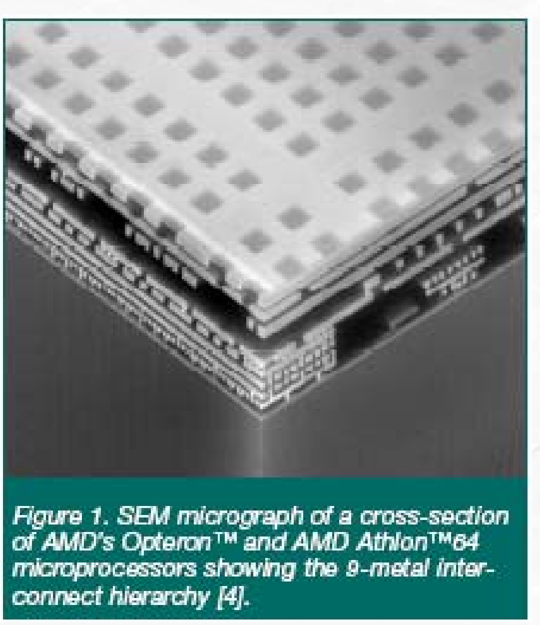
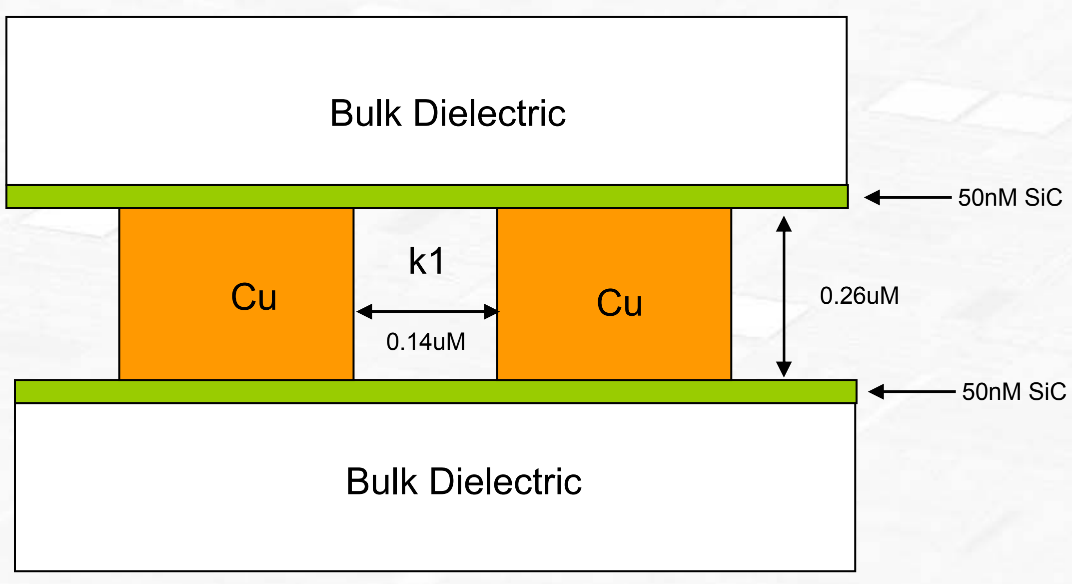


Figure 1. SEM micrograph of a cross-section of AMD's Opteron™ and AMD Athlon™64 microprocessors showing the 9-metal interconnect hierarchy [4].



If bulk dielectric = 2.6 (SiLK*) then k_{eff} = 2.94
If bulk dielectric = 2.2 then k_{eff} = 2.57
If bulk dielectric = 1.5 then k_{eff} = 1.96
If bulk dielectric = 1.0 (Air) then k_{eff} = 1.5

* SiLK Semiconductor Dielectric, Trademark of the Dow Chemical Company

Thanks to Navjot Chhabra

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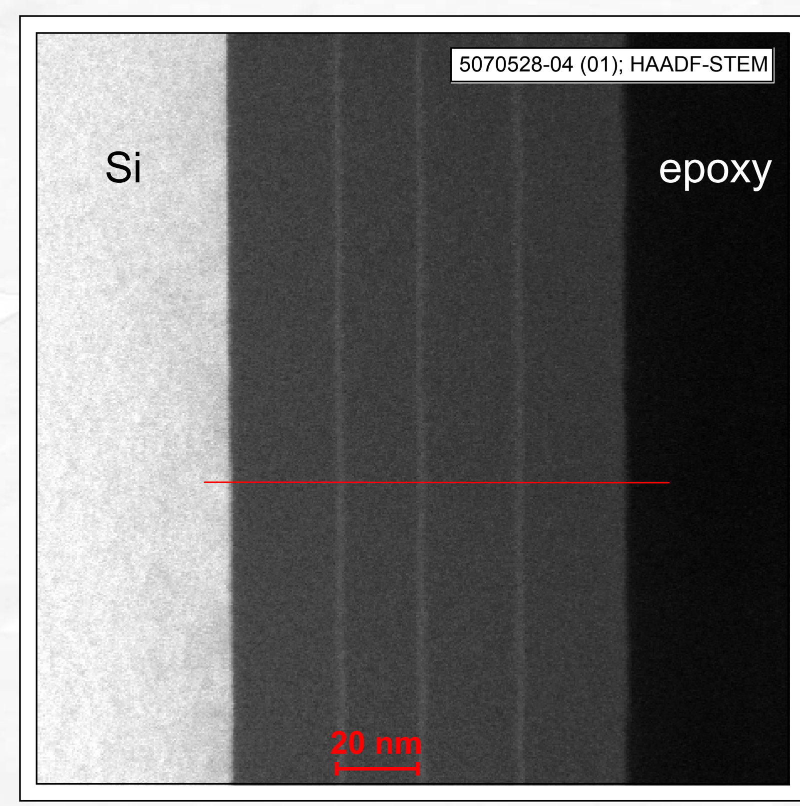
Example of Need for Multiple Methods Low K Stack (STEM-EELS)



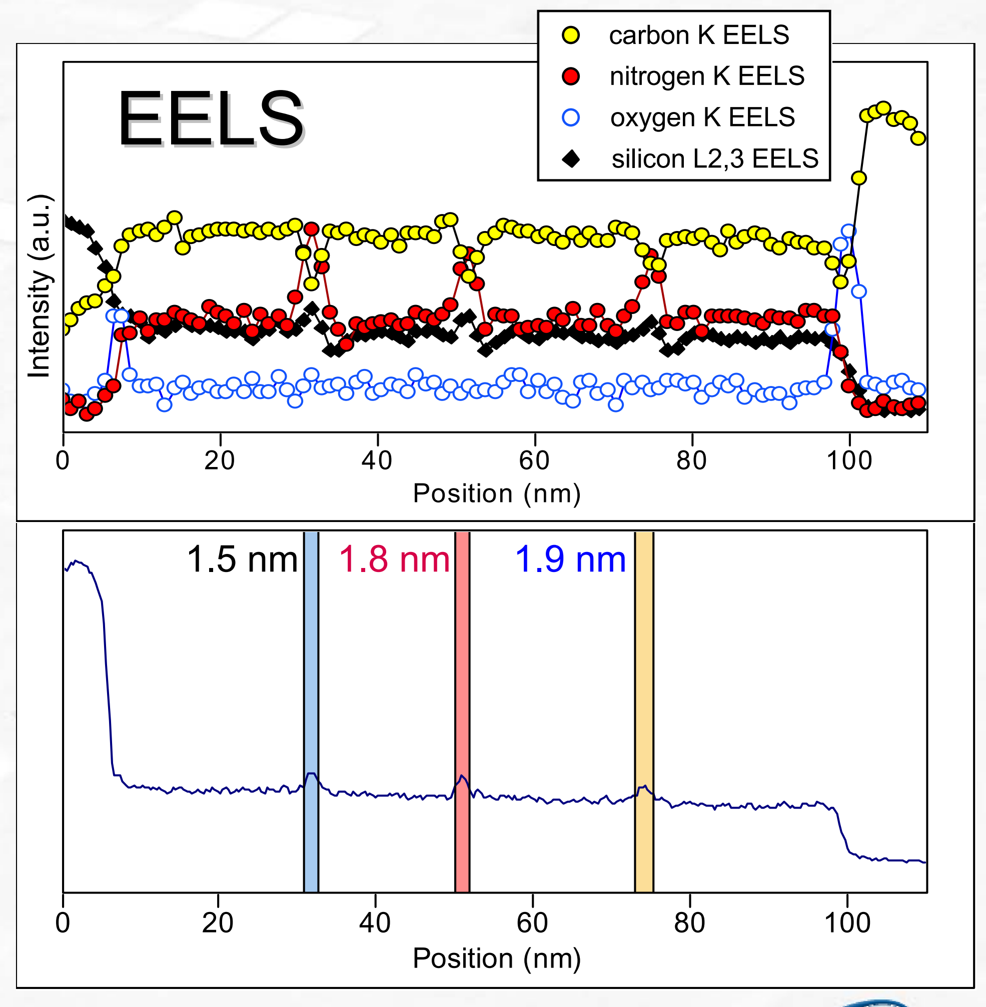


Image Intensity

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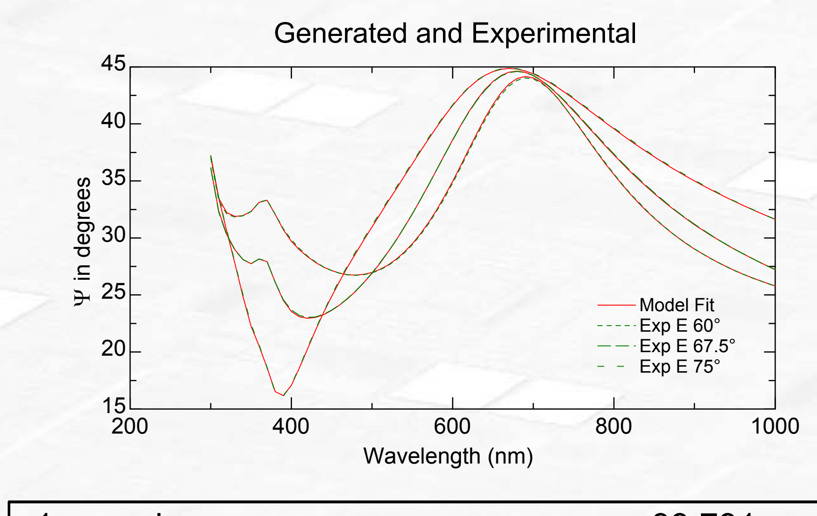
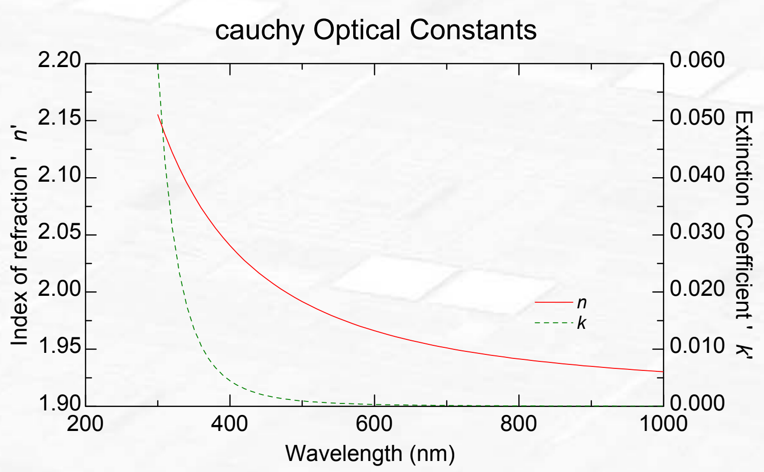
Optical Metrology
SE analysis: Single Layer Model





1	cauchy	99.791 nm
0	si_jaw	1 mm

n @ 630 nm = 1.9609

Unable to detect interfaces

Still Method of Choice for Manufacturing due to small Spot size

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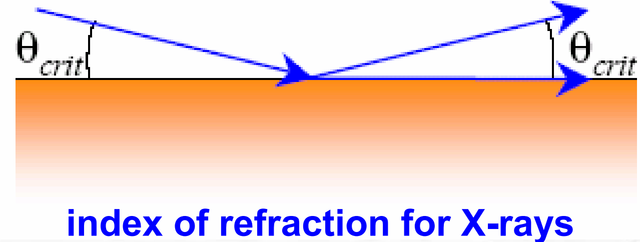
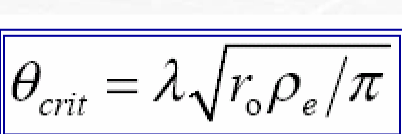
Bulk X-ray Reflectivity

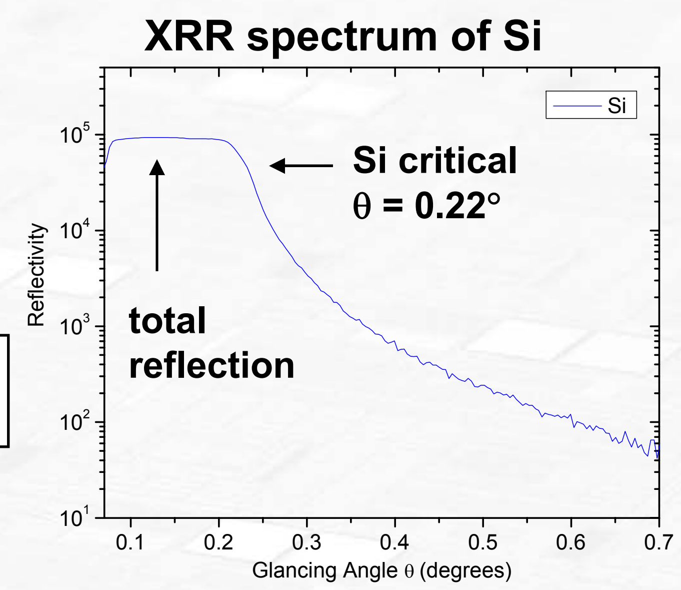


Si
D= 2.33 g/cm³

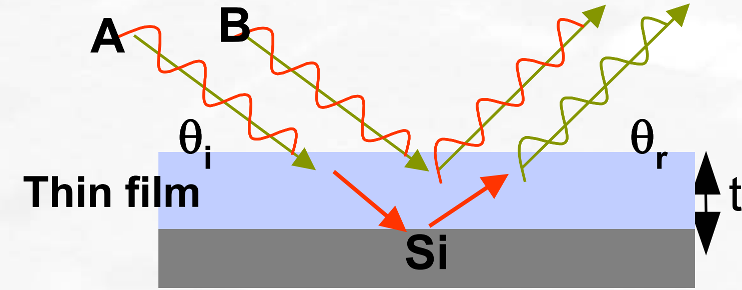


$$\theta_{crit} = \lambda\sqrt{r_o \rho_e / \pi}$$

λ = X-ray wavelength= 1.5406 A
r_o = classical electron radius=2.8×10^{-15} m
ρ_e = electron density



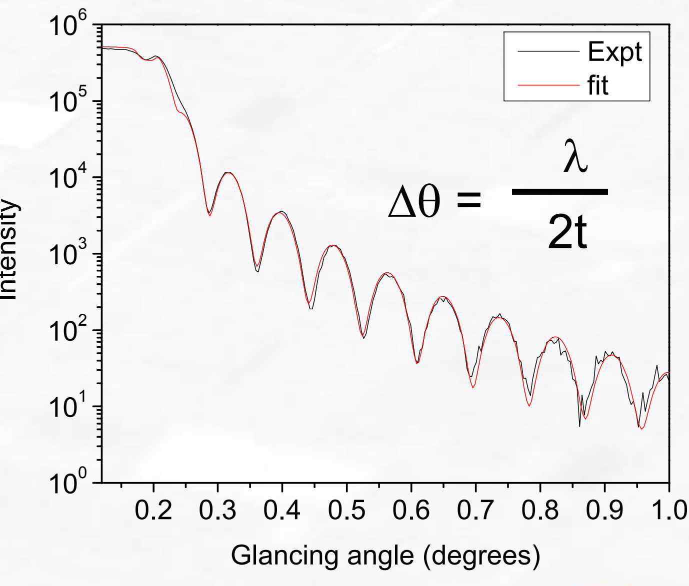
Thin film Thickness & Density



Bragg equation

$$2t\sin\theta = n\lambda$$

$$\lambda = 1.5406 \text{ A}$$

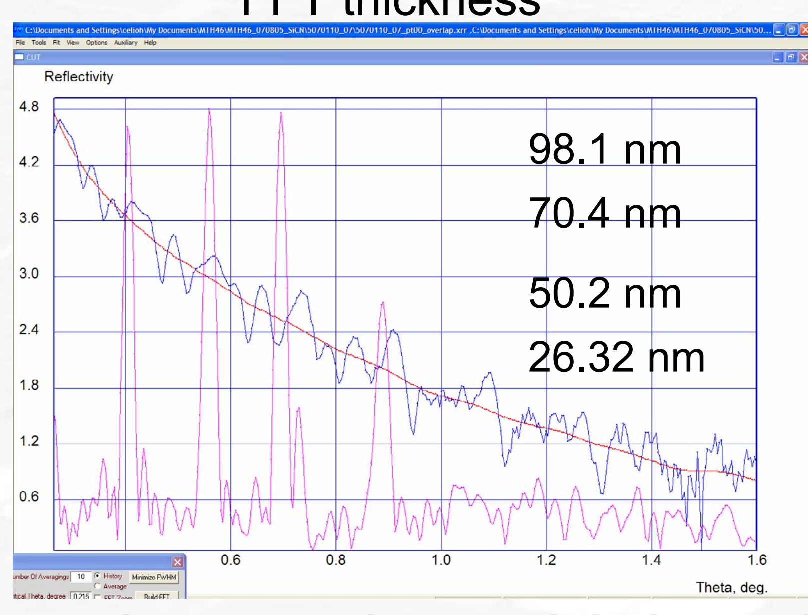


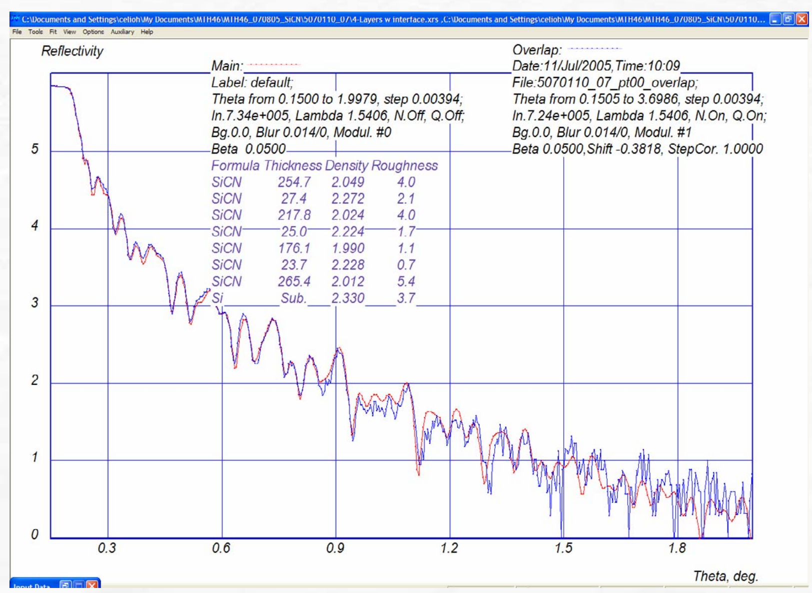
XRR analysis: multi-layer and interfaces

Total thickness

- XRR Thickness =99.0 nm and SE Thickness= 99.8 nm
- XRR shows **three interfaces**

FFT thickness





Three Layers have higher density

	Formular		Thickness (A)		Density (g/cm3)		Roughness (A)
Layer#1	:SiCN;		254.7		2.049		4
Layer#2	:SiCN;		27.4		2.272		2.1
Layer#3	:SiCN;		217.8		2.024		4
Layer#4	:SiCN;		25		2.224		1.7
Layer#5	:SiCN;		176.1		1.99		1.1
Layer#6	:SiCN;		23.7		2.228		0.7
Layer#7	:SiCN;		265.4		2.012		5.4
Layer#8	:Si;		: -1.0;		2.33		3.7

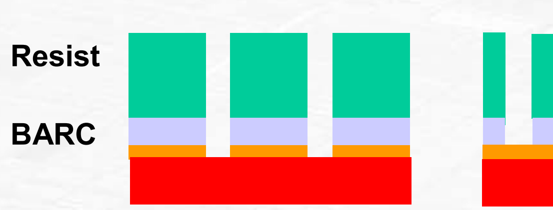
AGENDA

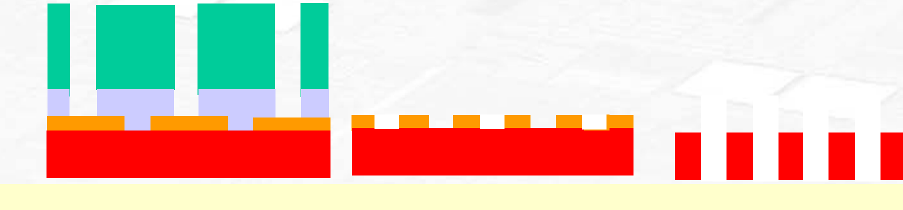
- Evolution of Micro to Nanoelectronics
- Transistor (FEP) Metrology Challenges
- Interconnect Metrology
- Patterning Metrology
- Trends & Conclusions

Lithography Technology

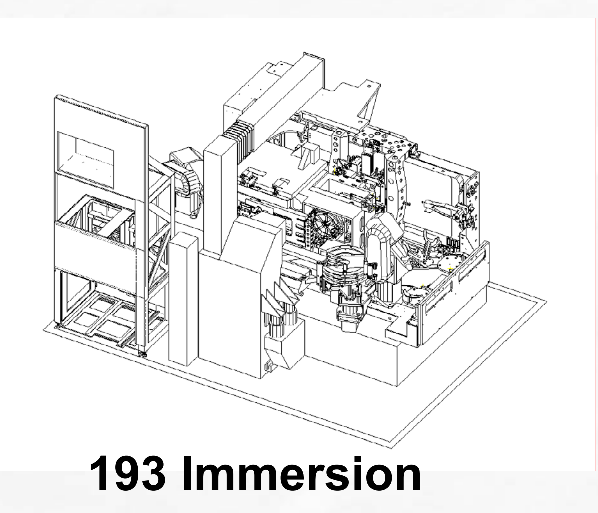
ITRS Manf. beta 1/2 Pitch	2010 2006 45 nm	2013 2009 32 nm	2016 2012 22 nm	2019 2015 16 nm
	193 nm Immersion	193 Immersion EUV?	193 Immersion EUV?	EUV

Exposure 2 Etch 2 Etch 2

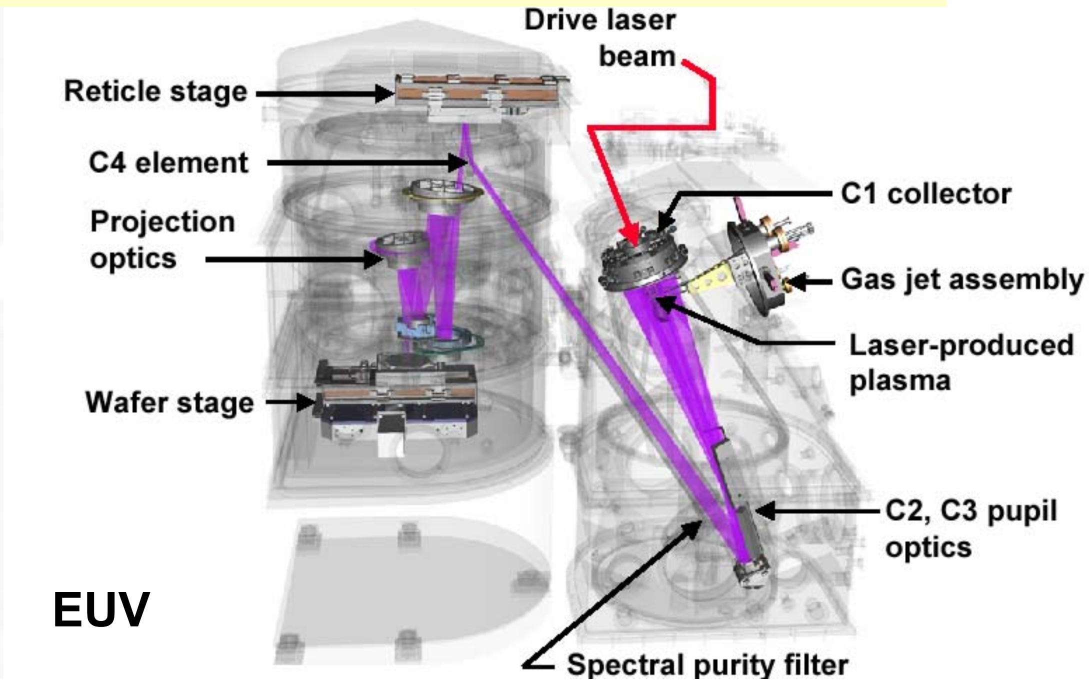




Near Term Dual Patterning & Immersion 193

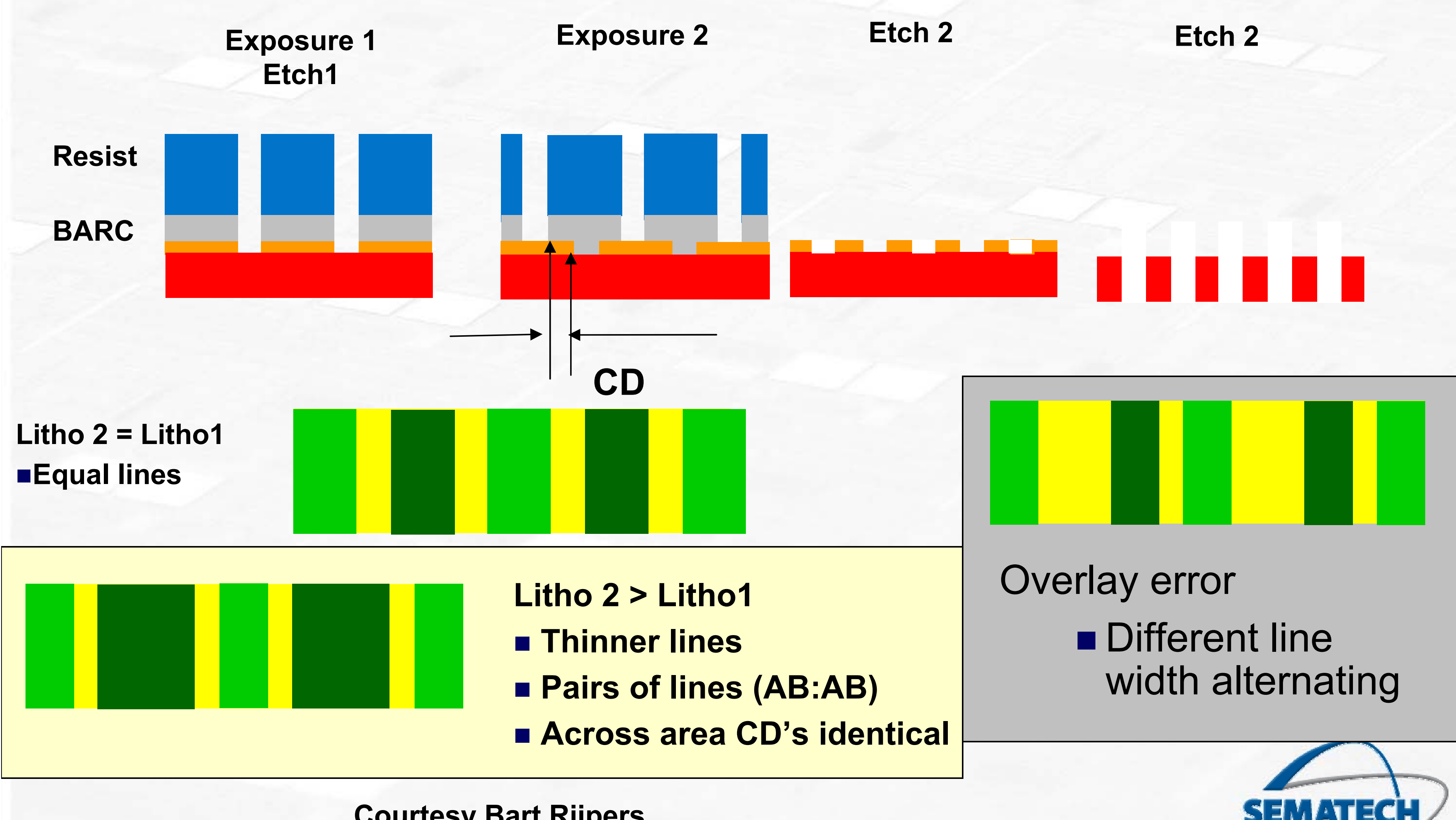


193 Immersion



EUV

Dual patterning for contacts (two exposures with etch steps) overlay control



Overlay Metrology Requirements

- $OL = \sqrt{(OL1)^2 + (OL2)^2}$
- OL = 70% single exposure OL

Courtesy Bart Rijpers

Low Energy SEM for CD Measurements

Sec
El
D

Sc

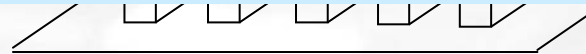
waf

CD-SEM is Extendable to 32 nm Node

Thanks to David Joy

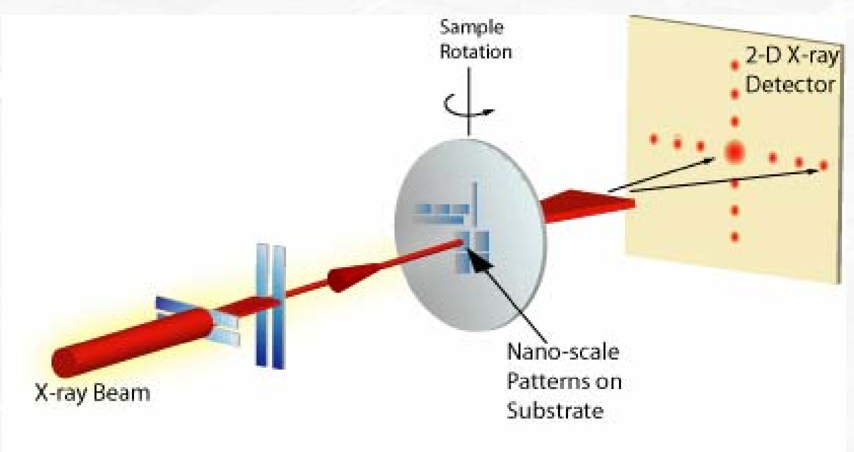
Scatterometry for CD Measurements

Scatterometry is Extendable to 32 nm Node



Potential New CD Methods also apply To Other Areas & Beyond CMOS

CD-SAXS



Win – Li Wu NIST

He Ion Microscope
New Imaging Physics

Alis Corp. (part of Zeiss)

CD Control Range – will it be relaxed?

- Vt behavior already dominates gate length for circuit performance and functionality
- Performance fluctuations due to CD will be dominated by leakage power and not by gate delay/speed
  - Frequency range of 30-35% == leakage spread of 20X
  - Borkar (Intel), 2002
- Ongoing ITRS Design TWG Discussion

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Conclusions

- ***CMOS Extension and Beyond CMOS both Require Characterization and Metrology at the NanoScale***
- **Interfacial Measurement is Increasing in Difficulty & Importance**
- **Sidewall Control will become more important**
- **New Problems often require New Methods such as Optical Second Harmonic Generation**
- **Dimensional Confinement and Surface State Effects must be included in Optical Modeling**

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- Christian Kisielowski, Dave Muller, and Steve Pennycook
- Peter Zeitzoff

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