Metrology Requirements and the Limits of Measurement Technology for the Semiconductor Industry

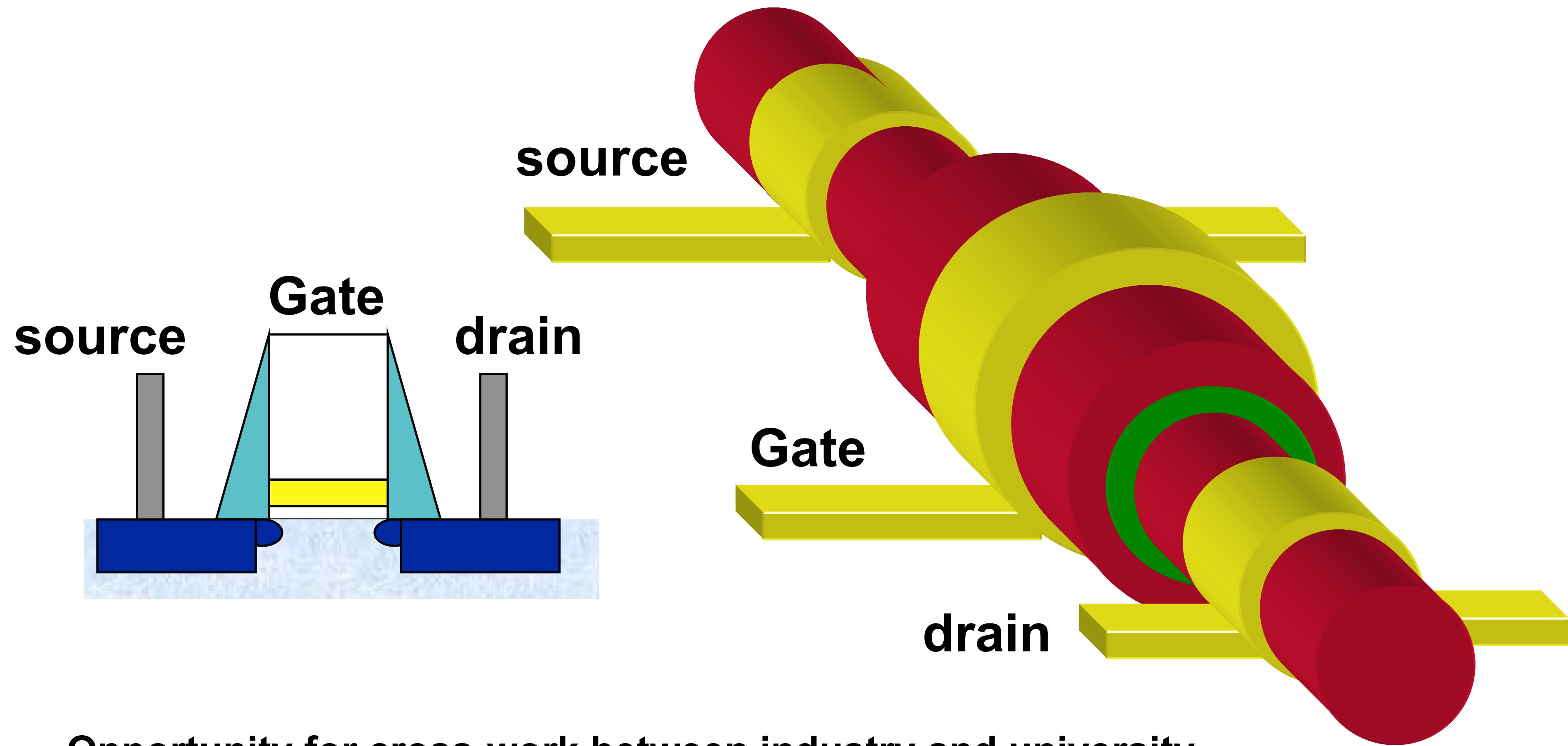
Based on the

International Technology Roadmap for Semiconductors

Alain C. Diebold

INTERNATIONAL SEMATECH

Measurements Today
Atomic Dimensions
Nanowire Transistor & Interconnection



Opportunity for cross-work between industry and university

AGENDA

- The ITRS Challenge
- Litho Metrology
- FEP Metrology
- Interconnect Metrology
- Materials Characterization

ITRS Challenge

	2001	2002	2004	2007	2010	2013	2016
Leading Production Technology Node = DRAM ½ Pitch	*130 nm*	*115 nm*	*90nm*	*65 nm*	*45 nm*	*32 nm*	*22 nm*
MPU / ASIC ½ Pitch (nm)	150	130	90	65	45	32	22
MPU Printed Gate Length (nm)	90	75	53	35	25	18	13
MPU Physical Gate Length (nm)	65	53	37	25	18	13	9

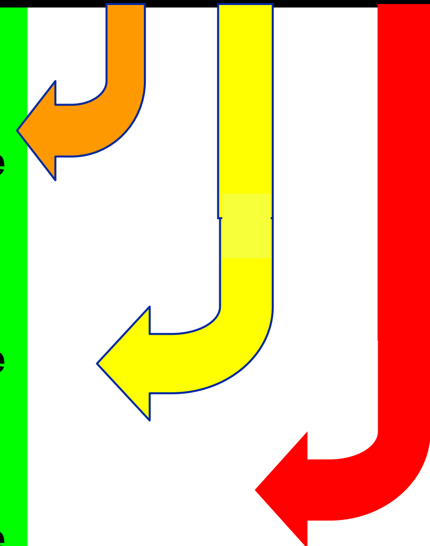
Leading Edge Tool Specifications set

45 nm Node Metrology R&D Materials available
10 nm structures difficult to obtain

Beta Site
90 nm Node

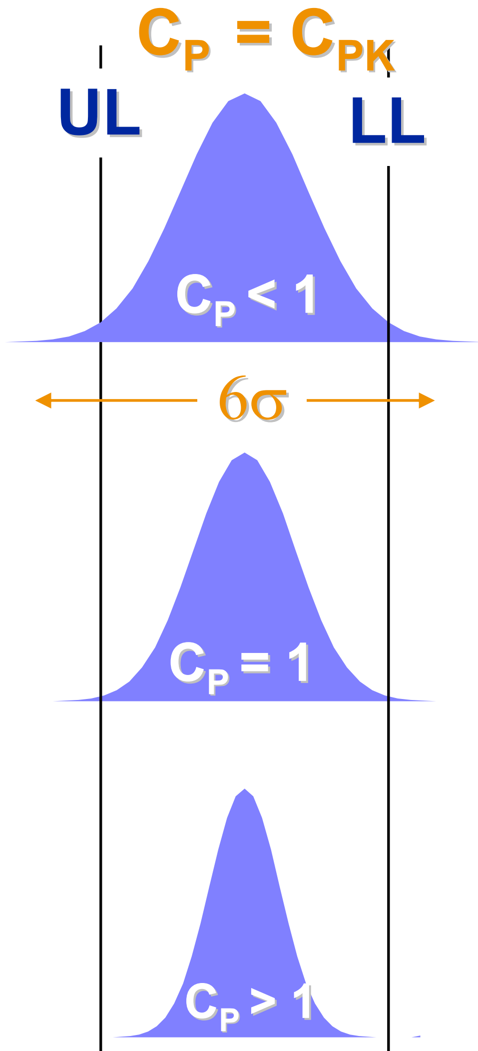
R&D
65 nm Node

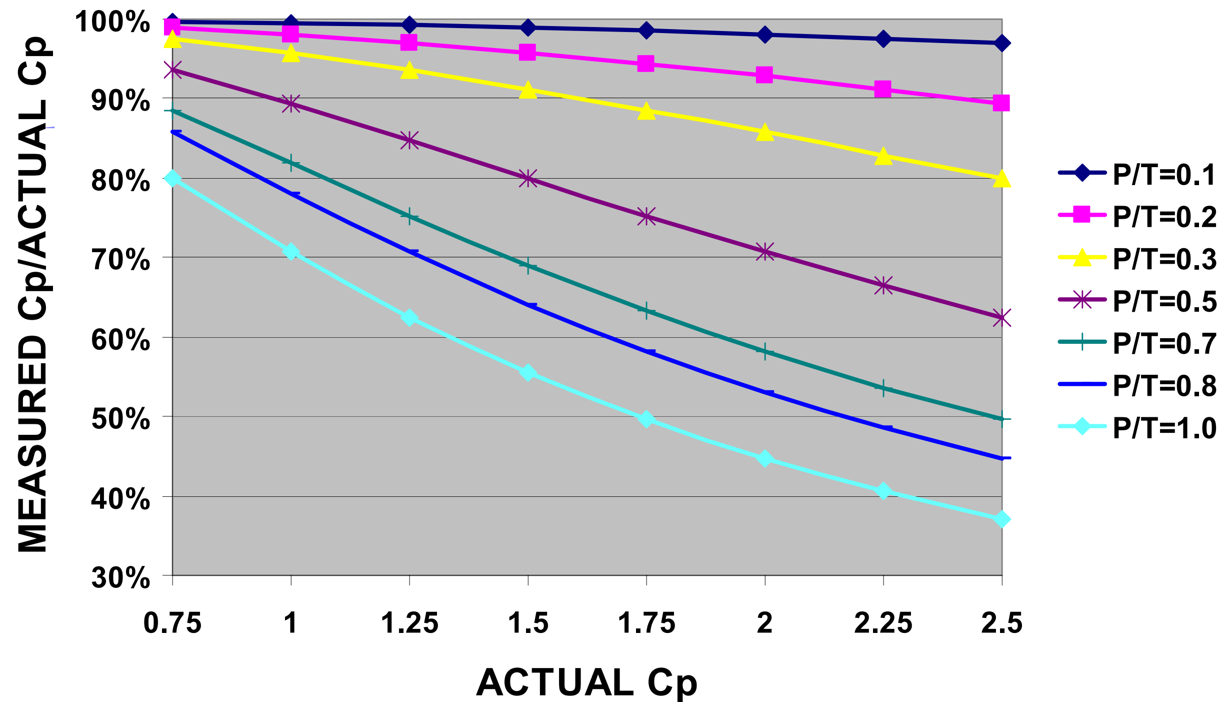
Early R&D
45 nm Node



INTERNATIONAL SEMATECH

Process control
Is based on Statistical Significance

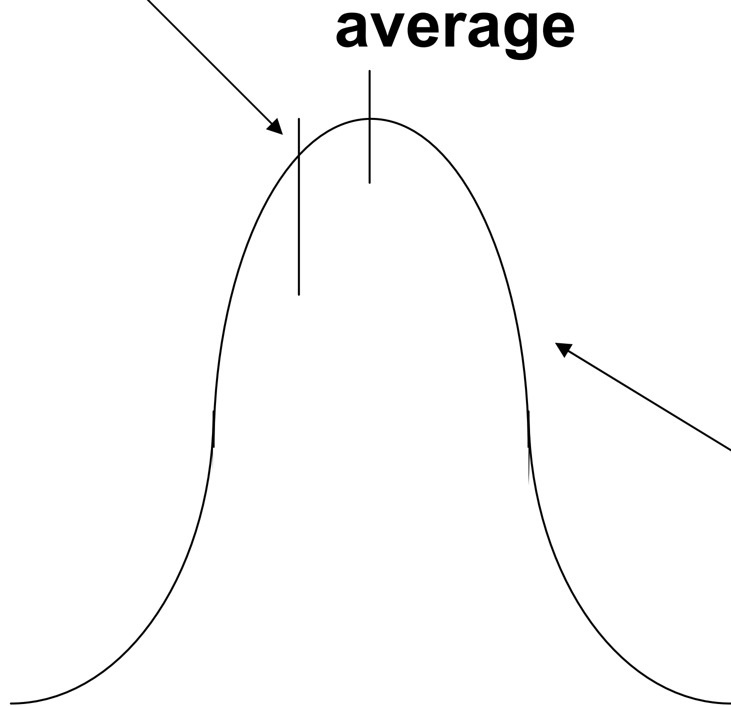




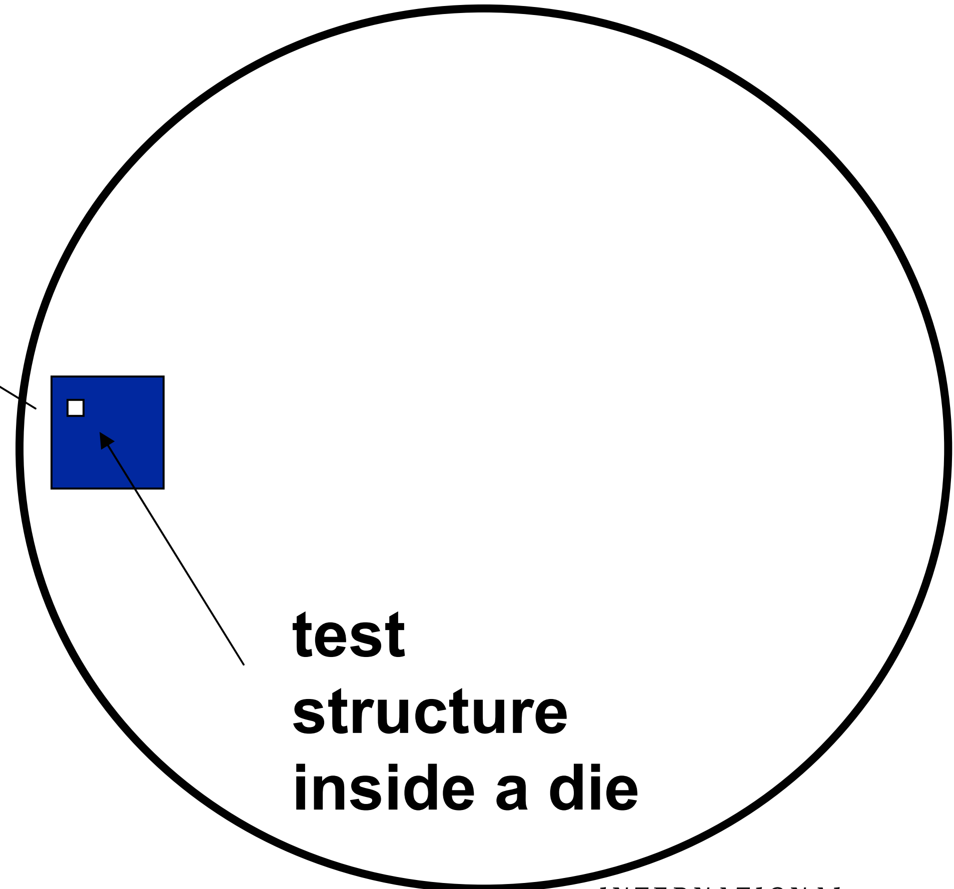
If Distribution is Centered

What are you Measuring?

single value from distribution

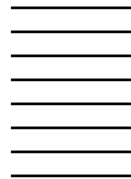


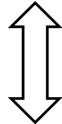
Distribution of linewidths inside test structure



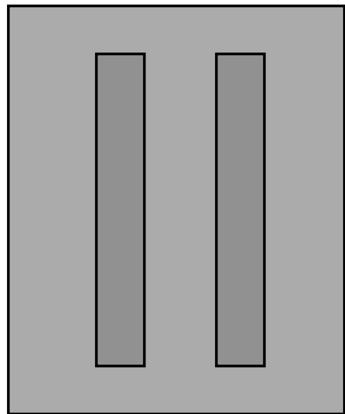
One Aspect of the Solution:
Average over large area & Amplify Signal from Microscopic Changes

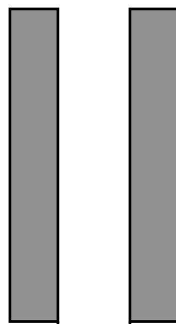
e.g.
150 nm lines
300 nm pitch

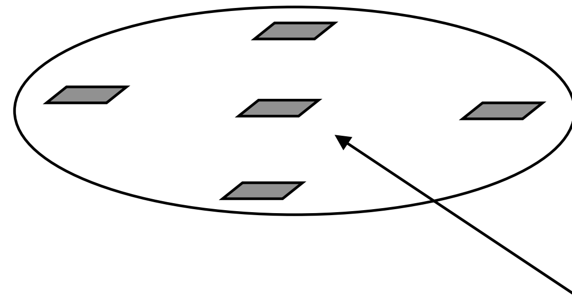




Optical CD using Overlay System







Rapid Sampling of test structures

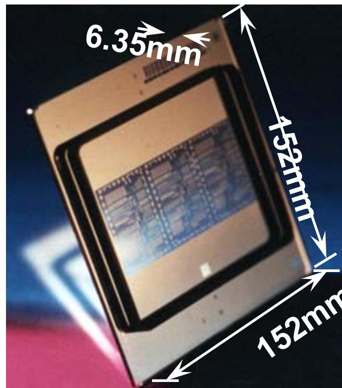
AGENDA

- How to control microscopic features
- Litho Metrology
- FEP Metrology
- Interconnect Metrology
- Materials Characterization

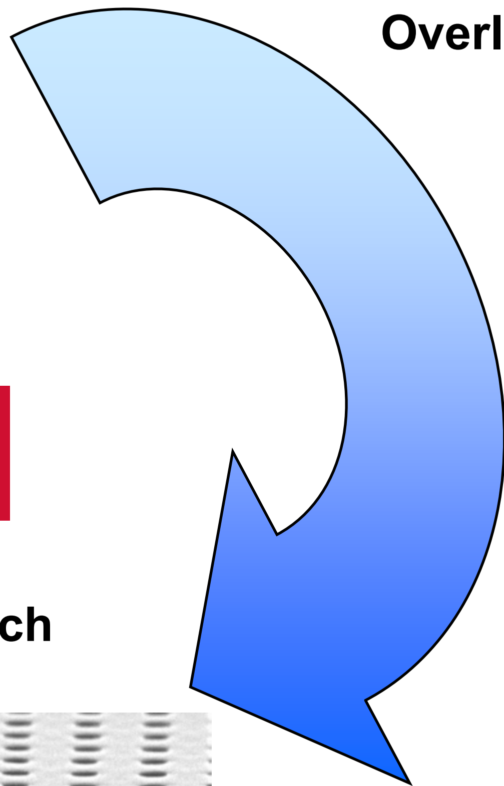
Litho Metrology

22 nm Node - 2016

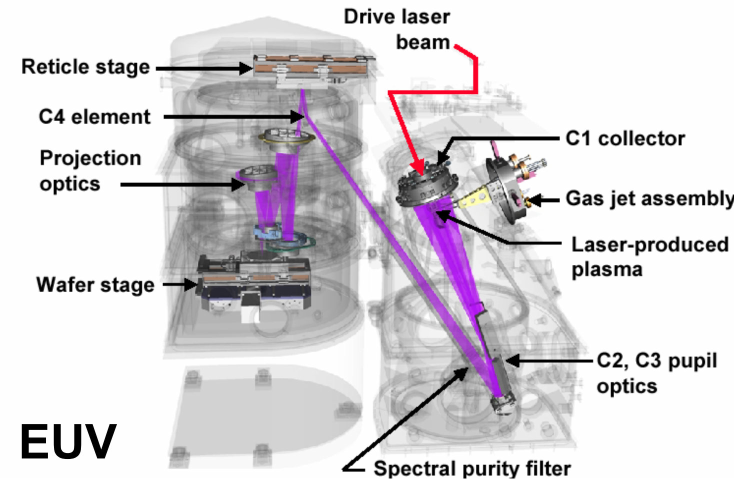
CD Control Starts at the Mask



52 nm mask line width
26 nm scattering bars

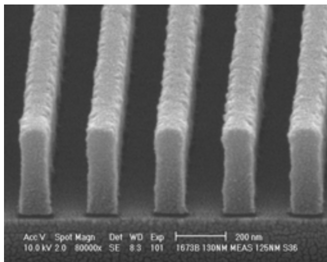


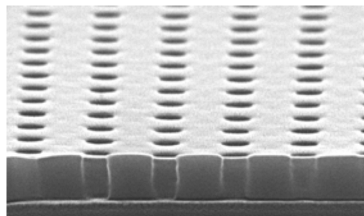
Overlay and CD Control after Exposure



13 nm printed line width

CD Control after Etch



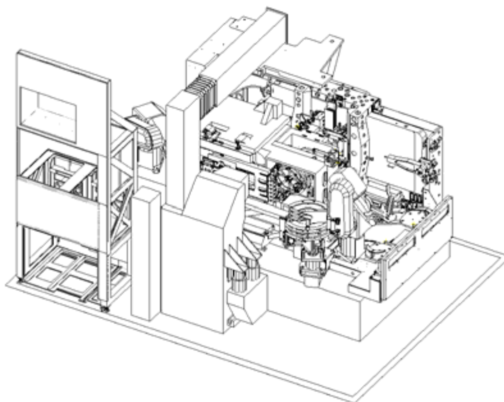


9 nm physical line width

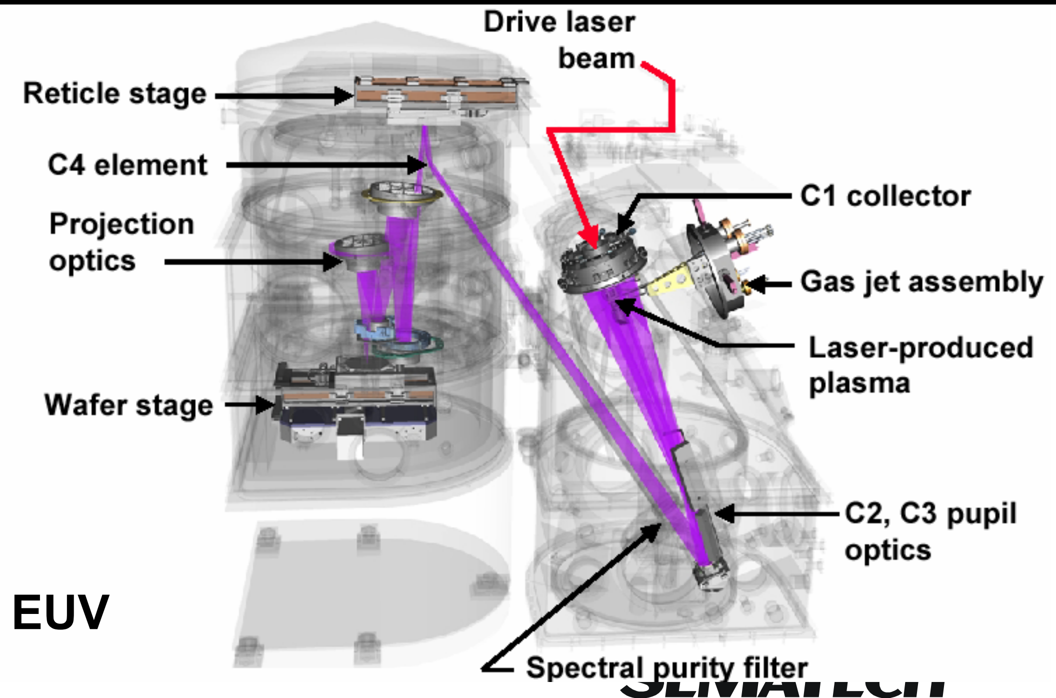
INTERNATIONAL SEMATECH

Litho Metrology

	193 nm		157 nm	EUV			
Technology Node	*130 nm*	*90nm*	*65 nm*	*45 nm*	*32 nm*	*22 nm*	*Driver*
Lithography Metrology							
Printed Gate CD Control (nm)	5.3	3	2	1.5	1.1	0.7	MPU
Wafer CD 3σ Precision P/T=0.2	1.1	0.6	0.4	0.3	0.2	0.1	MPU
Line Edge Roughness (nm)	4.5	2.7	1.8	1.3	0.9	0.65	MPU
Precision for LER	0.9	0.54	0.36	0.26	0.18	0.13	

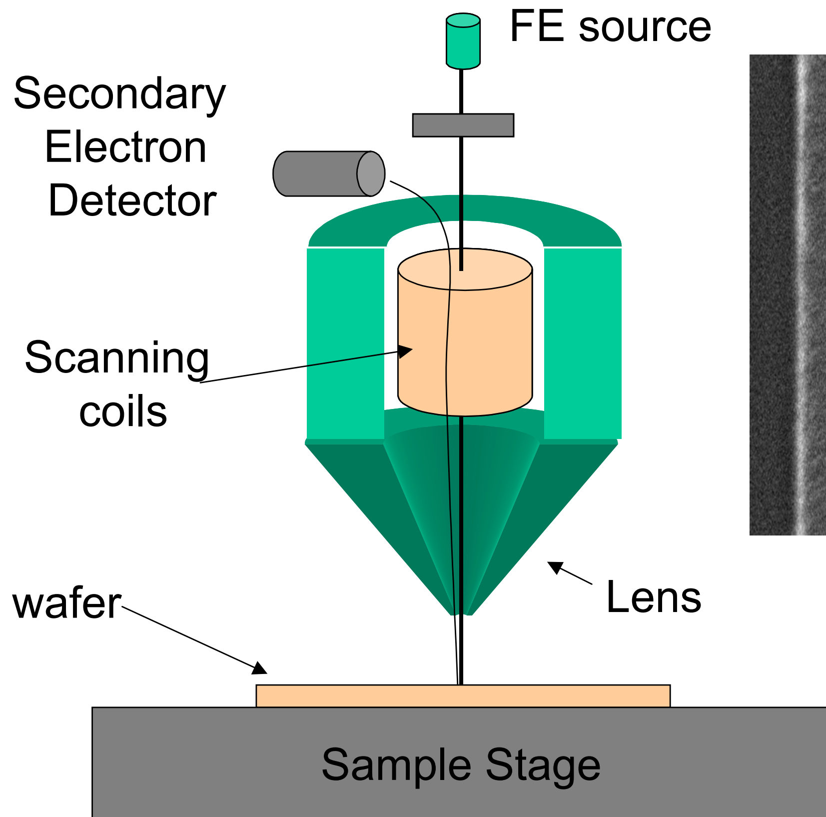


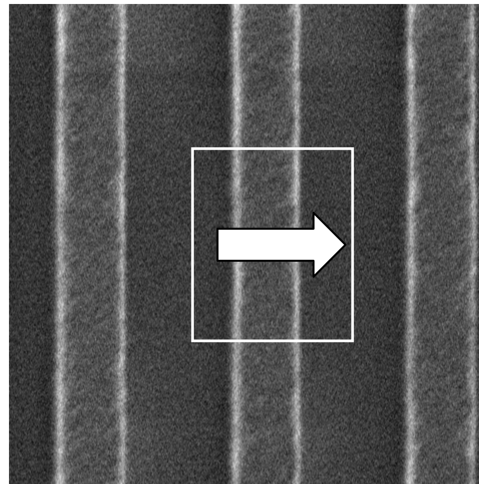
193 and 157 nm

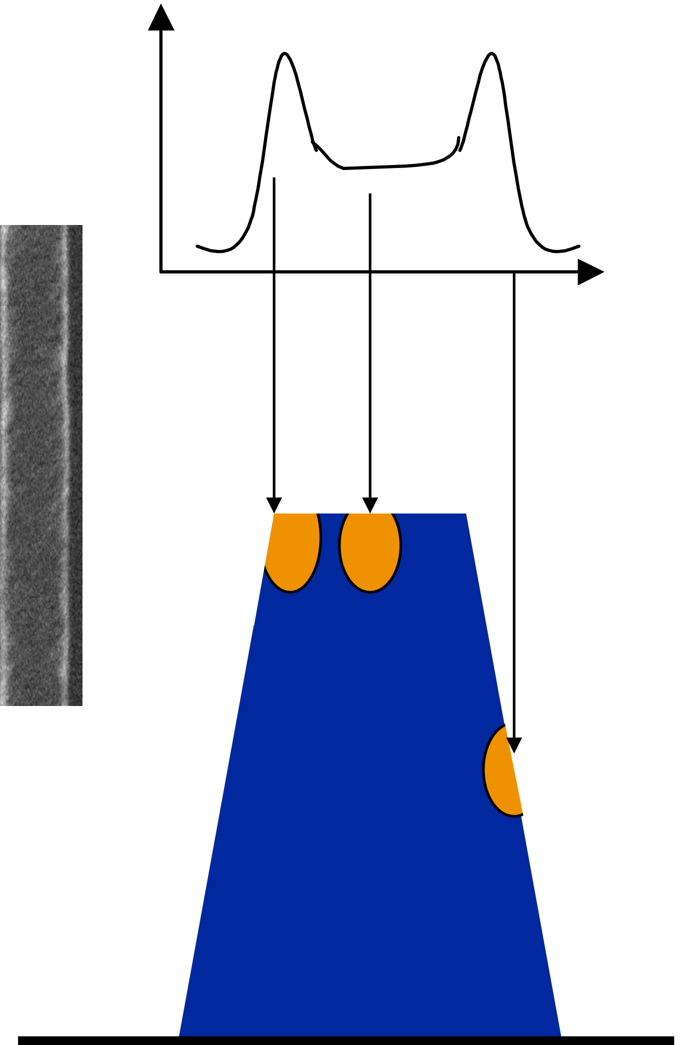


EUV

Low Energy SEM for CD Measurements



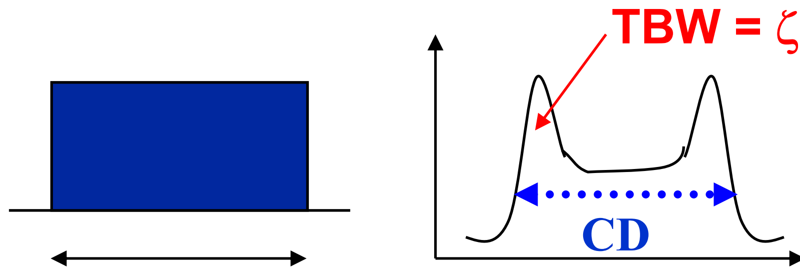




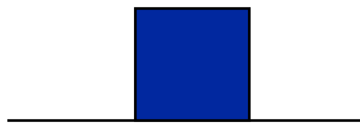
Thanks to David Joy

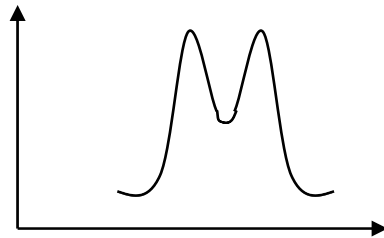
INTERNATIONAL SEMATECH

Limits of SEM for CD Measurements

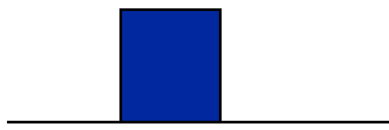


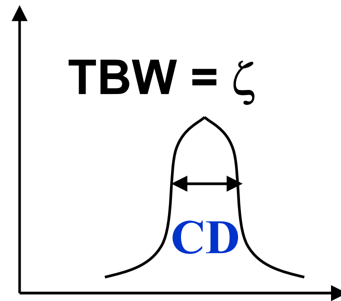
20 nm





10 nm





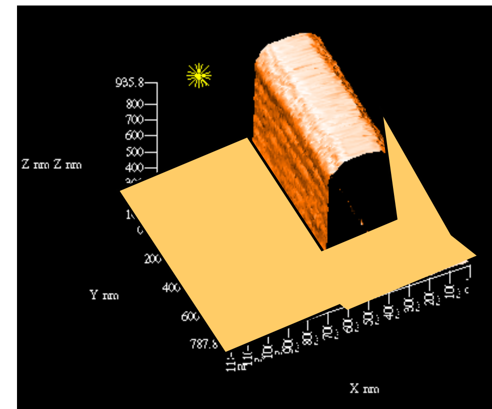
5 nm

Gabor's limit

Thanks to David Joy

Loss of Depth of Field

DoF = (resolution)/(convergence angle)



INTERNATIONAL SEMATECH

Challenges: Round Top Resist & LER

Line Edge Roughness Requires Better Dimensional Precision

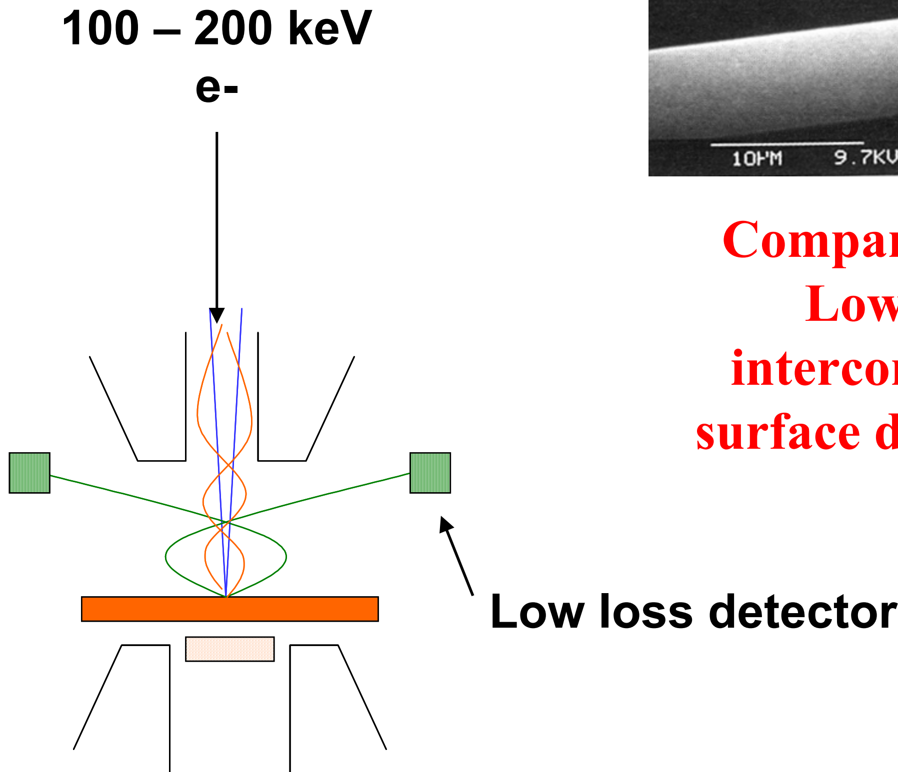
Issue facing 50 nm lines from 130 µm node in 2001

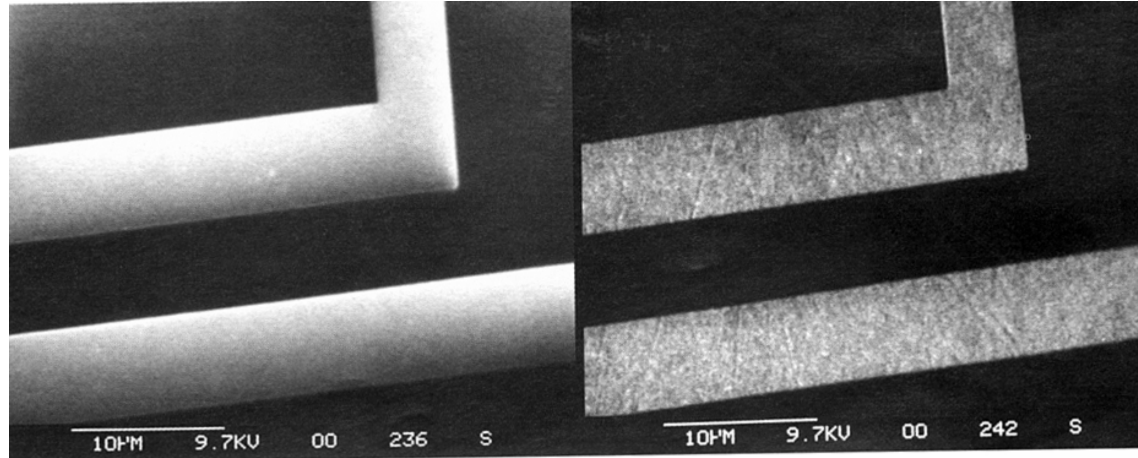
INTERNATIONAL SEMATECH

Lithography CD Metrology

Improve CD-SEM thru 65 nm node

High Voltage CD-SEM





Comparison of conventional SE (left) and Low Loss (right) images of copper interconnects. Note the greatly enhanced surface detail and lack of edge brightness in the Low Loss image.

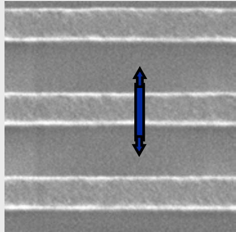
Micrograph courtesy of O C Wells

Figures from David Joy

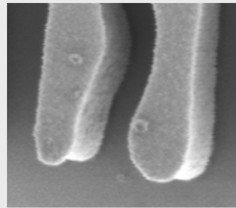
INTERNATIONAL SEMATECH

3D CD Metrology SEM – Scatterometry – CD-AFM

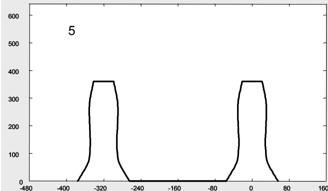
Commercially available



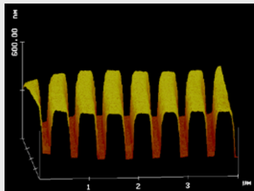
Software comparison of top down line scan of edge to golden image



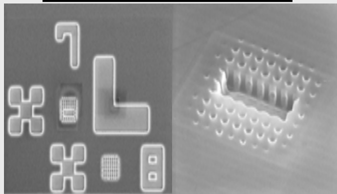
Tilt Beam SEM



Scatterometry

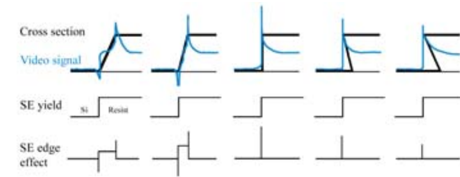


CD-AFM



Dual Beam FIB (destructive)

R&D



Software to convert top down image to 3D image

INTERNATIONAL SEMATECH

Scatterometry for CD Measurements

Mirror

$\Theta_{in} = \Theta_{out}$

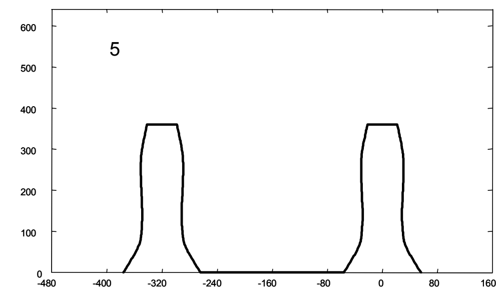
Multi-wavelength
Light Source

Polarization
Sensitive
Detector

Incident Polarized
White Light

0th order

Real Time Calculation of line width & shape Eliminates Libraries



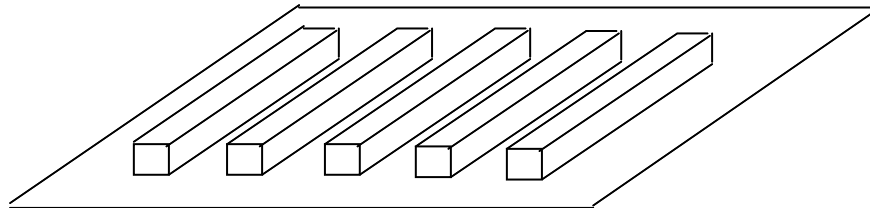
INTERNATIONAL
SEMATECH

CD-AFM Limited by Probe Tip

Carbon Nanotube Probe tips

Average vs Individual

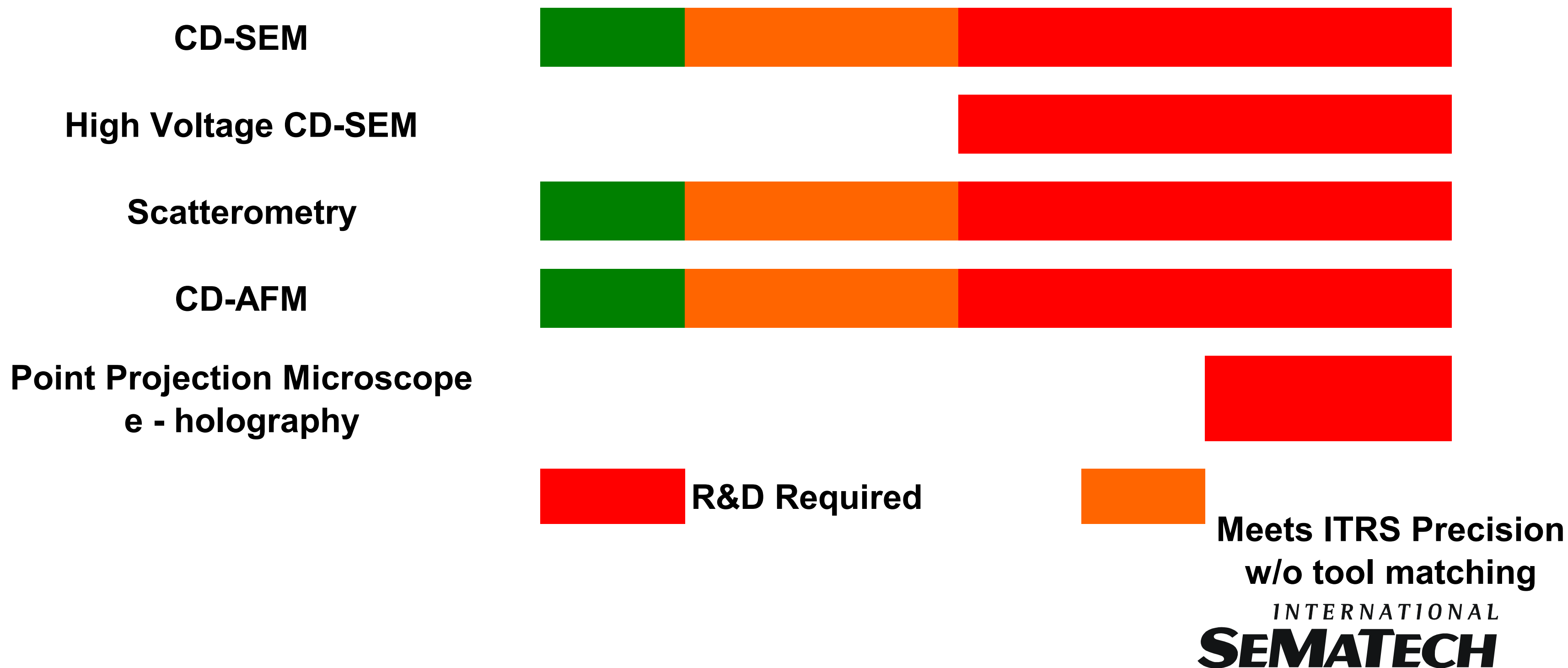
- CD-SEM measures one line at a time
- Scatterometry gives an average over many lines
- Reports indicate a large number (80 different lines) CD-SEM measurements in test area required to match scatterometry average
- Lose individual line information



INTERNATIONAL SEMATECH

Hi-thruput CD Potential Solutions

	2001	2002	2004	2007	2010	2013	2016	
Leading Production Technology Node = DRAM ½ Pitch	*130 nm*	*115 nm*	*90nm*	*65 nm*	*45 nm*	*32 nm*	*22 nm*	*Driver*
MPU / ASIC ½ Pitch (nm)	150	130	90	65	45	32	22	
MPU Printed Gate Length (nm)	90	75	53	35	25	18	13	
MPU Physical Gate Length (nm)	65	53	37	25	18	13	9	



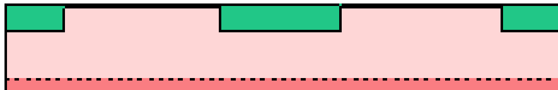
INTERNATIONAL SEMATECH

AGENDA

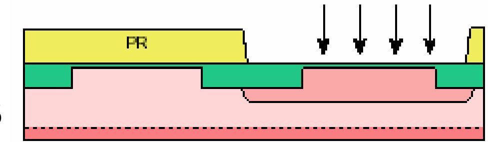
- How to control microscopic features
- Litho Metrology
- FEP Metrology
- Interconnect Metrology
- Materials Characterization

Front End Metrology

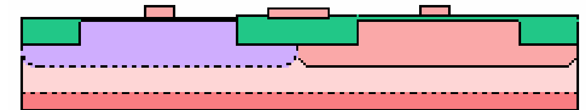
Shallow Trench Isolation



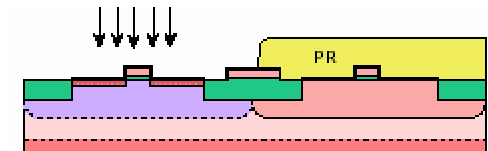
Pattern & Implant Wells

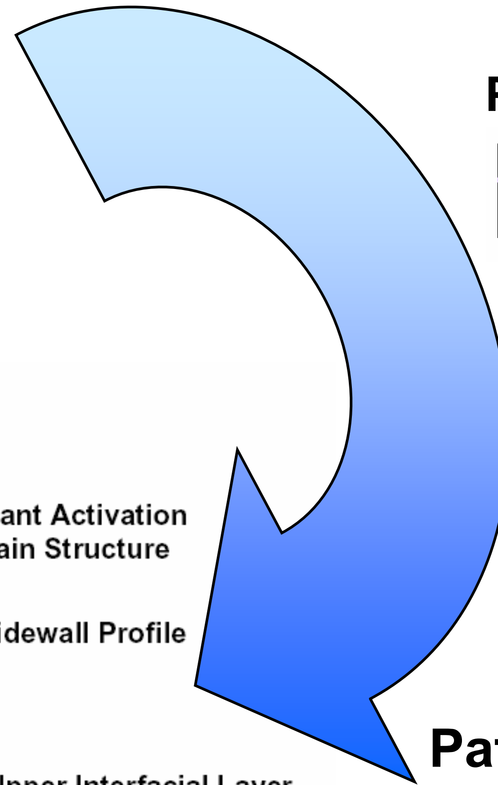


Pattern & Gate Dielectric

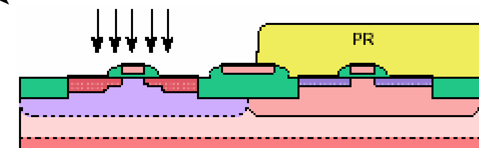


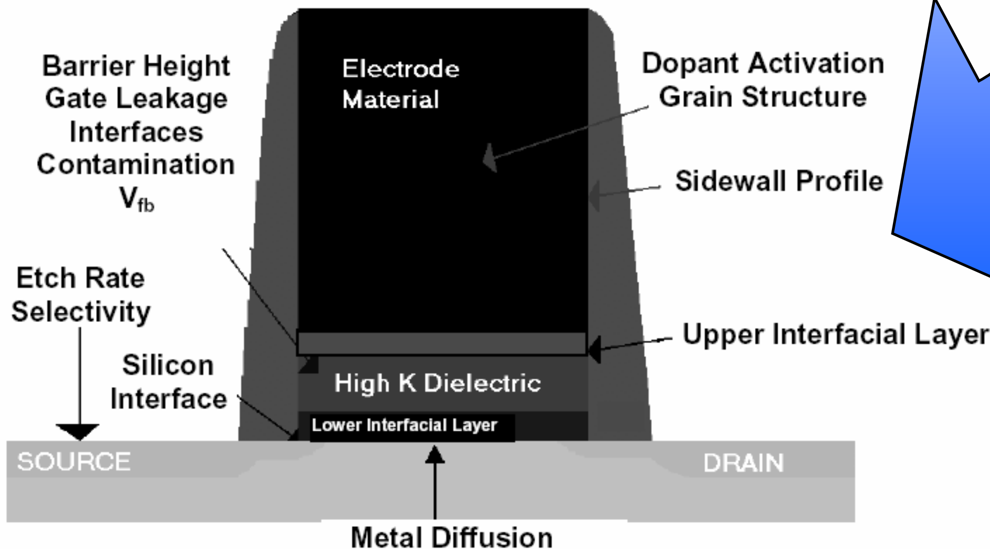
Pattern Poly/metal Implant LDD





Pattern & Implant S/D

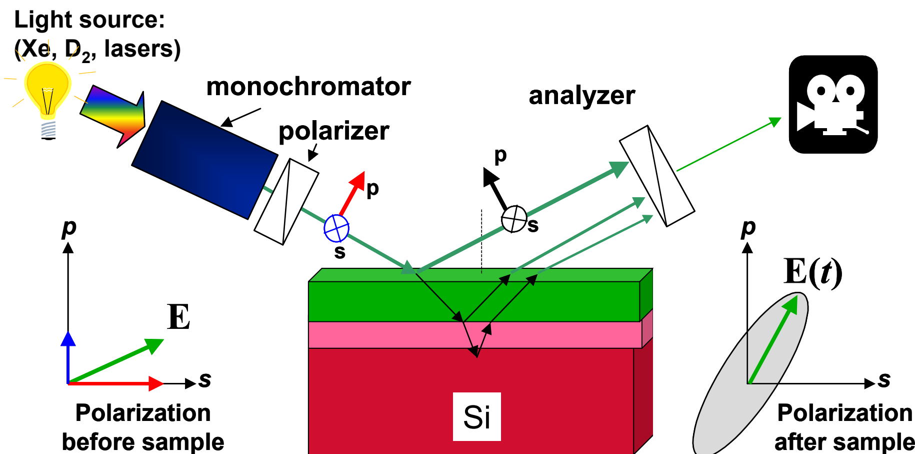




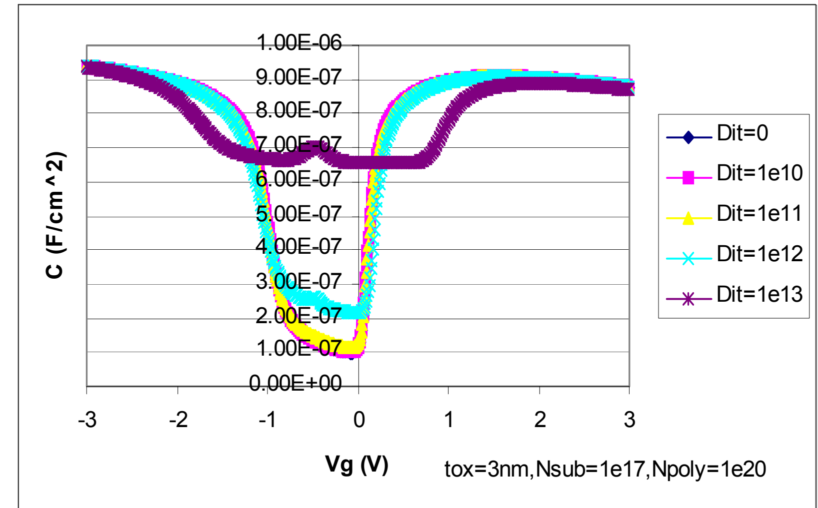
FEP : High κ Metrology

Technology Node	*130 nm*	*90nm*	*65 nm*	*45 nm*	*32 nm*	*22 nm*	*Driver*
Front End Processes Metrology							
High Performance Logic EOT equivalent oxide thickness (EOT) nm	1.3-1.6	0.9-1.4	0.6-1.1	0.5–0.8	0.4–0.6	0.4–0.5	MPU
Logic Dielectric EOT Precision 3σ (nm)	0.005	0.004	0.0024	0.0024	0.0016	0.0016	MPU
Metrology for Ultra-Shallow Junctions at Channel Xj (nm)	26	14.8	10	7.2	5.2	3.6	MPU

High κ near UV light absorption Makes thin interfacial layer difficult to measure

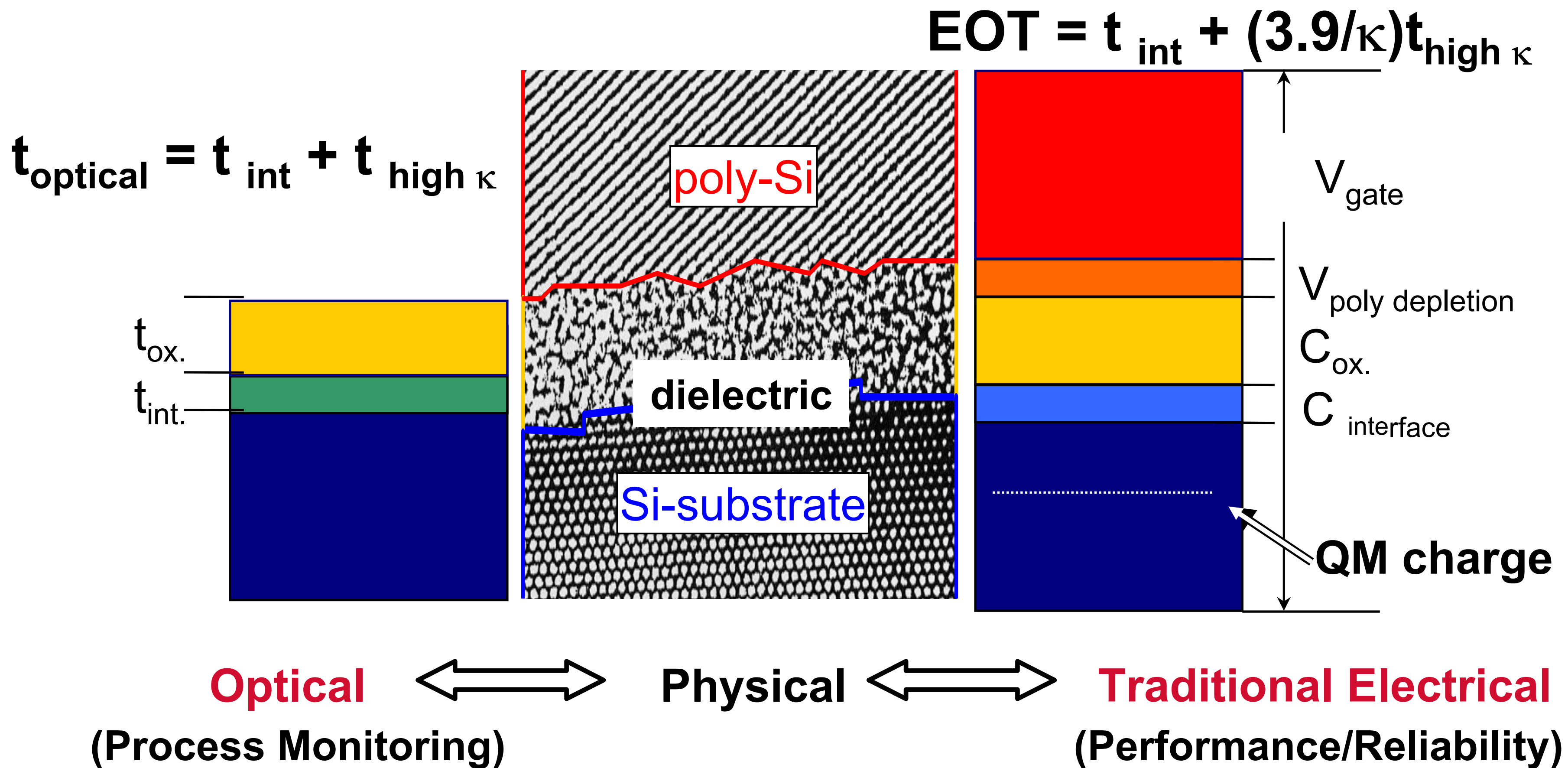


"Out of the Furnace" High D_{it} = Error in EOT



Optical/X-ray vs Electrical Measurement

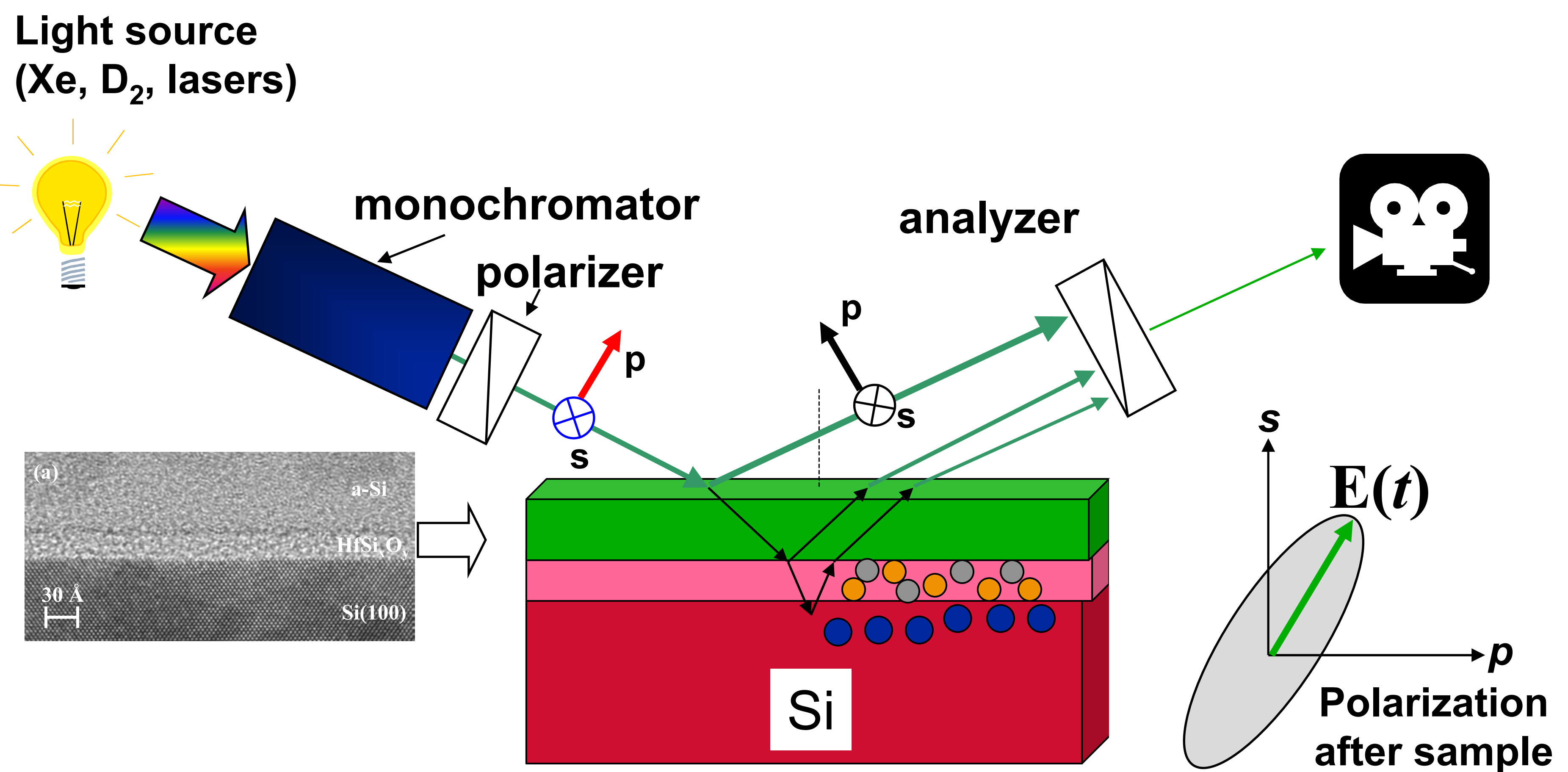
- C-V Structures receive Further Processing
- Optical thickness vs electrical EOT
- Capacitance of a very thin interface can have big effect



See also : C Richter in Char & Met for ULSI 2000

INTERNATIONAL SEMATECH

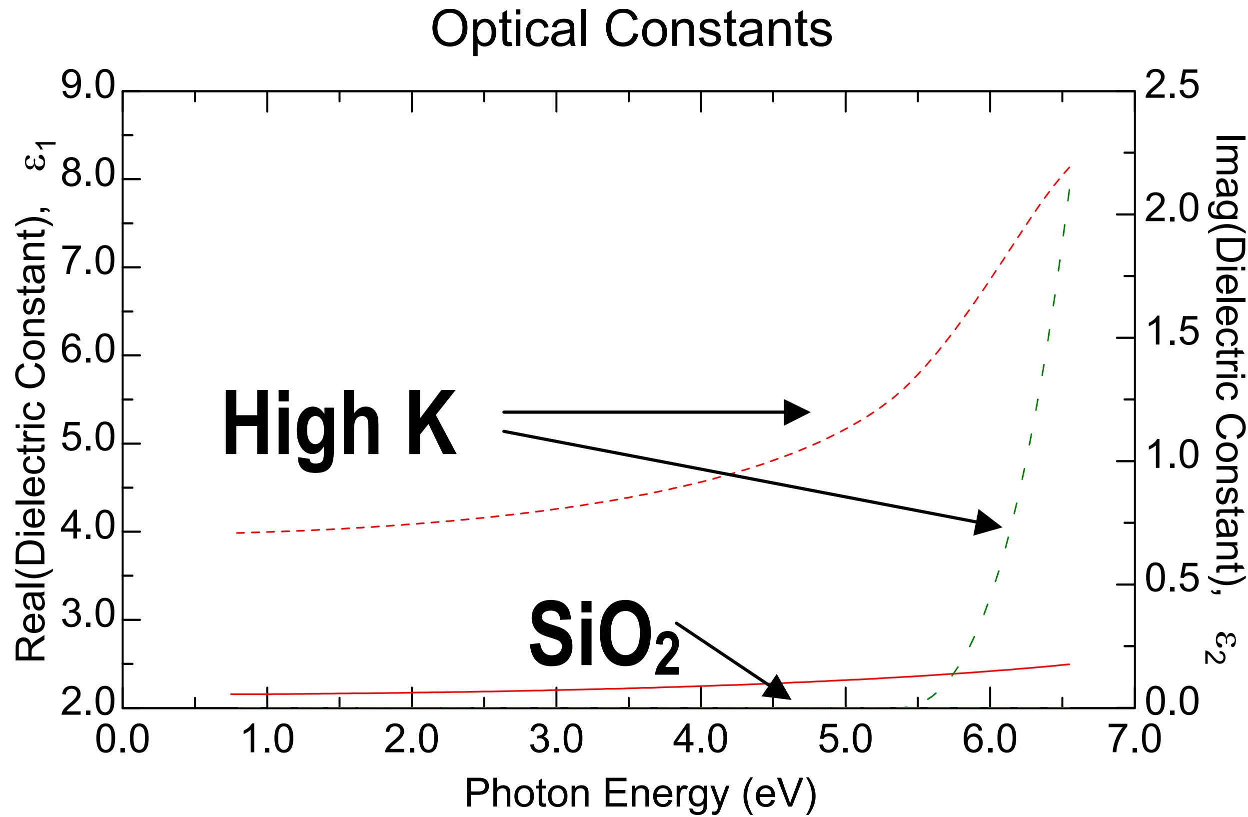
SPC requires measurement to Average Gate Dielectric over large area



2002 ALMC concensus method for TEM

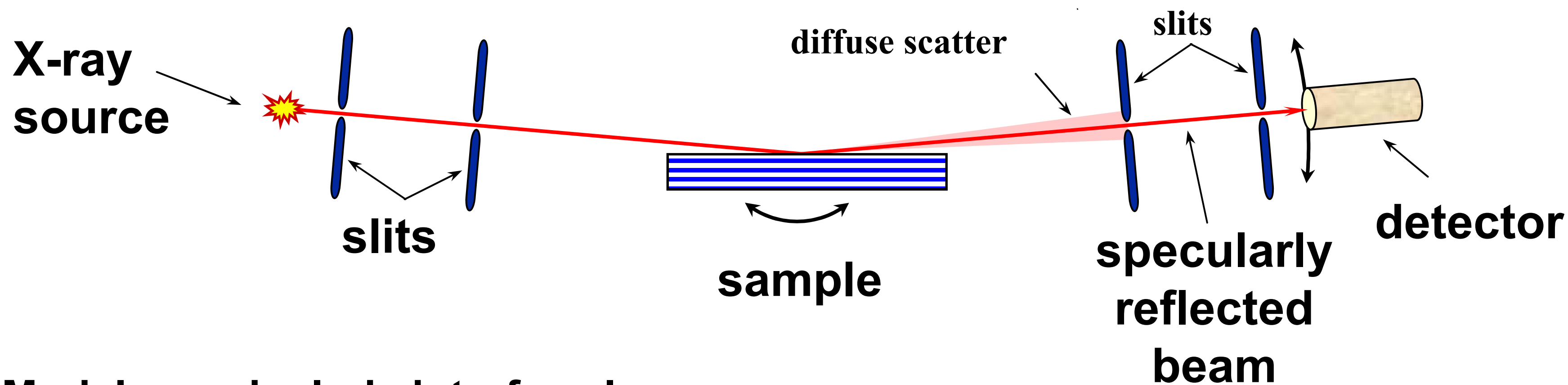
INTERNATIONAL SEMATECH

New Optical Models for higher κ

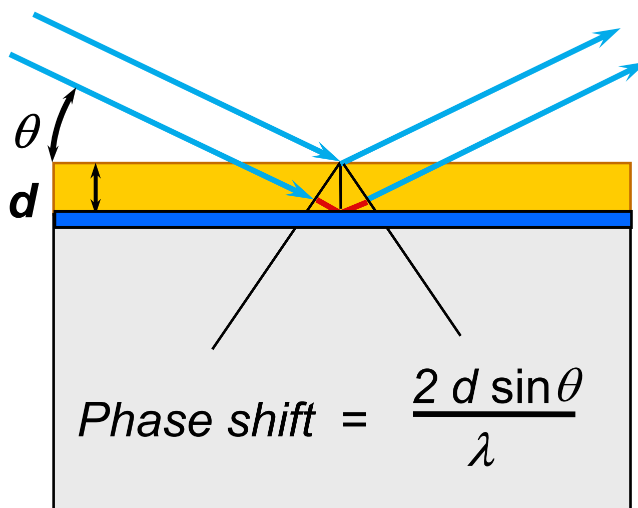


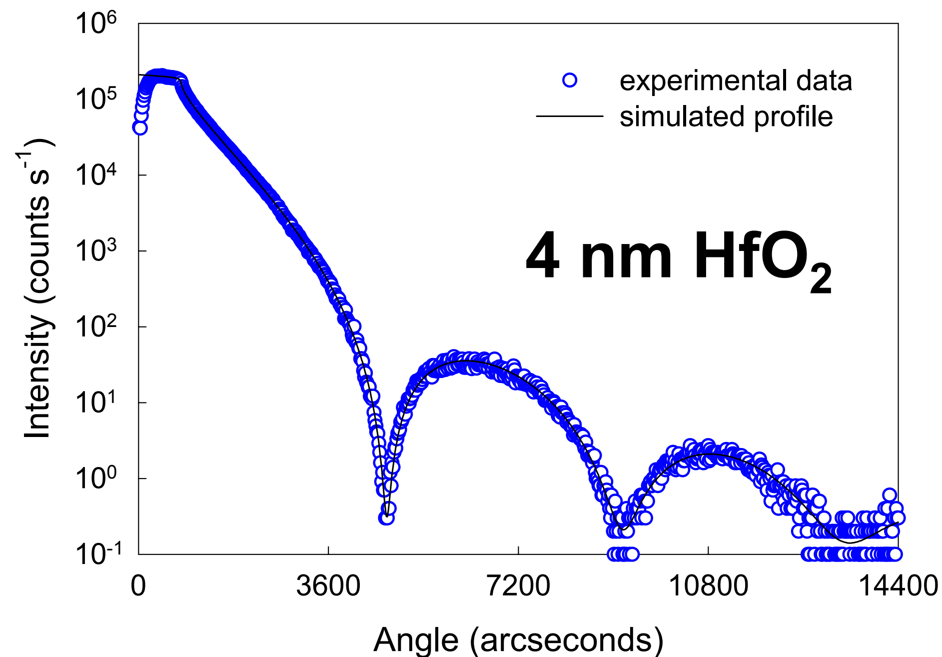
In-Line Metrology Suppliers continue to use older damped oscillator models

Simplified X-ray Path for X-ray reflectometer



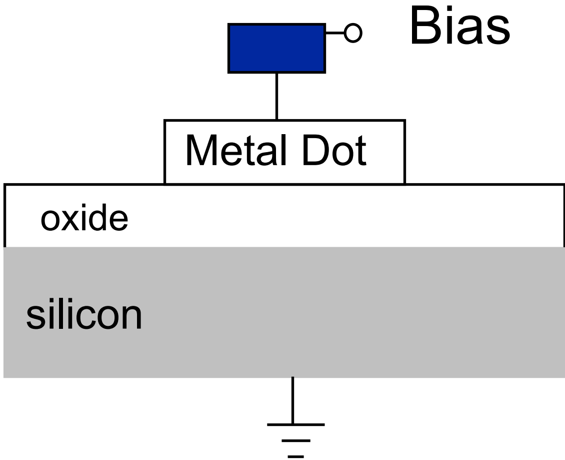
Models can include interface layer

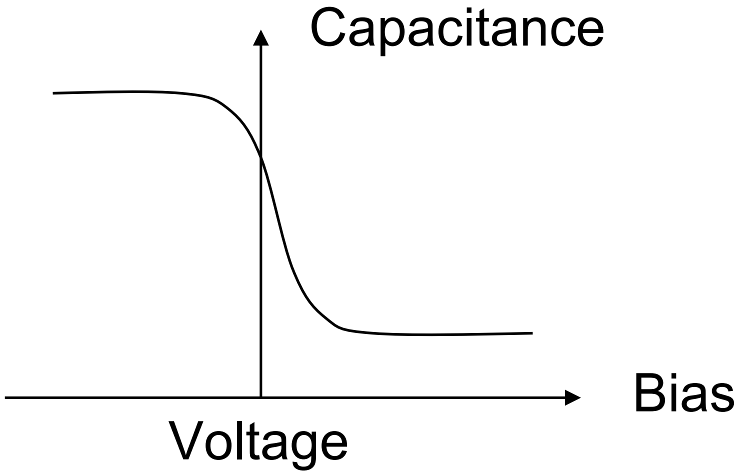


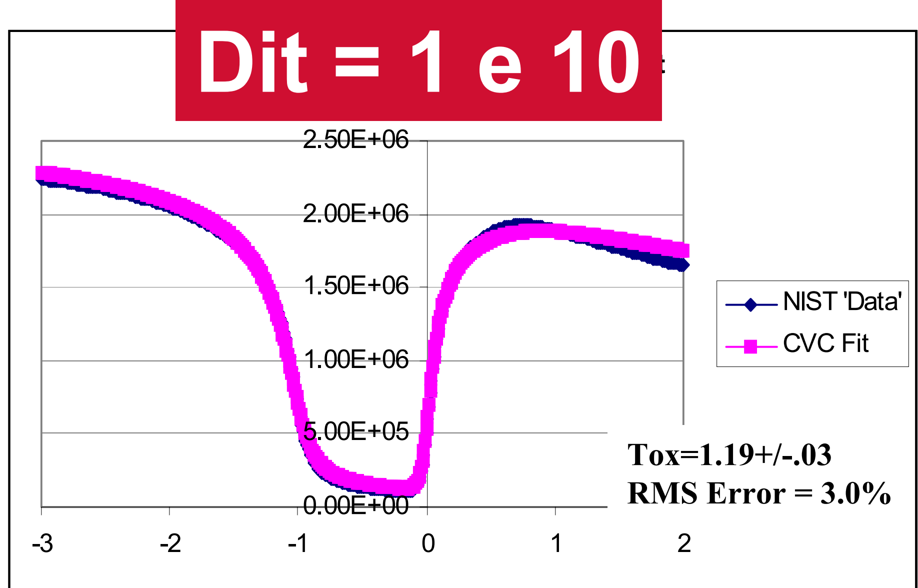


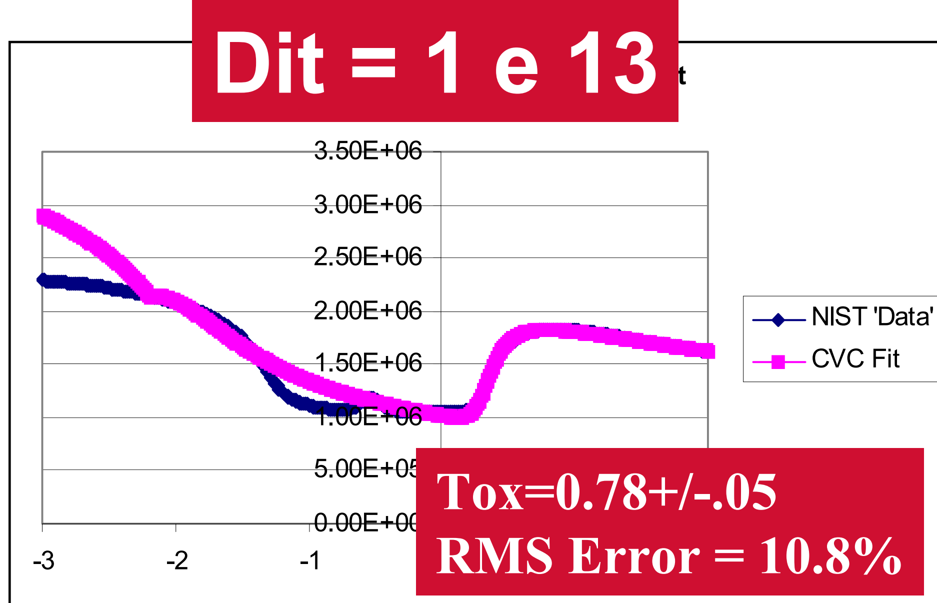
Thanks to Rich Matyi

NIST + ISMT : C-V Full Curve Fits for Tox=1nm

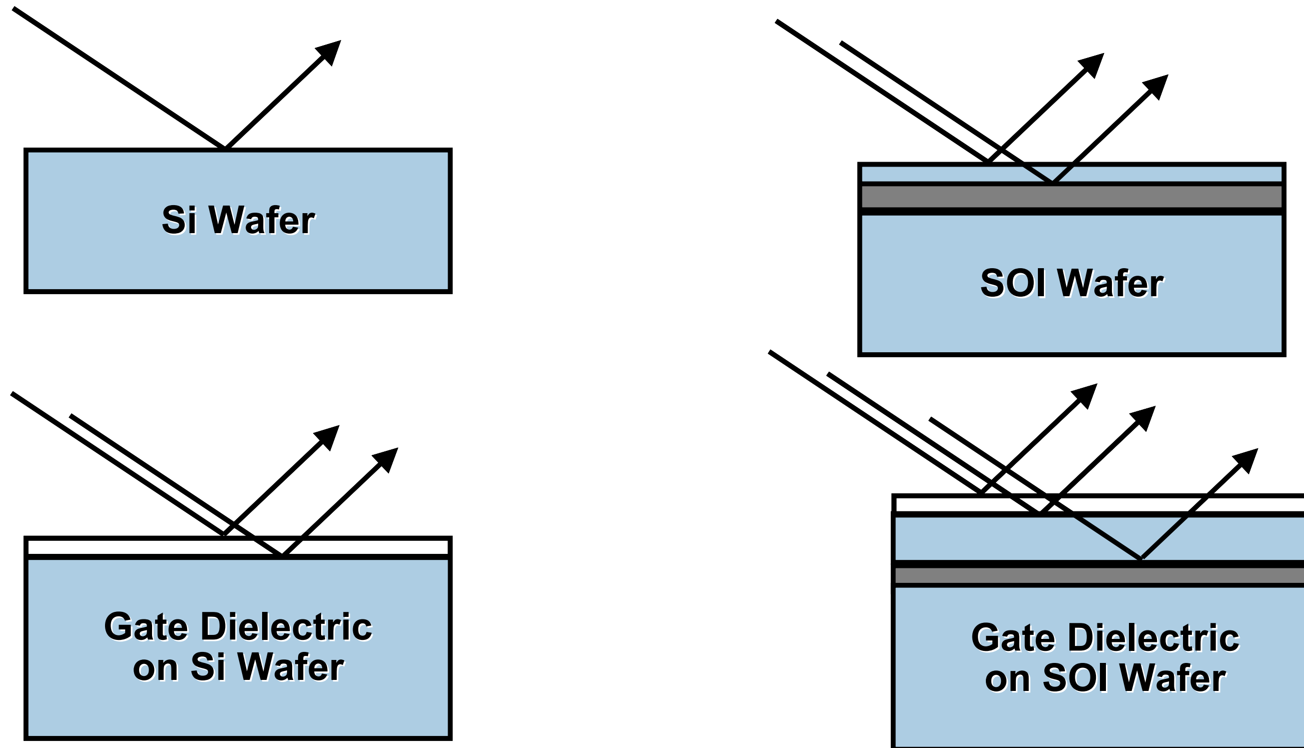








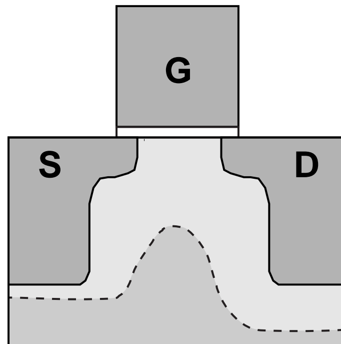
Extra reflection from SOI Wafers Impacts Optical Measurements and Light Scattering



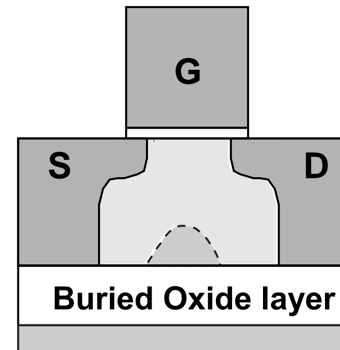
Quantum confinement for sub 20 nm silicon
Need SOI Optical Constants

Beyond Classical CMOS

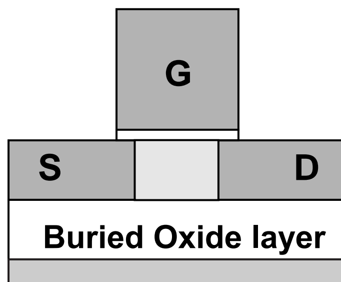
Bulk MOSFET



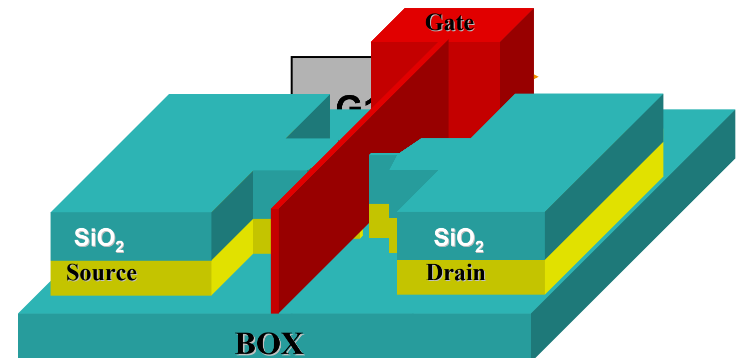
Partially-Depleted SOI



Ultra-Thin Body SOI



Double-Gate MOSFET



INTERNATIONAL SEMATECH

AGENDA

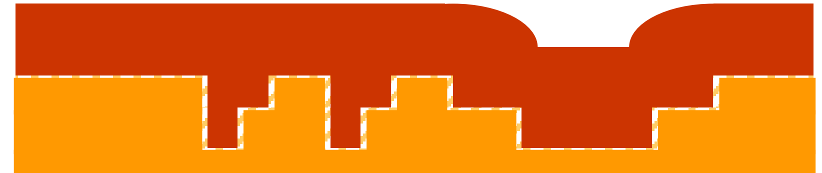
- How to control microscopic features
- Litho Metrology
- FEP Metrology
- Interconnect Metrology
- Materials Characterization

Interconnect Metrology

Pattern Low κ Control Line width/depth and shape

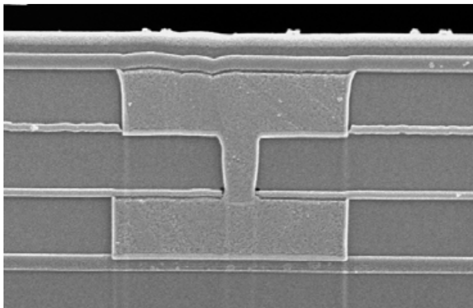
Deposit barrier and copper

Control barrier/copper & voiding



Chemical Mechanical Polishing

Control Flatness



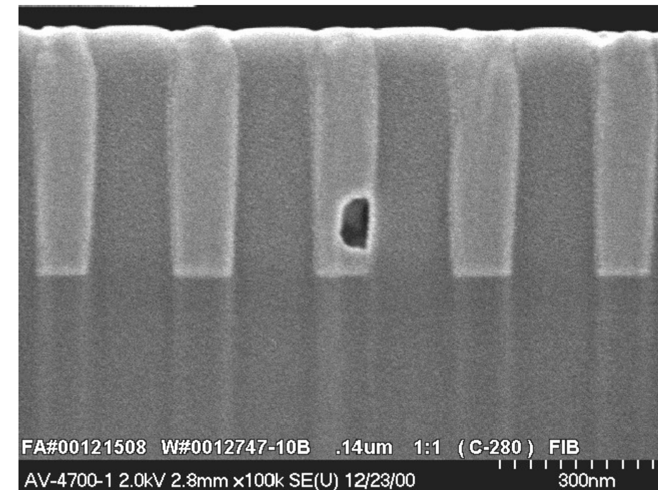
Low k / barrier
etch stop / low k

INTERNATIONAL SEMATECH

Gaps in Interconnect Metrology

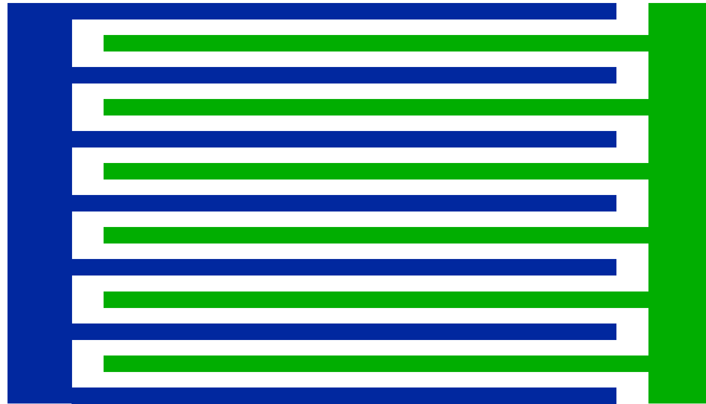
Technology Node	130 nm	90nm	65 nm	45 nm	32 nm	22 nm
Interconnect Metrology						
Barrier layer thick (nm) process range (±3σ) Precision 1σ (nm)	13 20% 0.04	10 20% 0.03	7 20% 0.02	5 20% 0.016	4 20% 0.013	
Void Size for 1% Voiding in Cu Lines	87	52	37	26	18	12
Detection of Killer Pores at (nm) size	6.5	4.5	3.25	2.25	1.6	1.1

- **VOID Detection in Copper lines**
- **Killer Pore Detection in Low κ**
- **Barrier / Seed Cu on sidewalls**
- **Control of each new Low κ**

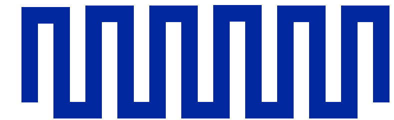


INTERNATIONAL SEMATECH

R-C test structures of new low κ Prior to manufacture

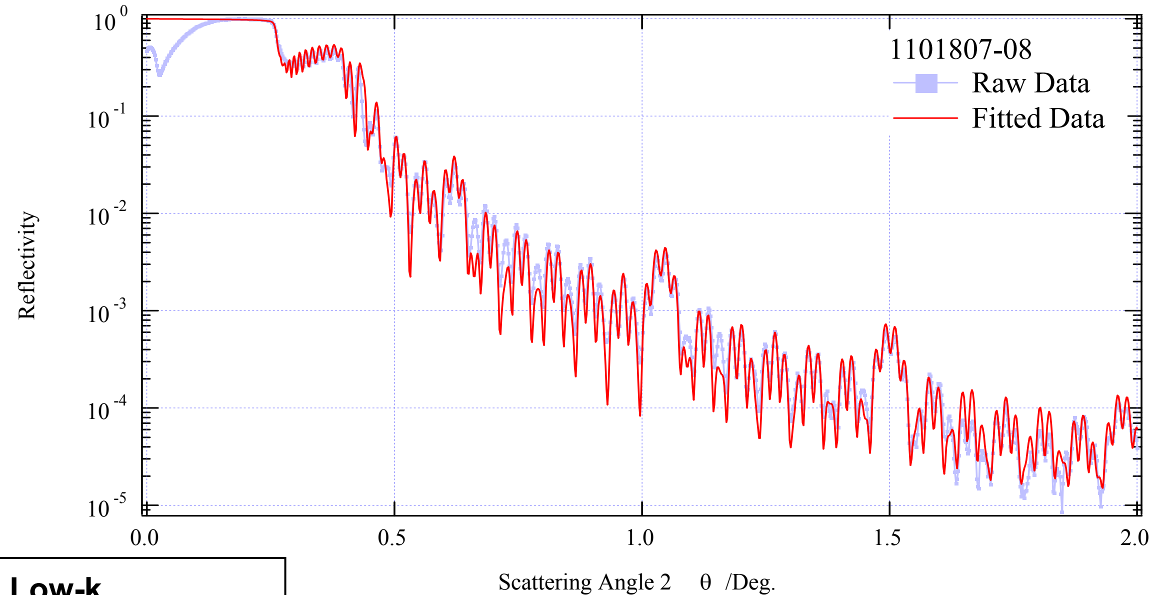


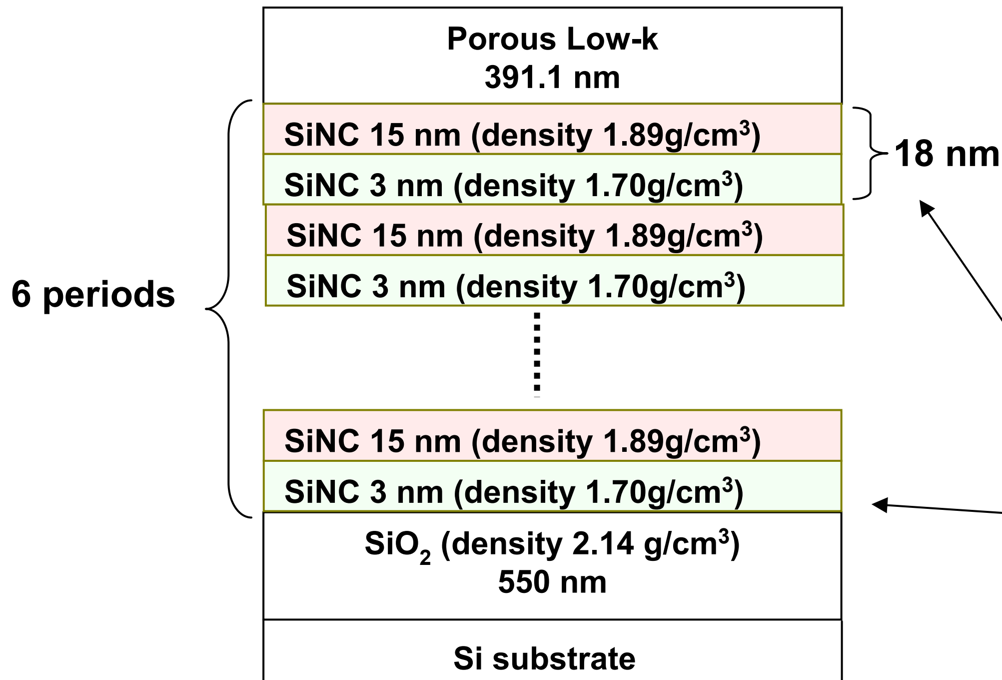
Capacitance Test

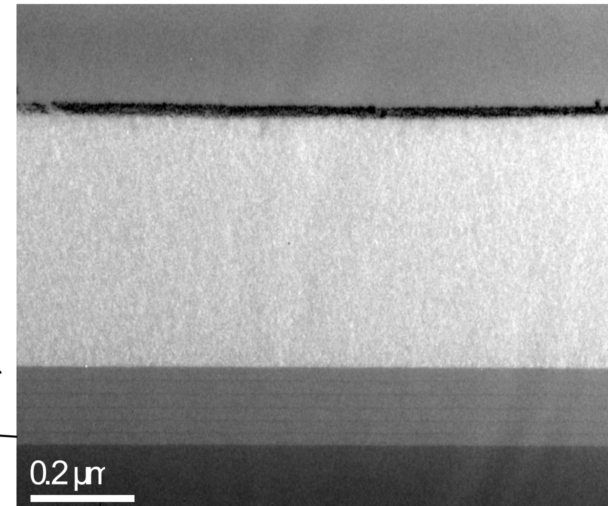


Resistance Test

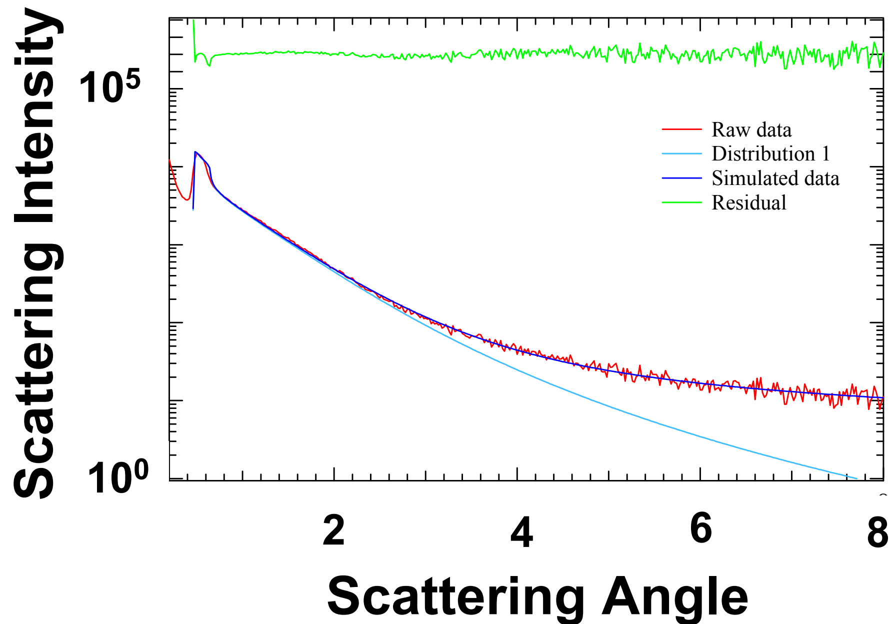
XRR for low κ process control

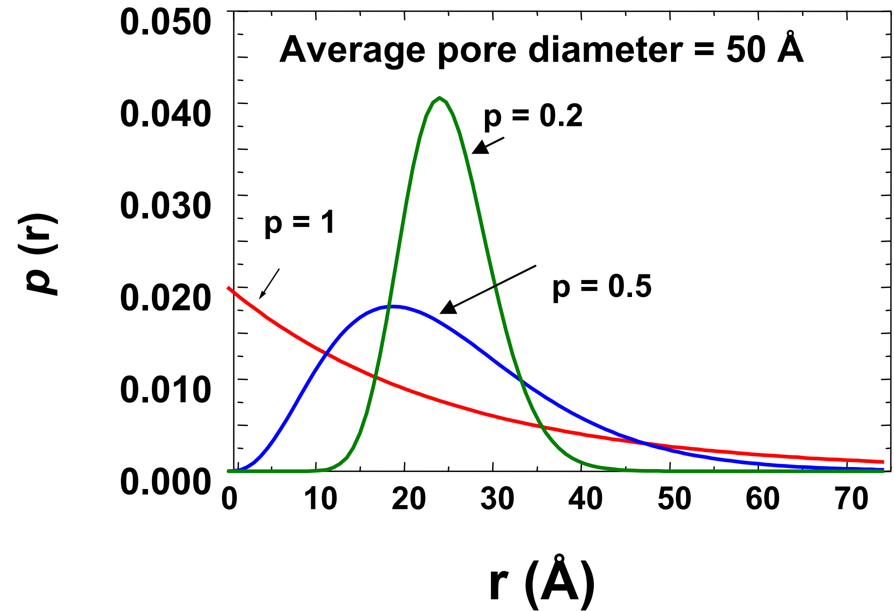






Pore Size Distribution
Diffuse (small angle) x-ray scattering



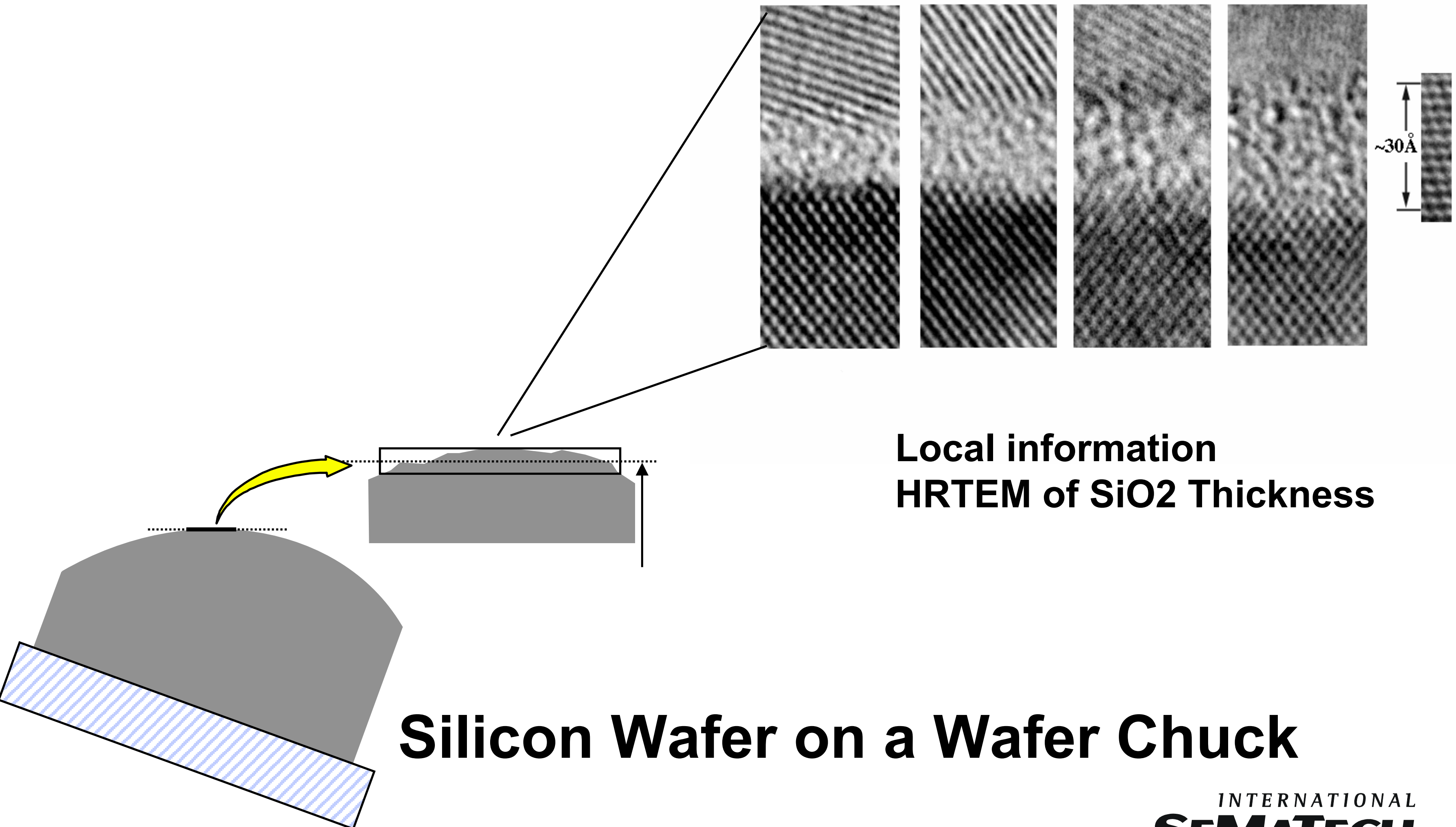


INTERNATIONAL SEMATECH

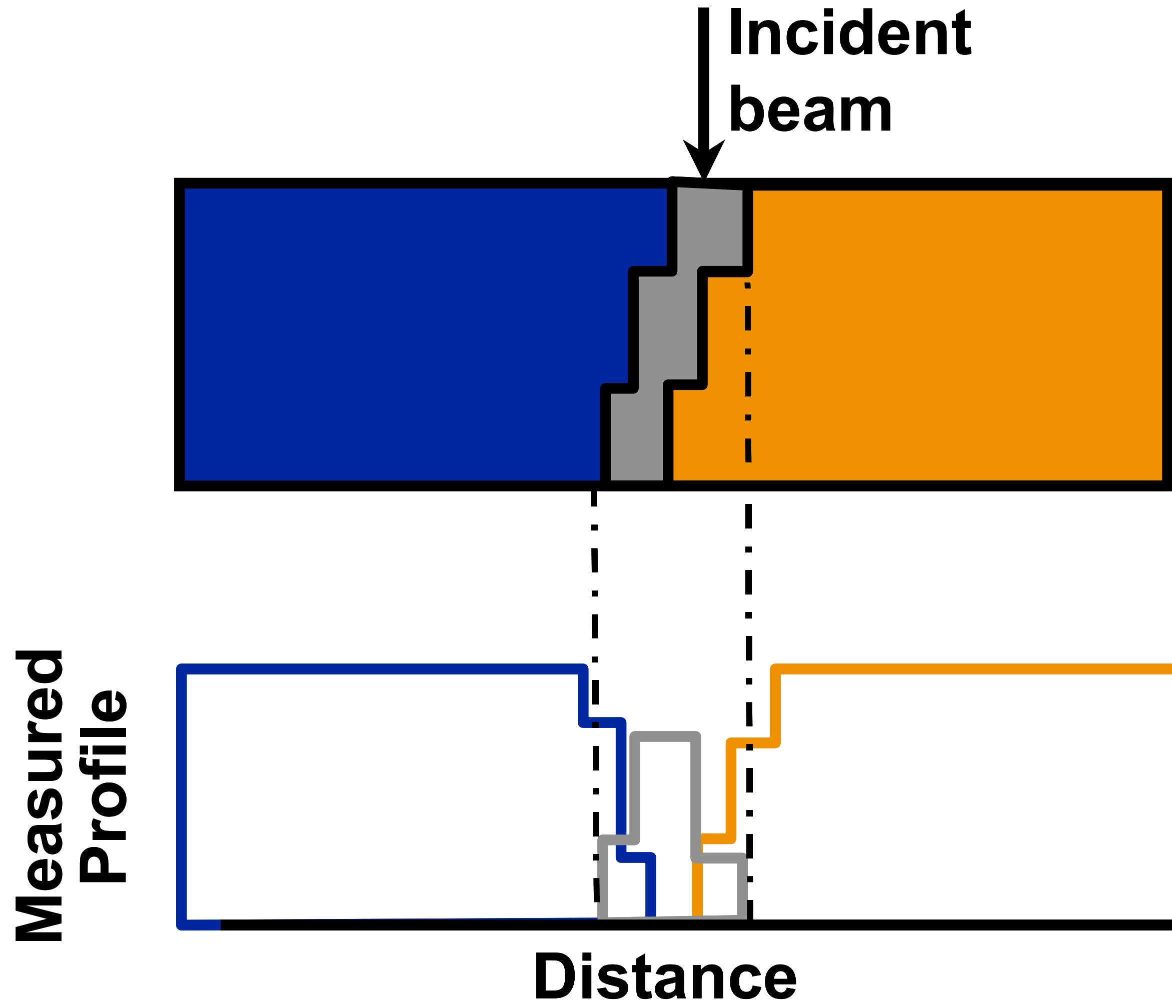
AGENDA

- How to control microscopic features
- Litho Metrology
- FEP Metrology
- Interconnect Metrology
- Materials Characterization

Method Dependent Observation of Film Properties

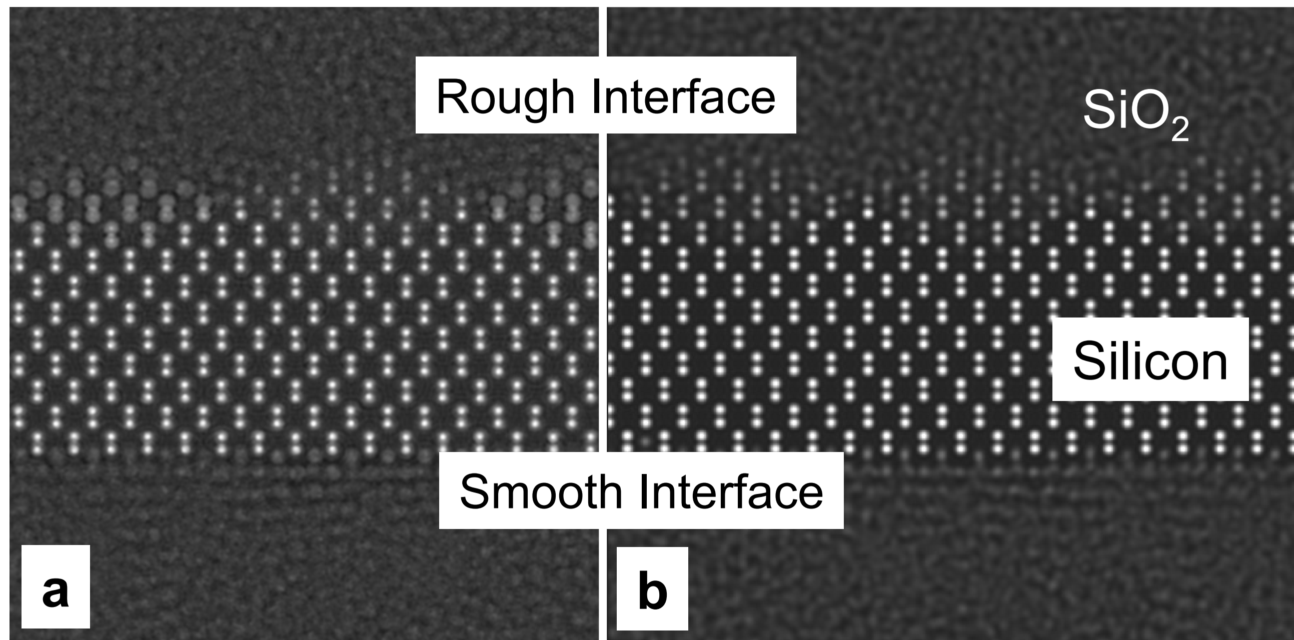


TEM Imaging of the Interface



TEM of thin gate dielectric

Simulation and Experimental Data show ADF-STEM and HR-TEM give same thickness



Consensus method uses 50 nm thick sample & ADF-STEM

Thanks to Dave Muller

INTERNATIONAL SEMATECH

Local Electrode Atom Probe

V_{accel}

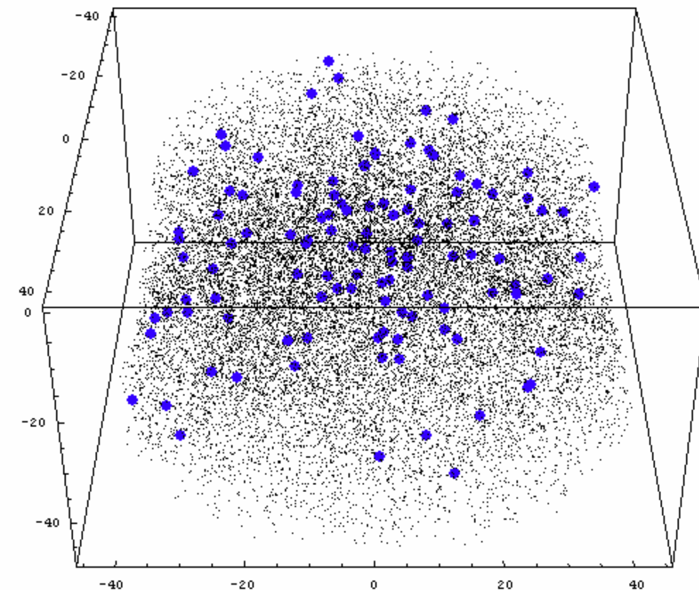
V_{pulseb}

V_{ex}

z

y

x



Atom Distribution

: < 100% detection

Metrology & New Structures

Memory

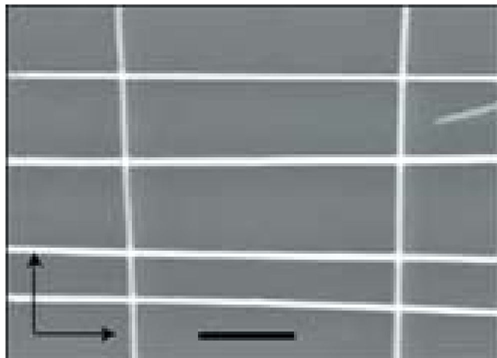
STORAGE MECHANISM	*BASELINE 2002 TECHNOLOGIES*		*MAGNETIC RAM*		*PHASE CHANGE MEMORY*	*NANO FLOATING GATE MEMORY*	*SINGLE/FEW ELECTRON MEMORIES*	*MOLECULAR MEMORIES*
DEVICE TYPES	*DRAM*	*NOR FLASH*	*PSEUDO-SPIN-VALVE*	*MAGNETIC TUNNEL JUNCTION*	*OUM*	*-ENGINEERED TUNNEL BARRIER -NANOCRYSTAL*	*SET*	*-BISTABLE SWITCH -MOLECULAR NEMS -SPIN BASED MOLECULAR DEVICES*

Logic

Device	Resonant Tunneling Diode – FET	Single Electron Transistor	Rapid Single Quantum Flux Logic	Quantum Cellular Automata	Nanotube Devices	Molecular Devices
Types	**3-terminal**	**3-terminal**	**Josephson Junction +inductance loop**	**-Electronic QCA -Magnetic QCA**	**FET**	**2-terminal and 3-terminal**

INTERNATIONAL SEMATECH

Metrology & Molecular Electronics

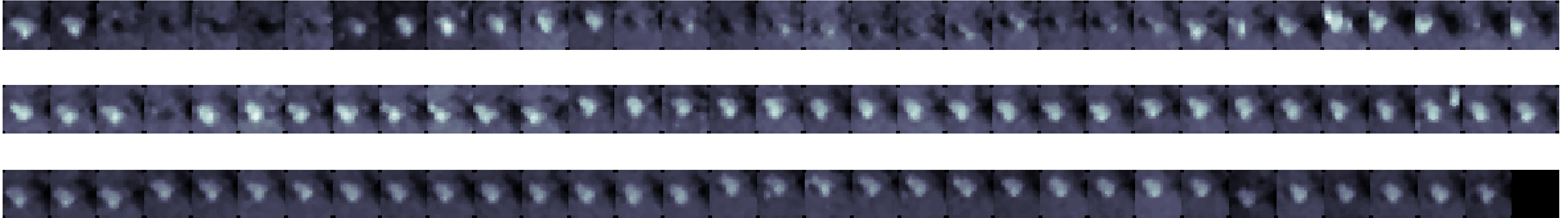


James Heath, Fraser Stoddart, and Anthony Pease

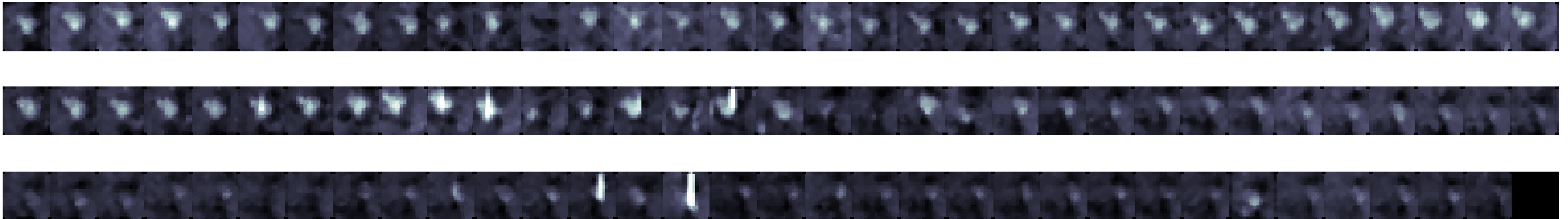
INTERNATIONAL SEMATECH

Metrology & Molecular Electronics

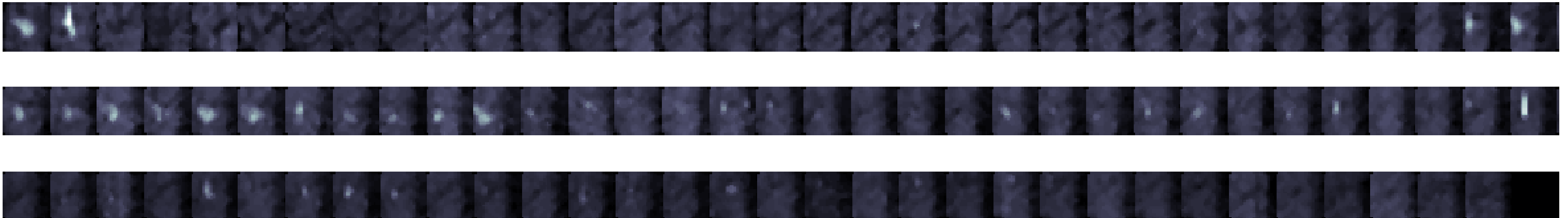
A



B



C

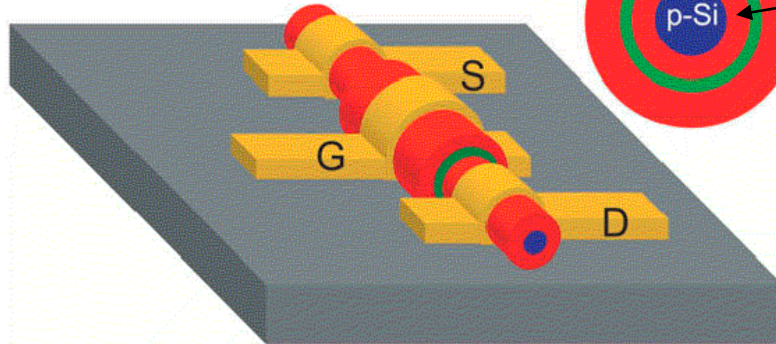


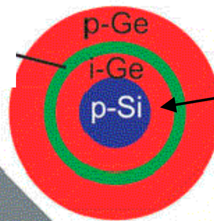
Paul Weiss's Group – STM of Conductance Switching

INTERNATIONAL SEMATECH

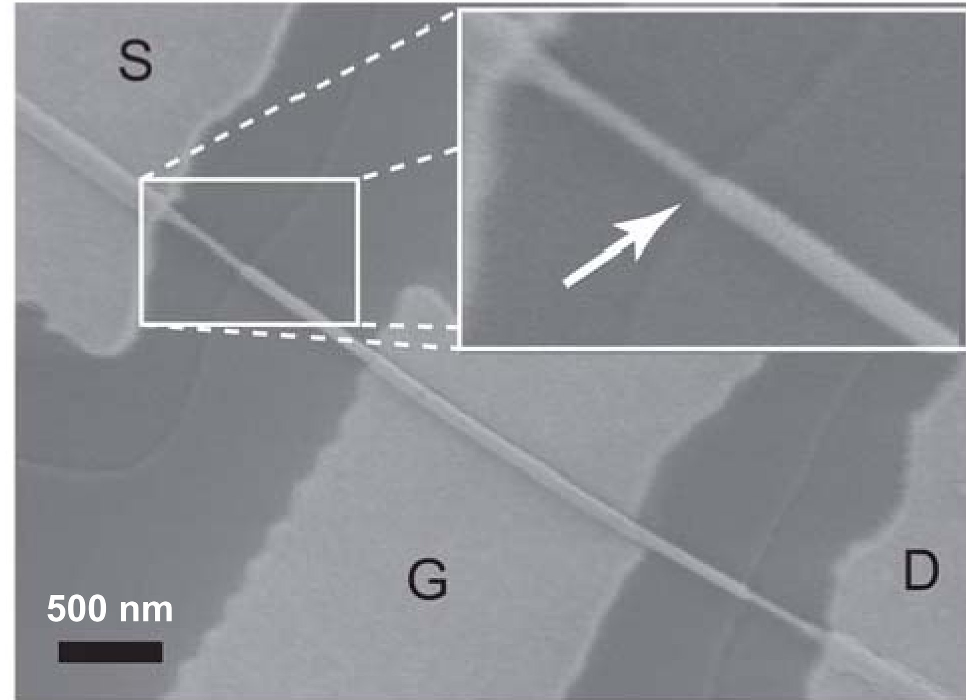
Nanowire Transistors and Interconnect

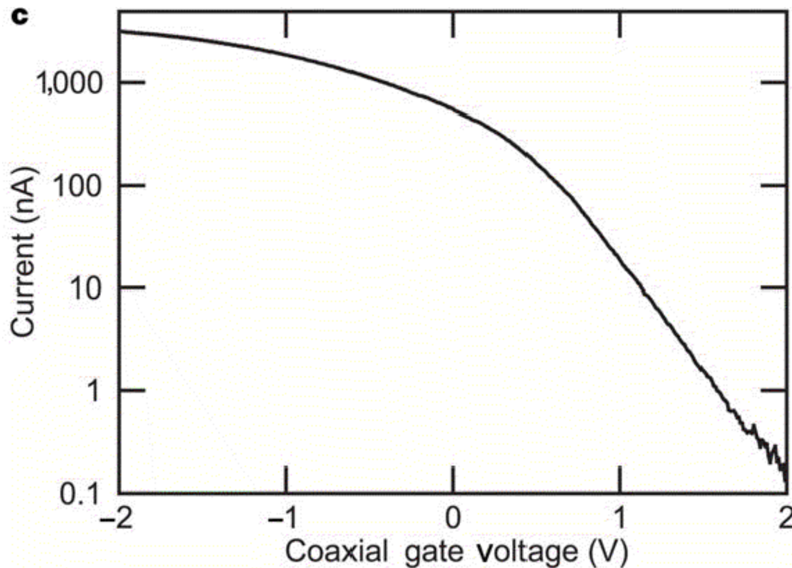
5 nm layer of Ge on top of 4 nm SiOx





10 nm p-Si core diameter & 10 nm i- Ge layer





L.J. LAUHON, M.S. GUDIKSEN, D. WANG & CHARLES M. LIEBER
***Nature* 420, 57 - 61 (2002)**

INTERNATIONAL SEMATECH

Conclusions

- **Measure Microscopic Features**
  - New Methods
  - Look for a Signal that reflects Microscopic Change
- **Improve Statistical Significance**
  - Average over Large AREAS
  - Use Statistical Metrology When Possible
- **Do these trends Conflict with smaller scribe line ?**

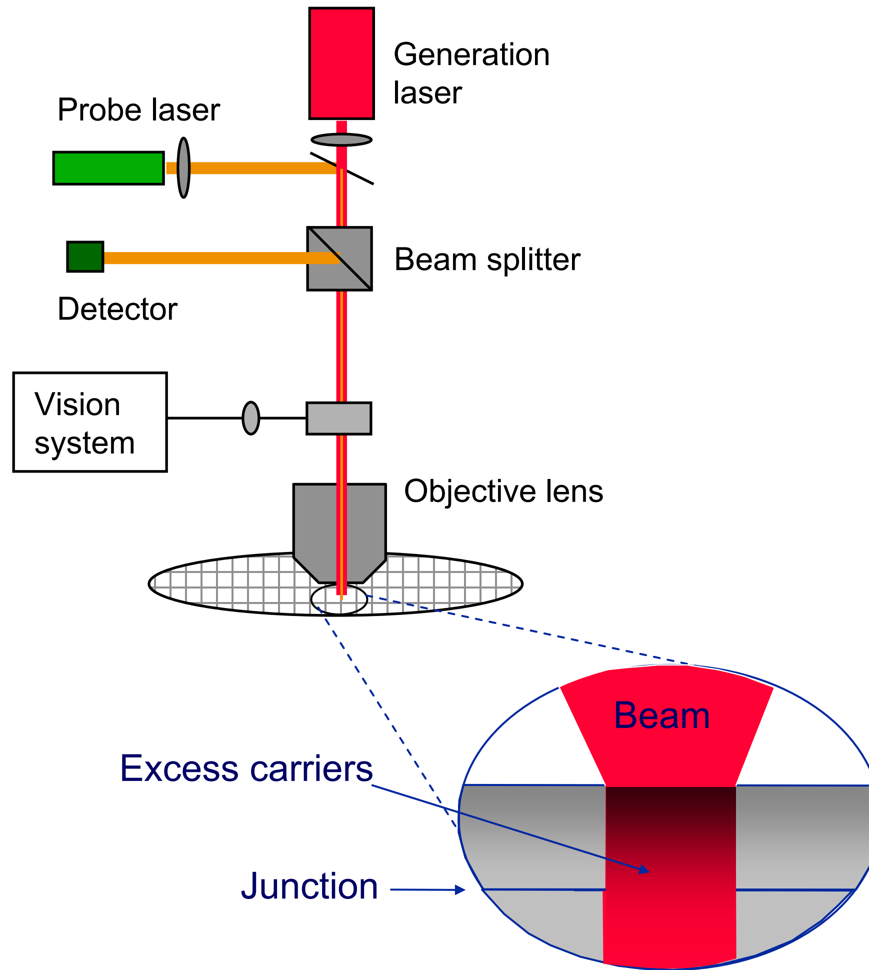
Metrology Roadmap
2002 Update

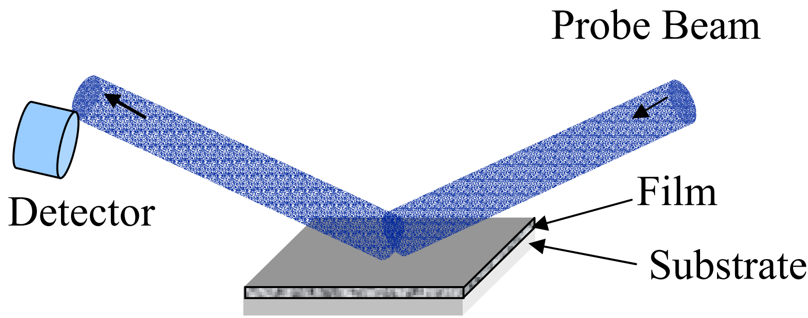
Europe	Ulrich Mantz (Infineon) Alec Reader (Philips Analytical) Mauro Vasconi (ST)
Japan	Masahiko Ikeno (Mitsubishi) Fumio Mizuno (Meisei University) Toshihiko Osada (Fujitsu) Akira Okamoto (SONY) Yuichiro Yamazaki (Toshiba)
Korea	DH Cho (Samsung)
Taiwan	Henry Ma (EPISIL)
US	Steve Knight (NIST) Alain Diebold (Int. SEMATECH)

Metrology Roadmap
2002 Update

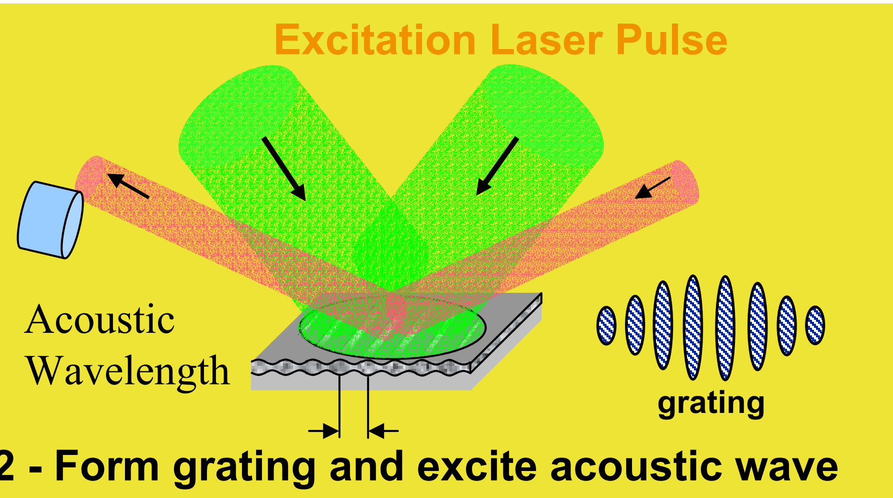
US	John Allgair	Motorola
	Alain Diebold	Int. SEMATECH
	Drew Evan	CEA
	David Joy	Univ. of Tenn
	Steve Knight	NIST
	Kevin Monahan	KLA-Tencor
	Noel Poduje	ADE
	Heath Pois	Thermawave
	Bhanwar Singh	AMD
	Andras Vladar	NIST
Speakers		
	Michael Gostein	Philips Analytical
	PY Hung	Int. SEMATECH
	Tom Kelly	Amigo
	Heath Pois	Thermawave
	Benzi Sender	Applied Materials

New Methods

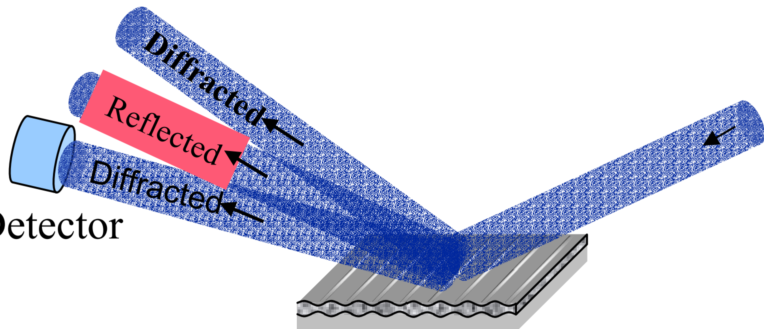




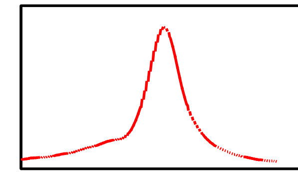
1 - Probe beam strikes surface



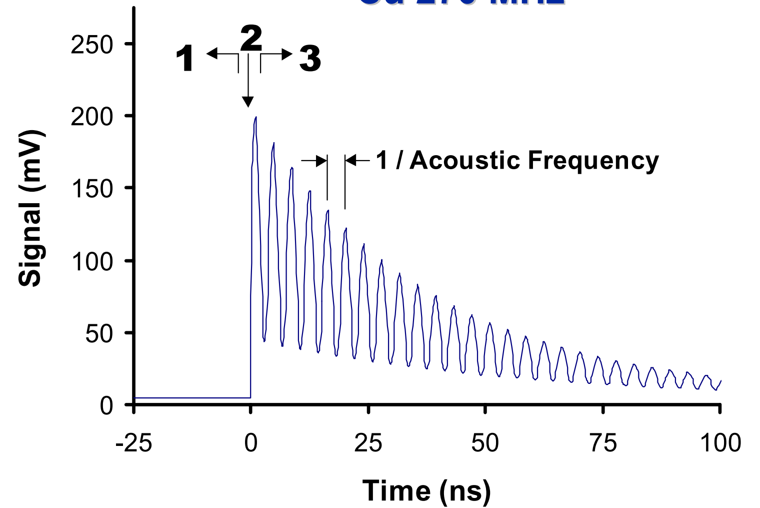
2 - Form grating and excite acoustic wave

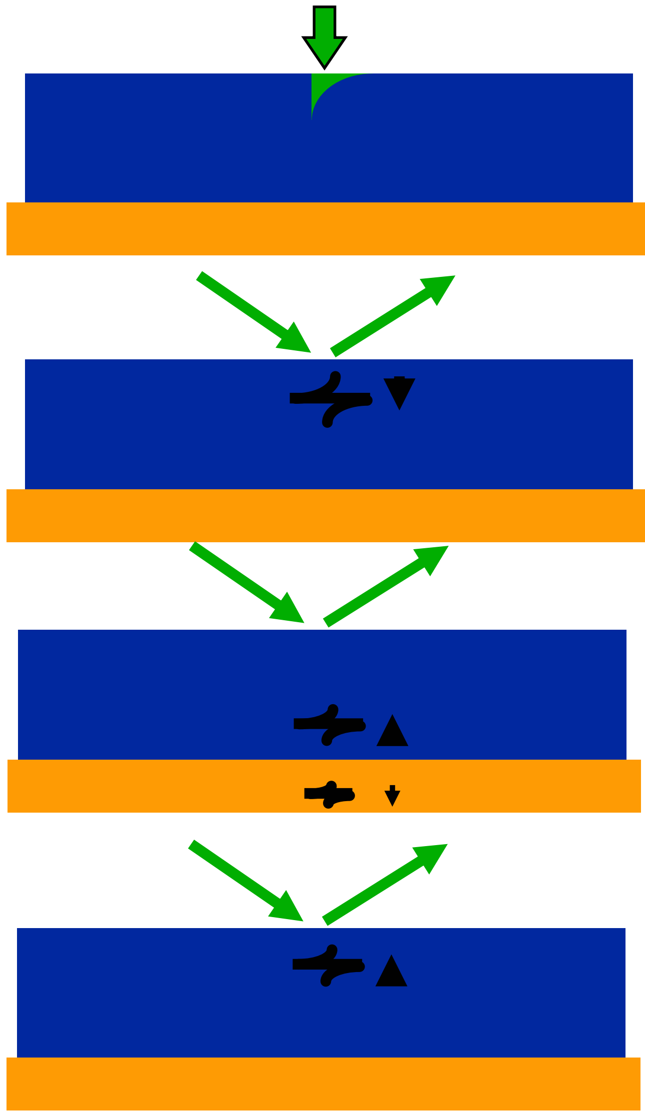
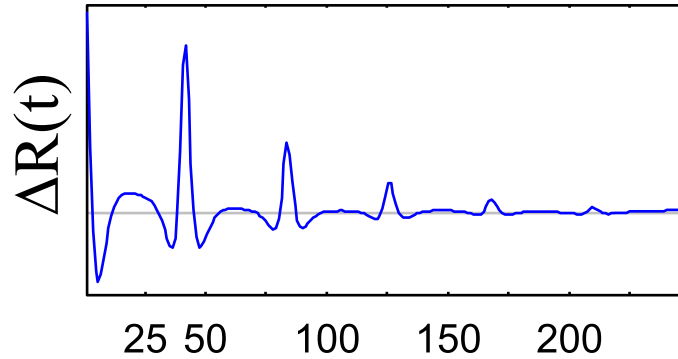


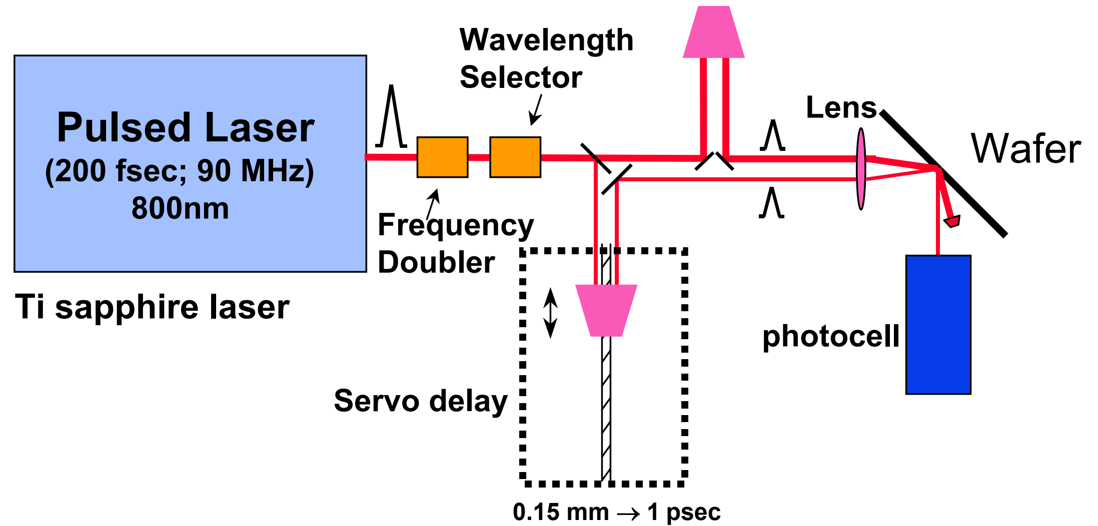
3 - Probe beam diffracted as wave travels parallel to surface



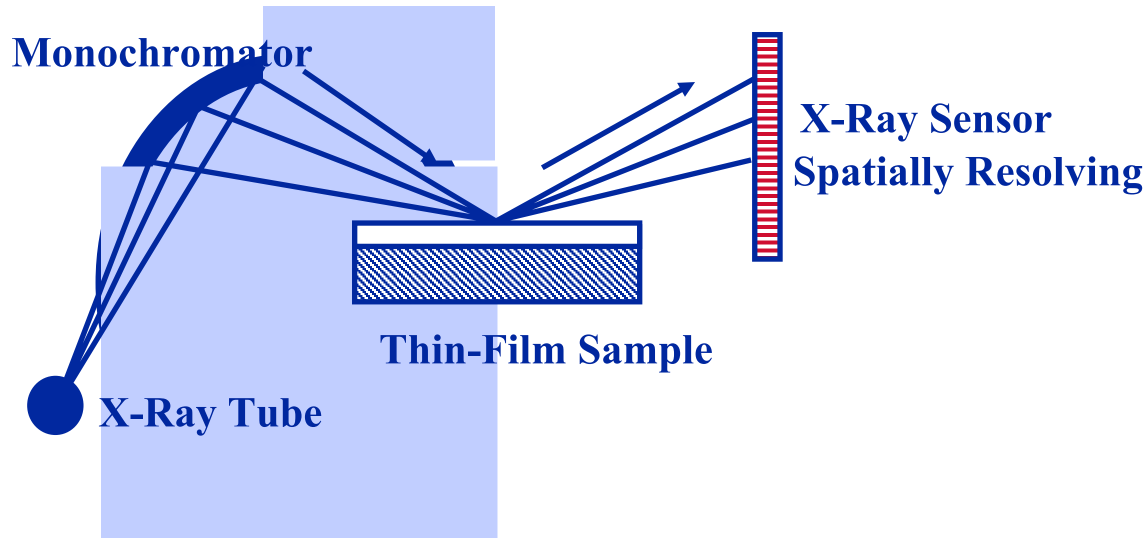
Cu 270 MHz

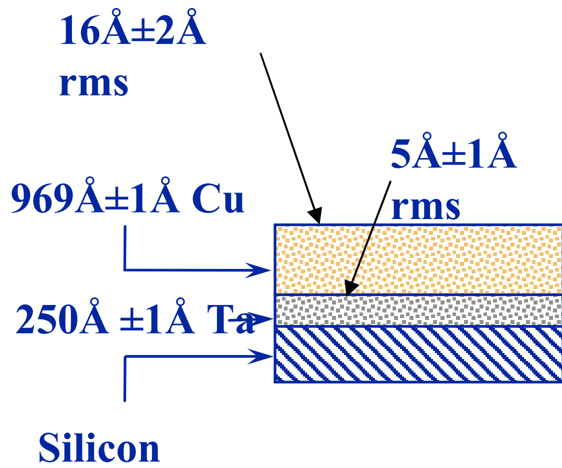


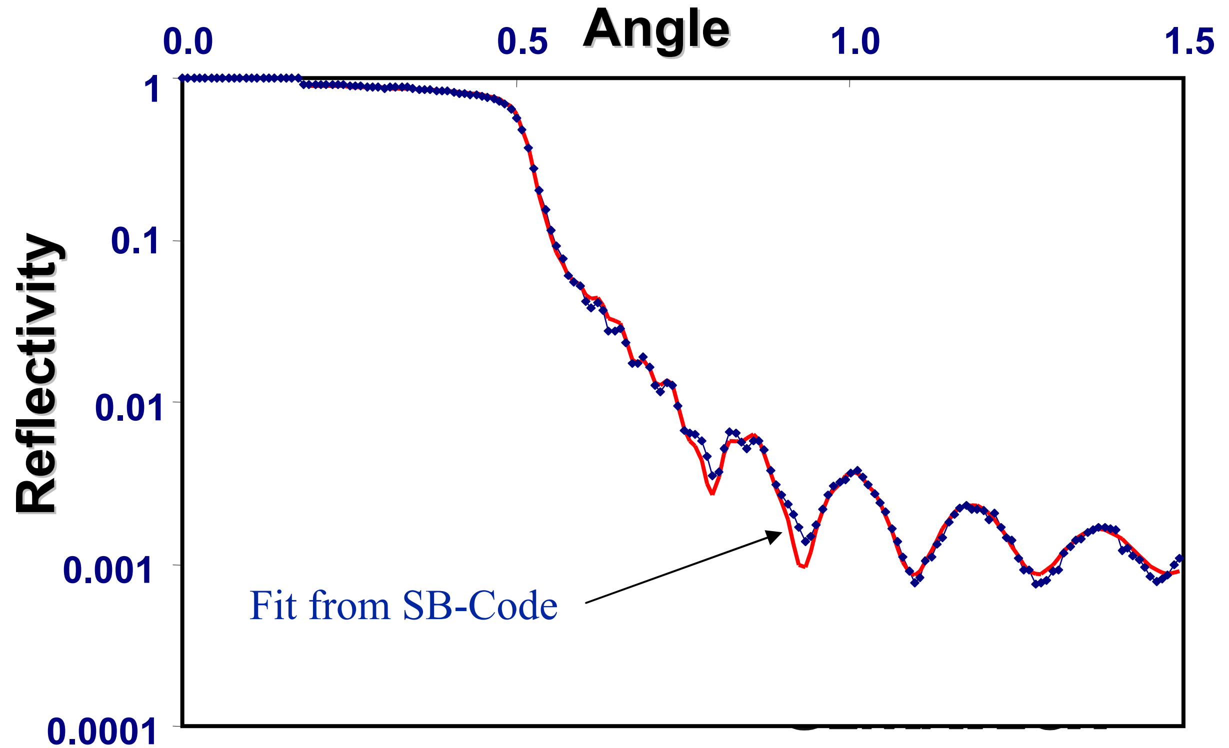





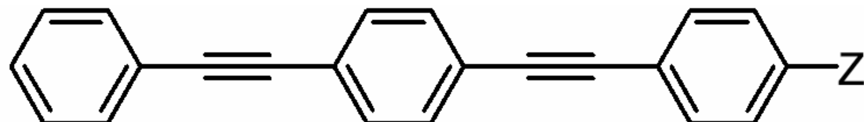
sampling speed (2 to 4 secs/pt)
less than a 10 mm diameter spot size


Monochromator
X-Ray Sensor
Spatially Resolving
Thin-Film Sample
X-Ray Tube


16Å±2Å
rms
5Å±1Å
rms
969Å±1Å Cu
250Å ±1Å Ta
Silicon

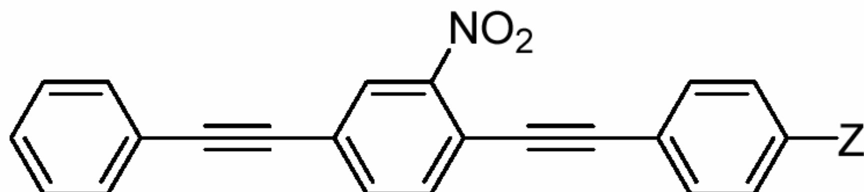

Angle
0.0
0.5
1.0
1.5
Reflectivity
1
0.1
0.01
0.001
0.0001
Fit from SB-Code

Metrology & Molecular Electronics



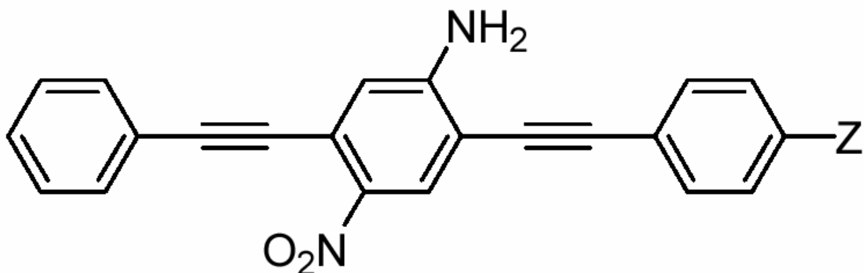
NH_4OH → **1**, Z = $SCOCH_3$

1', Z = S^-, 4,4'-di(ethynylphenyl)-1-benzenethiolate



NH_4OH → **2**, Z = $SCOCH_3$

2', Z = S^-, 4,4'-di(ethynylphenyl)-2'-nitro-1-benzenethiolate



NH_4OH → **3**, Z = $SCOCH_3$

3', Z = S^-, 2'-amino-4,4'-di(ethynylphenyl)-5'-nitro-1-benzenethiolate

SEMATECH

Use of HRTEM for Calibration

High Resolution TEM (Phase Contrast) has a ~ 10% error for Thickness Determination Due to Cs

Specimen Thickness A	Specimen Tilt (mrad)	Defocus	Cs (mm)	Oxide Model Thickness	Oxide Measured Thickness	% Error
154	0	-425	0.5	10.56	9.84	-6.8
154	0	-156	0.5	10.56	11.4	8
154	0	-20	0.5	10.56	10.44	-1.1
154	12.6	-425	0.5	10.56	9.12	-13.6
154	25	-425	0.5	10.56	10.68	1.1
154	0	-425	0.5	10.56	8.88	-15.9

HRTEM Image Simulations for Gate Oxide Metrology

S. Taylor, J. Mardinly, M.A. O'Keefe, and R. Gronsky

Characterization and Metrology for ULSI Technology 2000

INTERNATIONAL SEMATECH