



CHIPS R&D Standards Summit

Attendee Packet

September 26-27, 2023







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CHIPS R&D Standards Summit Background

The CHIPS R&D Standards Summit aims to bring together thought leaders from industry and academia to collectively shape the future and drive innovation in semiconductor and microelectronics standards. The summit's purpose and objectives are:

- 1. Drive innovation and efficiency. The summit aims to identify strategic standards priorities that will drive innovation and increase value and efficiency across the semiconductor and microelectronics sector. By identifying key priorities, stakeholders can pave the way for a smoother, more efficient innovation pipeline.
- 2. Enable standards at the pace of innovation. The summit will also focus on identifying opportunities for innovation in standards development to keep up with the rapid pace of innovation in the industry. This includes exploring incubators and accelerators that can expedite the standards-setting process, ensuring that technological breakthroughs can be quickly integrated.
- 3. Build a diverse and skilled workforce. We understand the importance of nurturing a standards-capable workforce that can meet the evolving needs of the industry. A vibrant semiconductor and microelectronics industry requires a skilled and diverse workforce to foster innovation through a broad range of perspectives and ideas. The summit will identify approaches to increase diversity in the semiconductor workforce.
- 4. Build a network of stakeholders. The summit will engage the semiconductor and microelectronics community in the launch of the CHIPS R&D Standards Program and build a network of stakeholders energized to lead strategic standards initiatives. This network and the CHIPS R&D Standards Program will drive future advancements, ensuring that the sector remains dynamic and responsive to the ever-changing demands of technology.

The summit's anticipated outcomes are to provide the semiconductor and microelectronics industry with strategic priorities, clearly defined technical scopes, and innovative methods for intra-sector collaboration through standardization. The summit is an opportunity for stakeholders to come together, share ideas, and shape the standards that will define the future of this critical industry.





Summit Resources

- <u>Standards Summit Main Page</u>
- <u>Standards Summit Overview</u>
- <u>Standards Summit Agenda</u>
- <u>Speakers</u>
- Location Information
- <u>Co-host Organizations</u>
- <u>Standards Summit Organizing Committee</u>
- Standards Summit Blog
- <u>FAQs</u>



Standards Summit Agenda (TENTATIVE)

Day 1 - Tuesday, September 26, 2023 (8:30am - 5:30pm ET)

SESSION #1: 8:30am - 9:30am - Overview and Keynote(s) (PLENARY)

- This introductory session will establish the motivation, purpose, and objectives for convening the CHIPS R&D Standards Summit.
- Keynote addresses will include CHIPS R&D Director Lora Weiss on the goals of the CHIPS R&D programs and the role of technical standards, NIST Senior Advisor Jayne Morrow on the United States Government National Standards Strategy for Critical and Emerging Technologies, and SEMI Americas President Joe Stockunas on the importance of standards in the semiconductor and microelectronics industries.
- Moderators will review the summit agenda and resolve attendee questions.

BREAK: 9:30am - 10:00am (Attendee Networking)

SESSION #2: 10:00am - 12:00pm – Strategic Standards Priorities – Topic Identification and Scoping (PLENARY)

- Part 1 Topic Identification (60 minutes): This panel will focus on surfacing topic areas that are high strategic priorities for the community in focusing on standards that drive innovation and speed commercialization.
- **Part 2 Topic Scoping (60 minutes):** Panelists will explore the appropriate scope for the strategic priority areas that emerged in the preceding session.

LUNCH BREAK: 12:00pm - 1:30pm

SESSION #3: 1:30pm - 2:30pm - Innovation in Standards Development, to include Incubators and Accelerators (PLENARY)

• This panel will consider whether concepts from incubators and accelerators, as practiced in the technology sector, might be adapted for use in standards development to allow standards processes to keep pace with innovation, broaden opportunities for participation in standards activities, and provide educational and training opportunities.

BREAK: 2:30pm - 3:00pm (Attendee Networking)

SESSION #4: 3:00pm - 4:00pm - Diverse, Standards-Capable Workforce (PLENARY)

• This panel will examine approaches for enabling a diverse, standards-capable workforce that can bring the range of skills and perspectives needed to meet the fast-paced and complex standards needs of the semiconductor and microelectronics sector. Speakers from educational institutions, industry, and standards setting organizations will discuss standards priorities in developing content for the microelectronics industry workforce.

SESSION #5: 4:00pm - 5:00pm - Pre-Standards Research (PLENARY)

• This panel will focus on pursuing the research needed to provide the science and technology foundations for sound, effective, and relevant standards.

SESSION #6: 5:00pm - 5:30pm - Day 1 Closing (PLENARY)



Day 2 - Wednesday, September 27, 2023 (8:30am - 5:30pm ET)

SESSION #7: 8:30am - 9:00am - Overview and Keynote(s) (PLENARY)

• Moderators summarize Day 1 highlights and review the Day 2 agenda before resolving attendee questions.

BREAK: 9:00am - 9:15am (Attendees relocate to breakout rooms)

SESSION #8: 9:15am - 10:15am - Strategic Standards Priorities - Topics (BREAKOUT)

• This breakout session will focus on surfacing topic areas that are high strategic priorities for the community in focusing on standards that drive innovation and speed commercialization. While detailed, specific standards needs will be relevant as examples in this discussion, the focus is on identifying higher-level categories for a deeper dive in subsequent sessions and follow-on workshops.

SESSION #9: 10:15am - 11:15am - Standards Priority Areas - Scoping (BREAKOUT)

• This breakout session will explore the appropriate scope for the strategic priority areas that emerged in the preceding session. Examples might include whether a packaging priority could focus on advanced 3D architectures or cover a broader set or whether a data priority could focus on real-time process data, machine learning for automation, or other areas.

LUNCH BREAK: 11:15am - 12:45pm

SESSION #10: 12:45pm - 1:45pm - Innovation in Standards Development, to include Incubators and Accelerators (BREAKOUT)

• This breakout session will consider whether concepts from incubators and accelerators, as practiced in the technology sector, might be adapted for use in standards development to allow standards processes to keep pace with innovation, broaden opportunities for participation in standards activities, and provide educational and training opportunities.

BREAK: 1:45pm - 2:15pm (Attendee Networking)

SESSION #11: 2:15pm - 2:30pm - Recap of Strategic Standards Priorities (PLENARY)

• This session will review the inputs from the strategic standards priorities breakout session discussions and prepare attendees for the following breakout session discussions.

SESSION #12: 2:30pm - 2:40pm - Remarks from U.S. Department of Commerce Secretary Gina Raimondo

• The session will include comments from U.S. Secretary of Commerce, Gina Raimondo, on the CHIPS for America program, including the role of standards in promoting innovation and advancement.

SESSION #13: 2:45pm - 3:45pm - Diverse, Standards-Capable Workforce (BREAKOUT)

• This breakout session will examine approaches for enabling a diverse, standards-capable workforce that can bring the range of skills and perspectives needed to meet the fast-paced and complex standards needs of the semiconductor and microelectronics sector. Speakers from educational institutions, industry, and standards setting organizations will discuss standards priorities in developing content for the microelectronics industry workforce.



SESSION #14: 3:45pm - 4:45pm - Pre-Standards Research (BREAKOUT)

• This panel will focus on pursuing the research needed to provide the science and technology foundations for sound, effective, and relevant standards. Examples from the CHIPS R&D Metrology Program, the National Nanotechnology Coordination Office (NNCO), and the Networking and Information Technology Research and Development (NITRD) Program will be considered to inform discussion of this topic.

BREAK: 4:45pm - 5:00pm (Attendees relocate to the main hall)

SESSION #15: 5:00pm - 5:30pm - Wrap-up and Next Steps (Day 2 Closing - Plenary)

• Moderators will describe summit highlights and next steps for CHIPS R&D Standards. Facilitators will convene a hotwash describing what went well and what could be improved for future CHIPS R&D Standards events.



Pre-Read Materials







for Reducing Risks and Mitigating Shortages

United States Standards Strategy (ANSI)

First published in 2000 as the National Standards Strategy for the United States (NSS), this strategy document is updated every five years to ensure that it continues to meet the needs of diverse U.S. interests and that it reflects technological advancements, industry growth areas, national and international priorities, and updates to relevant U.S. government policy. The strategy details 12 strategic initiatives that diverse stakeholders can implement to meet national and individual organizational objectives.

U.S. Government National Standards Strategy for Critical and Emerging Technologies

This strategy outlines how the U.S. government will strengthen U.S. leadership and competitiveness in international standards development and ensure that the "rules of the road" for critical and emerging technologies (CET) standards embrace transparency, openness, impartiality, consensus, effectiveness and relevance, coherence, and broad participation.

<u>President's Council of Advisors on Science and Technology,</u> <u>Revitalizing the U.S. Semiconductor Ecosystem</u>

This report focuses on the transformative investments in R&D, startups, education, and workforce development essential to the long-term health and competitiveness of the U.S. semiconductor ecosystem.

U.S. Government Accountability Office, July 2022, Semiconductor Supply Chain: Policy Considerations from Selected Experts for Reducing Risks and Mitigating Shortages

This report summarizes the views of selected experts on policy options to reduce semiconductor supply chain risks and help mitigate future shortages in the U.S.









Semiconductor Industry Association and Oxford Economics, 2021, Chipping In, the Positive Impact of the Semiconductor Industry on the American Workforce and How Federal Industry Incentives Will Increase Domestic Jobs

Oxford Economics has quantified the economic contribution of the U.S. semiconductor industry by using an economic impact analysis at the national level in the U.S. This technique highlights the importance of the semiconductor industry to the U.S. economy in terms of jobs, wages, and gross domestic products (GDP).

Congressional Research Service, 2020, Semiconductors: U.S. Industry, Global Competition, and Federal Policy

This report discusses the technical challenges the semiconductor industry faces, domestic and global supply chains, secure and trusted production of semiconductors for national security, and federal policies. This report also discusses current legislation to address these concerns, including federal assistance for the domestic semiconductor industry and funding for R&D activities.

Hunt and Zwetsloot, 2020, The Chipmakers: U.S. Strengths and Priorities for the High-End Semiconductor Workforce

This report explores the composition of the talented workforce that undergirds continued U.S. leadership in the semiconductor industry and assesses workforce policy options for protecting and promoting technological competitiveness going forward.

For more information, please email askchips@chips.gov - thank you!