CHIPS *for* AMERICA

Metrology Gaps in the Semiconductor Ecosystem:

First Steps Toward Establishing the CHIPS R&D Metrology Program

CHIPS Research and Development Office

June 5, 2023

CHIPS *for* AMERICA

NIST NATIONAL INSTITUTE OF STANDARDS AND TECHNOLOGY
U.S. DEPARTMENT OF COMMERCE

CHIPS for America includes the CHIPS Program Office, responsible for semiconductor incentives, and the CHIPS Research and Development Office, responsible for R&D programs. Both sit within the National Institute of Standards and Technology (NIST) at the Department of Commerce.

NIST promotes U.S. innovation and industrial competitiveness by advancing measurement science, standards, and technology in ways that enhance economic security and improve our quality of life. NIST is uniquely positioned to successfully administer the CHIPS for America program because of the bureau's strong relationships with U.S. industries, its deep understanding of the semiconductor ecosystem, and its reputation as fair and trusted.

Visit https://www.chips.gov to learn more.

TABLE OF CONTENTS

CHIPS for AMERICA

NIST NATIONAL INSTITUTE OF STANDARDS AND TECHNOLOGY
U.S. DEPARTMENT OF COMMERCE

EXECUTIVE SUMMARY

This publication, *Metrology Gaps in the Semiconductor Ecosystem*, describes the creation, development, and strategic priorities of the CHIPS Research and Development Metrology Program (CHIPS R&D Metrology Program). This document combines the results of more than two years of rigorous stakeholder engagement, market research, strategic planning, and organizational development activities completed by NIST to design a program positioned to strengthen the U.S. semiconductor industry through advanced measurement, standardization, modeling, and simulation. *Metrology Gaps in the Semiconductor Ecosystem* describes the program's priority focus areas, the process for selecting these priorities, and anticipated next steps.

This publication serves as a roadmap for the CHIPS R&D Metrology Program's research portfolio. It describes the extensive work that has been undertaken to ensure that the research portfolio is aligned with CHIPS Act, external stakeholder needs, and NIST capabilities.

This publication will be used as a guideline for researchers supported with CHIPS R&D Metrology Program resources to develop project plans, including research activities and outcomes, with overarching goals in line with the CHIPS Act. For each of the 10 programmatic focus areas, there will be a research roadmap outlining research goals, technical activities, and research outcomes and impacts

This publication is divided into two sections:

1. **Overview of the CHIPS R&D Metrology Program:** The overview summarizes the CHIPS Act mandates for the CHIPS R&D Metrology Program, the program's structure, the development timeline, and process for setting R&D priorities.

2. **Development of the CHIPS R&D Metrology Program Strategy:** This section goes into more detail to provide a chronological, in-depth description of program development activities completed to date and the data-driven process for identifying seven

metrology R&D grand challenges ("Grand Challenges"), 32 elements that provide a technical path to overcome those challenges ("Path Forward Elements"), and 10 Priority Programmatic Focus Areas that constitute the initial R&D portfolio scope. This section also describes how NIST will continue to engage with stakeholders to further refine the program's priorities.

NIST has engaged in stakeholder engagement, internal capability assessment, and strategic planning activities since December 2020. Highlights of these activities include:

- execution of two metrology R&D workshops to understand technology gaps affecting onshore semiconductor manufacturing capabilities (April 2022),
- formation of an internal group of NIST metrology subject matter experts (SMEs) and laboratory directors to review stakeholder requirements (October 2022), and
- statistical analysis of portfolio recommendations conducted by NIST researchers to prioritize metrology R&D areas (November 2022).

Data collected through stakeholder engagement and internal planning confirmed that industry, academia, and government organizations require more advanced metrology across all stages of the semiconductor design and manufacturing value chain, including basic and applied R&D in the laboratory, prototyping at scale, factory fabrication, and assembly, packaging, and performance verification. This process resulted in a list of 10 Priority Programmatic Focus Areas to address the highest-priority metrology gaps affecting the domestic microelectronics industry.

The 10 Priority Programmatic Focus Areas for the CHIPS R&D Metrology Program fall into one of two categories:

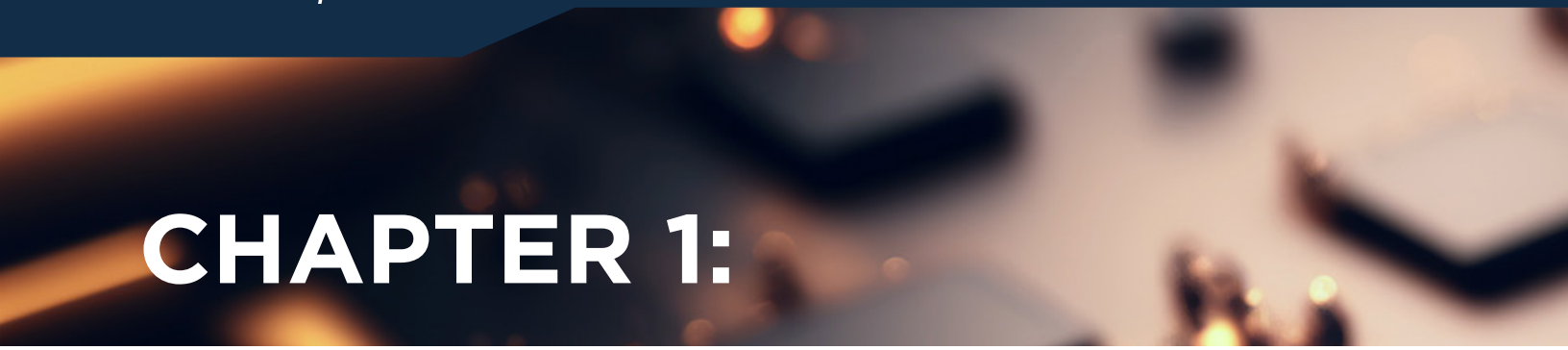
Automation, Virtualization, and Security:

1. Advanced Metrology for Supply Chain Trust and Assurance
2. Verification and Validation of Advanced Models
3. Advanced Modeling for Next-Generation Manufacturing Processes
4. Standards for Automation, Virtualization, and Security
5. Interoperability Standards for Equipment and Software

Metrology for Next-Generation Microelectronics:

1. Metrology for Advanced Materials and Devices
2. Metrology for Nanostructured Materials Characterization
3. Advanced Measurement Services
4. Advanced Metrology for 3D Structures and Devices
5. Materials Characterization Metrology for Advanced Packaging

This publication serves as a resource for stakeholders interested in learning more about the CHIPS R&D Metrology Program and will be used as a tool to assist future program decision-making and R&D investment allocation. It is formal documentation of the NIST process for understanding stakeholder requirements, metrology R&D gaps, and industry trends that directly inform the program's mission, strategy, and operations.



CHAPTER 1:

OVERVIEW OF THE CHIPS R&D METROLOGY PROGRAM

A. CHIPS ACT OVERVIEW

The United States remains a global leader in chip design as well as research and development (R&D), however, has fallen behind in manufacturing and today accounts for only about 10 % of commercial global production.[1] While the U.S. produces few semiconductors, our country remains one of the world's largest users of chips—for entertainment and consumer electronics, for cars and public transportation systems, and for critical systems like utilities and national defense. This makes us vulnerable to supply chain disruptions from far-off events over which we have little control.

Recognizing this, Congress passed the William M. (Mac) Thornberry National Defense Authorization Act for Fiscal Year 2021 (NDAA), of which Sections 9902 and 9906 authorize semiconductor manufacturing and R&D activities in the U.S.[2] The CHIPS Act of 2022 enhanced the CHIPS program with new authorities and appropriated $50 billion to the Department of Commerce to implement the CHIPS for America program.[3] A *Strategy for the CHIPS for America Fund*[4] describes how the Department of Commerce will use this investment to catalyze long-term growth in the domestic semiconductor industry to build a secure and resilient semiconductor supply chain, enhancing our national and economic security. The two main components of the Commerce program are shown in Figure 1.

$39 billion for incentives	**$11 billion for R&D**
Two component programs to:	Four integrated programs to:
• Attract large-scale investments in advanced technologies such as leading-edge logic and memory • Incentivize expansion of manufacturing capacity for mature and other types of semiconductors	• Conduct research and prototyping of advanced semiconductor technology • Strengthen semiconductor advanced test, assembly, and packaging • Enable advances in measurement science, standards, material characterization, instrumentation, testing, and manufacturing

Figure 1: CHIPS for America. The first component is $39 billion for semiconductor manufacturing incentives and the second component is $11 billion for the CHIPS R&D program. The CHIPS R&D program is designed to grow the microelectronics and semiconductor R&D ecosystem.

The metrology provision of the CHIPS Act included below can be found at 15 U.S.C 4656(e), Microelectronics Research at the National Institute of Standards and Technology.

> *"The Director of the National Institute of Standards and Technology shall carry out a microelectronics research program to enable advances and breakthroughs in measurement science, standards, material characterization, instrumentation, testing, and manufacturing capabilities that will accelerate the underlying research and development for metrology of next-generation microelectronics and ensure the competitiveness and leadership of the United States within this sector."*

The CHIPS R&D program is responsible for administering $11 billion to create a dynamic semiconductor innovation ecosystem in the U.S. in collaboration with academia, industry, workforce development organizations, allied nations, and other stakeholders. This effort includes the national semiconductor technology center (NSTC), a National Advanced Packaging Manufacturing Program (NAPMP), and up to three Manufacturing USA institutes to advance research and commercialization of semiconductor technologies.

A critical component of the CHIPS Act is the CHIPS R&D Metrology Program to advance measurement science, standards, material characterization, instrumentation, testing, and manufacturing capabilities, as further described below.

B. OVERVIEW OF THE CHIPS R&D METROLOGY PROGRAM

The CHIPS Act supports metrology's critical role in restoring U.S. leadership in the semiconductor industry through microelectronics research and development of next-generation measurement science methods, standards, and manufacturing methods. The Act specifies metrology activities across the CHIPS R&D initiative. The Act calls for NIST to establish a metrology program that will strengthen the U.S. semiconductor industry through multidisciplinary R&D efforts. The Act also calls for the NSTC to support advanced metrology and characterization for manufacturing of microchips using 3 nanometer transistor processes or more advanced processes as well as metrology for security and supply chain verification. The Act also calls for both the NAPMP and Manufacturing USA institutes to strengthen semiconductor advanced test capabilities to support the domestic ecosystem. Figure 2 illustrates how the metrology program, the subject and scope of this publication, fits within the CHIPS R&D program.

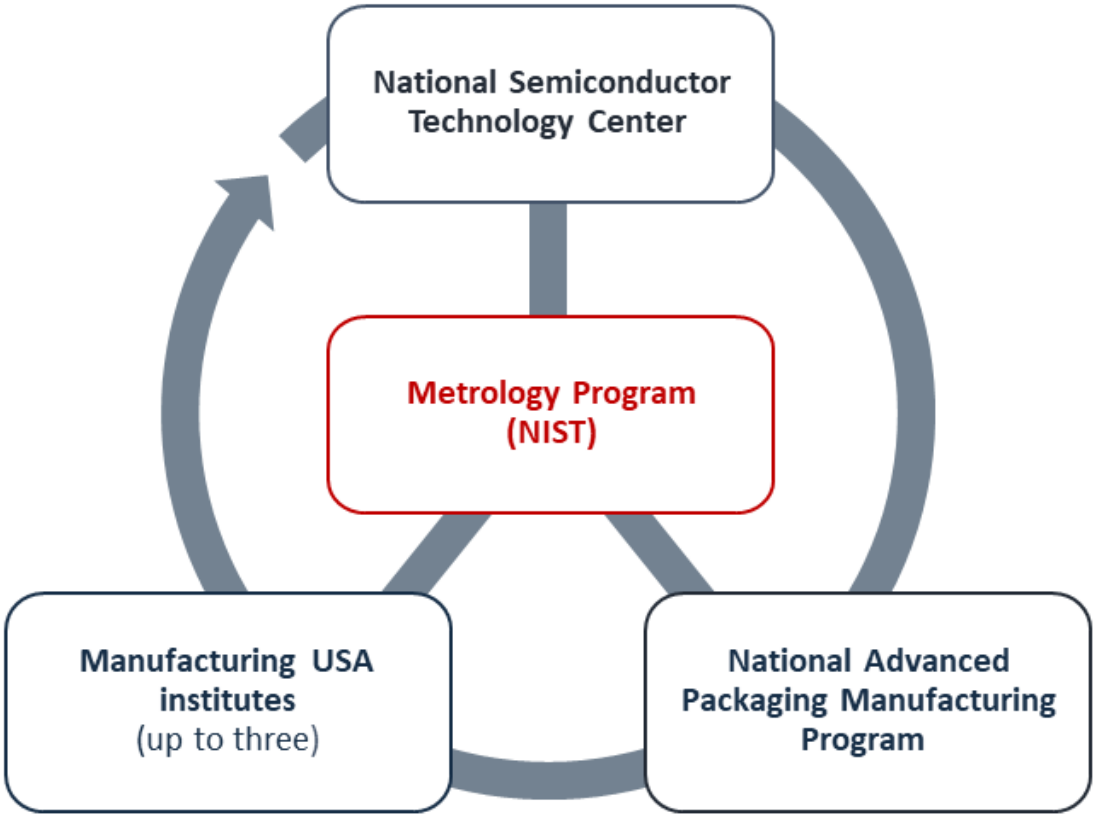


Figure 2: CHIPS R&D Program. The CHIPS R&D program has four components: the Metrology Program, the National Semiconductor Technology Center, the National Advanced Packaging Manufacturing Program, and Manufacturing USA institute(s). Metrology is foundational and fundamental for all CHIPS R&D programs and will be closely tied to other CHIPS R&D programs. The Metrology Program relies on industry stakeholders to identify high-impact research areas. The Metrology Program includes commercialization activities to promote dissemination of program outcomes.

The CHIPS R&D Metrology Program will catalyze innovation with emphasis on measurements that are accurate, precise, and fit-for-purpose for the production of microelectronic materials, devices, circuits, and systems. This work will leverage NIST's proven measurement science expertise, foundational communications and computing research capabilities, standards development contributions, and stakeholder engagement practices to address the highest priority metrology challenges identified across industry, academia, and government agencies. NIST is at the forefront of pioneering new approaches for testing and characterization of integrated devices.[5,6] Through the CHIPS R&D Metrology Program, NIST will expand upon its strong track record of supporting the semiconductor technology and manufacturing ecosystem by developing, advancing, and deploying standards, reference materials, best practices, and measurement methods. As microelectronic systems become more complex, with ever-decreasing feature sizes, and extension into the third dimension, along with an expanding palette of materials, and a more diverse set of devices, the measurement challenges also become more

complex. Through extensive consultation with stakeholders, NIST has identified programmatic focus areas to deliver strategic solutions that will provide a strong foundation for domestic material, equipment, and chip producers to excel.

The CHIPS R&D Metrology Program is committed to ensuring that the direct results of federally funded scientific research are made available and usable by the public, industry, and the scientific community. The semiconductor industry places the highest value on fully vetted data. Outcomes of the CHIPS R&D Metrology Program will include data, measurement methods, reference process design kits, reference materials, standards, publications, and related digital products. The CHIPS R&D Metrology Program will establish a digital exchange ecosystem to provide stakeholders with access to CHIPS metrology research results.

C. CHIPS R&D METROLOGY PROGRAM ALIGNMENT

Soon after the William M. (Mac) Thornberry National Defense Authorization Act for Fiscal Year 2021 (NDAA) became law, the NIST staff gathered information on its current capabilities related to metrology in the semiconductor industry. The outcome of NIST's early stakeholder engagements was the identification of eight metrology R&D topic areas that reflected the technology needs of the U.S. semiconductor industry:

1. Metrology for materials and dimensional scaling
2. In-line metrology for high-throughput manufacturing
3. Material quality for suppliers
4. Digital enablers to improve design and manufacturing
5. Novel metrologies for advanced packaging
6. Critical areas for the future of advanced packaging
7. Materials and devices: characterization, modeling, and design
8. Security and trust across semiconductor development and supply chain

These eight topic areas informed the agenda for two industry workshops[7] convened in April 2022 that identified the highest-priority metrology R&D needs that, if addressed, would strengthen the domestic semiconductor industry. These stakeholder workshops generated findings described in NIST's S*trategic Opportunities for U.S. Semiconductor Manufacturing*[8] report released in September 2022, one of the agency's first publications describing R&D opportunities and gaps related to CHIPS Act priorities. This report identified 7 Grand Challenges and 32 Path Forward Elements that serve as guidance for the metrology R&D needed to build a resilient, secure, and robust U.S. semiconductor industry. As detailed later in Section 2, NIST leadership led an exercise to identify and prioritize programmatic focus areas to be included in the CHIPS R&D Metrology Program research portfolio.

The following data table illustrates how the 10 Priority Programmatic Focus Areas align with the 7 Grand Challenges and 32 Path Forward Elements identified by NIST stakeholders in April 2022.

Summary of CHIPS R&D Metrology Program Focus Area Alignment

In September 2022, NIST published a report titled *Strategic Opportunities for U.S. Semiconductor Manufacturing*, which identifies 7 Grand Challenges that need critical attention from a metrology perspective to achieve the future state vision of a U.S.-led global semiconductor industry. The 7 Grand Challenges encompass a total of 32 Path Forward Elements that describe potential strategies for addressing identified challenges. NIST developed these elements through extensive outreach, knowledge sharing, and coordination with academia, the manufacturing industry, and government partners. Many of the 32 Path Forward Elements described similar R&D concepts aligned with common stakeholder needs. As a result, the CHIPS R&D Metrology Program consolidated the 32 Path Forward Elements into 20 Programmatic Focus Areas in October 2022. By November 2022, the CHIPS R&D Metrology Program further refined its portfolio to a set of 10 Priority Programmatic Focus Areas to address the most critical metrology R&D gaps.

Seven Grand Challenges (7) *Published September 2022*	**Path Forward Elements (32)** *Published September 2022*	**Priority Programmatic Focus Areas (10)** *Published November 2022*
1. Metrology for Materials Purity, Properties, and Provenance: New measurements and standards are needed to satisfy stringent requirements for the purity, physical properties, and provenance of materials.	1. New measurements with increased sensitivity and throughput for detection of particles and contaminants in materials throughout the supply chain, including in-line quality assessment. 2. Innovative, higher-throughput techniques for measuring physical properties for microelectronics feed materials. 3. Evaluation and correlation of properties data across the materials supply infrastructure to support both standards and provenance. 4. Standard Reference Materials (SRMs) for trace impurity detection and reference data, including those for thermophysical properties of materials. 5. Documentary standards that can assist manufacturers in following materials through the supply chain.	Metrology for Advanced Materials and Devices

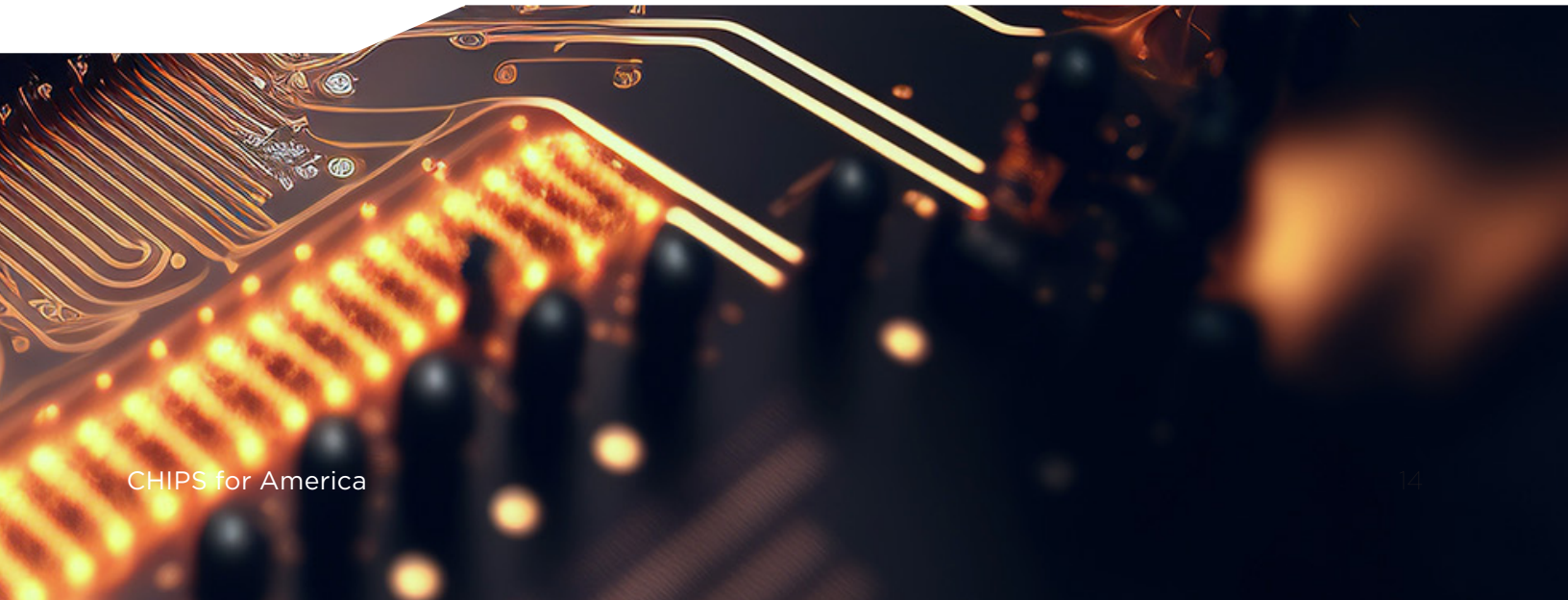
Seven Grand Challenges (7) *Published September 2022*	**Path Forward Elements (32)** *Published September 2022*	**Priority Programmatic Focus Areas (10)** *Published November 2022*
2. *Advanced Metrology for Future Micro-electronics Manufacturing:* Breakthroughs in physical and computational metrology are needed for advanced manufacturing of future-generation devices.	6. Properties of new materials and devices, such as Gate All Around (GAA), Complementary Field Effect Transistor (CFET), and novel interconnects and dialectics. 7. Physical properties characterization for surfaces, buried features, interfaces and, devices with increased resolution, sensitivity, accuracy, and throughput. 8. Rapid, high-resolution, non-destructive techniques for characterizing defects and impurities and correlating them with performance and reliability. 9. Evaluation and correlation of relevant data across the semiconductor manufacturing process. 10. Standards for process design, development, and control, such as reference materials and documentary standards. 11. Statistical analysis for rare but catastrophic defects such as stochastic events in extreme ultraviolet lithography.	Metrology for Advanced Materials and Devices Metrology for Nanostructured Materials Characterization

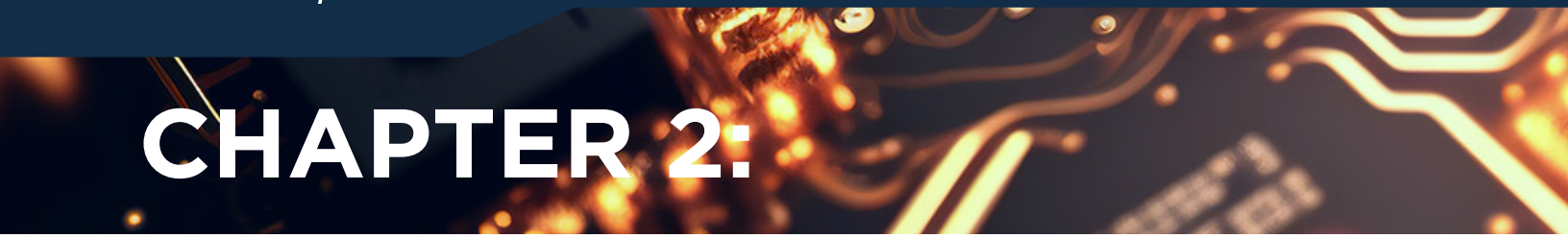
Seven Grand Challenges (7) *Published September 2022*	**Path Forward Elements (32)** *Published September 2022*	**Priority Programmatic Focus Areas (10)** *Published November 2022*
3. *Enabling Metrology for Integrating Components in Advanced Packaging:* New metrology is needed to enable complex integration of sophisticated components and novel materials for advanced microelectronics packaging.	12. Measurements for in situ, rapid measurements and verification methods for interfaces and subsurface interconnects, and internal 3D structures including warpage, voids, substrate yield, stresses, adhesion, and reliability with improved throughput and resolution. 13. Physical properties for films, surfaces, buried features, and interfaces. 14. Methods for integrating chiplets, dialects, Systems on a Chip (SoCs), and memories into packages. 15. Mechanical measurements for component integration. 16. Evaluation and correlation of data across the packaging process. 17. Standards for packaging, such as reference materials and documentary standards for areas including chiplets and SoCs.	Advanced Metrology for 3D Structures and Devices Materials Characterization Metrology for Advanced Packaging

Grand Challenges (7) *Published September 2022*	**Path Forward Elements (32)** *Published September 2022*	**Priority Programmatic Focus Areas (10)** *Published November 2022*
4. *Modeling and Simulating Semiconductor Materials, Designs, and Components:* Advanced metrology tools are needed for effectively modeling and simulating next-generation semiconductor materials, processes, devices, circuits, and system designs.	18. Multi-physics models, including those that capture thermal, chemical, physical, mechanical, signal integrity, reliability, power consumption, and other parameters. 19. Measurements of material, component, and circuit properties across a broad temperature, bias, and frequency range as input to, and as verification of, the above models. 20. Application and validation of advanced analytics such as machine learning (ML) and artificial intelligence (AI) for modeling and optimization of complex materials, circuits, and systems operating in real environments. 21. Methods for robustly estimating model uncertainty.	Verification and Validation of Advanced Models
5. *Modeling and Simulating Semiconductor Manufacturing Processes:* Breakthroughs are needed to enable tools to seamlessly model and simulate the entire semiconductor manufacturing process.	22. Modeling, data analysis, and validation tools to enable efficient process development and optimization. 23. Standards, protocols, and standards data for automation and virtualization. 24. Measurements and standards supporting digital twins, from individual processing steps up to complete chip fabrication and system assembly. 25. Application and validation of advanced analytics such as ML and AI for modeling and optimization of complex manufacturing process design, development, automation, and integration.	Advanced Modeling for Next-Generation Manufacturing Processes

Seven Grand Challenges (7) *Published September 2022*	**Path Forward Elements (32)** *Published September 2022*	**Priority Programmatic Focus Areas (10)** *Published November 2022*
6. *Standardizing New Materials, Processes, and Equipment for Microelectronics:* New standards and validation methods are needed to accelerate the development of future information and communication technologies.	26. SRMs, data, instruments, and calibration and measurement services; product development kits, and a diversity of best-known methods. • Reference materials to detect defects, contaminants, and trace impurities at the nanoscale. • Reference materials for nanoscale dimensional and materials characterization. • Calibration, validation, and new methods to enable high-accuracy fleet matching for equipment in both process development and high-volume manufacturing (i.e., matching the suite of tools to the process/materials of use). • SRMs and data for advanced packaging and heterogeneous integration, including high-frequency electrical properties and thermomechanical properties. 27. Standards for interoperable equipment and software from different vendors that ensure the protection of intellectual property, data integrity, and provenance across the supply chain. 28. Standards for tracking materials from creation to end use in the fab, including anything that could alter the properties of the material.	Advanced Measurement Services Interoperability Standards for Equipment and Software Standards for Automation, Virtualization, and Security

Seven Grand Challenges (7) *Published September 2022*	**Path Forward Elements (32)** *Published September 2022*	**Priority Programmatic Focus Areas (10)** *Published November 2022*
7. *Metrology to Enhance Security and Provenance of Microelectronic-based Components and Products:* Advances in metrology are needed to enhance the security and provenance of microelectronic components and products across supply chains and to improve trust and assurance.	29. Methods, reference design kits, and guidelines for security analytics and automation, including pervasive security to address formalized threat models. 30. Enhanced vulnerability management across the overall product life cycle from inception to end of life. • Formal testing and processes for independent verification and validation. • Tracking of materials and components, as well as detecting and mitigating trigger mechanisms. • Common test structures, test methods, and test and measurement strategies for end-to-end provenance. 31. Documentary standards for hardware security and provenance. 32. Development and use of trusted emerging techniques (AI and ML methods) across the entire semiconductor value chain.	Advanced Metrology for Supply Chain Trust and Assurance





CHAPTER 2:

DEVELOPMENT OF THE CHIPS R&D METROLOGY PROGRAM STRATEGY

This section describes the process by which NIST identified areas for investment of CHIPS R&D Metrology Program resources.

In June 2021, the NIST Leadership Board (NLB)[9] created a formal working group to help NIST establish a vision for how the CHIPS R&D Metrology Program would achieve the goals set out in the NDAA. The outcome of NIST's early stakeholder engagements was the identification of eight metrology R&D topic areas that reflected the technology needs of the U.S. semiconductor industry.

A. INITIAL PROGRAM PLANNING AND STAKEHOLDER ENGAGEMENT

April 2021: Preparatory Phase for the CHIPS R&D Metrology Program

In April 2021, the NLB engaged the chief of the Nanoscale Device Characterization Division to assess and characterize the current NIST metrology landscape, relevant aspects of the semiconductor manufacturing industry, and concepts around metrology R&D portfolios that supported the language in the NDAA. By June 2021, the NIST Semiconductor Metrology Working Group was formed, consisting of SMEs representing the six NIST laboratory programs. The working group's initial objective was to understand fundamental metrology R&D gaps affecting domestic semiconductor researchers. This would serve as the basis for more targeted stakeholder engagement, gap identification, and priority setting for the CHIPS R&D Metrology Program. The working group first studied the historical landscape of NIST capabilities and previous metrology advancements. Next, they evaluated the newly identified areas of metrology research as they pertained to the future needs of the microelectronics industry and the gaps in current capabilities. The working group continued its engagement efforts through March 2022, interacting with domestic and global stakeholders from industry and academia to identify areas in which metrology could play a critical role in supporting microelectronics R&D innovation. As part of this engagement, NIST executed bilateral discussions, knowledge sharing sessions, seminars, webinar series, and virtual workshops to collect program planning data.

From this research, the working group developed a comprehensive project plan in February 2022 highlighting overarching objectives, the future vision, possible initiatives, and. This project plan provided an overview of the four technical program elements (listed below) that would enhance future breakthroughs in microelectronics metrology while aligning with the goals of the CHIPS Act.

1. Advance physical metrology for next-generation microelectronics, including 3D transistors, 3D memory, and 3D heterogeneous integration/advanced packaging.

2. Accelerate innovation in computational metrology, virtualization, and automation through improved collection, distribution, and consumption of manufacturing and metrology datasets.

3. Develop and deliver critically needed measurement services (e.g., Standard Reference Materials (SRMs), calibration services, Standard Reference Instruments (SRIs) and Standard Reference Data (SRD)).

4. Facilitate and support metrological and documentary standards development in areas of industry priority.

The working group also analyzed the needs of the industry and how those needs could be addressed through the CHIPS Act and NIST directives.[10] The working group established three enabling program elements to ensure programmatic success:

1. Establish a state-of-the-art metrology laboratory with equipment, tool sets, and facilities essential for conducting next-generation microelectronics research in collaboration with academia and industry.

2. Engage and collaborate with external stakeholders (e.g., U.S. industry, academia, standards development organizations, and technical and professional organizations) in planning and executing the CHIPS R&D Metrology Program in coordination with relevant programs (e.g., NSTC, NAPMP, Manufacturing USA Institutes, recipients of

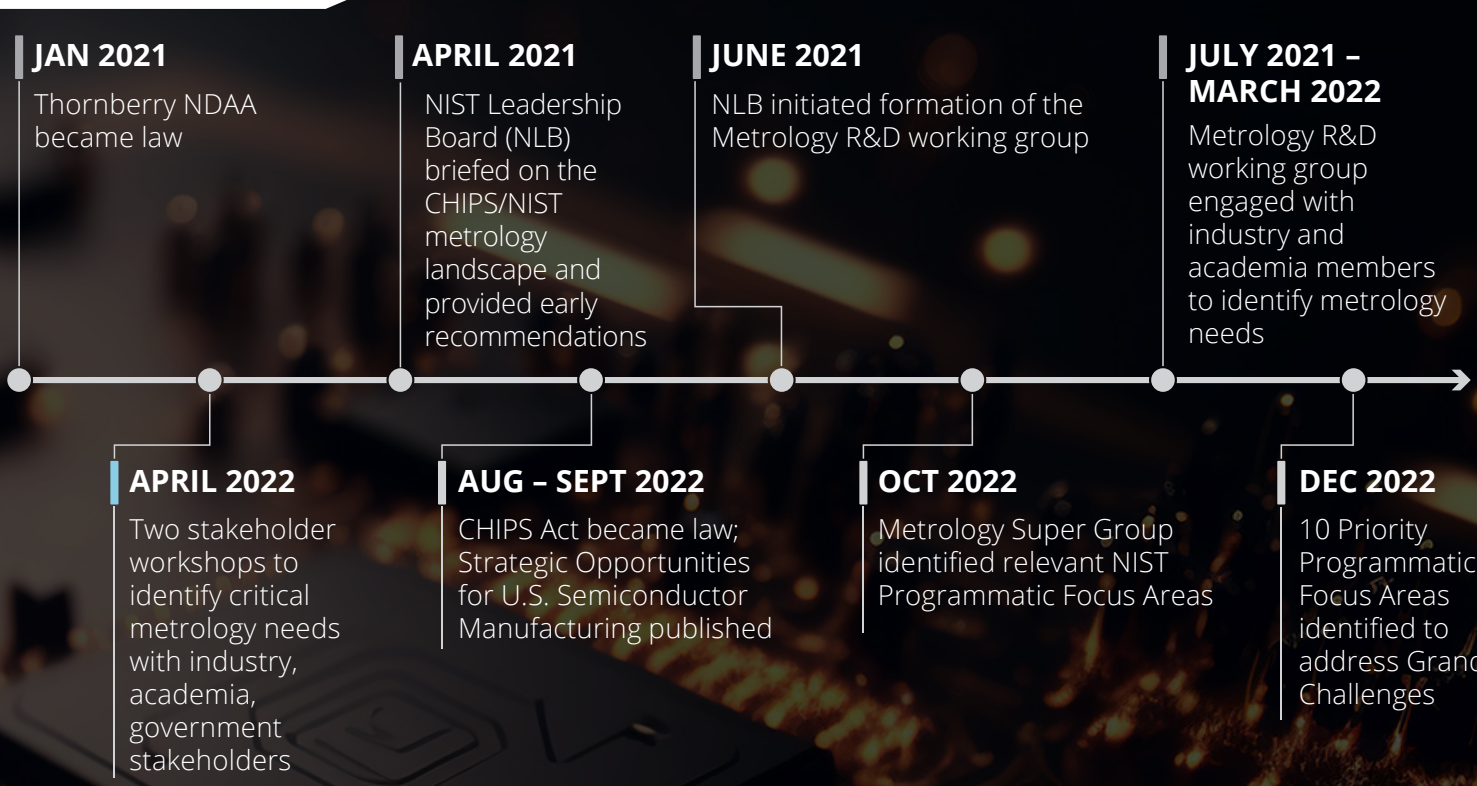


Figure 3: Timeline of CHIPS R&D Metrology Program Development Activities

CHIPS Act Incentives, and academic and private sector research centers) for increased impact and to expedite dissemination and adoption. Special efforts will be made to target minority-serving institutions and underserved communities.

3. Develop talent and workforce through advanced research experiences for postdoctoral students, graduate students, and other research associates from U.S. industry and academia.

NIST staff members developed the four technical program elements and three enabling program elements described above through extensive market research and reviews of literature describing the evolving needs of the domestic semiconductor industry. The working group built on this initial assessment of the industry landscape by engaging with stakeholders representing commercial entities, academic institutions, government agencies, and standards organizations supporting microelectronic metrology innovation. This outreach allowed NIST staff members to begin planning stakeholder engagements to advance program strategy, such as the semiconductor metrology R&D workshops hosted in April 2022, and helped determine the eight major topics covered in those discussions.

July 2021 - March 2022: NIST Conducts External Stakeholder Engagement

Beginning in the summer of 2021 and extending through March 2022, the working group engaged microelectronic stakeholder organizations to determine what gaps were present in metrological advancement and to identify the risks they posed for the manufacturing industry in the U.S. To begin collecting data, the working group hosted listening sessions and seminars to engage with industry, academia, government, and standards organizations. They developed a regular NIST Semiconductor Seminar Series to meet weekly to aggregate and align relevant agency-wide expertise and capabilities with stakeholder-identified microelectronic metrology R&D needs. The working group obtained insights discussed during the NIST Semiconductor Seminar Series by collaborating with each of the NIST laboratories, artificial intelligence researchers, and the National Cybersecurity Center of Excellence.

The working group developed over 100 one-slide briefs capitalizing on current NIST research in metrology, standards, and other research areas related to microelectronics manufacturing as a reference point for industry engagement. NIST engaged with private-sector innovators and academic institutions invested in semiconductor metrology research through one-on-one interviews, email correspondence, and technical presentations. These engagements illustrated how NIST and other stakeholders could advance the metrology and modeling of emerging design, fabrication, testing, packaging, and assembly technologies. The key findings of this initial stakeholder engagement effort revealed that metrology is a fundamental technology enabler needed across all aspects of the semiconductor supply chain as the industry moves to advanced devices based on emerging 3D devices and heterogeneous integration. Industry and academic leaders expressed strong interest in collaborating with NIST to address these metrology needs for advanced devices. Stakeholders noted that 3D metrology standards and various services such as transistor design, circuit design, the physical characterization of internal components and materials, and manufacturing processes need to account for vertical (three-dimensional) rather than horizontal (two-dimensional) microelectronic architectures.

The preliminary conversations that took place during these working sessions, along with the structure and strategies that the working group developed, paved the way for the next phase of external engagement: stakeholder workshops. This outreach helped the working group outline several topic areas to present to a broader population of private sector, academic, and government stakeholders to reference when brainstorming top-priority R&D challenges affecting advanced metrology, and strategies needed to enhance competitiveness in the global market.

April 2022: NIST Hosts External Metrology R&D Workshops

In April 2022, NIST held two semiconductor metrology R&D workshops that convened metrology experts from industry, academia, government, nonprofit research institutions, and the working group to identify metrology needs for advances in semiconductor manufacturing. This allowed NIST to develop a neutral data collection process for external stakeholder input, thus capturing metrology requirements of a diverse group of semiconductor companies and academic researchers. Both workshops included two full-day sessions featuring panel discussions and breakout groups to foster collaboration and identify specific, actionable metrology R&D technology gaps. To reach a sufficient number and diversity of stakeholders, NIST staff members notified the public by posting the workshop agenda and an event flyer[11] on the NIST website, promoting workshop registration at six NIST CHIPS Act events[12] in February and March 2022, and developing an email distribution list reaching over 1,000 semiconductor metrology experts in industry, academia, and government, and nonprofit research institutions.

External stakeholders engaged with NIST SMEs throughout the two workshops; the first workshop was attended by more than 400 attendees and the second workshop was attended by more than 350 attendees. The first and second workshops featured breakout sessions with stakeholders from industry, academia, government, and nonprofit research institutions; they were attended by more than 145 participants. The participants had research backgrounds that spanned a variety of semiconductor fields such as supply chain, manufacturing, and packaging. NIST hosted and moderated both workshops with the help of additional facilitators. The workshops enabled NIST staff to collect extensive insights into stakeholder needs and identify translational metrology research challenges that must be addressed for next-generation microelectronics. These stakeholder-focused workshops generated the data required to write and publish NIST's Strategic Opportunities for U.S. Semiconductor Manufacturing report.

B. DEVELOPMENT OF THE SEVEN GRAND CHALLENGES

June 2022 - September 2022: NIST Publishes the Seven Grand Challenges

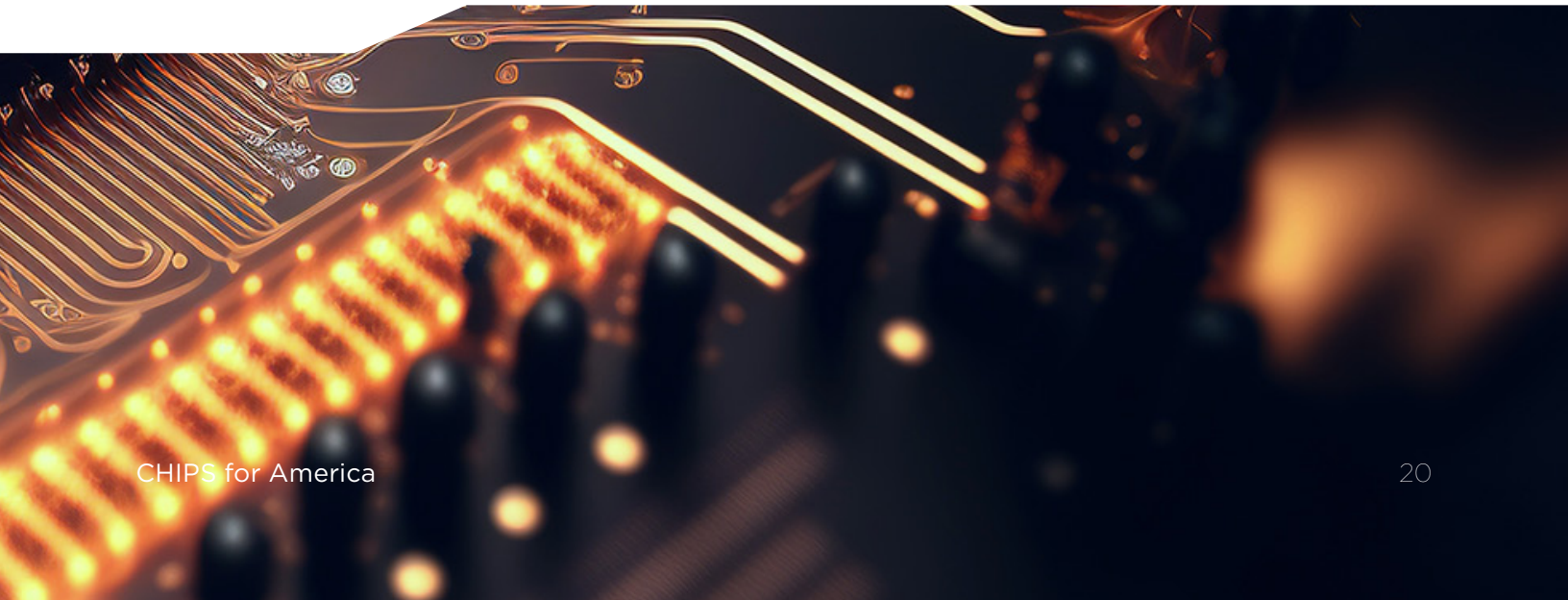
To identify gaps in microelectronic metrology critical to enhanced U.S. competitiveness, NIST analyzed stakeholder input and recommendations from the April 2022 workshops and published the findings in the Strategic Opportunities for U.S. Semiconductor Manufacturing document in September 2022. This document highlights the 7 Grand Challenges for metrology and aligns those challenges with actionable strategies and 32 Path Forward Elements for NIST to consider for future projects. The purpose of this document was to distill findings from stakeholder engagement conducted by the CHIPS R&D Metrology Program between July 2021 and April 2022. This document represents the views and

THE SEVEN GRAND CHALLENGES:

A U.S.-led semiconductor industry's future depends on improving the domestic sectors, and that effort begins with addressing the critical needs at various levels. The seven Grand Challenges are introduced in the Strategic Opportunities for the U.S. Semiconductor Industry document, where each challenge elaborates on the collective metrology needs of the industry in measurement, standardization, and modeling and simulation. It is serving as a vital tool for the leadership to understand the pressing needs of the industry and pathways to overcome those challenges utilizing the resources made available by the CHIPS Act.

Grand Challenge	Industry Gaps	Strategic Focus
Metrology for Materials Purity, Properties, and Provenance	Meet increasingly stringent requirements for semiconductor materials purity, physical properties, and provenance across a diverse supply chain through the development of new measurements and standards.	Develop measurement technologies, properties data, and standards focused on defect and contaminant identification to support uniform materials quality and traceability across the supply chain.
Advanced Metrology for Future Microelectronics Manufacturing	Ensure that critical metrology advances are made to keep pace with cutting-edge and future microelectronics and semiconductor manufacturing, while maintaining a competitive U.S. advantage.	Advance the physical and computational metrology tools adaptable to next-generation manufacturing of advanced complex, integrated technologies, and systems.
Enabling Metrology for Integrating Components in Advanced Packaging	Provide enabling metrology that spans multiple length scales and physical properties and supports acceleration of advanced packaging concepts for future-generation microelectronics.	Develop metrology for complex integration of sophisticated components and new materials to support a strong domestic advanced microelectronics packaging industry.
Modeling and Simulating Semiconductor Materials, Designs, and Components	Improve the tools needed to effectively model and simulate future semiconductor materials, processes, devices, circuits, and microelectronic system designs.	Create advanced design simulators using multi-physics models and next-generation concepts such as artificial intelligence and digital twins, empowering U.S. microelectronics designers.

Grand Challenge	Industry Gaps	Strategic Focus
Modeling and Simulating Semiconductor Manufacturing Processes	Seamlessly model and simulate the entire semiconductor value chain, from materials inputs to chip fabrication, system assembly and end products.	Develop advanced computational models, methods, data, standards, automation, and tools to enable domestic semiconductor manufacturers to improve yields, accelerate time to market and enhance competitiveness.
Standardizing New Materials, Processes, and Equipment for Microelectronics	Create the standards and validation methods necessary to accelerate the development and manufacturing of future information and communication technologies.	Create standards, validation tools and protocols for next-generation materials, processes, and equipment, paving the way for accelerated innovation and cost-competitiveness in U.S. industry.
Metrology to Enhance Security and Provenance of Microelectronic-based Components and Products	Create the metrology advances needed to enhance the security and provenance of microelectronic components and products across supply chains and increase trust and assurance.	Pursue a comprehensive approach to hardware security protection that includes standards, protocols, formal testing processes, and advanced computational technologies, while providing avenues for assurance and provenance of microelectronic components across the supply chain and end products.



perspectives on high-priority R&D challenges for microelectronic metrology as expressed by NIST stakeholders. In addition to the challenges described, NIST developed 32 Path Forward Elements that proposed strategic and actionable next steps that were distributed across the 7 Grand Challenges. The report also describes why the 32 Path Forward Elements support a particular Grand Challenge and how the R&D community supporting semiconductor metrology innovation could be positioned to drive required technical breakthroughs. The chart below outlines each of the seven Grand Challenges as well as the strategic focus points needed to address each gap.

The seven Grand Challenges were developed to provide insight into future semiconductor industry metrology needs and begin developing actionable strategies to address them. These challenges were developed through sustained engagement with industry to identify research and technology gaps, limitations of current resources, and the need for a shared understanding of priority focus areas for the future of microelectronics metrology. The publication of the Strategic Opportunities for U.S. Semiconductor Manufacturing report represents an early step toward formalizing the program's assessment of the microelectronic industry's highest-priority metrology challenges and examining how these needs aligned with NIST's mission.

After the publication of the *Strategic Opportunities for U.S. Semiconductor Manufacturing* report, the working group recognized that the 32 Path Forward Elements described many overlapping metrology concepts and R&D strategies that could be consolidated to eliminate redundancy within the list and more closely align microelectronic metrology needs with NIST's capabilities and mission. Guided by the principle of addressing

THE SEVEN GRAND CHALLENGES DEVELOPMENT: KEY STATISTICS

- Six months of stakeholder outreach
- Frequent webinars and educational seminars
- Two stakeholder workshops
- 400+ participants
- Over 60 % of participants represented private industry, academia, standards organizations, or nonprofit research organizations

20 PROGRAMMATIC FOCUS AREAS

Based on their similarities and aptitudes, 32 Path Forward Elements are grouped into 20 Programmatic Focus Areas. Each focus area addresses needs in multiple technological areas across the semiconductor industry. Investments in these R&D-focused areas will be essential to empower the domestic semiconductor industry.

metrology R&D gaps that could be applied to a wide variety of semiconductor-enabled use cases related to communications, computing, life sciences, transportation, and national security, the working group initiated a process to down select the 32 Path Forward Elements into 20 Programmatic Focus Areas. The development of 20 Programmatic Focus Areas achieved two objectives while retaining the scope and content of the original 32 Path Forward Elements. First, the Programmatic Focus Areas remained consistent with input collected from stakeholders participating in the April 2022 workshops. Second, they illustrated high priority R&D areas for NIST leadership to consider during future R&D portfolio planning and investment decision-making.

In October 2022, the acting director of the CHIPS R&D Metrology Program determined that the 20 Programmatic Focus Areas still represented too broad of a range of R&D topic areas to include in the program's initial portfolio. The acting director recruited data analysts from the NIST ITL Statistical Engineering Division ("the ITL team") and tasked these individuals with developing a process to further refine the 20 Programmatic Focus Areas by crowdsourcing recommendations from NIST metrology SMEs on the R&D priorities that would most effectively deliver on CHIPS Act directives. The ITL team designed a decision analytic framework that leveraged the expertise beyond a single decision-maker to account for diverse interpretations of the CHIPS Act and semiconductor R&D objectives that may be unique to different NIST laboratories. The ITL team then developed a quantitative survey instrument based on this crowdsourcing framework to evaluate a subset of the 20 Programmatic Focus Areas for potential inclusion in a more focused CHIPS R&D Metrology Program portfolio.

C. FORMATION OF THE NIST METROLOGY SUPER GROUP

October 2022: NIST Identifies and Recruits Super Group Members

The acting director of the CHIPS R&D Metrology Program identified 54 lead researchers and managers at NIST who had experience and expertise in the microelectronics space. This group of experts became known as the NIST Super Group. Their expertise enabled the prioritization of the 20 Programmatic Focus Areas into 10 Priority Programmatic Focus Areas.

To begin the prioritization exercise, Super Group members reviewed the CHIPS Act with associated supporting information and discussed the legislation's primary goals. Then the ITL team instructed each Super Group member to identify a portfolio containing up to 10 Priority Programmatic Focus Areas that the member felt best addressed, according to their own understanding, the needs described in the CHIPS Act. Portfolio selection criteria were unprompted, as the Super Group was instructed to make their selections based upon focus areas they viewed as the most effective means to advance the CHIPS Act's overarching goals and enhance semiconductor metrology in the U.S. The ITL team advised experts to prioritize the metrology topics that would be most impactful to domestic semiconductor manufacturing capabilities, but Super Group members were allowed to consider NIST capabilities and interests when selecting their portfolio. This approach was distinctly different from a simple ranking exercise as portfolio identification allowed for the Super Group members to consider interdependencies among selected programmatic focus areas. The ITL team sought to understand both these interdependencies and the relative importance of the selected programmatic focus areas through this exercise.

D. NIST METROLOGY PORTFOLIO SELECTION

October 2022: Super Group Selects Priority Programmatic Focus Areas

The ITL team's first step toward identifying and prioritizing Super Group members' recommended CHIPS R&D Metrology portfolio was to establish their data collection model. The ITL team created a custom web application that allowed respondents to provide their preferences consistent with the data collection model. The ITL team survey included five focused sections, presenting a sequence of steps for Super Group members to select a portfolio. Members first entered their name, organizational unit (OU), degree areas, and professional experience. This collection of demographic information allowed the ITL team to examine the overall makeup of the Super Group in terms of technical backgrounds and experiences. These demographics also prepared the ITL team to analyze and interpret results from an organizational standpoint, understanding how an individual's background impacted their scoring of each programmatic focus area and identifying potential biases related to organizational or research interests.

Members were then presented with a list of the 20 Programmatic Focus Area titles and directed to select up to 10 to include in their portfolio. Each of the programmatic focus area titles had a link to a full description derived from the seven Grand Challenges publication. These titles appeared in random order each time the survey was accessed to minimize bias in participant responses due to the specific ordering of the programmatic focus area options. Respondents were asked to select their portfolio of programmatic focus areas not based on the needs of their laboratory or their own personal research interests, but rather on what programmatic focus areas were most vital in achieving the objectives of the CHIPS Act. Once respondents selected up to 10 Priority Programmatic Focus Areas for inclusion in their respective portfolios, they proceeded to provide a relative importance score for each one. Each programmatic focus area within the portfolio was provided a score ranging from 1 to 10 that represented how important each respondent believed that focus area was in comparison to the others within their portfolio. For example, a programmatic focus area scored 10 was interpreted to be twice as important as a focus area that received a score of 5. When a respondent felt that multiple programmatic focus areas had similar levels of importance, the same relative score was assigned to these areas.

After creating their portfolios and establishing relative importance scores for each programmatic focus area within their portfolio, respondents were asked to identify any groupings of focus areas where they felt that interdependencies (synergies) existed. Specifically, participants were instructed to identify groups of programmatic focus areas within their portfolios that provided a larger overall benefit toward achieving the goals of the CHIPS Act when treated as a group rather than as the sum of the contributions from the individual focus areas. For each interdependent group, the strength of the synergies was solicited using a drop-down menu and a low, medium, and high scale.

In the final section of the survey, respondents were given an opportunity to provide a rationale for their choices, which included specific input on their selections of programmatic focus areas and their relative importance scores, as well as their synergy groupings. This input provided direct, qualitative feedback into why the respondents selected their programmatic focus areas, as well as justification for their relative importance

scores. It also gave the ITL team insight into how these individuals felt their choices effectively supported the goals of the CHIPS Act and the need for metrology advancement. Respondents had approximately one week to review the CHIPS Act language and complete the survey.

E. CLUSTER ANALYSIS RESULTS

Mid-November 2022: ITL Team Begins Analyzing and Interpreting Responses

To analyze the results of the data collection, the ITL team assessed the general composition of the portfolios provided by the Super Group. After exploring general overall trends across the portfolios provided, the ITL team analyzed, via quantitative identification of similarities and differences among the set of portfolios, and the fundamental number and nature of the collective voices within the Super Group. To accomplish this task, the ITL team used statistical cluster analysis followed by intra-cluster characterization methods to understand key programmatic focus areas within each portfolio, if necessary.

By mid-November 2022, after developing the survey application and receiving the participant responses, the results of the Super Group were analyzed. Out of 54 individuals, 50 total experts responded to the survey, which the ITL team deemed a tremendous response rate. The immediate general trends observed showed that many experts (32) included the maximum number of programmatic focus areas (10) in their portfolios, but some included fewer, with 6 being the fewest number of focus areas included in a Super Group member's portfolio. The programmatic focus area Metrology for Advanced Materials and Devices was included in more portfolios (36) than any other focus area. The ITL team leveraged a robust set of cluster analysis techniques to examine the degree of agreement among the 50 portfolios. Every cluster analysis technique considered illustrated that not all experts agreed. Rather, there were two distinct groups (clusters) of portfolios where a high level of agreement within the group was achieved.

After reviewing the initial findings of the cluster analysis, the ITL team dug deeper into the data to determine the meaning of the clusters in terms of programmatic focus area priority. They began by analyzing where most responses came from, and how the background of these individuals impacted their portfolio composition. This analysis showed that participants were largely split between a material science-centric background and an IT and modeling-centric background. One cluster had a large portion of respondents from both the ITL and the Engineering Laboratory. These respondents more often included IT and modeling programmatic focus areas in their portfolios, such as Advanced Supply Chain Trust and Assurance, Modeling for Manufacturing Process, and Process Optimization. The other cluster showed a stronger correlation with respondents with a background in physics, chemistry, and physical sciences. This group included a higher proportion of respondents from the Physical Measurement Laboratory (PML), Material Measurement Laboratory (MML), and Communications Technology Laboratory (CTL). These respondents more often included the materials science programmatic focus areas in their portfolios, such as Advanced Packaging, Measurement Services, and Materials and Devices. Soliciting the input of 50 experts representing all NIST laboratory programs was intended to minimize organizational bias in the portfolio selection process. However, cluster analysis results indicated that the top priority focus areas for the CHIPS R&D Metrology Program identified by the Super Group align with proven NIST research capabilities related to automation, virtualization, security, standards development, and physical measurement techniques.

From each cluster, the ITL team identified the programmatic focus areas that were most prominent among the portfolios in terms of inclusion and average relative importance score. The ITL team proposed that the top five programmatic focus areas from each cluster be considered for further pursuit. The following list presents the top five programmatic focus areas within each cluster in descending priority order.

Automation, Virtualization, and Security:

1. Advanced Metrology for Supply Chain Trust and Assurance
2. Verification and Validation of Advanced Models
3. Advanced Modeling for Next-Generation Manufacturing Processes
4. Standards for Automation, Virtualization, and Security
5. Interoperability Standards for Equipment and Software

Metrology for Next-Generation Microelectronics:

1. Metrology for Advanced Materials and Devices
2. Metrology for Nanostructured Materials Characterization
3. Advanced Measurement Services
4. Advanced Metrology for 3D Structures and Devices
5. Materials Characterization Metrology for Advanced Packaging

The ITL team's cluster analysis approach, with the Super Group's input, allowed NIST to take the 32 original Path Forward Elements, consolidate them into 20 Programmatic Focus Areas, and then further consolidate them into 10 Priority Programmatic Focus Areas to inform the future path of actionable research projects. Creating a Super Group with representation from each OU at NIST provided the ITL team with a holistic view of each department's priorities. These 10 Priority Programmatic Focus Areas provide an outline for actionable projects that NIST will begin planning, implementing, and recruiting partnerships for to ensure the metrological needs in these two areas are not neglected.

F. NIST CAPACITY FOR CHIPS ACT IMPLEMENTATION

The CHIPS R&D Metrology Program identified the 10 Priority Programmatic Focus Areas through stakeholder-driven gap identification, market and policy analysis, and internal evaluation. This process yielded a robust microelectronic R&D community and actionable findings that equip this program to meet the needs and priorities described in the CHIPS Act. As a result, the CHIPS R&D Metrology Program is positioned to support CHIPS Act mandates by delivering enhanced metrological capabilities to all sectors of the microelectronic manufacturing industry through intramural research, external funding opportunities, and continuous stakeholder engagement. NIST metrology R&D capabilities have played an essential role in the communications, computing, and materials science innovation ecosystem for decades. The semiconductor industry represents a diverse set of stakeholders that will increasingly rely on high-performance, scalable microelectronic design and manufacturing capacity to remain competitive. CHIPS R&D Metrology Program researchers plan to equip these stakeholders with technical leadership and innovation to transform current challenges into well-scoped R&D opportunities and differentiate onshore manufacturing capabilities from international competition. The CHIPS R&D

Metrology Program features experts with a proven track record of developing disruptive measurement science approaches, contributing lasting standards, and providing datasets and tools that reduce barriers to innovation.

The CHIPS R&D Metrology Program will leverage insights collected since April 2021 to scope near-term R&D project ideas that maximize the efficiency and impact of current funding. NIST will implement a variety of stakeholder engagement activities to ensure program activities continue to target high-priority metrology needs and complement—rather than overlap with— other microelectronic R&D investments pursued by industry, academia, and government. In January 2023, NIST revisited its earlier assessment of U.S. semiconductor industry R&D needs to serve as an input to permanent stakeholder engagement and strategic planning processes

Aligning Focus Areas with U.S. Semiconductor Industry Needs

To ensure that these programmatic focus areas and future project milestones align with high-priority industry needs, the CHIPS R&D Metrology Program conducted a landscape assessment that leveraged two microelectronic industry roadmaps published by the IEEE: *The Heterogeneous Integration Roadmap*,[13] and the *International Roadmap for Devices and Systems, Metrology Chapter*.[14] This meta-analysis identified shared technology gaps and innovation opportunities affecting current and future microelectronics metrology stakeholders and validated data collected during the CHIPS R&D Metrology Program development. The findings published in the *Heterogeneous Integration Roadmap and International Roadmap for Devices and Systems, Metrology Chapter* corroborated NIST's baseline understanding of the current landscape of the microelectronics industry, evolving semiconductor technology requirements, and agreed-upon short- and long-term metrology needs.

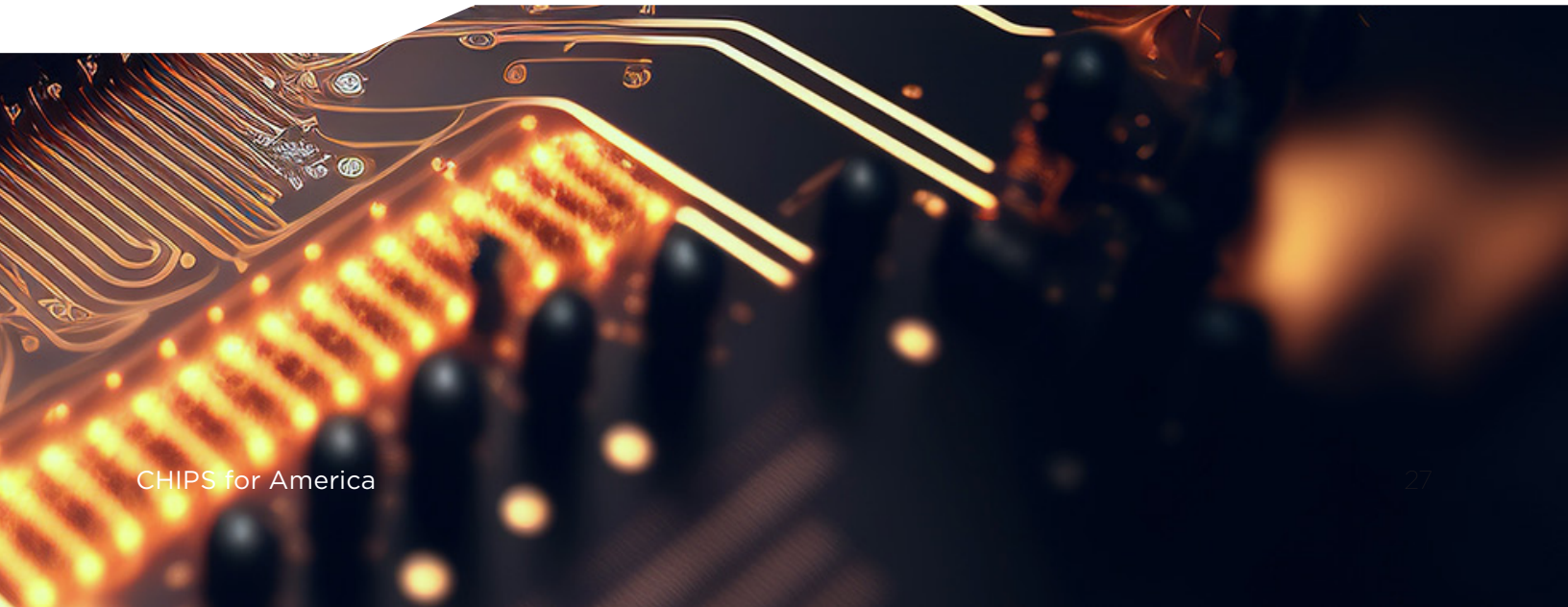
NIST compared external roadmap findings against the results of the cluster analysis conducted by the ITL team and definitions for the 10 Priority Programmatic Focus Areas to validate the program's initial investment focus. These two IEEE roadmaps provide a list of critical technology enablers related to manufacturing process control and quality assurance across the semiconductor supply chain that NIST referenced to guide stakeholder engagement activities supporting CHIPS R&D Metrology Program development. Ongoing NIST analysis of these and other semiconductor roadmap documents will be used to evaluate how projects selected within the 10 Priority Programmatic Focus Areas align with industry needs, deliver impact to NIST stakeholders, and complement ongoing R&D activities supporting microelectronics metrology.

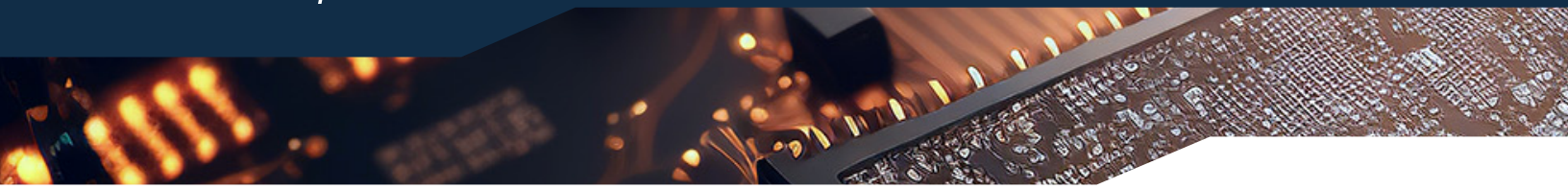
Future Stakeholder Engagement and Strategic Planning

The rigorous stakeholder engagement activities completed since 2021 played a critical role in defining the mission, vision, and 10 Priority Programmatic Focus Areas guiding the CHIPS R&D Metrology Program's strategy and future funding decisions. Data collected through stakeholder interviews and workshops confirmed that both private sector and academic R&D organizations require more advanced metrology capabilities across all stages of the semiconductor technology design and manufacturing process: basic and applied R&D in the laboratory, prototyping at scale, factory fabrication, assembly, packaging, and performance verification. The CHIPS R&D Metrology Program remains committed to a stakeholder-driven approach to program development that will continuously leverage

subject matter expertise from leading microelectronic suppliers, manufacturers, product developers, and system designers to gather requirements, assess technology gaps, collect feedback, and evaluate impact.

Moving forward, CHIPS R&D Metrology Program leadership will reference input provided by internal and external stakeholders for budget formulation and execution, project prioritization, project planning, and project management. Maintaining external engagement will remain a major focus for the CHIPS R&D Metrology Program to enhance communications and outreach methods and collect input that directly informs future R&D project planning and implementation. NIST will continue to leverage a variety of methods to conduct stakeholder engagement such as virtual seminars, working group meetings, in-person events, technology demonstrations, and external research partnerships focused on commercialization and technology transfer. Additionally, the CHIPS R&D Metrology Program will regularly publish research updates and opportunities for stakeholder participation in program development via social media, the NIST website, newsletters, and dedicated mailing lists aligned with topics supported by its research portfolio. Stakeholders can look forward to a future opportunity to subscribe to a CHIPS R&D Metrology Program mailing list to stay current on NIST activities across microelectronic metrology R&D Priority Programmatic Focus Areas.





3. ACKNOWLEDGMENTS

This report was prepared with the collaboration of NIST staff members identified below. These individuals contributed to the process of understanding stakeholder requirements, metrology R&D gaps, and industry trends that informed the development activities for the CHIPS R&D Metrology Program. NIST appreciates the time and effort provided by each of these individuals.

CONTRIBUTORS

Hannah Brown, Deputy Associate Director for Laboratory Programs, NIST

Marla L. Dowell, Director, CHIPS R&D Metrology Program, NIST

David Gundlach, Chief, Nanoscale Device Characterization Division, PML, NIST

William F. Guthrie, Chief, Statistical Engineering Division, ITL, NIST

Paul D. Hale, Chief, RF Technologies Division, CTL, NIST

R. Joseph Kline, Materials Research Engineer, MML, NIST

Dennis D. Leber, Mathematical Statistician, ITL, NIST

David Newton, Mathematical Statistician, ITL, NIST

James K. Olthoff, Associate Director for Laboratory Programs, NIST

Ellen L. Ryan, Deputy Division Chief, CTL, NIST

Sivaraj Shyam-Sunder, Director, Special Programs Office, NIST

4. ENDNOTES

1 The White House, "Building Resilient Supply Chains, Revitalizing American Manufacturing, and Fostering Broad-Based Growth: 100- Day Reviews under Executive Order 14017," June 2021, 9, https://www. whitehouse.gov/wp-content/uploads/2021/06/100-day-supply-chain-review-report.pdf.

2 Pub. L. No. 116-283, tit. XCIX, §§ 9902, 9906 (2021) (codified at 15 U.S.C. §§ 4652, 4656).

3 CHIPS Act of 2022, Pub. L. No. 117-167, Div. A (2022) ("CHIPS Act of 2022").

4 National Institute of Standards and Technology (2022) A Strategy for the CHIPS for America Fund. Available at https://www.nist.gov/chips/implementation-strategy

5 National Academies of Sciences, Engineering, and Medicine 2019. An Assessment of the Communications Technology Laboratory at the National Institute of Standards and Technology: Fiscal Year 2019. Washington, DC: The National Academies Press. https://doi.org/10.17226/25602.

6 National Academies of Sciences, Engineering, and Medicine 2021. An Assessment of Selected Divisions of the Physical Measurement Laboratory at the National Institute of Standards and Technology: Fiscal Year 2021. Washington, DC: The National Academies Press. https://doi.org/10.17226/26312.

7 National Institute of Standards and Technology (2022) Semiconductor Metrology R&D Workshops. Available at https://www.nist.gov/news-events/events/2022/04/semiconductor-metrology-rd-workshops

8 National Institute of Standards and Technology (2022) Strategic Opportunities for U.S. Semiconductor Manufacturing. Available at https://nvlpubs.nist.gov/nistpubs/CHIPS/NIST.CHIPS.1000.pdf.

9 The NLB consists of members of the NIST Program Coordination Office and senior leadership positions within the NIST Office of the Director. National Institute of Standards and Technology. "Leadership." NIST, U.S. Department of Commerce, 2022, https://www.nist.gov/director/leadership.

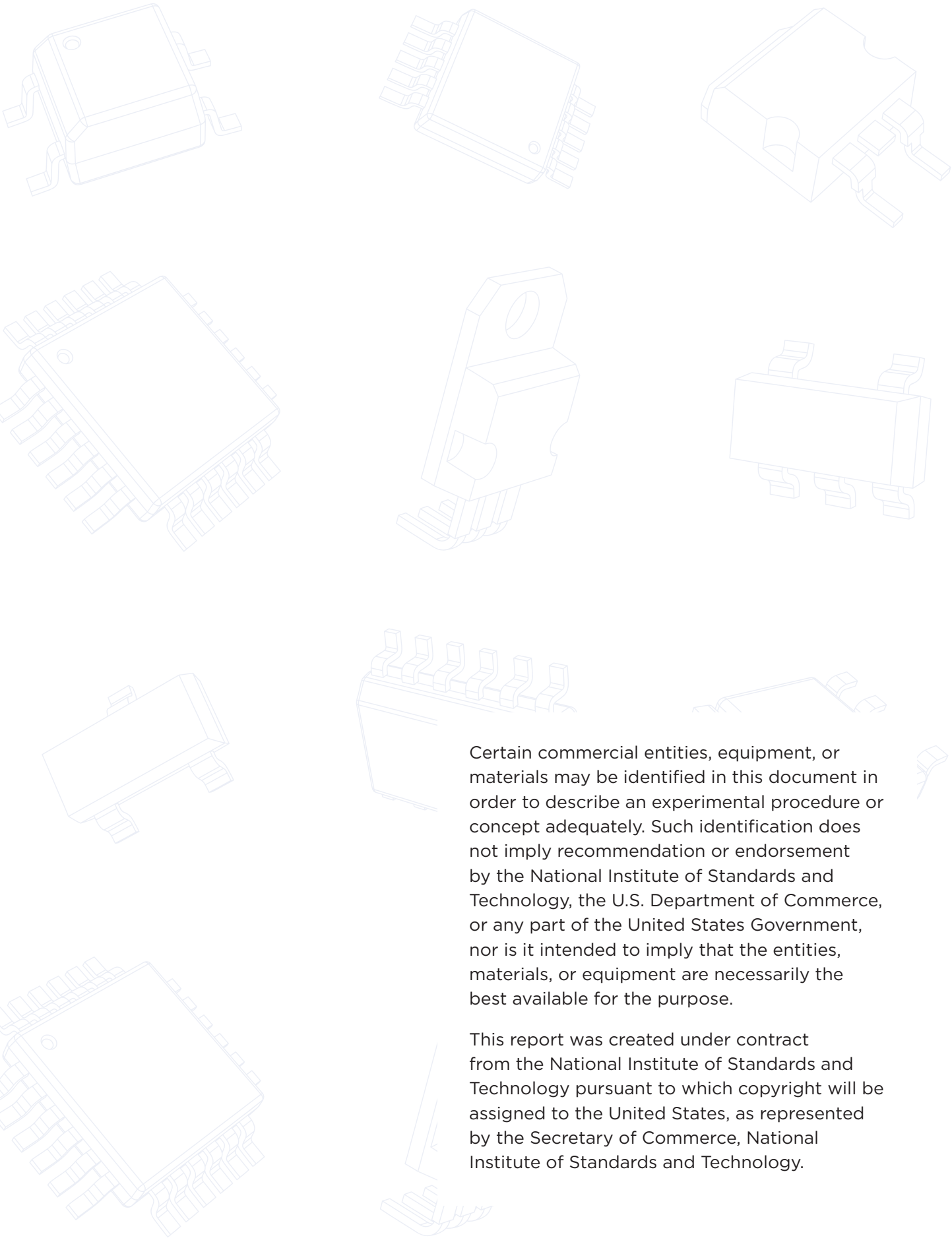
10 NIST directives are administrative orders that are reviewed and approved by the NIST Directives Review Board. NIST directives establish requirements and assignment of responsibilities for NIST activities conducted pursuant to specified authorities.

11 National Institute of Standards and Technology. (2022, March 7). Workshop Flyer (Final). Retrieved March 27, 2023, from https://www.nist.gov/system/files/documents/noindex/2022/03/07/Workshop%20Flyer%20%28Final%29.pdf.

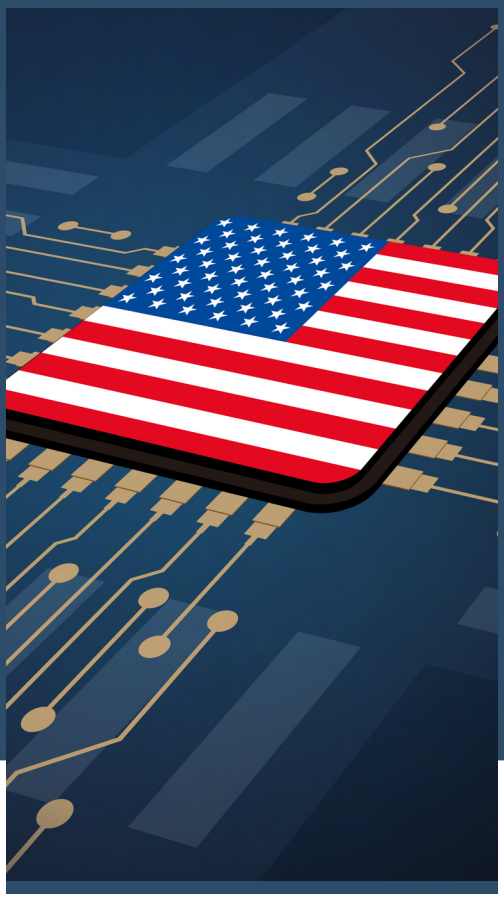
12 National Institute of Standards and Technology. (n.d.). CHIPS Act Events. Retrieved March 27, 2023, from https://www.nist.gov/semiconductors/chips-act-events

13 Heterogeneous Integration Roadmap, IEEE Electronics Packaging Society, 2021 Edition: https://eps.ieee.org/technology/heterogeneous-integration-roadmap.html

14 IEEE-International Roadmap for Systems and Devices- Metrology Chapter, 2021 Edition, IEEE-IRDS https://irds.ieee.org/editions/2021



Certain commercial entities, equipment, or materials may be identified in this document in order to describe an experimental procedure or concept adequately. Such identification does not imply recommendation or endorsement by the National Institute of Standards and Technology, the U.S. Department of Commerce, or any part of the United States Government, nor is it intended to imply that the entities, materials, or equipment are necessarily the best available for the purpose.



https://www.CHIPS.gov

askchips@chips.gov