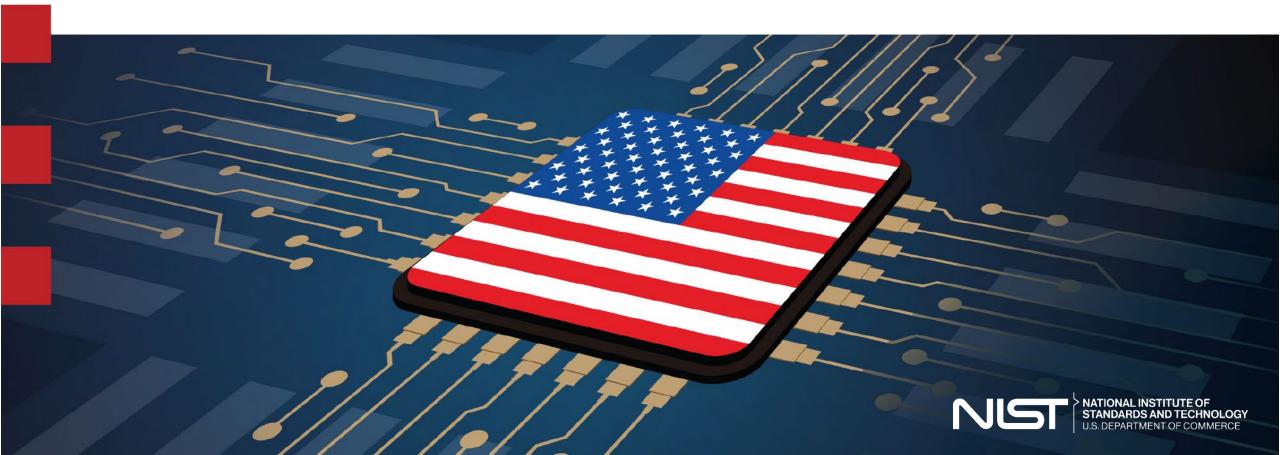


# CHIPS R&D Education and Workforce Development (EWD) Guidebook

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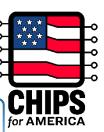






- Statements and responses to questions about advanced microelectronics research and development programs in this webinar:
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## Overview of CHIPS R&D Office Goals



#### **Vision**

A vibrant and self-sustaining U.S. domestic semiconductor ecosystem that revitalizes American manufacturing, grows a skilled and diverse workforce, and leads the world in semiconductor research and innovation.

#### **Mission**

Accelerate the development and commercial deployment of foundational semiconductor technologies by establishing, connecting, and providing access to domestic tools, resources, workers, and facilities.

#### 2030 Goals

- U.S. Technology Leadership: The United States establishes the capacity to invent, develop, prototype, and deploy the foundational semiconductor technologies of the future.
- Accelerated Ideas to Market: The best ideas achieve commercial scale as quickly and cost effectively
  as possible.
- Robust Semiconductor Workforce: Inventors, designers, researchers, developers, engineers, technicians, and staff meet evolving domestic commercial-sector and government needs.

## **Policy and National Security Context**



#### **Unique or Emerging Directives**

#### CHIPS and Science Act (2022)

- Prohibit malign foreign talent recruitment programs
- Research security training
- Integration of workforce development into R&D efforts

#### **CHIPS Act (2021)**

- Domestic production requirements
- Domestic control requirements to protect intellectual property from foreign adversaries
- Workforce initiatives as a required component of most CHIPS-funded activities

#### **Executive Order 14080 (2022)**

- Prioritize strengthening and expanding regional manufacturing and innovation ecosystems
- Prioritize the generation of benefits for communities

#### **National Security Policy Memorandum 33 (2021)**

- Research security program requirements
- Disclosure of conflicts of interest / commitment

#### **Application Requirements**

- Domestic Research and Development Requirements
- □ Domestic Control and Intellectual Property Rights Management Plan
- ☐ Research Security Plan
- ☐ Commercial Viability and Domestic Production (CVDP) Plan
- ☐ Education and Workforce☐ Development (EWD) Plan



#### CHIPS R&D recommends EWD plans include the following elements, where applicable:

Workforce Needs Metrics and Milestones

Industry-Relevant Training

Strategic Partnerships Recruitment and Retention

#### **Key Components:**

- Workforce Needs Assessment: An assessment of the relevant workforce needs for some portion or portions of the semiconductor industry
- **SMART Targets:** A description of the specific goals EWD activities are expected to achieve and quantifiable metrics to demonstrate success toward EWD targets
- Training Opportunities: A description of the proposed EWD activities and demonstration of alignment with specific job opportunities and skills needs, consistent with the workforce needs assessment, and leverage known best practices

Key Point: EWD Plans are intended to ensure that EWD activities address domestic workforce needs and support good jobs that will benefit American workers and help sustain the domestic semiconductor industry.



#### **1** Workforce Needs Assessment

- ☐ When developing EWD plans, applicants are advised to consider:
  - > The current workforce by occupation, skill set, wage, and demographics
  - The pool of available workers with relevant or related skills, including from underserved communities
  - > The projected available and demanded workforce with relevant or related skills
  - Description of how the applicant will regularly update the needs assessment
  - Any workforce **challenges to address** (e.g., skills shortages, persistent vacancies, education and training program gaps)
  - If applicable, current barriers to filling identified skill and personnel gaps



#### Metrics and Milestones (SMART Targets)

- ☐ When developing EWD plans, applicants are advised to consider:
  - **Quantifiable metrics to demonstrate impact**, such as the number of workers enrolled and trained, incumbent workers retrained or upskilled, persons placed in a job, or the percentage improvement in employee earnings and retention
  - Information demonstrating the relevance of the EWD activities to the funded research or to industry, consistent with the NOFO objectives and workforce needs assessment
  - > A process, including resources and data, for evaluating EWD activities over time, such as a plan to report such progress to CHIPS R&D and its designated third parties, if applicable
  - > Specific goals the applicant establishes for EWD activities, the entity designated to implement tactics to achieve those specific goals, and how the activities will be tailored to the communities they serve
  - Evidence that the organization can attain its EWD targets within the time proposed, based on factors such as available resources, past experience, or existing partnerships with proven academic or labor groups
  - Projected deadlines for achieving both final and intermediate EWD targets, with metrics for evaluating progress during the period of performance

### Frequently Asked Questions



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## How will the CHIPS R&D Office use the proposed metrics and milestones (SMART Targets)?

SMART targets help ensure that the applicant can evaluate, scale, or modify its EWD plan based on their level of success. SMART goals can also help demonstrate that EWD programs align with NOFO objectives, timelines, and resources.

- Applicants must propose SMART (Specific, Measurable, Achievable, Relevant, and Time-Bound) EWD targets, such as the number of students trained or engaged in research and subsequently placed in good jobs in the domestic semiconductor industry, to be achieved under the EWD plan. (NAPMP M&S NOFO 1.6.1)
- Applications should further identify SMART milestones describing measurable steps toward achieving the proposed Institute-level EWD targets, such as the number of students trained or engaged in research and subsequently placed in good jobs in the domestic semiconductor industry. (MFG USA DTI NOFO 1.4.4.2)



#### 3 Industry-Relevant Training

- ☐ When developing EWD plans, applicants are advised to consider:
  - Aligning with current or proposed industry-wide or internally developed competency standards, skill requirements, or with requirements for stackable, industry-recognized credentials or certifications
  - Efforts to support the hiring of participants that have successfully completed EWD programs by specific industry partners, into good jobs
  - Engaging with K-12 institutions, Career and Technical Education (CTE) providers, labor organizations, and community-based solution providers to **strengthen pathways for the future R&D workforce** to access careers in manufacturing, design, research, and packaging, if appropriate
  - Including proven training models (such as registered apprenticeships), best practices, curriculum, and pedagogy for training or up/re-skilling new, incumbent, or returning workers

### **Frequently Asked Questions**

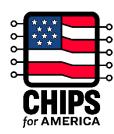


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## How can applicants demonstrate that EWD plans are aligned with U.S. industry needs?

Evidence may include letters of interest or commitment submitted by employers and labor organizations; community-based organizations and local officials; semiconductor and/or supply chain companies with operations or facilities in the selected region or relevant regional semiconductor industry cluster; and/or other stakeholders.

- Provide evidence of alignment with U.S. industry needs, such as demonstrated linkages between the skills to be developed in the programs and available jobs or to industry-recognized credentials or certifications. Other evidence may include letters of interest from potential employers and labor organizations. (NAPMP M&S NOFO 4.6.1.6(d)(v))
- To accomplish the mission, vision, and objectives... the CHIPS Manufacturing USA Institute must work with employer partners and engage educational institutions, to support the creation and widespread adoption of training materials and curricula. (MFG USA DTI NOFO 1.4.4)
- CHIPS R&D encourages applicants, in providing an EWD plan, to...demonstrate that the EWD efforts that involve employer partners, are worker centered, industry-aligned, and promote high quality jobs. (MFG USA DTI NOFO 1.4.4)



- 4 Strategic Partnerships
  - ☐ When developing EWD plans, applicants are advised to consider:
    - ➤ Outreach to underserved communities and engagement with partner institutions that deliver quality employment and training pathways, such as labor organizations, government agencies, and industry organizations, including local employers in the semiconductor or adjacent fields
    - > Commitments from such partner organizations with letters of commitment describing the roles and responsibilities of each participating entity and the resources each will provide
    - Opportunities to sustain or scale successful EWD activities beyond the period of performance, including through the receipt of other Federal or non-Federal funds
    - > Past, current, or pending support for the proposed and/or existing EWD efforts from other Federal entities



### 5 Recruitment and Retention

- ☐ When developing EWD plans, applicants are advised to consider:
  - > New or expanded opportunities for individuals to participate in the semiconductor industry workforce, including for populations underrepresented in the industry
  - ➤ Demonstrated **links between the skills to be developed and in-demand, high-quality jobs** such as those consistent with the Good Jobs Principles, which emphasizes employment likely to provide "family-sustaining benefits that promote economic security and mobility"
  - > Investments in supportive services such as childcare, transportation, and housing and the promotion of a safe and respectful workforce culture that prevents harassment and discrimination

### **Frequently Asked Questions**

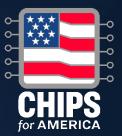


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## What recruitment and retention information would CHIPS R&D like to see in an application?

The Department supports good jobs for all workers as a building block for economic growth and recognizes that meeting business' talent needs requires tapping into the talent in all our communities.

- CHIPS R&D encourages applicants to, in providing an EWD plan, describe any efforts to attract
  and retain a diverse student and trainee population (NAPMP M&S NOFO 1.6.1)
- Describe any efforts to maximize access to and participation in the semiconductor workforce, including efforts to attract and retain a diverse student and trainee population such as supportive services and outreach to underserved communities. (NAPMP M&S NOFO 4.6.1.6(d)(v))
- Plans could include investing in pre-apprenticeship programs or building recruitment partnerships
  with community-based organizations that have a track record of serving underserved communities,
  as demonstrated within the proposal. Plans could also include the Institute or its members,
  investing in supportive services such as childcare, transportation, and housing, and promoting a
  safe and respectful workforce culture that prevents harassment and discrimination.
  (MFG USA DTI NOFO 1.7.2)



## **Thank You**

