CHIPS R&D Digital Twin Technical Standards Workshop

DRAFT AGENDA

DAY 1: December 14, 2023 / 8:30 AM – 5:35 PM		
TIME	**TOPIC**	**PRESENTER**
7:30 – 8:30 am	Check-in	
8:30 – 8:35 am	Introduction to the workshop / review agenda / logistics	Yaw Obeng (*CHIPS R&D Office*)
8:35 –8:45 am	Opening Remarks	Eric Lin (*CHIPS R&D Deputy Director*)
8:45 – 9:00 am	**Keynote:** Leveraging CHIPS Acts public-private partnerships to evolve standards for design & manufacturing digital twins	Tom Katsioulas (*Archon Design Solutions, Inc.*)
9:00 – 10:30 am	**Panel 1: Tutorial on digital twin standards**	Carol Handwerker (*Purdue University*) *Moderator*
	1) Key-takeaways after the Dec 4-5th workshop SEMI's Smart Manufacturing Initiative 2) Building and managing a digital twin-based semiconductor manufacturing operation 3) IPC digital twin standards 4) IOT/big data / digital twins for Lam Research semiconductor fabrication equipment	1) Mark de Silva (*SEMI*) 2) Paul Schneider (*Intel*) 3) Matt Kelly (*IPC*) (Virtual) 4) Krishan Chawla (*LAM Research*) (Virtual)
10:30 – 10:45 am	Break	
10:45 – 11:45 am	**Breakout Session 1**: Discuss and prioritize ideas related to panel 1	Led by *SIDEM* and *Corner Alliance* facilitators
11:45 – 12:00 pm	**Report Out** from Breakout Session 1	NIST facilitators and/or workshop participants
12:00 – 1:15 pm	Lunch	
1:15 – 2:15 pm	**Panel 2: Digital Twin for supply chain – packaging, test, and security**	Mark de Silva (*SEMI*) *Moderator*
	1) Simulation: atomic through virtual systems 2) Closing the loop between virtual and real models 3) AI for digital twin 4) Secure data flow 5) Testing data for digital twin	1) Kenneth Larsen (*Synopsys*) 2) Adam Cron (*Synopsys*) 3) James Moyne (*U. Michigan*) (Virtual) 4) Dave Huntley (*PDF Solutions*) (Virtual) 5) Ken Butler (*Adantest*)
2:15 – 3:15 pm	**Breakout Session 2**: Discuss and prioritize ideas related to panel 2	Led by *SIDEM* and *Corner Alliance* facilitators
3:15 – 3:30 pm	**Report Out** from Breakout Session 2	NIST facilitators and/or workshop participants
3:30 – 4:00 pm	Break	
4:00 – 4:45 pm	**Panel 3: What is the current state of research for digital twins?**	Adam Cron (*Synopsys*) *Moderator*

	1) iNEMI Heterogenous Integration Modelling and Simulation TWG 2) Data analytics and decision-making methodologies specifically tailored for Internet of Things (IoT) enabled smart and connected products/systems. 3) Chip production improvement with digital twin 4) High-Level Approaches to Hardware and Embedded Security	1) Chris Bailey (*Arizona State University*) 2) Raed Al-Kontar (*University of Michigan*) 3) Giulia Pedrielli (*Arizona State University*) 4) Ramesh Karri (*NYU*)
4:45 –5:15 pm	**Breakout Session 3**: Discuss and prioritize ideas from panel 1, panel 2, and panel 3	Led by *SIDEM* and *Corner Alliance* facilitators
5:15 – 5:35pm	**Report Out** from Breakout Session 3	NIST facilitators and/or workshop participants
5:35pm	Adjourn	

DAY 2: December 15, 2023/ 8:30 AM – 12:00 PM		
8:30 - 9:30 am	**PANEL 4: Summary Discussion / Takeaways from Day 1**	Giulia Pedrielli (*Arizona State University*) *Moderator*
	Questions: • What are the technical standards gaps? • What information is needed to address the gaps? • How do we prioritize which standards to work on? • Who can help with the standards development effort? • Which SSO's should be working on these issues?	Panelists: 1) Bapi Vinnakota (*Open Compute Project*) 2) Matt Kelly (*IPC*) (Virtual) 3) Chen Sun (*Aylar Labs*) (Virtual) 4) Mark de Silva (*SEMI*) 5) Debendra Das Sharma (*UCIe Consortium Standards*) (Virtual)
9:30 – 10:30 am	**Breakout Session 4**: Discuss and prioritize ideas related to panel 4	Led by *SIDEM* and *Corner Alliance* facilitators
10:30 –11:00 am	Break	
11:00 – 12:00pm	**Report Out** from Breakout Session 4 and consolidation of priorities	NIST facilitators and/or workshop participants
12:00 –12:30 pm	Discuss next steps	Yaw Obeng & Jan Obrzut (*CHIPS R&D Office*)
12:30 pm	End of workshop - adjourn	