

CHIPS Portal Update: How to Select Application Pipeline

Beginning on July 21, 2023, applicants may select the appropriate application pipeline for a submission within the application portal. There are three application pipelines that the CHIPS Program Office has defined:

1. **Front-End and Back-End Commercial Fabrication Facilities:** Under the currently released NOFO, this application pipeline is for leading-edge, current-generation, and mature-node front-end manufacturing, as well as back-end production facilities.
2. **Large-Scale Supply Chain Facilities:** Under the currently released NOFO, this application pipeline is for large-scale commercial semiconductor material and manufacturing equipment facilities exceeding \$300 million in capital expenditures, as well as wafer manufacturing facilities of any size.
3. **Other Facilities:** The last application pipeline is for other all facility types that are not covered in the first two categories.

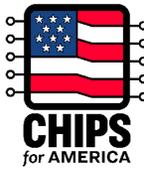
See below for detailed descriptions and relevant application process details for the application pipelines.

Application Pipeline #1 – Front-End and Back-End Commercial Fabrication Facilities

Under the currently released NOFO, this application pipeline is for leading-edge , current-generation , and mature-node front-end manufacturing, as well as back-end production facilities is accepting pre-applications and full applications on a rolling basis, and includes:

Leading-Edge Facilities for logic or memory that utilize the most advanced front-end fabrication processes which achieve the highest transistor and power performance. For logic, this currently includes facilities that produce semiconductors at high volumes using extreme ultraviolet (EUV) lithography tools. For memory, this currently includes facilities capable of producing 3D NAND flash chips with 200 layers and above, and/or dynamic random-access memory (DRAM) chips with a half-pitch of 13 nm and below.

Current-Generation Facilities that produce semiconductors that are not leading edge, up to 28 nm process technologies, and include logic, analog, radio frequency, and mixed-signal devices. New and expanded current-generation front-end fabrication facilities will deliver manufacturing capacity for current-generation semiconductor technologies, as well as new and specialty technologies such as devices based on compound semiconductor materials.



Mature-Node Facilities that fabricate generations of: (a) logic and analog chips that are not based on FinFET, post-FinFET transistor architectures, or any other sub-28 nm transistor architectures; (b) discrete semiconductor devices such as diodes and transistors; (c) optoelectronics and optical semiconductors; and (d) sensors.

Back-end Production Facilities for the assembly, testing, or packaging of semiconductors that have completed the front-end fabrication process. This category includes advanced packaging of semiconductors. The Department is particularly interested in projects that ensure competitive operating costs within the United States (e.g., through automation).

Application Pipeline #2 – Large-Scale Supply Chain Facilities

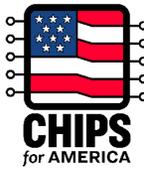
Under the currently released NOFO₂, this application pipeline is for large-scale commercial semiconductor material and equipment facilities exceeding \$300 million in capital expenditure, and wafer manufacturing facilities of any size. For potential applications for wafer manufacturing facilities and semiconductor materials and manufacturing equipment facilities, pre-applications (which are recommended) will be accepted on a rolling basis beginning on Friday, September 1, 2023 and full applications will be accepted on a rolling basis beginning on Monday, October 23, 2023. This pipeline includes:

Wafer Manufacturing Facilities for the high-volume production of semiconductor wafers, including wafers made from silicon, silicon carbide, and gallium nitride. These facilities are the sites of ingot production and wafer slicing, lapping, polishing, cleaning and inspection.

Semiconductor Materials Facilities for the manufacture or production, including growth or extraction, of materials used to manufacture semiconductors, which are the chemicals, gases, raw and intermediate materials, and other consumables used in semiconductor manufacturing. Specific examples include but are not limited to polysilicon; photoresists and ancillaries (developers, strippers, litho solvents, and anti-reflective and hardmask layers); sputter targets (including tantalum, titanium, and aluminum); and materials specifically used in quantum information systems (such as hafnium and niobium). Applications for the construction, expansion, or modernization of commercial semiconductor materials facilities will be eligible for this NOFO only if the capital investment, as defined in Section IV.I.7, equals or exceeds \$300 million.

Semiconductor Manufacturing Equipment Facilities for the physical production of specialized equipment integral to the manufacturing of semiconductors and subsystems that enable or are incorporated into the manufacturing equipment. Specific examples of semiconductor manufacturing equipment include but are not limited to deposition equipment, including chemical vapor deposition, physical vapor deposition, and atomic layer deposition; etching equipment (wet etch, dry etch); lithography equipment (steppers, scanners, extreme ultraviolet); wafer slicing equipment, wafer dicing equipment, and wire bonders; inspection and measuring equipment, including scanning electron microscopes, atomic force microscopes, optical inspection systems, and wafer probes; certain metrology and inspection systems; and ion implantation and diffusion/oxidation furnaces.

Applications for the construction, expansion, or modernization of commercial semiconductor equipment facilities will be eligible for this NOFO only if the capital investment, as defined in Section IV.I.7, equals or exceeds \$300 million. Only facilities of the types listed above are eligible for funding under this NOFO at this time.



Application Pipeline #3 – Other Facilities

This application pipeline is for all facility types that are not covered in the first two categories.

At a later date, the CHIPS Program Office expects to launch an additional funding process for applications relating to semiconductor materials and manufacturing equipment facilities with capital investments under \$300 million, as well as an additional funding process for applications relating to R&D facilities. The CHIPS Program Office will provide future guidance regarding potential additional funding opportunities.

Note: Statements of interest from all potential applicants are being accepted on a rolling basis; statements of interest must be submitted at least 21 days prior to submitting a pre-application or full application.