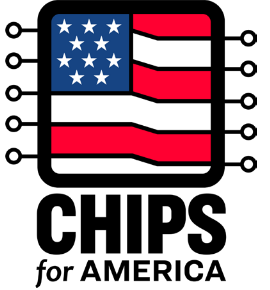
Power Delivery and Thermal Management



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NIST NATIONAL INSTITUTE OF STANDARDS AND TECHNOLOGY
U.S. DEPARTMENT OF COMMERCE

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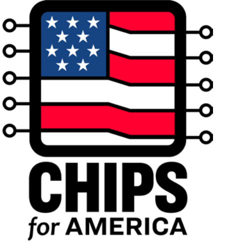
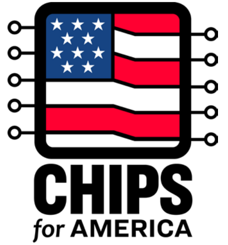


Statements and responses to questions about advanced microelectronics research and development programs in this webinar:

- Are informational, pre-decisional, and preliminary in nature.
- Do not constitute a commitment and are not binding on NIST or the Department of Commerce.
- Are subject in their entirety to any final action by NIST or the Department of Commerce.

Nothing in this presentation is intended to contradict or supersede the requirements published in any future policy documents or Notices of Funding Opportunity.

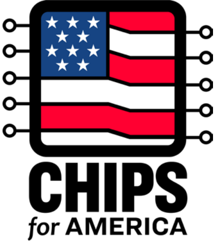
Key Dates



July 9, 2024	October 17, 2024	October 22, 2024	December 20, 2024	TBD	TBD
NOI (Released)	Advanced Packaging R&D (Released)	Advanced Packaging R&D Proposer's Day	Concept Papers Due Date	Invitation for Full Application Submission	Full Application Due

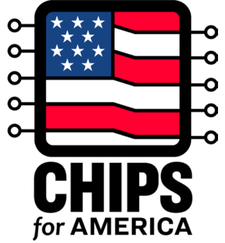
CHIPS for America QR Code:
CHIPS NAPMP NOFO 2
(full text)

Power Delivery and Thermal Management



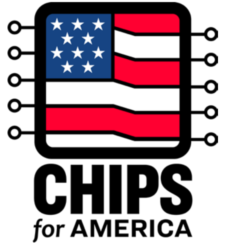
- Address power delivery, power efficiency, and thermal management challenges for advanced packaging.
- Create test devices, utility chiplets and improved models to develop and refine thermal and power solutions for the advanced packaging ecosystem.
- Ensure that thermal dissipation and power delivery will no longer be gating factors that limit advanced packaging.

Power Delivery and Thermal Management



Critical Objectives	Key Outputs	Out of Scope
➢ Power Delivery and Management ➢ Thermal Management ➢ Higher Fidelity Power and Thermal Models ➢ Integrated Power and Thermal Management	➢ Test devices and utility chiplets ➢ Multi-use solutions ➢ Standards, metrologies and data derived from test devices ➢ Test and evaluation at prototype- and pilot-scale manufacturing ➢ Proven equipment, tools, processes, materials, models and devices with improved performance available for the CHIPS ecosystem	➢ Single-use thermal and power solutions ➢ Conventional air-cooling approaches ➢ Discrete packaged wide bandgap devices ➢ Discrete passives ➢ Development of batteries

Power Delivery and Thermal Management



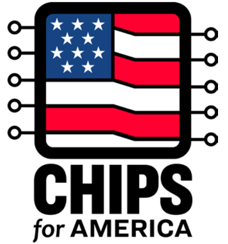
Drivers

- Innovate to deliver power efficiently, locally, and dynamically
- Produce less waste heat
- Support integration with emerging technologies, such as photonics and connectors
- Spread and tolerate heat more effectively
- Improve heat removal and management strategies
- Improve models to accelerate design and validation
- Multi-use solutions that benefit many applications and the Chiplet ecosystem

Outcomes

- Enable advanced packaging for reliable operation at higher power densities and improved energy efficiencies

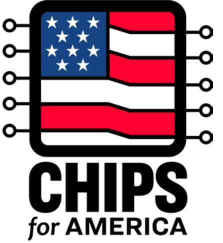
Four Critical Objectives



Objective	High Performance	Low-Power
1. Power Delivery and Management	Power delivery at high density and high efficiency for 3DHI devices	Design optimization, energy efficiency, and integrated energy harvesting technologies
2. Thermal Management	Thermal solutions compatible with advanced substrates, 3DHI, and other advanced packaging design aspects to reduce hotspots, maintain thermal targets, and enable reliability	Compact and lightweight thermal solutions
3. Thermal and Power Models	Validated, higher fidelity thermal and power models that accurately predict power and thermal distributions across chiplet stacks and accelerate advanced system design and evaluation	
4. Integrated Thermal and Power Management	Achieve efficiency and power density goals with integrated designs that couple power delivery and thermal management strategies, for use with fine-pitch, bonded stacks of chiplets	

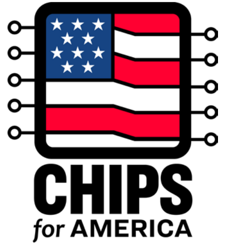
Proposals for the Thermal and Power Delivery R&D Area must address one or more of the four objectives

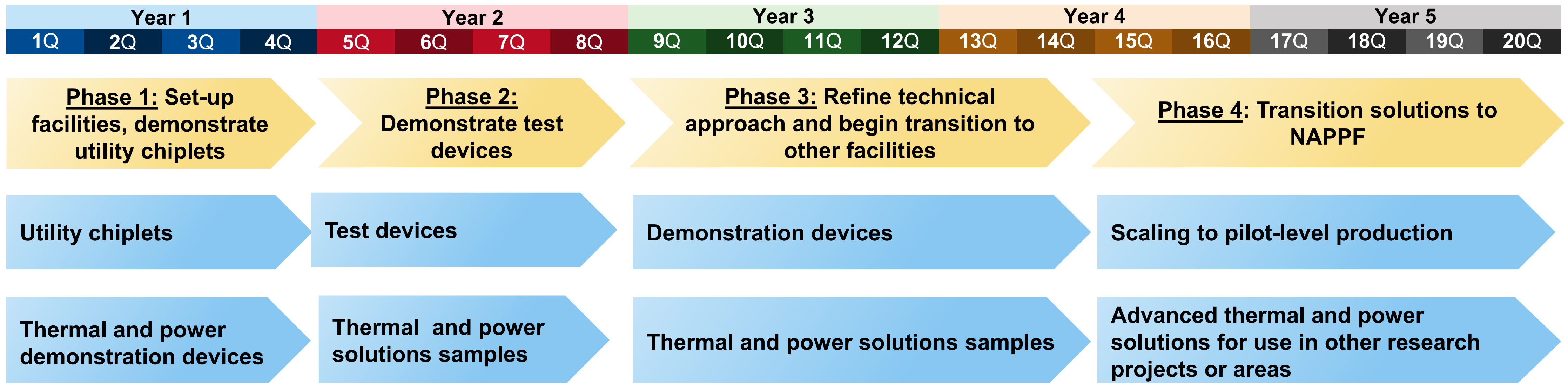
Key Outputs



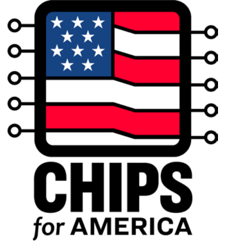
- Novel equipment, tools, materials, processes, devices, data and models that demonstrate improved performance for Thermal and Power solutions.
- Utilization of test devices and chiplets to demonstrate performance in 3DHI stacks with a path to scale.
- Standards, metrologies and data derived from test devices.
- Test and evaluation at prototype- and pilot-scale manufacturing.
- Proven processes, materials, models and devices with improved performance available for the CHIPS ecosystem:
  - Power delivery and thermal management chiplets to support the chiplet ecosystem
  - Thermal solutions and power solutions made available to other CHIPS R&D projects
  - Thermal solutions that do not constrain connectivity and are compatible with advanced substrates and 3DHI

Key Deliverables



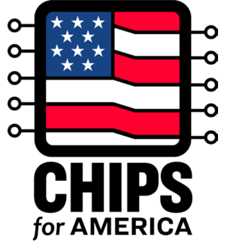


In Scope



- Thermal and power solutions that are modular, reusable, and useful for multiple applications within the chiplet ecosystem
- Thermal management
  - Vertical heat extraction
  - Local heat spreading
  - Embedded cooling
  - Advanced methods for active and passive cooling of 3DHI devices to reliably operate at higher power density
- Wide bandgap chiplets using 3DHI for power delivery
- Advanced models, materials, and architectures to achieve specific thermal goals such as low-resistance thermal interfaces
- On chiplet embedded structures, passives, 3D stacks, and films for power delivery and thermal management

Out of Scope



- **Single-use thermal and power solutions**

  Why? Modular / multi-use solutions that will most benefit the chiplet ecosystem

- **Conventional air-cooling approaches**

  Why? To drive improvements in power density, efficiency, size, weight and connectivity

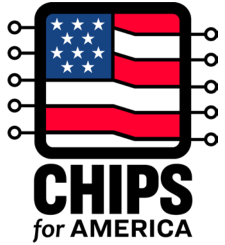
- **Discrete packaged devices and Discrete passives**

  Why? Advanced Packaging is about scale down and scale out - greater connectivity and many heterogenous chiplets integrated together within a package

- **Development of batteries**

  Why? Improvements in energy harvesting with possible integrated storage would benefit low-power and sensor applications, not stand-alone batteries

Collaboration with Other R&D Areas



- Integrate embedded features
- Match fine scale & bonding
- Accommodate abundant wires

- Leverage emerging technologies
- Avoid constraining connectivity
- Improved reliability

Leverage new equipment, tools and processes

Equipment, tools, processes, and process integration

Power delivery, and thermal management

Connectors (Photonics & RF)

Materials and substrates

- Advanced models for chiplet stacks
- Leverage to accelerate design

Chiplets ecosystem

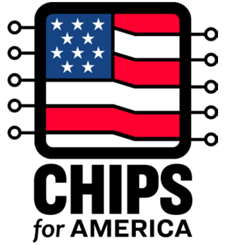
Co-design/ Electronic Design Automation

Best prototypes piloted at NAPPF

National Advanced Packaging Piloting Facility

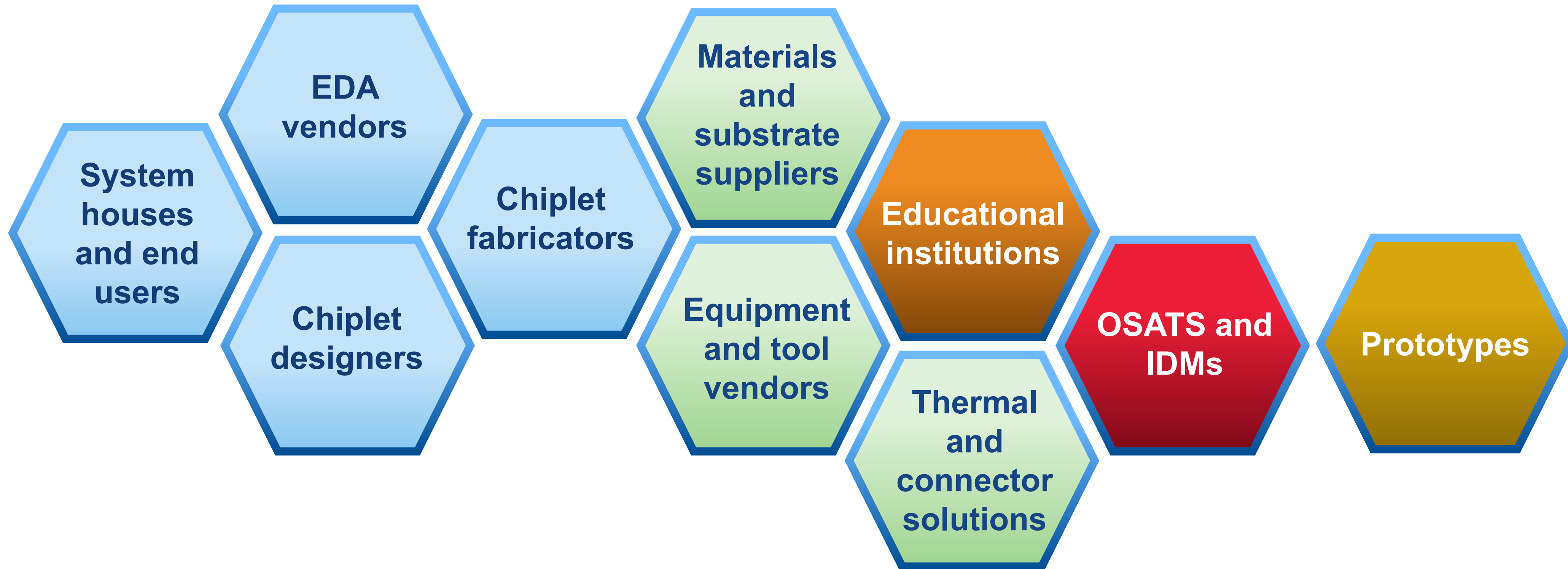
Multi-use thermal and power solutions for chiplet ecosystem

Program Structure

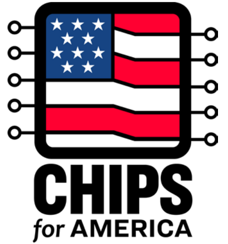


- Multiple awards varying in scope and funding are expected
    - Up to approximately $250,000,000 anticipated for funding multiple awards in amounts ranging from a minimum of approximately $10,000,000 up to a maximum of approximately $50,000,000
- Multi-disciplinary, multi-organization project teams are strongly encouraged
- Project teams should expect to collaborate with other R&D Areas
- Applicants must propose a detailed project plan for achieving Project-Level Technical Targets
- Projects should be divided into 4 phases over a period of performance of 5 years
    - Phase 1 *(12 months)*
    - Phase 2 *(12 months)*
    - Phase 3 *(18 months)*
    - Phase 4 *(18 months)*
    - While cost share is not be required, CHIPS R&D will give preference to applications that demonstrate credible cost share commitments. Cost share generally consists of labor, materials, equipment, software, facilities costs, and other investments directly related to the project.

Collaboration is Critical for Success

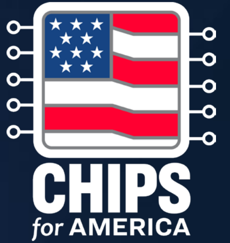


Successful execution will require collaboration between proposers and each R&D Area. Proposers must clearly understand the ideas presented in each R&D Area. We encourage you to begin identifying your individual contributions to the ecosystem as well as partners who can help accomplish the vision and goals of the NAPMP.



Next Steps

- NOFO 2: Concept papers due 12/16
- Visit CHIPS.gov for resources, including:
  - Upcoming R&D Area Webinars
  - FAQs
  - Funding opportunities and NOFO updates
- Join our mailing list
- Contact us
  - askchips@chips.gov – general inquiries
  - apply@chips.gov – application-related inquiries



Thank you for attending

Visit CHIPS.gov for future updates and additional information