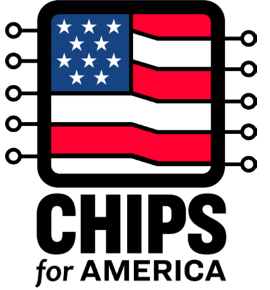

Connectors, Including RF & Photonics

PM: Christopher Myatt

October 22, 2024

NIST
NATIONAL INSTITUTE OF STANDARDS AND TECHNOLOGY
U.S. DEPARTMENT OF COMMERCE

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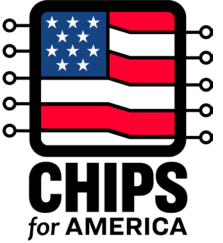

Statements and responses to questions about advanced microelectronics research and development programs in this webinar:

- Are informational, pre-decisional, and preliminary in nature.
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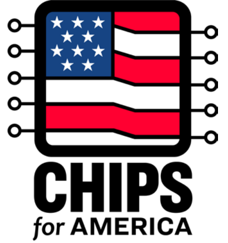
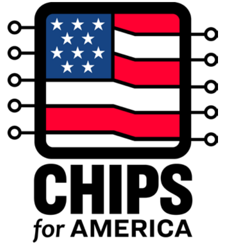
Key Dates



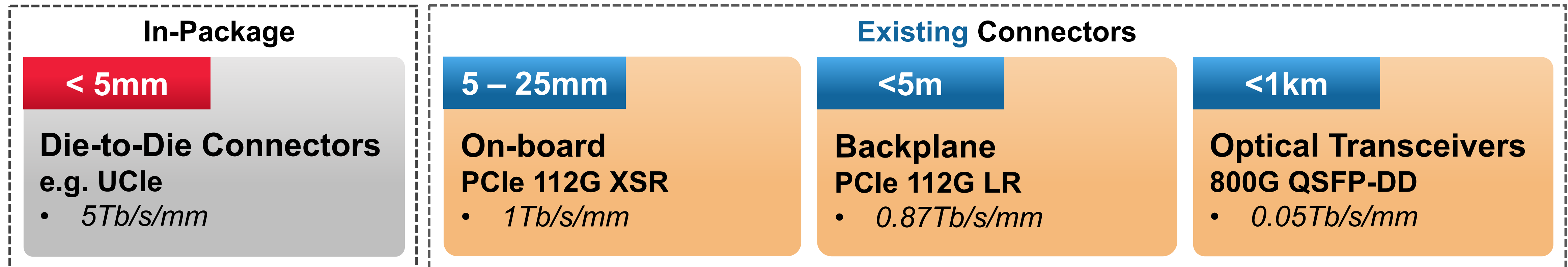
July 9, 2024	October 17, 2024	October 22, 2024	December 20, 2024	TBD	TBD
NOI (Released)	Advanced Packaging R&D (Released)	Advanced Packaging R&D Proposer's Day	Concept Papers Due Date	Invitation for Full Application Submission	Full Application Due

CHIPS for America QR Code:
CHIPS NAPMP NOFO 2
(full text)

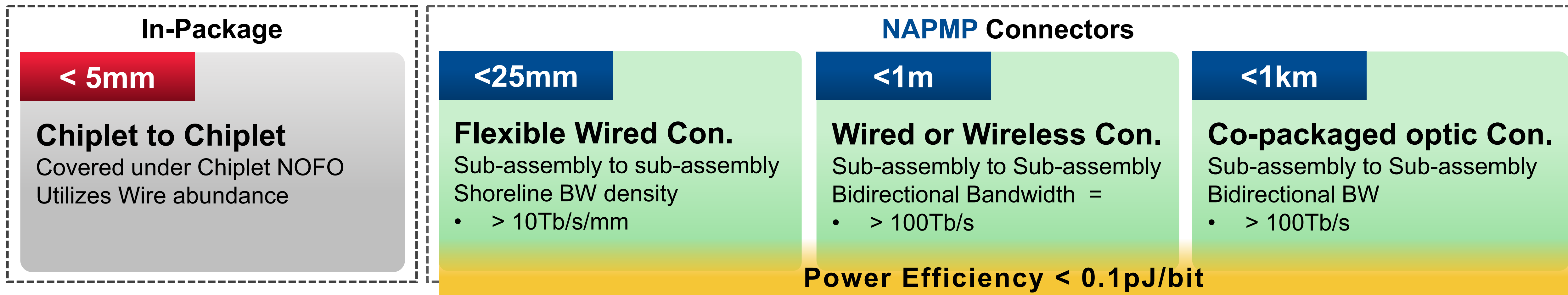
Existing Connectors vs. NAPMP Vision



Connectors currently limit data communication in and out of the package

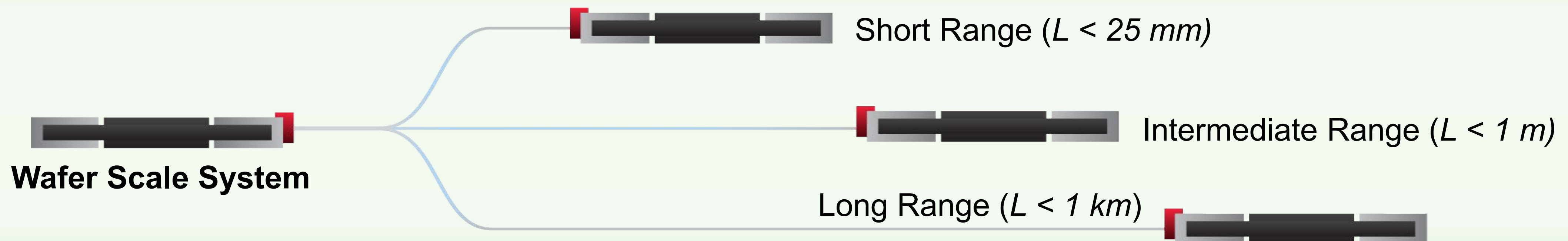


NAPMP Vision for high efficiency, high bandwidth, low error rate connectors

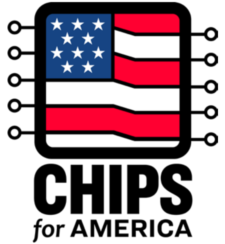


Three Length Scale Objectives

Objective	Length Scale	Key Characteristics
Short Range (e.g. Wired)	L < 25 mm	Data rates of > 10 Gb/s/channel & density of 10 Tb/s/mm Power efficiency < 0.1 pJ/bit including all energy for full functionality
Intermediate Range (e.g. RF, Wired, or Photonic)	L < 1 m	Aggregate data rate > 100 Tb/s bidirectional from package Power efficiency < 0.1 pJ/bit including all energy for full functionality
Long Range (e.g. Photonic)	L < 1 km	Aggregate data rate > 100 Tb/s bidirectional from package Power efficiency < 0.1 pJ/bit including all energy for full functionality



Connector Technology, Including Photonics and RF R&D Areas



RDA Drivers

- Recent years have seen an explosion of progress in high performance computing. Data transmission in these systems requires innovation for high data-rate, low latency, small footprint, error-free, and energy efficient connections.

Objectives

- Development of short-range, wired connections to enable high speed connectivity between neighboring packages.
- Development for intermediate range wired, photonic, or wireless connectors between local wafer-scale systems (but not necessarily nearest neighbor).
- Development of long-range connectors capable of connecting wafer-scale systems at a range up to and exceeding the length of a server site, or approximately 1 km

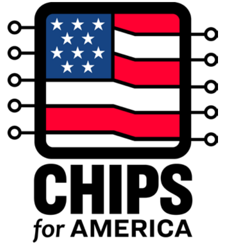
Key Outputs

- Novel connectors, tools, materials, processes and devices with improved performance
- Standards and metrologies derived from test devices; test and evaluation at proto- and pilot-scale manufacturing
- Provide new connector solutions, including devices, equipment, tools, processes, and process integration, to research projects in other areas of packaging research

Out of Scope

- Traditional ball grid array (BGA) or land grid array (LGA) connectors,
- Conventional wire bonding
- Traditional free space optical components

Key Technical Metrics: Connectors



- Technical Metrics are intended to push the state of the art
- Targets are aggressive, but value will be placed on versatility, flexibility, and manufacturability in approach
- Performers can call out specific targets that are out of scope or at risk
- Performers should specify their target FOM and the trade-offs considered for their technology to optimize the overall performance

<table>
<tr><th></th><th>Objective 1</th><th>Objective 2</th><th>Objective 3</th></tr>
<tr><td>Distance</td><td>5 - 25 mm</td><td>< 1 m</td><td>< 1 km</td></tr>
<tr><td>Bandwidth Req.</td><td>10Gb/s/channel & 10Tb/s/mm</td><td>>100 Tb/s bidirectional</td><td>>100 Tb/s bidirectional</td></tr>
<tr><td>Efficiency</td><td colspan="3">< 0.1 pJ/b</td></tr>
<tr><td rowspan="3">Clock Rate
OR
RF Freq.
OR
Wavelength</td><td>Applicant Defined</td><td>Applicant Defined</td><td>Applicant Defined</td></tr>
<tr><td>N/A</td><td>20 – 220 GHz</td><td>N/A</td></tr>
<tr><td>N/A</td><td colspan="2">Align with existing MSA* or provide justification</td></tr>
<tr><td>Latency</td><td colspan="3"><2 ns + TOF</td></tr>
<tr><td>BER (w/ error correction)</td><td colspan="3">$<10^{-12}$</td></tr>
</table>

* e.g. CW-WDA MSA

Optimize for: $$\text{s-FoM} = \frac{(\text{BW/shoreline}) * \text{link length}}{\text{Efficiency} * \text{connector area} * \text{latency}}$$

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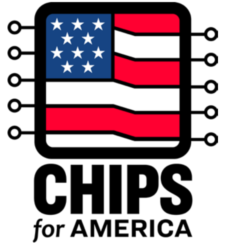
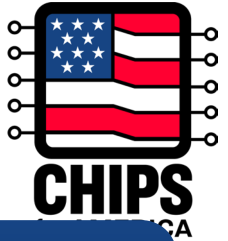
Specifications



Applicants must call out their targets for the following parameters	
Bandwidth/shoreline (Gb/s/mm)	The effective data rate assuming all signal escapes are from the edge of the sub-assembly
Bandwidth/area (Gb/s/mm^2)	The effective data rate accounting for all the area used by the connector
Total chiplet area (mm^2)	Total Area of the chiplet including any elements needed to enable full functionality
Link length (mm)	The length in mm between the transmitter and receiver
Energy efficiency (pJ/bit)	The amortized energy per bit transmitted, including source (laser), modulation, SerDes, error correction, etc.
Clock rate *OR* RF freq. *OR* Wavelength	Proposer specified. Explain adherence to an MSA or other interoperability specifications should be stated
Latency (ns)	Total time for the electrical data being transmitted to be prepared, transmitted and received, in usable error-free electrical form, including time of flight (TOF) which can be stated separately
Composite bit error rate (BER)	The effective error rate after error correction

Key Outputs



3-5 Year Outputs

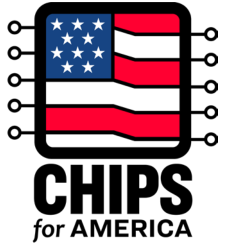
- New materials, designs, documentation, processes, and tools to prototype and demonstrate manufacturability.
- Innovative approaches for both flexible wired and wireless connections relying on RF/mm-wave and/or optical approaches
- New measurement methods for connector chiplets and substrate/sub-assembly features, to improve materials, models, designs, processes and tools for connector solutions and data transfer management.
- Connector modeling capabilities for complex advanced packaging flows; Validated connector models and connector assembly reliability data that are aligned with new design tools developed under the NAPMP Co-Design/Electronic Design Automation RDA and other semiconductor R&D initiatives.
- The assembly technologies and processes will involve development of tooling for bonding.

10 Year Outputs

- Scale down and scale out connectors are no longer gating factors limiting advanced packaging for all data rate transfer distances.
- Devices assembled with advanced packaging connectors operate reliably at higher power performance and higher energy efficiency.
- Chiplets and connector substrate features developed under this award are readily available in the chiplets ecosystem.
- Extreme interconnect density needs of next-generation packaging will drive fine pitches (< 10 μm pitch) and line/space (< 1 μm L/S) circuitry.

Goal: Drive innovation and adoption for high data-rate, low latency, small footprint, error-free, and energy efficient connections between packaged sub-assemblies.

Key Deliverables



Example Deliverable Plan for TA3

		Year 1				Year 2				Year 3				Year 4				Year 5			
		1Q	2Q	3Q	4Q	5Q	6Q	7Q	8Q	9Q	10Q	11Q	12Q	13Q	14Q	15Q	16Q	17Q	18Q	19Q	20Q

Area	Item	Phase 1: Develop preliminary connector solutions	Phase 2: Develop prototypes of initial solutions	Phase 3: Refinement of connector solutions	Phase 4: Transfer of the leading solutions to the NAPPF
PIC	Faster / More accurate modulators	Layout/ Determine Specs	Prototypes	Process/ Quality Optimization	Transfer to NAPPF
PIC	Consolidate EIC / PIC	Layout/ Determine Specs	Prototypes	Process/ Quality Optimization	Transfer to NAPPF
PIC	Smaller footprint, denser shoreline	Layout/ Determine Specs	Prototypes	Process/ Quality Optimization	Transfer to NAPPF
PIC	Athermal design	Layout/ Determine Specs	Prototypes	Process/ Quality Optimization	Transfer to NAPPF
Connector /Coupling	Microlens vs. Evanescent	Decision on Method	Prototypes	Process/ Quality Optimization	Transfer to NAPPF
Connector /Coupling	Fiber attach: Vertical or horizontal	Determine Specs	Work w/ Tool Vendors	Process/ Quality Optimization	Transfer to NAPPF
Connector /Coupling	Method of wafer testing	Decision on Method	Work w/ Tool Vendors	Process/ Quality Optimization	Transfer to NAPPF
Operation	Energy budget per bit	Model/Estimate	Prelim. Measurements	Final Design Results	Verify results in NAPPF Parts
Operation	Error correction	Design Circuit / Sware	Software V&V	Test in Device	Verify results in NAPPF Parts

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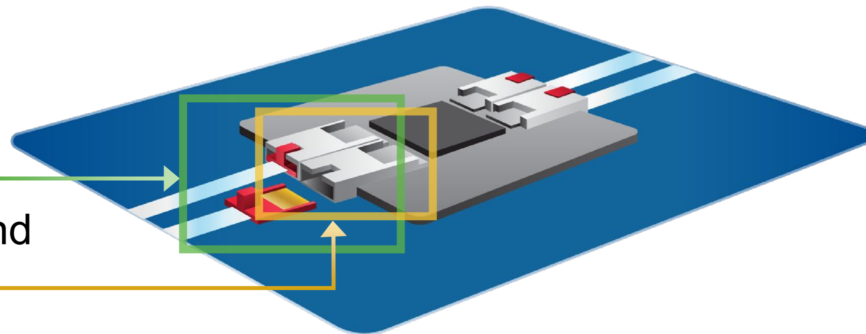
In Scope/Out of Scope

In Scope

- Chiplet sub-assembly to substrate connectors and connection techniques, such as:
  - Automated, low loss, reliable fiber attachment approaches such as high fiber count fiber array units (FAUs) that may contain polarization maintaining fibers
  - Flip-chip optical connections, including evanescent coupling, between substrate waveguides and transceiver chiplets

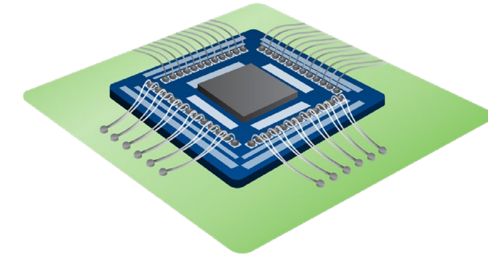
In Scope — Connectors including both a **fiber connector** and a **connector interface**



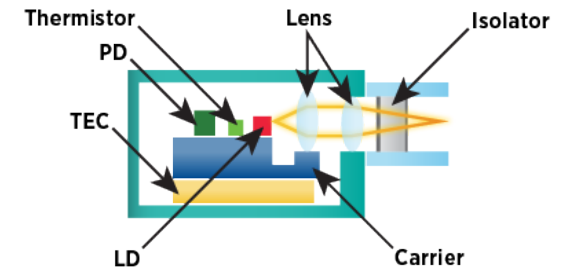
Out of Scope

- Traditional ball grid array (BGA) or land grid array (LGA) connectors
- Conventional wire bonding
- Traditional free space optical components

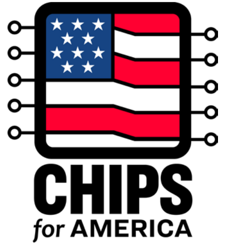
Out of Scope — Connectors utilizing **wire bonds** from substrate to package



Out of Scope — Traditional free space optical components such as those used in some pluggable transceivers



Collaboration with Other R&D Areas

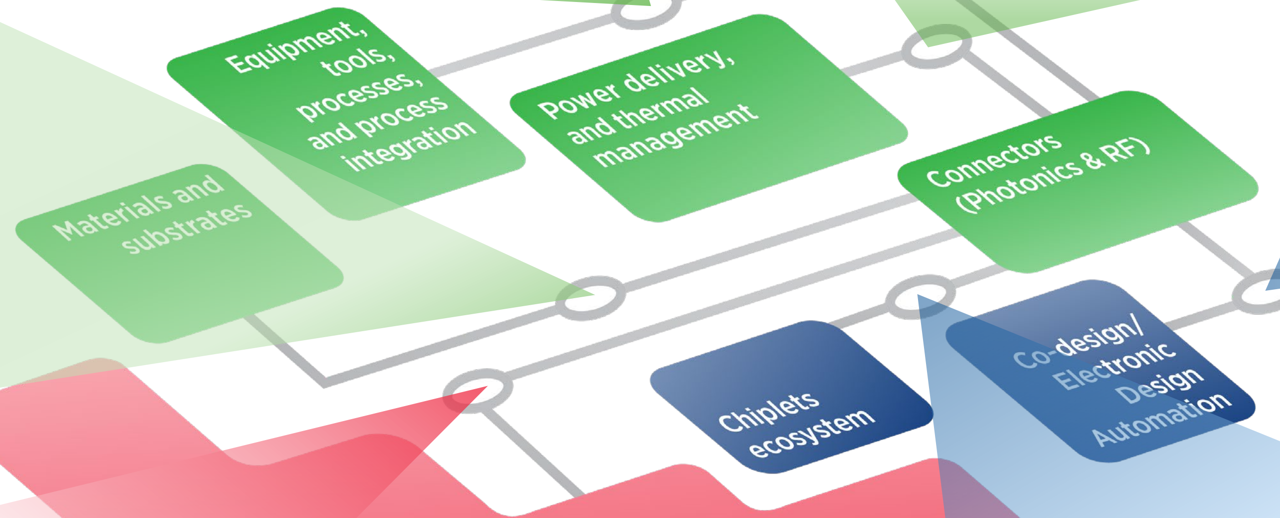


- Tools must offer process capabilities to process connector technology
- Process flow needs to be compatible with other process flows (i.e. post fiber attach reflow...)

- Minimize thermal burden
- Avoid localized hotspots
- Enable reliability in extreme conditions

- Chiplet to substrate optical coupling
- In-substrate optical routing
- Match fine scale & bonding

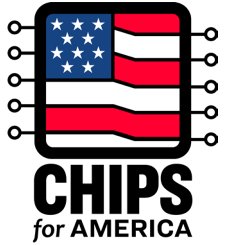
- Advanced models
- Leverage to accelerate design



Transition Connector technology and processes to NAPPF

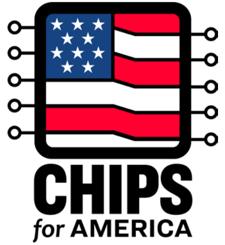
- Optimize for chiplet interconnect technology
- Chiplet-like connector interface

Program Structure



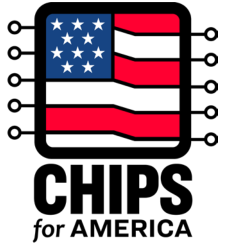
- Multiple awards varying in scope and funding are expected:
  - Up to approximately $250,000,000 anticipated for funding multiple awards in amounts ranging from a minimum of approximately $10,000,000 up to a maximum of approximately $100,000,000
- Multi-disciplinary, multi-organization project teams are strongly encouraged
- Applicants must propose a detailed project plan for achieving Project-Level Technical Targets
- Projects should be divided into 4 phases over a period of performance of 5 years:
  - Phase 1 (12 months)
  - Phase 2 (12 months)
  - Phase 3 (18 months)
  - Phase 4 (18 months)
- While cost share is not required, CHIPS R&D will give preference to applications that demonstrate credible cost share commitments

Collaboration is Critical for Success



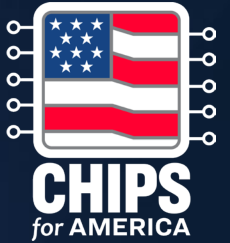
- System houses and end users
- EDA vendors
- Chiplet designers
- Chiplet fabricators
- Materials and substrate suppliers
- Equipment and tool vendors
- Educational institutions
- Thermal and connector solutions
- OSATS and IDMs
- Prototypes

Successful execution will require collaboration between proposers and each R&D Area. Proposers must clearly understand the ideas presented in each R&D Area. We encourage you to begin identifying your individual contributions to the ecosystem as well as partners who can help accomplish the vision and goals of the NAPMP.



Next Steps

- NOFO 2: Concept papers due 12/16
- Visit CHIPS.gov for resources, including:
  - Upcoming R&D Area Webinars
  - FAQs
  - Funding opportunities and NOFO updates
- Join our mailing list
- Contact us
  - askchips@chips.gov – general inquiries
  - apply@chips.gov – application-related inquiries



Thank you for attending

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