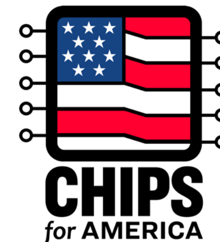


# CHIPS Metrology Community

## Opportunities for Metrology Program Collaboration Across the Semiconductor Industry

NIST NATIONAL INSTITUTE OF STANDARDS AND TECHNOLOGY
U.S. DEPARTMENT OF COMMERCE

# Disclaimer

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- Such identification is not intended to imply recommendation or endorsement by the National Institute of Standards and Technology, nor is it intended to imply that the entities, materials, or equipment are necessarily the best available for the purpose.
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  - Are information, pre-decisional, and preliminary in nature.
  - Do not constitute a commitment and are not binding on the National Institute of Standards and Technology or the Department of Commerce.
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- Nothing in this presentation is intended to contradict or supersede the requirements published in any future policy documents or Notices of Funding Opportunity.

# Today's Speakers

CHIPS for AMERICA

**Dr. Marla Dowell**

Director,
CHIPS Metrology
Program

**Dr. Paul Hale**

Deputy Director,
CHIPS Metrology
Program

**Dr. Isvar Cordova**

Program Manager,
CHIPS Metrology
Program

**Dr. Rebecca Routson**

Program Manager,
CHIPS Metrology
Program

# Agenda and Objectives

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## Agenda

- Introduction of the CHIPS Metrology program
- Discuss the Purpose, Vision and Engagement Opportunities with the CHIPS Metrology Community
- Review the Memorandum of Understanding
- Steps to Join CHIPS Metrology Community

**By the end, attendees should better understand:**

- What is the CHIPS Metrology Program
- What is the CHIPS Metrology Community
- How to Join the CHIPS Metrology Community

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# CHIPS for America

## $39 billion for incentives

Two component programs to:

1. Attract large-scale investments in advanced technologies such as leading-edge logic and memory, and advanced packaging
2. Incentivize expansion of manufacturing capacity for mature and other types of semiconductors

## $11 billion for R&D

Four integrated programs to:

1. Conduct research and prototyping of advanced semiconductor technology
2. Strengthen semiconductor advanced packaging, assembly, and test
3. Enable advances in measurement science, standards, material characterization, instrumentation, testing, and manufacturing

Together with CHIPS initiatives from other agencies, including DOD, State, NSF, and Treasury

# CHIPS for America Vision

## Economic Security

This act enables us to build more resilient supply chains for important components.

## National Security

This act enables us to bring the most sophisticated technologies back to the U.S.

## Future Innovation

Chips are key to the technologies and industries of the future, so we need to be at the forefront. This act will ensure long-term U.S. leadership in the sector.

# CHIPS R&D Programs

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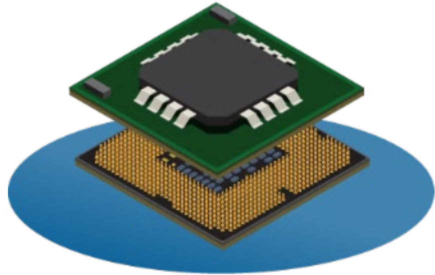
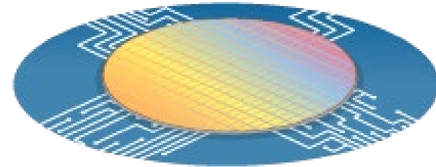


CHIPS National Semiconductor Technology Center (NSTC) Program

Natcast is a purpose-built nonprofit organization and operator of the NSTC consortium



CHIPS National Advanced Packaging Manufacturing Program (NAPMP)

CHIPS Manufacturing USA Program

CHIPS Metrology Program

# CHIPS Metrology Program

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## VISION:

CHIPS Metrology catalyzes innovation with an emphasis on accurate, precise, and fit-for-purpose measurements for producing microelectronic materials, devices, circuits, and systems.

## MISSION:

Measure, innovate, and lead to enhance a vibrant U.S. ecosystem for semiconductor manufacturing and to promote U.S. innovation and industrial competitiveness.

## GOALS:

1. Expanding measurement solutions for the semiconductor ecosystem.
2. Increase the number of solvers by harnessing the diversity of people and ideas, inside and outside of NIST.
3. Expand education and outreach opportunities that inspire excitement about manufacturing careers and expand career pathways.

# Purpose of the Community

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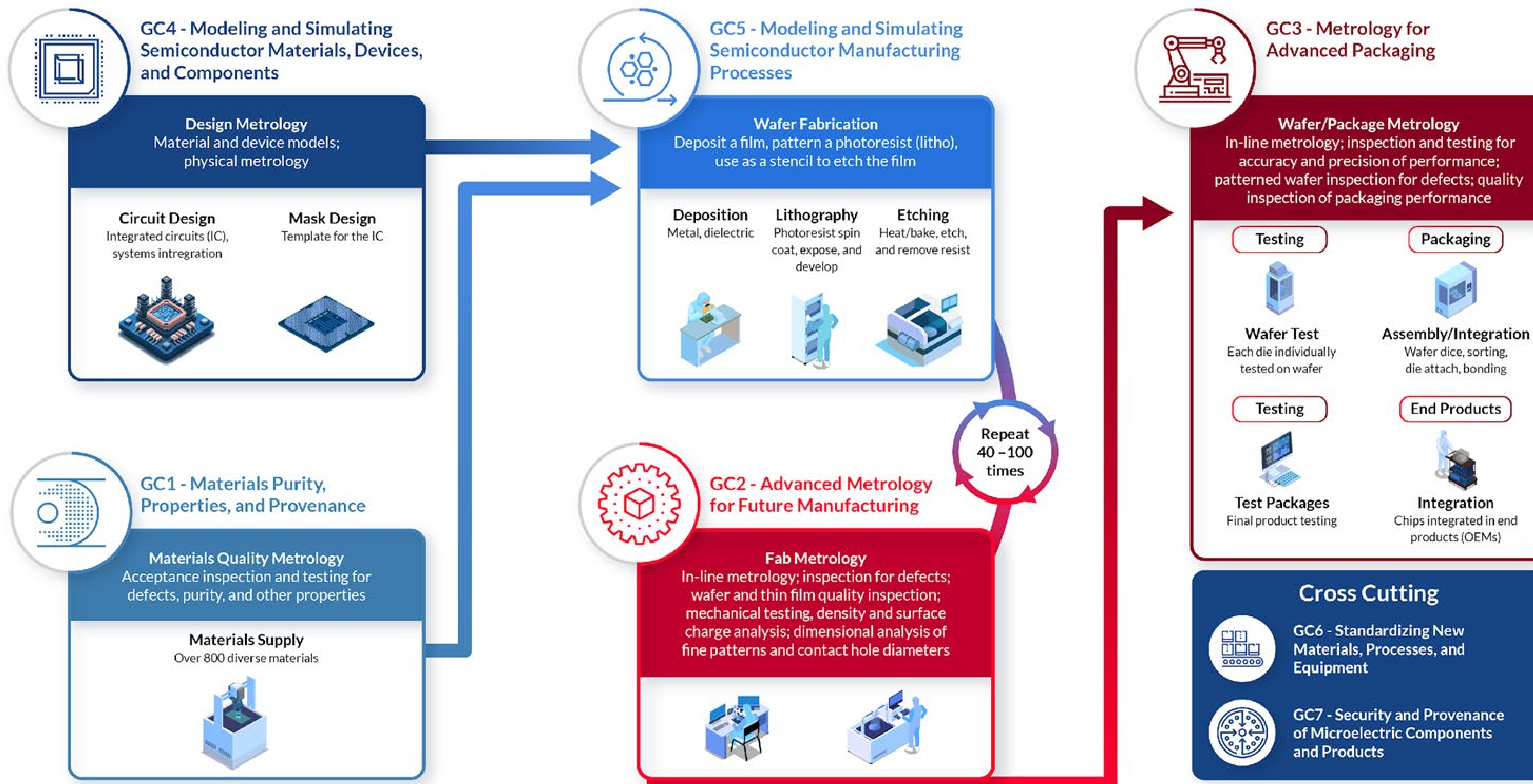
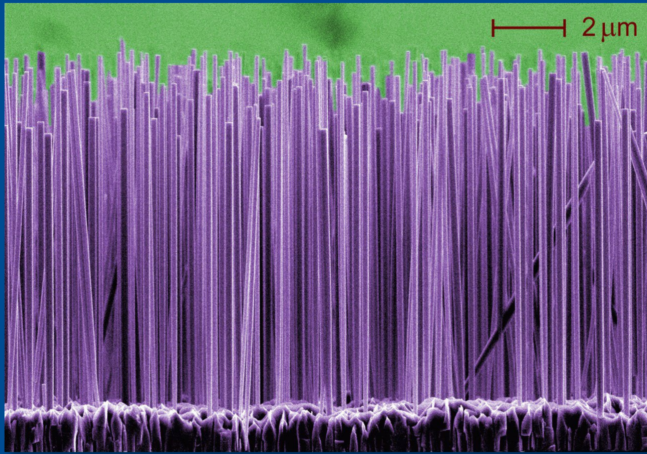
The Community:

- Consists of **engagement groups** working to advance breakthrough measurements that are accurate, precise, and fit-for-purpose to produce microelectronic materials, devices, circuits, and systems.
- Facilitates collaborations to help **improve data and knowledge sharing** among all stakeholders in the semiconductor field.
- **Helps stakeholders inform the industry standards** that are critical for enhancing U.S. economic or national security competitiveness to meet unprecedented demand for next generation networks.
- Helps **close cultural and knowledge gaps** between "fab," "lab," and equipment providers.

# CHIPS Metrology Grand Challenges (GC)



# Grand Challenge 1:
## Metrology for Materials Purity, Properties, and Provenance



**The challenge:** Meet increasingly stringent requirements for semiconductor material purity, physical properties, and provenance across a diverse supply chain through development of new measurements and standards.

**The strategy:** Develop measurement technologies, properties data, and standards focused on defect and contaminant identification. The objective is to support uniform materials quality across suppliers and to enable tracking of potential sources of impurity.

**The path forward:** Conduct high-impact R&D and related activities in critical areas:

- New measurements with increased sensitivity and throughput for detection of particles and contaminants in materials throughout the supply chain, including in-line quality assessment.
- Innovative, higher-throughput techniques for measuring physical properties for microelectronics feed materials.
- Evaluation and correlation of properties data across the materials supply infrastructure to support both standards and provenance.
- Standard Reference Materials (SRMs) for trace impurity detection and reference data, including those for thermophysical properties of materials.
- Documentary standards that can assist manufacturers in following materials through the supply chain, such as detailed versions of certificates of analysis (shows material properties, keeps track of any potential source of contamination)

https://nvlpubs.nist.gov/nistpubs/CHIPS/NIST.CHIPS.1000.pdf

# Grand Challenge 2:

## Advanced Metrology for Future Microelectronics Manufacturing

https://nvlpubs.nist.gov/nistpubs/CHIPS/NIST.CHIPS.1000.pdf

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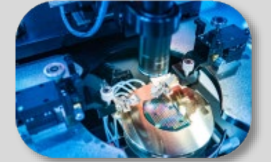
**The challenge:** Ensure that critical metrology advances are made to keep pace with cutting-edge and future microelectronics and semiconductor manufacturing, while maintaining a competitive U.S. advantage.



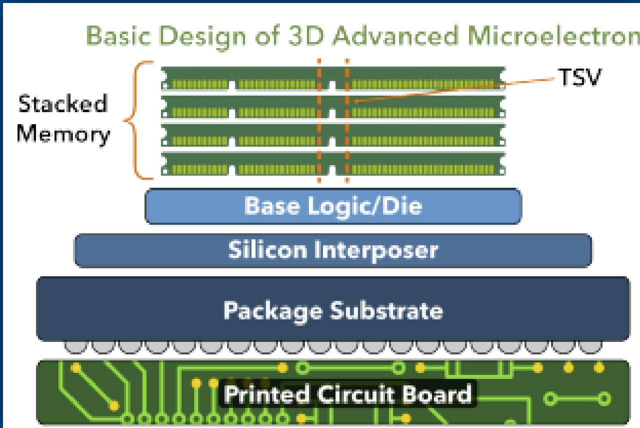
**The strategy:** Develop advanced physical and computational metrology adaptable to next-generation manufacturing of advanced complex, integrated technologies and systems.

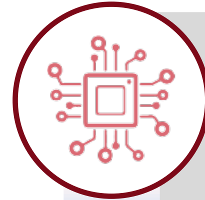
**The path forward:** Conduct activities in critical areas to develop innovative, cost-effective metrology applicable to 3D device and next-generation manufacturing, including tools and methods in the following critical areas:

- Properties of new materials and devices, such as GAA, complementary FET, and novel interconnects and dielectrics.
- Physical properties characterization (e.g., size, roughness, thermal, mechanical, electrical, magnetic, optical) for surfaces, buried features, interfaces, and devices with increased resolution, sensitivity, accuracy, and throughput.
- Rapid, high-resolution, non-destructive techniques for characterizing defects and impurities and correlating them with performance and reliability.
- Evaluation and correlation of relevant data across the semiconductor manufacturing process.
- Standards for process design, development, and control, such as reference materials and documentary standards.
- Statistical analysis for rare but catastrophic defects such as stochastic events in extreme ultraviolet (EUV) lithography.

# Grand Challenge 3:

## Enabling metrology for integrating components in advanced packaging



**The challenge:** Provide enabling metrology that spans multiple length scales and physical properties and supports acceleration of advanced packaging concepts for future-generation microelectronics.

**The strategy:** Develop metrology to enable complex integration of sophisticated components and novel materials for advanced microelectronics, strengthening the domestic semiconductor packaging industry and U.S. leadership in this critical sector.

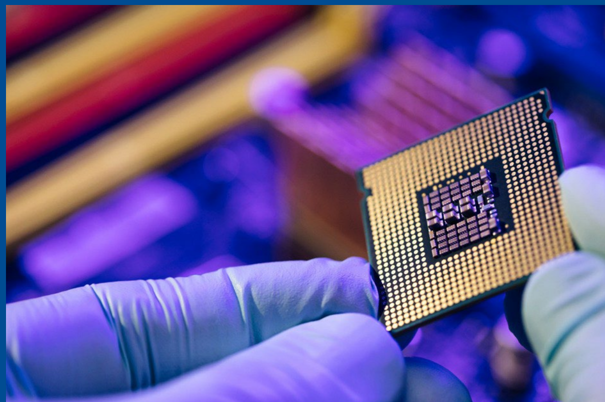
**The path forward:** Conduct R&D to develop metrology to address the unique challenges presented by advanced packaging, including subsurface features and aspects related to heterogenous integration and other innovative concepts. Critical areas include:

- Measurements for in situ, rapid measurements and verification methods for interfaces and subsurface interconnects, and internal 3D structures including warpage, voids, substrate yield, stresses, adhesion, and reliability with improved throughput and resolution.
- Physical properties (e.g., size, thermal, mechanical, electrical, magnetic, optical) for films, surfaces, buried features, and interfaces.
- Methods for integrating chiplets, dielets, SoCs, and memories into packages.
- Mechanical measurements for component integration (e.g., hybrid bonding and interfacial adhesion and bond integrity).
- Evaluation and correlation of data across the packaging process.
- Standards for packaging, such as reference materials and documentary standards for areas including chiplets and SoCs.

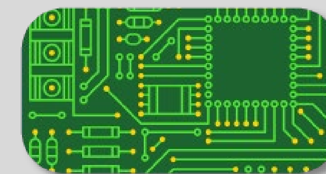
https://nvlpubs.nist.gov/nistpubs/CHIPS/NIST.CHIPS.1000.pdf

# Grand Challenge 4:

## Modeling and Simulating Semiconductor Materials, Designs, and Components



**The challenge:** Improve the tools needed to effectively model and simulate future semiconductor materials, processes, devices, circuits, and microelectronic system designs.



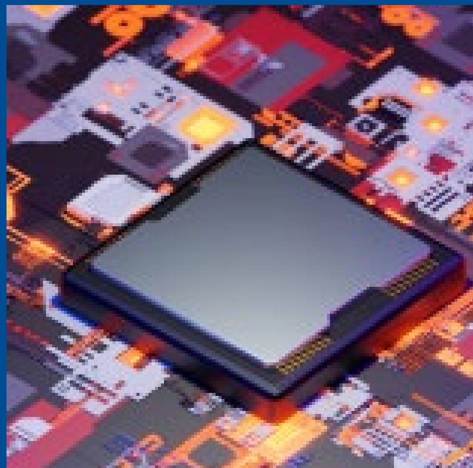
**The strategy:** Develop advanced design simulators based on multi-physics models, a spectrum of critical measurements, and next-generation concepts such as artificial intelligence, creating a suite of tools to empower U.S. microelectronics designers.

**The path forward:** Conduct R&D to develop robust data, mathematical models, and measurement techniques for important future device parameters that are needed to support effective design simulators. Critical R&D areas include:

- Multi-physics models, including those that capture thermal, chemical, physical, mechanical, signal integrity, reliability, power consumption, and other parameters.
- Measurements of material, component, and circuit properties across a broad temperature, bias, and frequency range as input to, and as verification of, the above models.
- Application and validation of advanced analytics such as ML and AI for modeling and optimization of complex materials, circuits, and systems operating in real environments.
- Methods for robustly estimating model uncertainty.

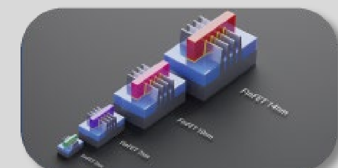
https://nvlpubs.nist.gov/nistpubs/CHIPS/NIST.CHIPS.1000.pdf

# Grand Challenge 5:
## Modeling and Simulating Semiconductor Manufacturing Processes



https://nvlpubs.nist.gov/nistpubs/CHIPS/NIST.CHIPS.1000.pdf

**The challenge:** Seamlessly model and simulate the entire semiconductor value chain, from materials inputs to chip fabrication, system assembly, and end products.

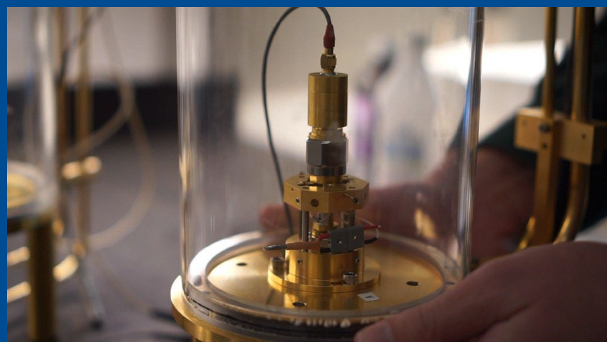


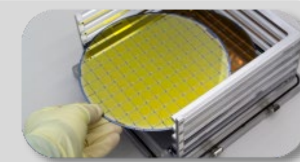
**The strategy:** Create a suite of advanced computational models, methods, data, standards, and tools that will enable domestic semiconductor manufacturers and the value chain to improve overall yields, accelerate time to market of devices, and enhance competitiveness in global markets.

**The path forward:** Conduct R&D to develop a variety of effective manufacturing simulation tools and related standards that can be applied to in-line processes and model key parameters. Critical R&D areas include:

- Modeling, data analysis, and validation tools to enable efficient process development and optimization.
- Standards, protocols, and standard data for automation and virtualization.
- Measurements and standards supporting digital twins, from individual processing steps up to the complete chip fabrication and system assembly.
- Application and validation of advanced analytics such as ML and AI for modeling and optimization of complex manufacturing process design, development, automation, and integration.

# Grand Challenge 6:
## Standardizing New Materials, Processes and Equipment for Microelectronics





**The challenge:** Create the standards and validation methods necessary to accelerate the development and manufacturing of future information and communication technologies.

**The strategy:** Create standards and validation protocols to support the use of new materials, processes, and equipment in future-generation microelectronics, paving the way for accelerated innovation and cost-competitiveness in U.S. industry.

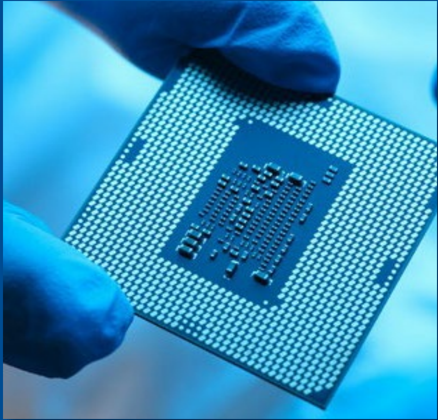
**The path forward:** Conduct R&D, data collection, process validation, and other standards-related activities to support the development of documentary standards, SRMs, and calibration protocols and services for next-generation semiconductor manufacturing. Critical areas of pursuit include:

- SRMs, data, instruments, and calibration and measurement services; product development kits; and a diversity of best-known methods.
  - Reference materials to detect defects, contaminants, and trace impurities at the nanoscale.
  - Reference materials for nanoscale dimensional and materials characterization.
  - Calibration, validation, and new methods to enable high-accuracy fleet matching for equipment in both process development and high-volume manufacturing (i.e., matching the suite of tools to the process/materials of use).
  - SRMs and data for advanced packaging and heterogeneous integration, including high-frequency electrical properties and thermomechanical properties.
- Standards for interoperable equipment and software from different vendors that ensure the protection of intellectual property (IP), data integrity, and provenance across the supply chain.
- Standards for tracking materials from creation to end use in the fab, including anything that could alter the properties of the material.

https://nvlpubs.nist.gov/nistpubs/CHIPS/NIST.CHIPS.1000.pdf

# Grand Challenge 7:

## Metrology to Enhance Security and Provenance of Microelectronic-based Components and Products



**The challenge:** Create the metrology advances needed to enhance the security and provenance of microelectronic components and products across supply chains and increase trust and assurance.

**The strategy:** Pursue a comprehensive approach to hardware security protection that includes standards, protocols, formal testing processes, and advanced computational technologies while providing avenues for assurance and provenance of microelectronic components across the supply chain and end products.

**The path forward:** Conduct activities to support the development of standards, protocols, and testing processes for analyzing security vulnerabilities in microelectronics across their entire life cycle. Critical areas of pursuit include:

- Methods, reference design kits, and guidelines for security analytics and automation, including pervasive security to address formalized threat models.
- Enhanced vulnerability management across the overall product life cycle from inception to end of life, including activities such as:
  - Formal testing and processes for independent V&V.
  - Tracking of materials and components, as well as detecting and mitigating trigger mechanisms.
  - Common test structures, test methods, and test and measurement strategies for end-to-end provenance.
- Documentary standards for hardware security and provenance.
- Development and use of trusted emerging techniques, e.g., AI and ML methods across the entire semiconductor value chain.

https://nvlpubs.nist.gov/nistpubs/CHIPS/NIST.CHIPS.1000.pdf

# CHIPS Metrology Program: How Far We've Come

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## Grand Challenge (GC) Funded Research Projects

- Over **$190 million** in funding has been provided to more than **40 approved research projects** in 6 Grand Challenges.
- Current projects are helping to develop new measurement instruments, measurement methods, and measurement-informed models and simulations for advanced microelectronics design and manufacturing.
- More information about the funded projects can be found on the CHIPS Metrology webpage. Additional project pages will be added this fall.

## Industry and Academia Collaboration

- Research teams have proposed several distinct industry collaborators to provide materials and software and/or conduct joint research with researchers.
- Several collaborations with U.S. universities, nonprofit consortiums, research institutes, and associations related to the microelectronics industries have also been proposed.

https://www.nist.gov/chips/research-development-programs/metrology-program

# METIS

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## What is METIS?

- The Metrology Exchange to Innovate in Semiconductors, or METIS, is a data exchange ecosystem developed by NIST that will give stakeholders access to CHIPS Metrology research results and serve to catalyze innovative breakthroughs in U.S. semiconductor manufacturing.

- METIS will make research and data available in a manner that guards intellectual property, protects U.S. security interests, is aligned with the approach used by NIST for access to research results, and is self-sustaining to meet future needs.

https://www.nist.gov/programs-projects/metis

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U.S. DEPARTMENT OF COMMERCE

# Purpose of the Community

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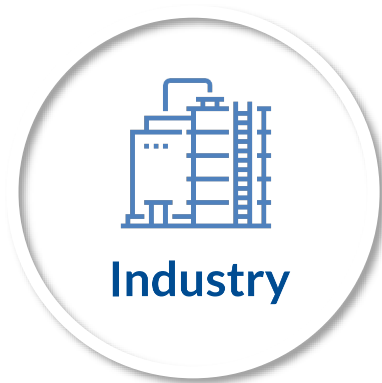
The Community:

- Are **engagement groups** working to advance breakthrough measurements that are accurate, precise, and fit-for-purpose to produce microelectronic materials, devices, circuits, and systems.
- Facilitate collaborations to help **improve data and knowledge sharing** among all stakeholders in the semiconductor field.
- **Help stakeholders inform the industry standards** that are critical for enhancing U.S. economic or national security competitiveness to meet unprecedented demand for next generation networks.
- Help **close the cultural and knowledge gaps** between "fab," "lab," and equipment providers.

# Target Audiences



Packaging

Manufacturing

Instrument Vendors

FAB Houses

Global Devices

EDA Tools

Engineers to Executive Leadership

Researchers working on microelectronics

Associations of industry employees, academia and government workers.

# The Community's Charter

- The purpose of this charter is to define the community’s scope, goals, roles and responsibilities, member overview and expectations, engagement opportunities, and Community digital domain.
- Scope: The CHIPS Metrology Community will work to advance breakthrough measurements that are accurate, precise, and fit-for-purpose to produce microelectronic materials, devices, circuits, and systems. Within this broad scope, the CHIPS Metrology Community will coordinate engagement opportunities to align with the focus areas of the seven Grand Challenges.

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CHIPS for AMERICA METROLOGY COMMUNITY

## CHIPS Metrology Community Charter Outline

### Background

The United States remains a global leader in chip design as well as research and development (R&D), however, has fallen behind in manufacturing and, as of June 2023, accounts for only about 10% of commercial global production. While the U.S. produces few semiconductors, our country remains one of the world’s largest users of chips—for entertainment and consumer electronics, for cars and public transportation systems, and for critical systems like utilities and national defense. This makes us vulnerable to supply chain disruptions from far-off events over which we have little control.

In response, the CHIPS Act of 2022 appropriated $50 billion to the Department of Commerce to implement the CHIPS for America program, $11 billion of which will be invested through CHIPS Research and Development Office (CHIPS R&D) programs to create a robust domestic R&D ecosystem to strengthen and revitalize the U.S. position in semiconductor research, development, and manufacturing.

Metrology plays a key role in semiconductor manufacturing. As devices become more complex, smaller, and multi-layered, the ability to measure, monitor, predict, and ensure quality in manufacturing becomes much more difficult and uncertain.

The CHIPS Metrology Program, one of the four initiatives within the CRDO, emphasizes measurements that are accurate, precise, and fit-for-purpose for the production of microelectronic materials, devices, circuits, and systems. In its work, it aligns its research and development portfolios based on the identified metrology needs of seven Grand Challenges (GCs):

GC4 - Modeling and Simulating Semiconductor Materials, Devices, and Components
GC5 - Modeling and Simulating Semiconductor Manufacturing Processes
GC3 - Metrology for Advanced Packaging
GC1 - Materials Purity, Properties, and Provenance
GC2 - Advanced Metrology for Future Manufacturing
Cross Cutting
GC6 - Standardizing New Materials, Processes, and Equipment
GC7 - Security and Provenance of Microelectric Components and Products

The CHIPS Metrology Program is establishing a community of practice to foster collaboration to help improve data and knowledge sharing across initiatives within the domain of these Grand Challenges, as well as to help stakeholders inform the industry standards that are critical for enhancing U.S. economic or national security competitiveness. **The purpose of this charter is to define the community’s scope,**

CHIPS for America 1

https://www.nist.gov/chips/metrology-community

# Community Goals

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1. Serve as a cross-company and cross-organization **networking forum** where matches between interests and skills can be more efficient.
2. **Bring together** individuals and organizations from across the **semiconductor industry ecosystem** in pursuit of working collaboratively **to advance metrology research and development**.
3. Nurture **high-impact partnerships** with stakeholders, government agencies, and academia to further industry engagement and collect insight for enhanced capabilities.
4. Provide **professional development opportunities** for participants to advance their expertise through access to webinars, equipment, facility use, conference registrations, data management plans, training, and other benefits.
5. Provide a source of **shared knowledge** regarding development of **new measurement capabilities and scaling resources** to reduce barriers.
6. Provide a strategic forum to connect subject matter experts and problem solvers with stakeholder's **shared measurement challenges and emerging technology needs**.

# Community Engagement

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**Engagement Opportunities:**

- Subject matter expert presentations
- Discussion forums
- Webinars
- Workshops
- Training, education and workforce development opportunities

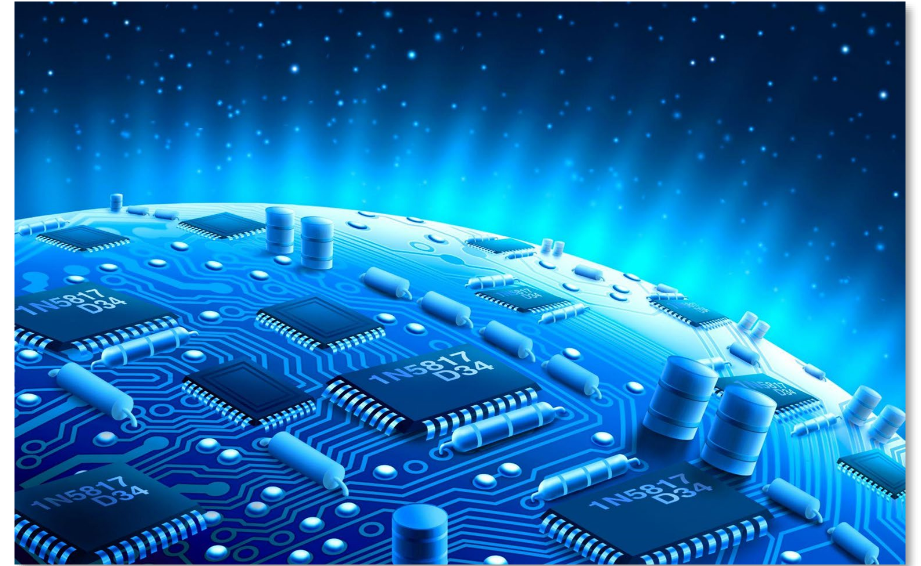
**Engagement Benefits:**

- Insights to currently funded projects
- Access to NIST expert knowledge
- Clear avenue for providing feedback on CHIPS Metrology
- Centralized place of sharing information and collaboration across different companies, agencies, and experience levels
- Data sharing while acknowledging IP constraints and proprietary information
- Structured place and time to access other stakeholders
- Professional development opportunities
- Opportunity to develop solutions to problems shared across industry

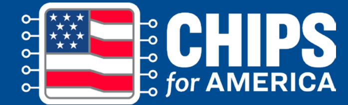
# Membership



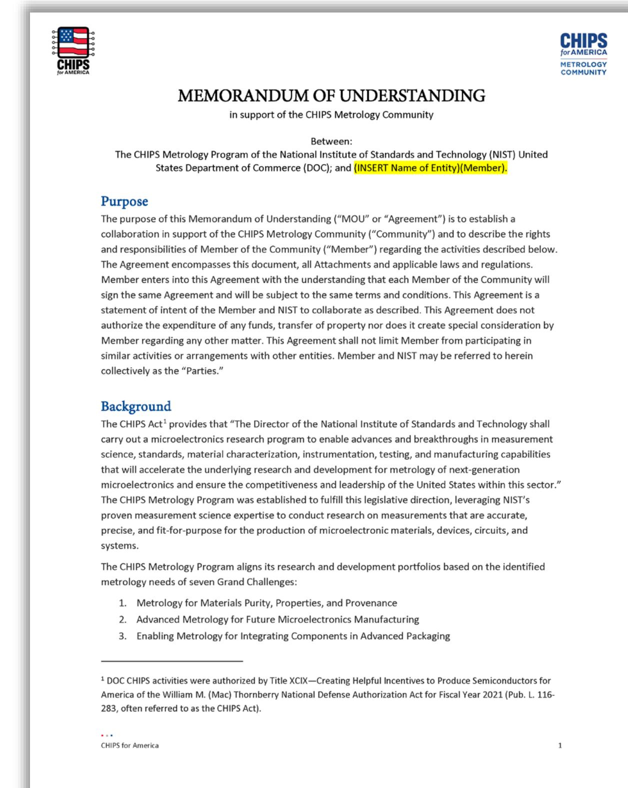
- Membership is currently free
- A signed Memorandum of Understanding (MOU) is required to become a member
- The CHIPS Metrology team will put the MOUs through an intake process to determine if the potential new member's goals align with CHIPS Metrology's initiative



# Memorandum of Understanding




- Does not create legally binding duties or obligations nor does this MOU limit or restrict the Parties from participating in similar activities or arrangements with other entities
- Outlines CHIPS Metrology's responsibilities and member's responsibilities
- Highlights that NIST & Members do not intend to exchange confidential or proprietary information – separate agreements are available
- Not an obligation of funds and does not authorize any transfer of funds between the Parties
- No fundraising efforts for general purposes related to this activity
- Not an endorsement by NIST/CHIPS
- Not primarily an avenue to sell or promote products or services
- Foreign adversaries are not eligible to become members of the Metrology Community



CHIPS for AMERICA

CHIPS for AMERICA METROLOGY COMMUNITY

MEMORANDUM OF UNDERSTANDING

in support of the CHIPS Metrology Community

Between:
The CHIPS Metrology Program of the National Institute of Standards and Technology (NIST) United States Department of Commerce (DOC); and (INSERT Name of Entity)(Member).

**Purpose**

The purpose of this Memorandum of Understanding ("MOU" or "Agreement") is to establish a collaboration in support of the CHIPS Metrology Community ("Community") and to describe the rights and responsibilities of Member of the Community ("Member") regarding the activities described below. The Agreement encompasses this document, all Attachments and applicable laws and regulations. Member enters into this Agreement with the understanding that each Member of the Community will sign the same Agreement and will be subject to the same terms and conditions. This Agreement is a statement of intent of the Member and NIST to collaborate as described. This Agreement does not authorize the expenditure of any funds, transfer of property nor does it create special consideration by Member regarding any other matter. This Agreement shall not limit Member from participating in similar activities or arrangements with other entities. Member and NIST may be referred to herein collectively as the "Parties."

**Background**

The CHIPS Act[1] provides that "The Director of the National Institute of Standards and Technology shall carry out a microelectronics research program to enable advances and breakthroughs in measurement science, standards, material characterization, instrumentation, testing, and manufacturing capabilities that will accelerate the underlying research and development for metrology of next-generation microelectronics and ensure the competitiveness and leadership of the United States within this sector." The CHIPS Metrology Program was established to fulfill this legislative direction, leveraging NIST's proven measurement science expertise to conduct research on measurements that are accurate, precise, and fit-for-purpose for the production of microelectronic materials, devices, circuits, and systems.

The CHIPS Metrology Program aligns its research and development portfolios based on the identified metrology needs of seven Grand Challenges:

1. Metrology for Materials Purity, Properties, and Provenance
2. Advanced Metrology for Future Microelectronics Manufacturing
3. Enabling Metrology for Integrating Components in Advanced Packaging

[1] DOC CHIPS activities were authorized by Title XCIX—Creating Helpful Incentives to Produce Semiconductors for America of the William M. (Mac) Thornberry National Defense Authorization Act for Fiscal Year 2021 (Pub. L. 116-283, often referred to as the CHIPS Act).

CHIPS for America 1

https://www.nist.gov/chips/metrology-community

# NIST Responsibilities

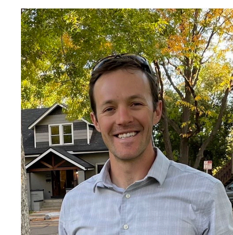
- Develop the strategy for the Community
- Proactively gather member feedback
- Invite experts to present on areas of interest and convening related panels for discussion
- Coordinate with speakers and collecting presentation materials
- Support smaller collaborative efforts between members
- Manage logistics for Community events
- Document and maintain Community materials on the public and member-accessible online domains
- Communicate with stakeholders
- Promote the Community to new potential members

# CHIPS Metrology Community Points of Contacts

**Dr. Marla Dowell**
Program Director

**Dr. Isvar Cordova**
Program Manager

**Antara Nandi**
Program Manager



**Sid Bittman**
Community Support

**Dr. Paul Hale**
Deputy Director

**Dr. Bob Keller**
Program Manager

**Dr. Rebecca Routson**
Program Manager

**Naeema Wali**
Community Support

**Sarah Hughes**
Metrology
Chief of Staff

**Jason Kahn**
Standards Advisor

# Member Responsibilities

- Participate in recurring Community engagements
- Participate in panel sessions, presentations, question and answer sessions, or other speaking opportunities where expertise and capacity are available
- Provide feedback into CHIPS Metrology research priorities and project performance
- Provide feedback or guidance on CHIPS Metrology training and/or workforce development activities
- Engage with other members in collaborative efforts
- Promote the existence of the CHIPS Metrology Community across stakeholder networks to increase awareness and participation
- Provide feedback to the Community Chair, Grand Challenge leads, and support staff

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METROLOGY COMMUNITY

CHIPS for AMERICA

# Next Steps to Join the Community

1. Download the MOU, review & sign.
2. Submit signed copy to metrologyprogram@chips.gov.
3. After receiving the signed copy, NIST will review the MOU & conduct a research security review (estimated a few weeks).
4. CHIPS Metrology will reach back out with status update and to provide onboarding materials and access for new Community members.

https://www.nist.gov/chips/metrology-community

# Initial Engagements

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- **Fall 2024 workshop – Mid-November 2024**
  - *Opportunity for in-person Community member engagement*

- **Winter 2024 digital engagement**
  - *First engagement dedicated to Community collaboration*

*Separate communication about each topic forthcoming for Community Members.*

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